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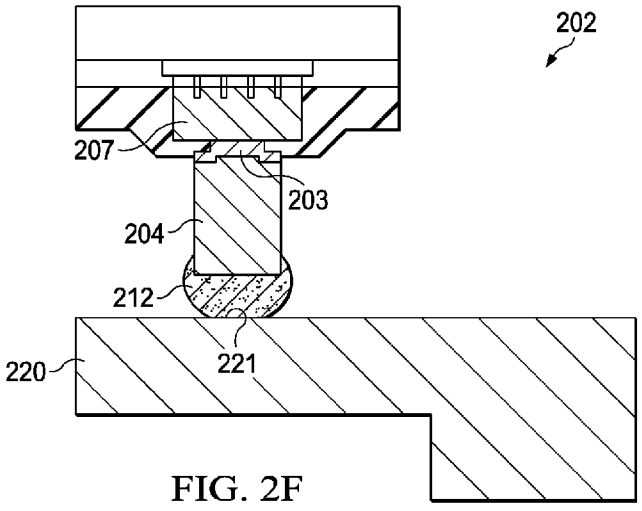

FIG. 2F

(57) Abstract: In described examples, an integrated circuit die is fabricating to have multiple contacts. A metal post (204) is formed on each contact (207). A bump (212) is formed on a contact region (221) of a leadframe (220) or on the post (204). The bump (212) is formed with a material that includes metal nanoparticles. The integrated circuit die is attached to the leadframe (220) by aligning the metal post (204) to the leadframe (220) and sintering the metal nanoparticles in the bump (212) to form a sintered metal bond between the post (204) and corresponding contact region (221) of the leadframe (220).

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[Continued on next page]

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SINTERED METAL FLIP CHIP JOINTS

[0001] This relates generally to bonding metal contact posts of a semiconductor die to a metal leadframe in a flip chip configuration, and more particularly to using sintered metal to form a solder free bond between the metal posts on the die and the leadframe.

BACKGROUND

[0002] Flip chip is a method for interconnecting semiconductor devices, such as IC chips and micro-electromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step. To mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit or leadframe, and then the solder is reflowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry or lead frame.

[0003] Processing a flip chip is similar to conventional IC fabrication, with a few additional steps. Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. This typically consists of several treatments. More recently, a process is used in which metal posts are formed on each metalized attachment pat to extend the height of the contact. A small dot of solder is then deposited on each metalized pad. Alternatively, the solder dots may be placed on the leadframe. The chips are then cut out of the wafer as normal.

[0004] To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying leadframe or circuit board. The solder is then re-melted to produce an electrical connection, typically using a Thermosonic bonding or alternatively a reflow solder process.

SUMMARY

[0005] In described examples, an integrated circuit die is fabricating to have multiple contacts. A metal post is formed on each contact. A bump is formed on a contact region of a leadframe or

on the post. The bump is formed with a material that includes metal nanoparticles. The integrated circuit die is attached to the leadframe by aligning the metal post to the leadframe and sintering the metal nanoparticles in the bump to form a sintered metal bond between the post and corresponding contact region of the leadframe.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a cross section of a conventional flip chip joint using solder.

[0007] FIGS. 2A-2G are a series of cross sectional views illustrating formation of a flip chip sintered metal joint.

[0008] FIG. 3 is a plot illustrating melting point vs. particle size in a sintering process.

[0009] FIGS. 4A-4D are a series of cross sectional views of another embodiment in which a sintered metal bond is formed.

[0010] FIG. 5 is a cross sectional view of a completed integrated circuit.

[0011] FIG. 6 is an illustration of a portion of a leadframe strip.

[0012] FIGS. 7A-7B illustrate another embodiment for forming posts.

[0013] FIG. 8 is an illustration of multiple IC dies mounted to a substrate using sintered metal bonds.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] Like elements in the drawings are denoted by like reference numerals for consistency.

[0015] Conventional FCOL (flip chip on leadframe) products typically use a solder alloy to bond metallic posts formed on the semiconductor die onto a leadframe. Typically, the posts are copper (Cu) and range in size from 75um circular to 100x300um oval, and the leadframe is copper. Although a solder bond provides a good connection between the copper posts and copper leadframe, it has solder joint quality/reliability issues. For example, infant mortality failures may occur due to voiding from the flux or the solder paste process. The adoption of lead (Pb) free solder by the industry has resulted in a more brittle solder. Thermally driven void development and growth may occur under thermal aging. Solder joint cracking may occur under temperature cycling. Also, the current carrying capacity of a solder joint may be less than optimum.

[0016] Example embodiments include an improved process for producing a FCOL device. An embodiment may print a metallic nanoparticle loaded solution onto the flip chip bumps or target substrate pads that will connect the two surfaces and be fused to form a solid metal-to-metal

connection. This may result in a bond that increases the maximum current allowed in a flip chip package. This process may improve joint cracking that has resulted from brittle Pb-free solder. This improved process may also prevent solder voiding during assembly and reliability stress.

[0017] FIG. 1 is a cross section of a conventional flip chip 102 with an example solder joint. At each contact region of semiconductor die 102, a metal layer 103, referred to as a "copper over anything" (COA) layer, may be deposited and then patterned to form a metalized contact region 103. A metallic post 104 is formed in contact with the metalized contact region 103. A solder dot 105 may be placed on either the post 104 or a leadframe 106 and then heated to form a solder bond between post 104 and leadframe 106, such as using a Thermosonic or reflow process. The solder forms a layer between post 104 and leadframe 106 and thereby may limit current capacity through post 104 to or from circuitry on die 102. Furthermore, as described hereinabove, if the solder is Pb free solder, then a tendency may exist for a crack to form between leadframe 106 and post 104 due to thermal cycling.

[0018] FIGS. 2A-2G are a series of cross sectional views illustrating formation of a flip chip sintered metal joint. In FIG. 2A, a small portion of a semiconductor die 202 is illustrated. Die 202 may extend to the left and to the right to include various circuitry and multiple contact regions. In this illustration, only a single contact region 207 is illustrated. On top of contact region 207, a COA copper layer has been deposited to form metal feature 203 that is in contact with contact region 207. For example, COA layer 203 may be applied by sputtering. Also, for example, a photo resist layer may then be applied and patterned to allow post 204 to be formed by electroplating. The photo resist may then be removed to reveal post 204 extending from the surface of die 202.

[0019] FIG. 2B illustrates an inkjet printer 210 depositing a series of droplets 211 that contain metal nanoparticles onto the metal post 204. Known techniques exist to fabricate three dimensional structures using ink jet printers or similar printers that can "print" various polymer materials. For example, see "3D printing," Wikipedia, Sept 4, 2014. Printing allows for the rapid and low-cost deposition of thick dielectric and metallic layers, such as 0.1 um–1000 um thick, while also allowing for fine feature sizes, such as 20um feature sizes.

[0020] The ink may include a solvent or several solvents to match rheology and surface tension, and metallic nanoparticles. For example, the size of the nanoparticle may be in a range of 2-100nm. The ink may also include a dispersant such as polyvinylpyrrolidone (PVP) or be

charge dispersed to prevent agglomeration of the particles. The ink may also include binders such as polymer epoxies, and other known or later developed ink additives.

[0021] The film residue that is left from the ink may then be cured in the case of solvent or dispersant based ink where solvent or dispersant is evaporated. Curing may be thermal (50-250°C), UV, Infrared, Flash Lamp, or of another form that is compatible with the ink being used.

[0022] In this example, the metal nanoparticles may be copper, or a mixture of copper and silver. In another example, the nanoparticles may be a mixture of copper and graphene, or copper and graphite. The graphite/grapheme mixtures allow for a higher current density without electromigration. In another embodiment, the nanoparticles may be copper oxide that is later reduced back copper during a sintering step that is described hereinbelow. In another example, the nanoparticles may be selected to bond to a metal post formed from a different metal than copper.

[0023] FIGS. 2C-2D illustrate how a "bead" or a "bump" 212 may build up on the top of metal post 204 formed from multiple droplets 211 dispensed from inkjet printer 210.

[0024] FIGS. 2E-2F illustrate how die 202 may be "flipped" and positioned over a leadframe 220. Leadframe 220 will usually have a set of leads, each of which has a contact region 221. Each post 204 is designed to align with a particular contact region 221. In these drawings, only a small part of leadframe 220 is shown for clarity. After the flipped die 202 is aligned with leadframe 220, it may be lowered so that each post 204 and bump 212 is brought into contact with each corresponding contact region 221.

[0025] FIG. 2F illustrates the result of a sintering process in which the bump 212 that is formed by metal nanoparticles is converted into a solid structure 213. Sintering is the process of compacting and forming a solid mass of material by heat and/or pressure without melting it to the point of liquefaction. The atoms in the materials may diffuse across the boundaries of the particles, fusing the particles together and creating one solid piece. Usually, the sintering temperature does not have to reach the melting point of the material; therefore sintering is often chosen as the shaping process for materials with extremely high melting points. Most, if not all, metals can be sintered. This applies especially to pure metals produced in vacuum which suffer no surface contamination.

[0026] Sintering the nanoparticles of bump 212 produces a solid structure 213 that forms a

sintered metal bond between post 204 and contact region 221 of leadframe 220. Adhesion of the sintered metal to the metal surface of the post and lead frame may occur in three ways, namely: (a) van der Waals forces, (b) mechanical adhesion/roughness, and (c) through the nanoparticle or lead frame surface chemical diffusion into the other. Unlike a joint formed by eutectic solder, sintered metal bond 213 will not melt and degrade the bond if the die is heated a second time.

[0027] Each sintered metal bond is usually porous as a result of spaces that remain between the nanoparticles after the sintering process. However, a sintering process may be continued until porosity is reduced or eliminated. A porous sintered bond may reduce thermo-mechanical reliability risk due to an ability to flex in response to stress applied to the bond by thermal or mechanical forces. The amount of porosity may be controlled by controlling one or more aspects of the sintering process, such as: selecting the size of the nanoparticles, selecting the temperature profile or other process parameters used to perform the sintering process, etc. Another way to control porosity is to add a sacrificial nanoparticle to the ink, such as poly-methyl methacrylate, or other polymer, silica, etc; then remove these particles during the sintering or after the sintering to increase the porosity. A nanoparticle sintered metal bond may have a porosity of approximately 20%. Generally, porosity may be selected to fall within a range of 0%-50%, while still providing good current carrying capacity and structural integrity.

[0028] Sintering may be performed in a number of ways. For example, the parts may be heated to an elevated temperature, but are not required to be heated to the melting point of the metal that forms the nanoparticles. For example, copper nanoparticles may be heated to a range of 80-300°C to form a solid structure. For comparison, the melting point of copper is 1,085°C.

[0029] FIG. 3 is a plot illustrating melting point vs. particle size for copper nanoparticles in a sintering process. The small nanoparticles may melt together at very low temperatures; however, as they melt together they get larger which causes the "bulk" melting temperature of the nanopartilces to go up. This causes an irreversible process in which higher temperature will only make the particles get bigger and thus melt at an even higher temperature. Thus, after the small nanoparticles are melted, the resulting structure cannot be un-melted like solder, unless the melting point of the bulk metal is reached. In the example of FIG. 3, sintering may occur at a temperature range of 80-300°C for copper nanoparticles, but the resulting sintered metal bond cannot be re-melted unless the temperature of the sintered metal structure is raised to 1085C, which is the melting point of bulk copper.

[0030] For example, in another embodiment, copper oxide nanoparticles may be sintered using a Xenon flash lamp using a known or later developed photon sintering process.

[0031] In another example, copper oxide nanoparticles may be sintered in a reducing atmosphere using a known or later developed forming gas or formic acid sintering process. In this case, the copper oxide is converted back to pure copper by the formic acid process. Usually, this process may be performed at a temperature in the range of 200-250°C.

[0032] FIGS. 4A-4D are a series of cross sectional views of another embodiment in which a sintered metal bond is formed. In this embodiment, a bump 412 may be formed on each contact region of leadframe 420 by depositing a series of droplets 411 that contain metal nanoparticles onto the contact region 421 of leadframe 420 by an inkjet printer 210. For example, as described hereinabove, the metal nanoparticles may be copper, or a mixture of copper and silver, or other metals. In another example, the nanoparticles may be a mixture of copper and graphene, or copper and graphite. The graphite/grapheme mixtures allow for a higher current density without electromigration. In another embodiment, the nanoparticles may be copper oxide that is later reduced back copper during a sintering step that is described hereinbelow. In another example, the nanoparticles may be selected to bond to a metal post formed from a different metal than copper.

[0033] FIG. 4C illustrates how die 402 may be "flipped" and positioned over leadframe 420. Die 402 may be similar to die 202 with a post 404 formed on each contact region of die 402 as described hereinabove. Leadframe 420 will usually have a set of leads, each of which has a contact region 421. Each post 404 is designed to align with a particular contact region 421. In these drawings, only a small part of leadframe 420 is shown for clarity. After the flipped die 402 is aligned with leadframe 420, it may be lowered so that each post 404 is brought into contact with each corresponding bump 412 on contact region 421.

[0034] FIG. 4D illustrates the result of a sintering process in which the bump 412 that is formed by metal nanoparticles is converted into a solid structure 413. As described hereinabove, sintering is the process of compacting and forming a solid mass of material by heat and/or pressure without melting it to the point of liquefaction. Sintering the nanoparticles of bump 412 produces a solid structure 413 that forms a sintered metal bond between post 404 and contact region 421 of leadframe 420. Unlike a joint formed by eutectic solder, sintered metal bond 413 will not melt and ruin the bond if the die is heated a second time.

[0035] FIG. 5 is a cross sectional view of a completed integrated circuit 500. Integrated circuit 500 may be formed using the sintered metal bonding process described in either FIGS. 2A-2G or 4A-4D. Semiconductor die 502 includes circuitry that may be connected to contact pads on which metal posts 504 are formed. Bumps may be formed on contact regions of leadframe 520 or on the posts 504, in which the bumps are formed with a material that includes metal nanoparticles. IC die 502 may be attached to leadframe 520 by aligning the metal posts 504 to the leadframe and sintering the metal nanoparticles in the bumps to form a sintered metal bond between each metal post and contact region of the leadframe, as described hereinabove.

[0036] In another example, a portion of the bumps may be formed on a portion of the posts, and another portion of the bumps may be formed on a portion of the contact regions of the leadframe.

[0037] After die 502 is attached to leadframe 520, a molding process may be performed to conventionally encapsulate the die and leadframe to form finished IC 500.

[0038] Finished IC 500 may be mounted on a substrate, such as a fiberglass printed circuit board, a ceramic circuit board, or any other known or later developed type of single layer or multilayer system substrate on which are formed various signal traces. For example, other ICs and electronic components may also be mounted on the substrate to form an electronic device or system.

[0039] Some integrated circuits have no-lead packages such as quad-flat no-leads (QFN) and dual-flat no-leads (DFN) devices that physically and electrically couple integrated circuits to printed circuit boards. Flat no-lead devices, also known as micro leadframe (MLF) and small outline no-leads (SON) devices, are based on a surface-mount technology that connects integrated circuits to the surfaces of printed circuit boards without through-holes in the printed circuit boards. In some examples, flat no-lead packages are near chip scale plastic encapsulated packages usually fabricated with a planar copper leadframe substrate. Perimeter lands on the package provide electrical coupling to the printed circuit board. The lands serve as contacts and may be referred to as leads internal to the integrated circuit; however, the leads do not extend beyond the boundaries of the integrated circuit package.

[0040] FIG. 6 is an illustration of a portion of a leadframe strip 600 that illustrates four repetitions of a leadframe 620. Each leadframe 620 includes a set of leads, such as lead 622, that may transition into a corresponding set of pins, such as pin 623. Each lead has a contact region

621 that is intended to align with a post on a semiconductor die. For example, as described hereinabove, dots of metallic nanoparticle material may be added to each contact region 621 on each leadframe 620 by an inkjet process. Alternatively, another additive process may be used to create the metallic nanoparticle bumps, such as: screen printing, electrostatic spraying, etc.

[0041] In this manner, an IC may be fabricated and attached to a leadframe in which sintered metal bonds are formed between the contacts on the IC die and the contact regions of the leadframe. Sintering may be performed at a temperature that is much lower than the melting point of the metal nanoparticles being use. For example, this allows the use of organic substrates for the leadframe structure or other substrate structure, which would not withstand a higher temperature process.

[0042] A sufficient volume of nanoparticle material may be printed for each bump to compensate for expected non-coplanarity of the die to substrate surface.

[0043] Sintering eliminates the problem of intermetallic growth between copper and tin-based Pb-free solder. Brittle solder fatigue and thermally activated void growth in solder may be eliminated by the sintered metal bond. Current carrying capacity of the joint may also be enhanced.

Other Embodiments

[0044] More embodiments are possible. For example, instead of copper posts and leadframes, other embodiments may use other types of metal for the posts and/or leadframes, such as aluminum, gold, nickel, etc.

[0045] Different metallic nanoparticles may be used in various embodiments, such as: copper, copper-silver hybrid, copper oxide, copper graphite, copper graphene, etc.

[0046] FIGS. 7A-7B illustrate another embodiment for forming posts. For example, in another embodiment, instead of printing a nanoparticle bump on top of a solid metal post, the entire post (or a significant portion thereof) may be formed by inkjet printing the nanoparticle material. In FIG. 7A, a small portion of a semiconductor die 702 is illustrated. Die 702 may extend to the left and to the right to include various circuitry and multiple contact regions. In this illustration, only a single contact region 707 is illustrated. On top of contact region 707, a COA copper layer has been deposited to form metal feature 703 that is in contact with contact region 707. For example, COA layer 703 may be applied by sputtering. A photo resist layer may then be applied and patterned to form metal region 703.

[0047] A stream of ink droplets 711 may then be applied to metal region 703 by inkjet printer 210 to form a metallic post 704. After die 702 is attached to a leadframe or other substrate, a sintering process as described hereinabove may be used to convert post 704 into a solid sintered metal post that is bonded to the leadframe, as described hereinabove.

[0048] FIG. 8 is an illustration of two semiconductor dies 801, 802 mounted to a multilayer substrate 840. For example, in other embodiments, instead of mounting a semiconductor die to a stamped or etched metal leadframe, the leadframe may be a multilayer substrate that has contact areas patterned onto it. In such an embodiment, the substrate 840 may extend beyond the semiconductor die, and two or more ICs and/or other electronic components may be mounted on the substrate. For example, the substrate may be a fiberglass printed circuit board, a ceramic circuit board, or any other known or later developed type of single layer or multilayer system substrate on which are formed various signal traces. For example, in this case, nanoparticle bumps such as bumps 841, 842 may be formed on each of the dies as described with regard to FIGS. 2A-2D, or may be formed on the substrate as described with respect to FIGS. 4A-4B. After the dies 801, 802 are mounted on substrate 840, all of the nanoparticle bumps may be sintered as described hereinabove in a single operation to form sintered metal bonds between the contact regions on the substrate and the contact posts on the dies.

[0049] Instead of flip chip configurations, other embodiments may be formed using sintered metal bonds, such as: stacked dies, dies with through silicon vias, etc.

[0050] In this description, the term "couple" and derivatives thereof mean an indirect, direct, optical, and/or wireless electrical connection. For example, if a first device couples to a second device, that connection may be through a direct electrical connection, through an indirect electrical connection via other devices and connections, through an optical electrical connection, and/or through a wireless electrical connection.

[0051] Although method steps may be presented and described herein in a sequential fashion, one or more of the steps shown and described may be omitted, repeated, performed concurrently, and/or performed in a different order than the order shown in the drawings and/or described herein. Accordingly, embodiments are not limited to the specific ordering of steps shown in the drawings and/or described herein.

[0052] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method for fabricating an integrated circuit, the method comprising:

fabricating an integrated circuit (IC) die having a plurality of contacts;

forming a metal post on each of the plurality of contacts;

forming a plurality of bumps on a plurality of contact regions of a leadframe or on the posts, wherein the plurality of bumps are formed with a material that includes metal nanoparticles; and

attaching the IC die to the leadframe by aligning the metal posts to the leadframe and sintering the metal nanoparticles in the plurality of bumps to form a sintered metal bond between each metal post and corresponding contact region of the leadframe.

2. The method of claim 1, wherein the sintering the metal nanoparticles forms a sintered metal bond that is porous.

3. The method of claim 2, wherein the sintered metal bond has a porosity ranging from 0% – 50%.

4. The method of claim 1, wherein a portion of the plurality of bumps is formed on a portion of the posts and another portion of the plurality of bumps is formed on a portion of the contact regions of the leadframe.

5. The method of claim 1, wherein forming the plurality of bumps is done by printing with an inkjet printer.

6. The method of claim 1, wherein forming a metal post is done by printing with an inkjet printer.

7. The method of claim 1, wherein sintering the metal nanoparticles is done by heating, by use of a Xenon flash tube, or by use of Formic acid.

8. The method of claim 1, wherein the metal nanoparticles include copper nanoparticles and silver nanoparticles.

9. The method of claim 1, wherein the metal nanoparticles include copper oxide nanoparticles.

10. The method of claim 1, wherein the metal nanoparticles include copper nanoparticles and graphite nanoparticles.

11. An integrated circuit comprising:

an integrated circuit (IC) die with a plurality of contacts, wherein a metal post is formed on each of the plurality of contacts; and

a leadframe, wherein a plurality of contact regions on the lead frame are aligned with the plurality of contacts and metal posts and coupled thereto by sintered metal bonds.

12. The IC of claim 11, wherein the sintered metal bonds are porous.

13. The IC of claim 12, wherein the sintered metal bond has a porosity ranging from 0% – 50%.

14. The IC of claim 11, wherein the sintered metal bonds include copper nanoparticles and silver nanoparticles.

15. The IC of claim 11, wherein the sintered metal bonds include copper oxide nanoparticles.

16. The IC of claim 11, wherein the sintered metal bonds include copper nanoparticles and graphite nanoparticles.

17. An integrated circuit leadframe comprising:

a plurality of leads configured to couple to a plurality of contacts on an integrated circuit die; and

a plurality of bumps formed on the plurality of leads configured to align with the plurality of contacts on the integrated circuit die, wherein the bumps are formed with a material that includes metal nanoparticles.

18. The leadframe of claim 17, wherein the leadframe is a multi-layer substrate.

19. The leadframe of claim 17, wherein the bumps have been sintered to form sintered metal bonds that are porous.

20. The leadframe of claim 17, wherein the metal nanoparticles include copper nanoparticles and silver nanoparticles; copper oxide nanoparticles; or copper nanoparticles and graphite nanoparticles.

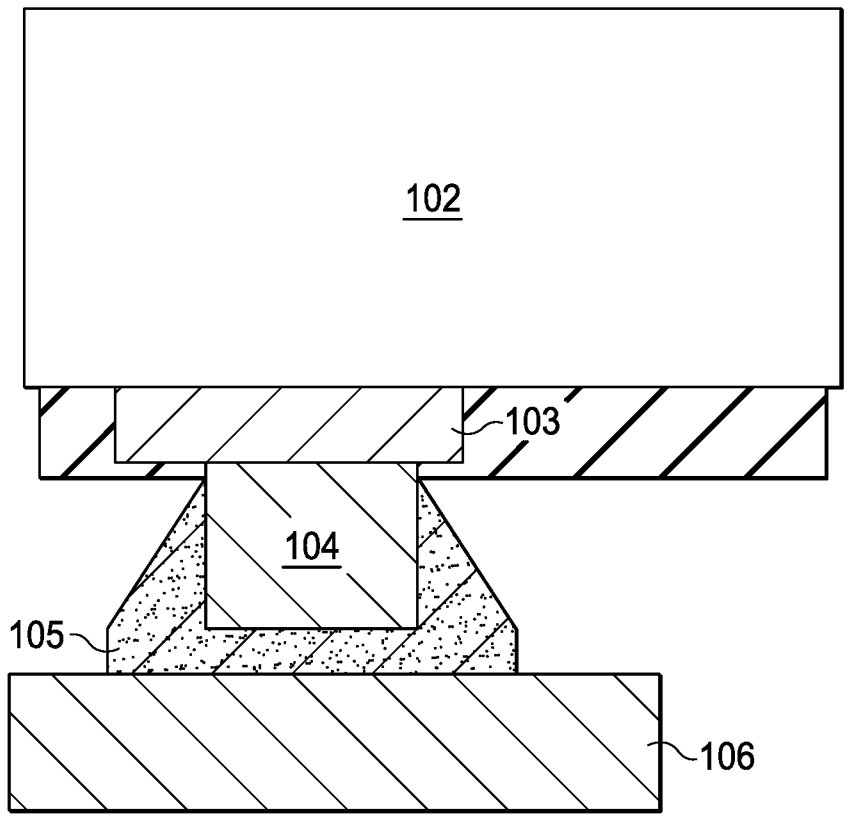


FIG. 1
(PRIOR ART)

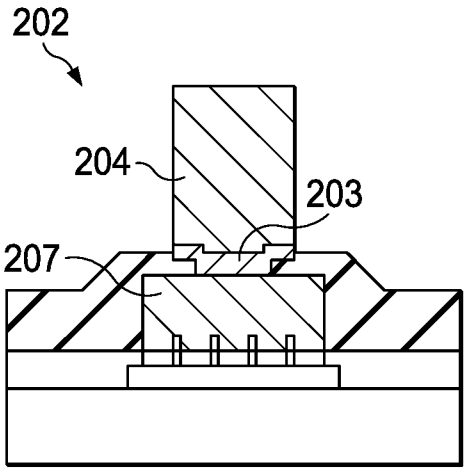


FIG. 2A

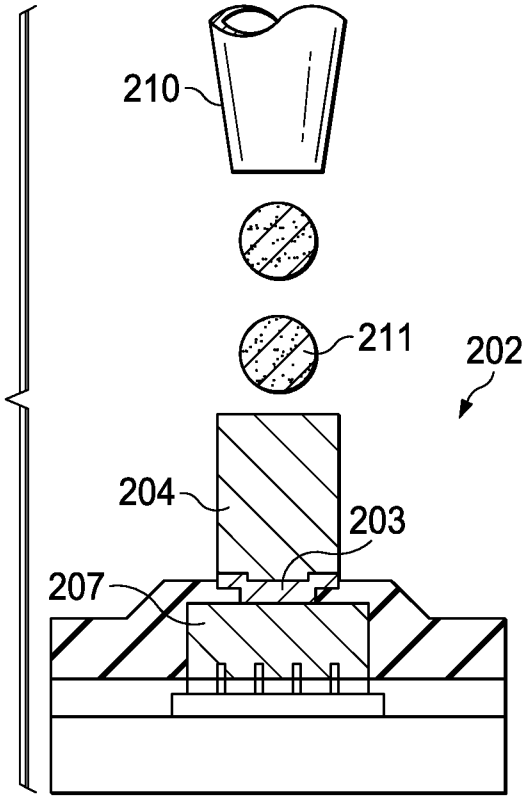


FIG. 2B

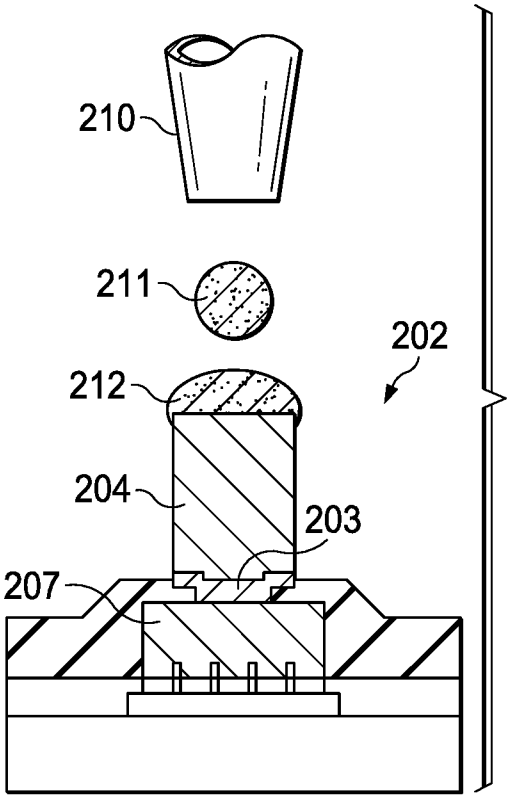


FIG. 2C

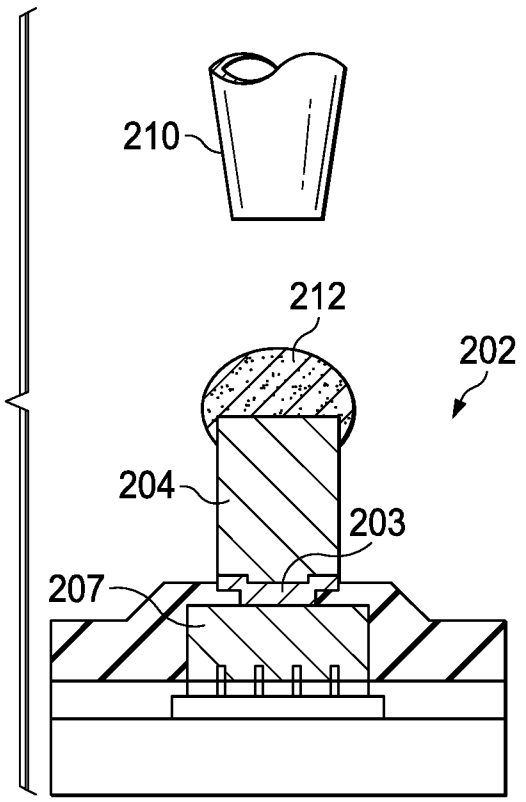


FIG. 2D

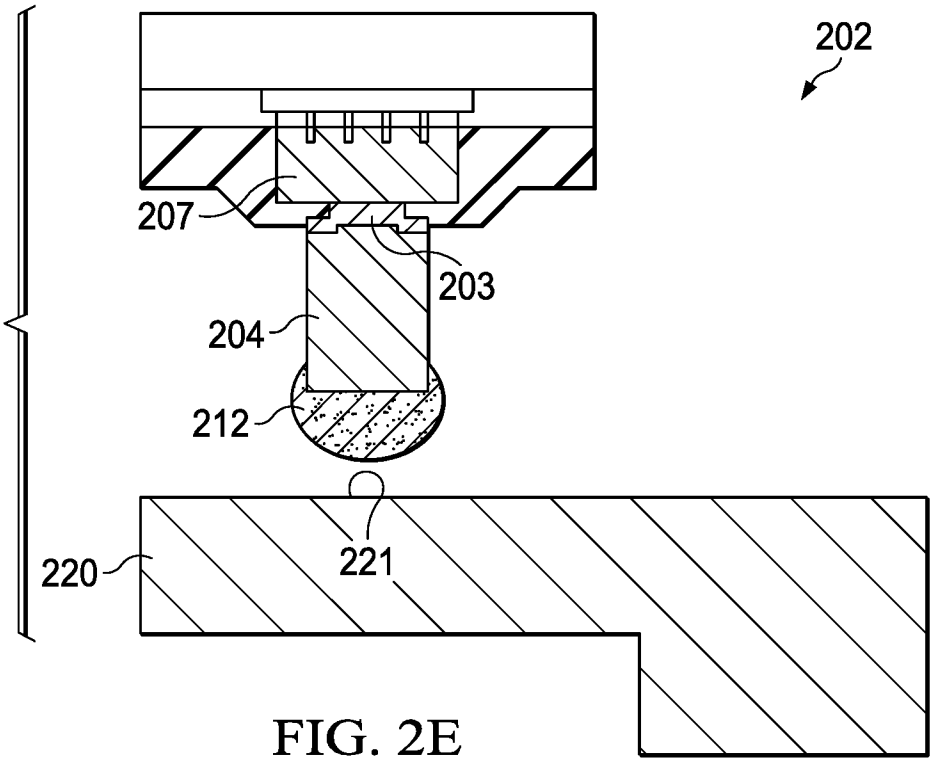


FIG. 2E

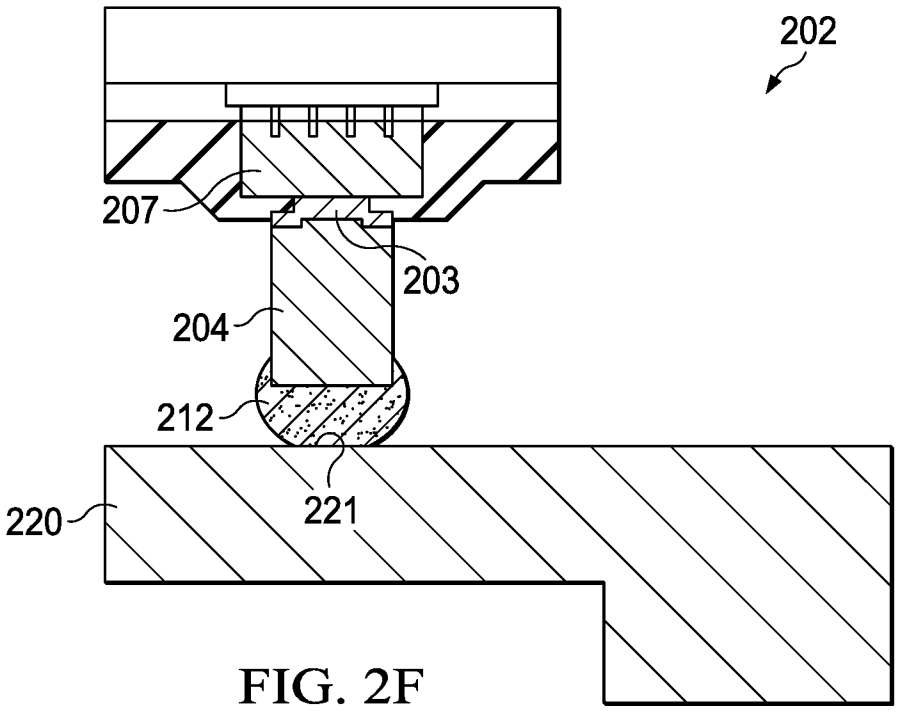
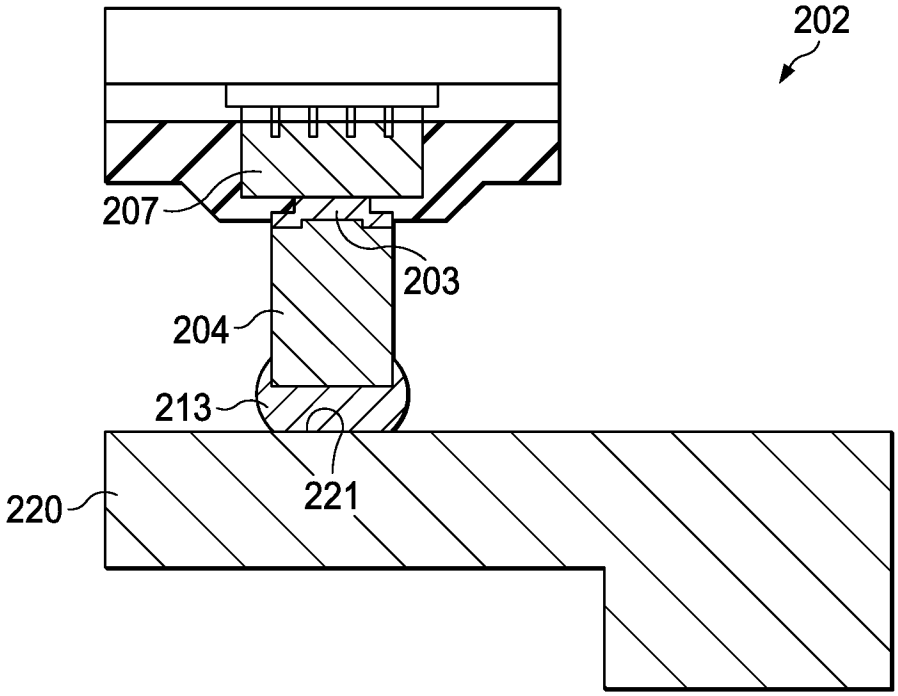


FIG. 2F

FIG. 2G


202
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203
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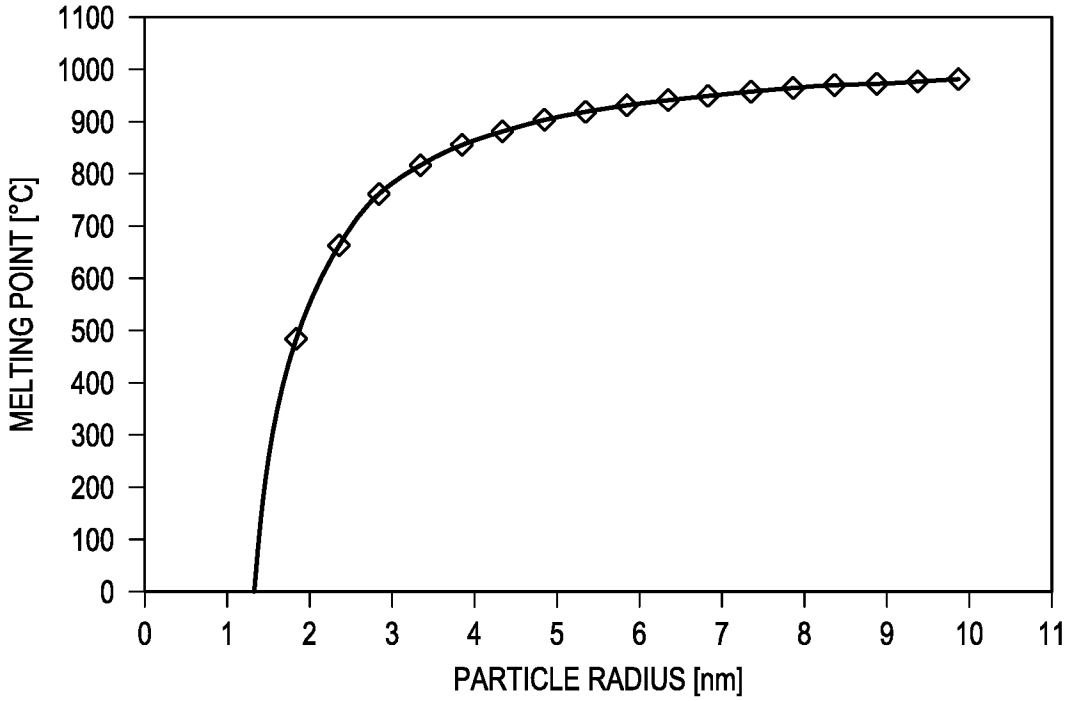
213
221
220

FIG. 3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900
800
700
600
500
400
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200
100
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0
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2
3
4
5
6
7
8
9
10
11
PARTICLE RADIUS [nm]

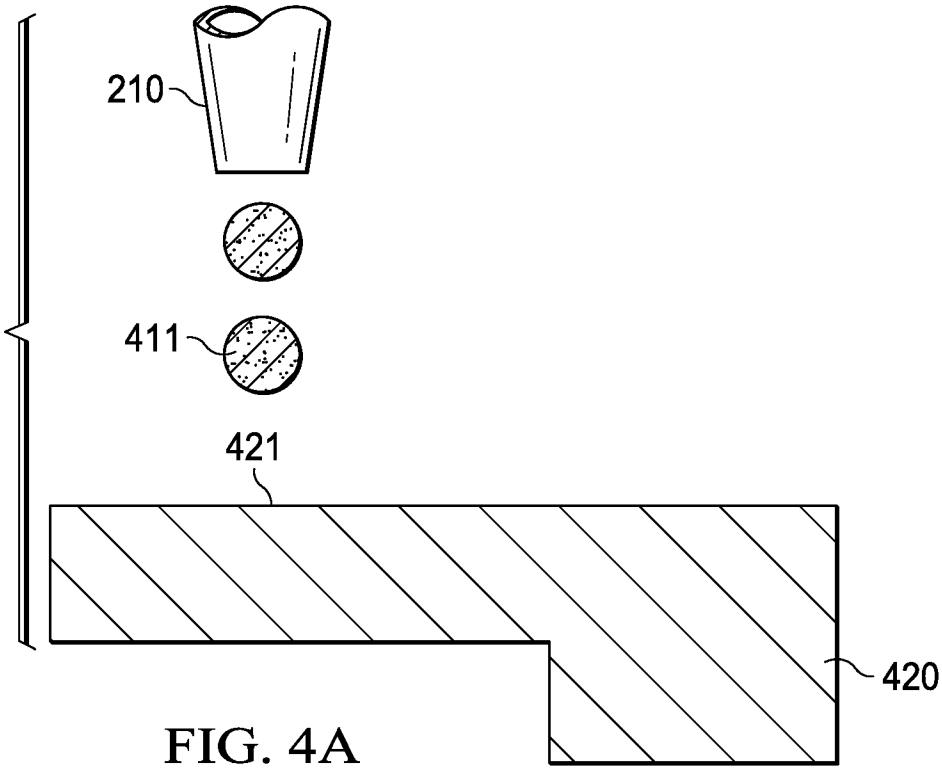


FIG. 4A

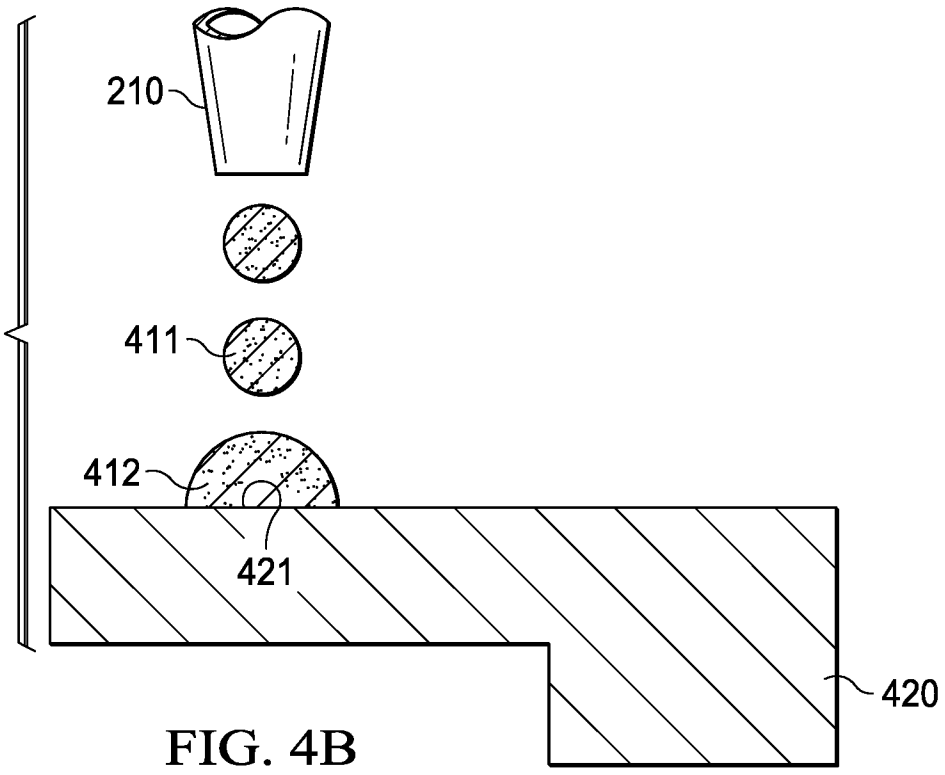


FIG. 4B

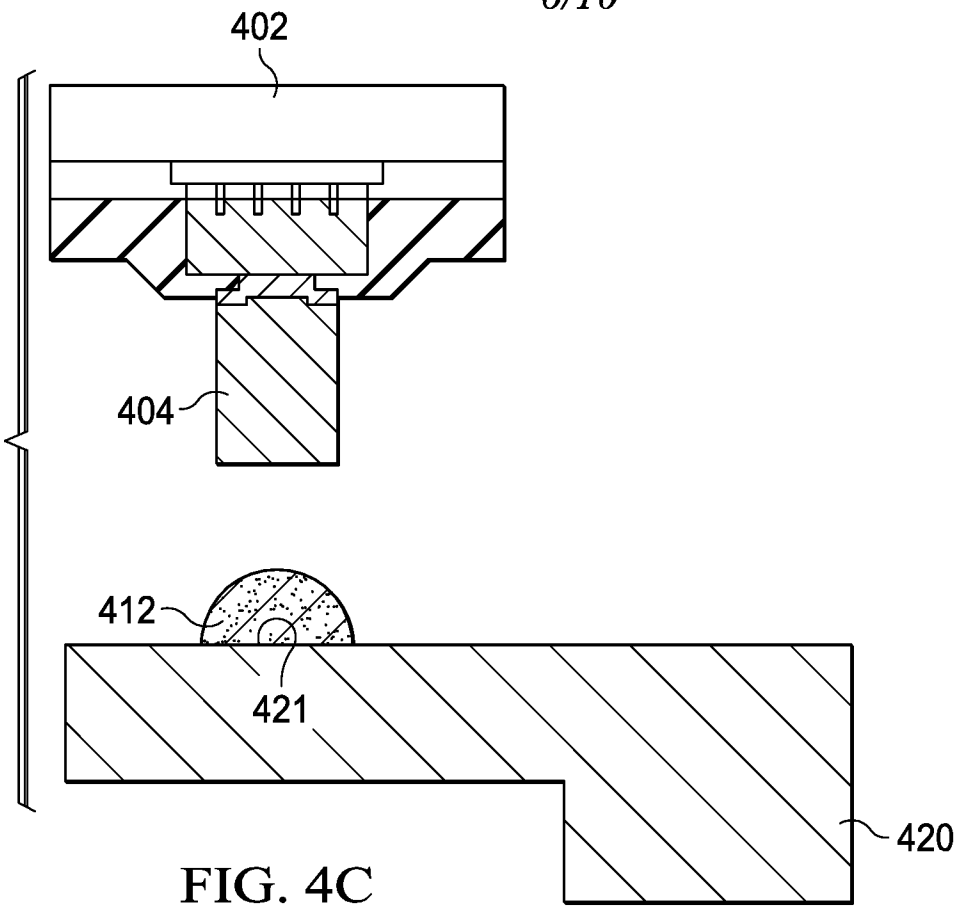


FIG. 4C

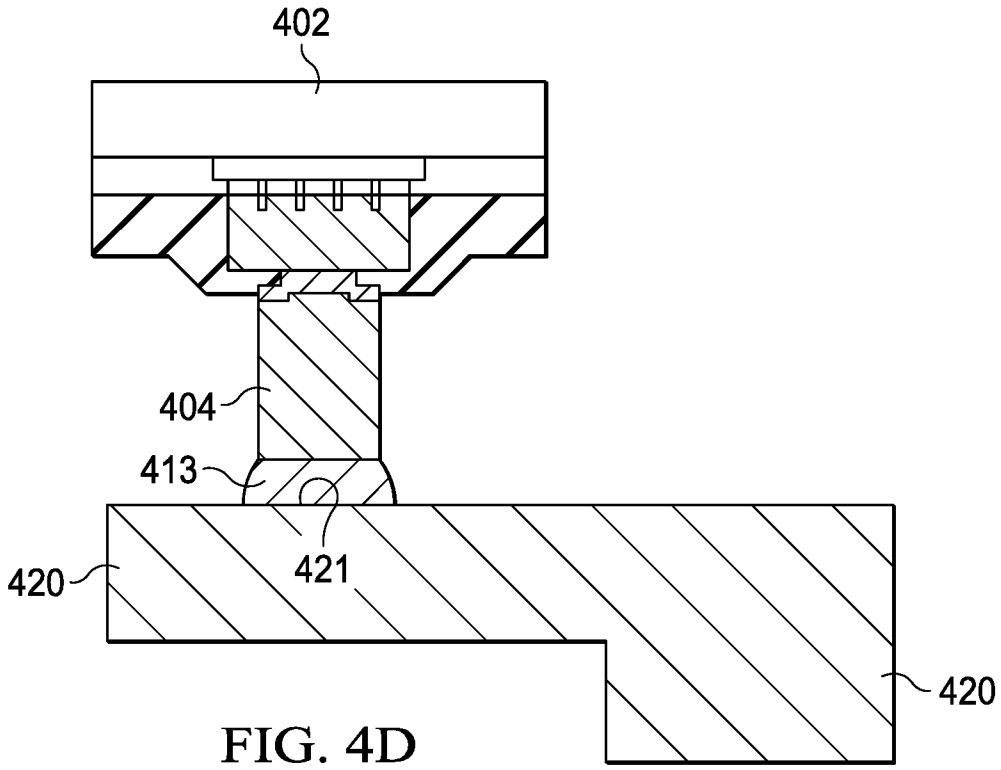
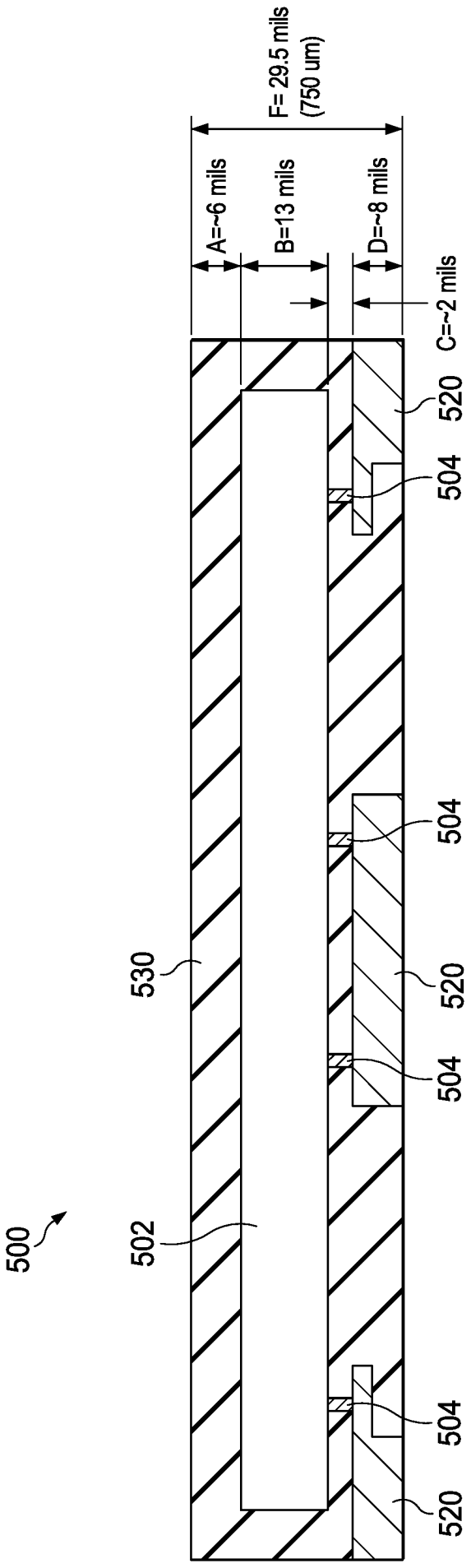


FIG. 4D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(750 um)
A=~6 mils
B=13 mils
D=~8 mils
C=~2 mils
520
504
504
530
520
504
500
502
504
520

FIG. 5

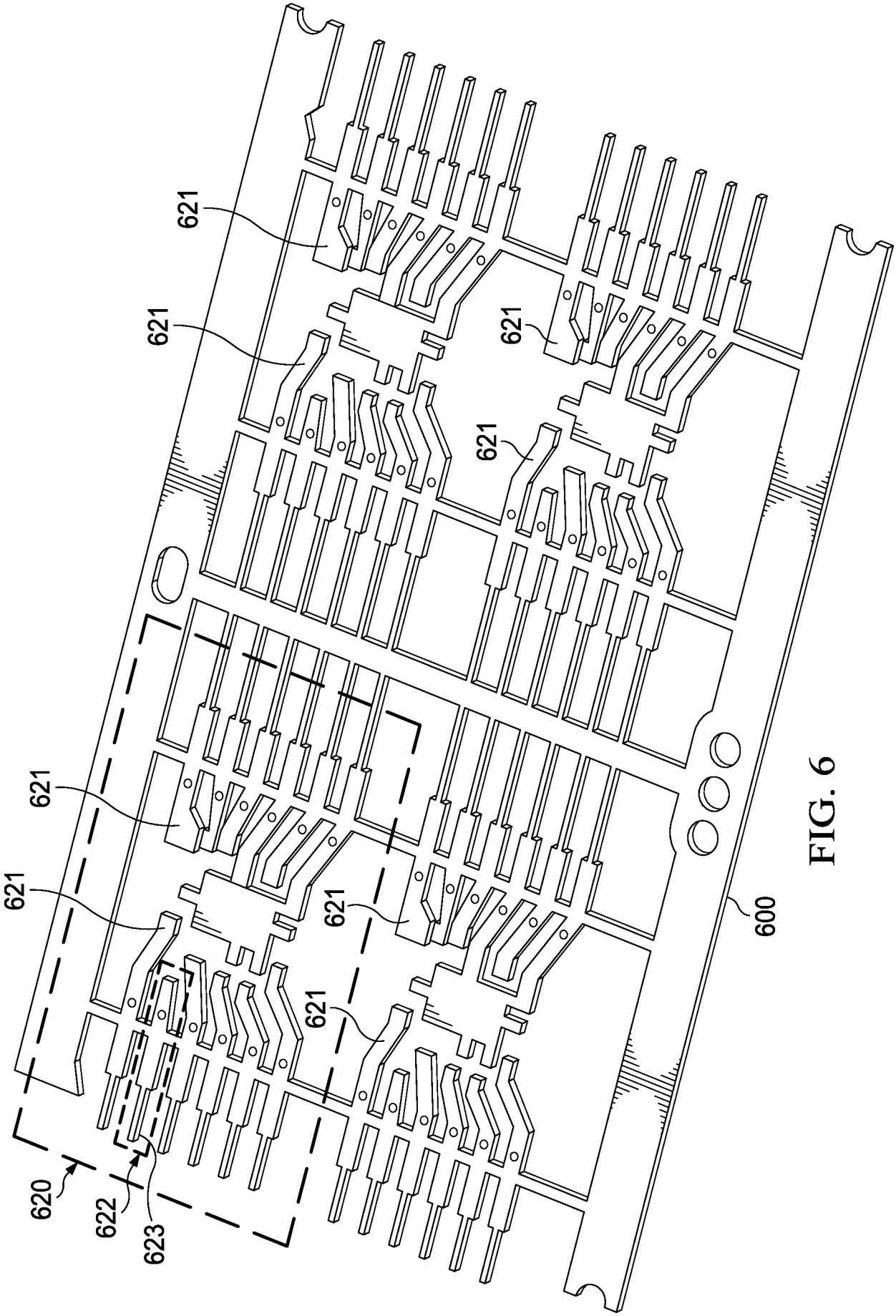

FIG. 6

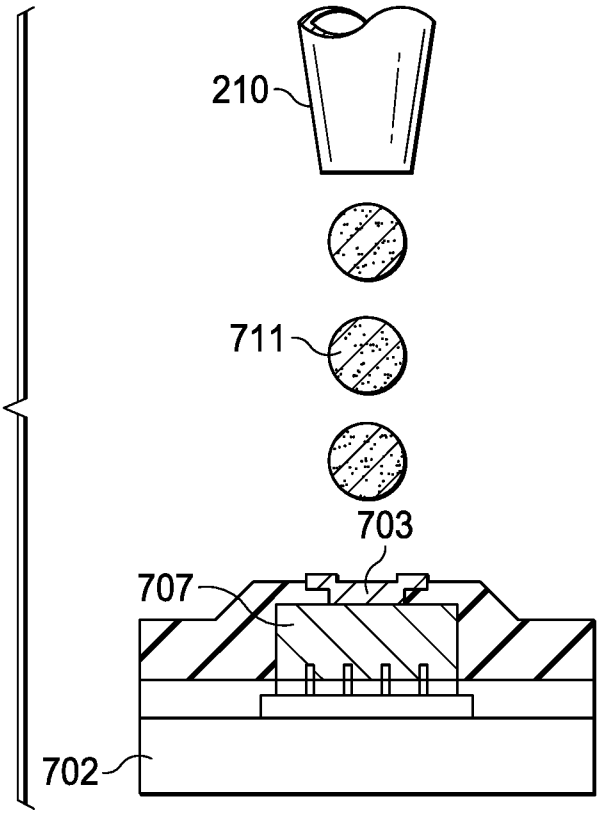

FIG. 7A

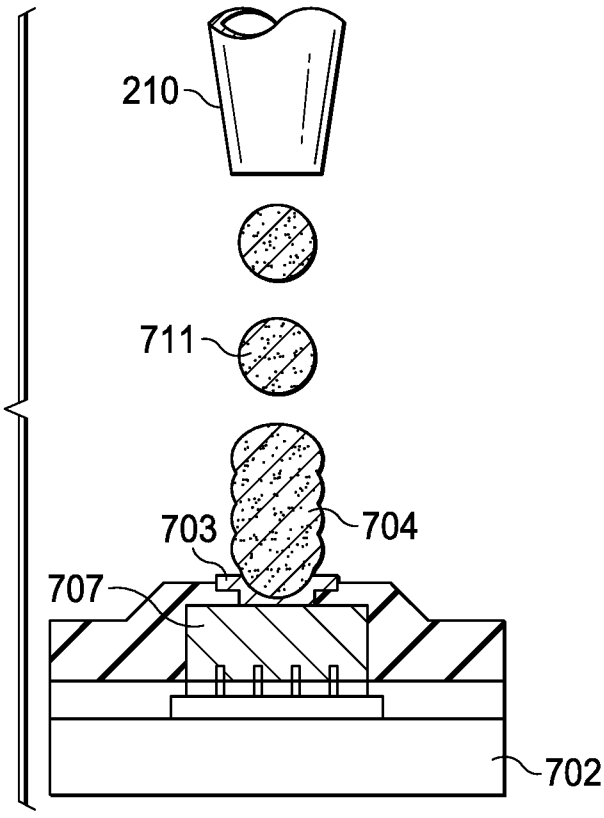

FIG. 7B

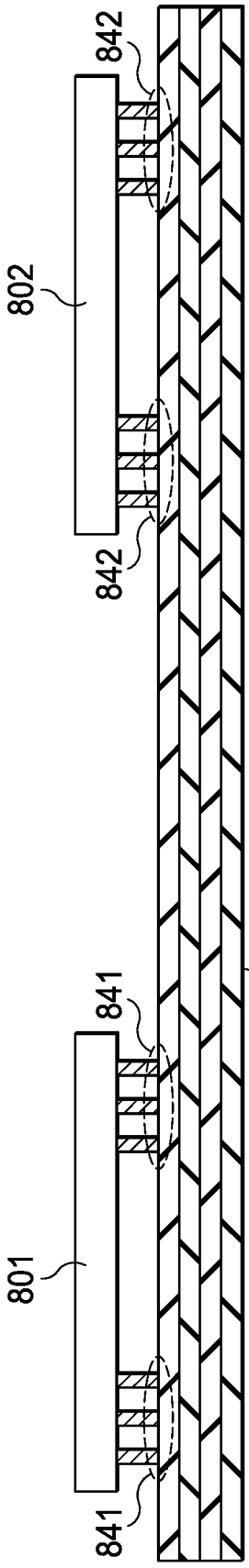

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/029000

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/495 *(2006.01)*
H01L 23/50 *(2006.01)*
B22F 3/10 *(2006.01)*
B82Y 30/00 *(2011.01)*
B33Y 80/00 *(2015.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00, 23/488, 23/495, 23/50, 23/52, B22F 3/10, 5/00, B82B 3/00, B82Y 30/00, 80/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0012246 A1 (VERTICAL CIRCUITS, INC.) 20.01.2011, [0002], [0003], [0005], [0006], [0109], claims 1, 16	1-8, 10-14, 16-20
A		9, 15
Y	US 2014/0077351 A1 (TESSERA, INC.) 20.03.2014, abstract, [0146], [0149], [0145], [0077]	1-8, 10, 14, 16-20
Y	US 2010/0006994 A1 (STATS CHIPPAC, LTD.) 14.01.2010	11-14, 16
Y	WO 1996/025763 A2 (INTERNATIONAL BUSINESS MACHINES CORPORATION et al.) 22.08.1996, p. 2, par. 2	18

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 June 2017 (08.06.2017)	13 July 2017 (13.07.2017)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	A. Pimenova Telephone No. 8-499-240-25-91