FORM 1

COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952

623458

Application for a Standard Patent or A Standard Patent of Addition

We, ALCATEL N.V. of Strawinskylaan 341
1077 XX Amsterdam, The Netherlands,

, hereby apply for the grant of a standard patent/~~patent of addition~~ for an invention entitled

"JITTER REDUCTION CIRCUIT IN A DEMULTIPLEXER"

which is described in the accompanying ~~provisional~~/complete specification.
Details of basic application(s) –

Number of basic application	P 38 42 694.3
Name of Convention country in which basic application was filed	Germany
Date of basic application	19 December 1988

Our address for service is:

PATENT DEPARTMENT,
STANDARD TELEPHONES AND CABLES PTY. LIMITED,
252-280 BOTANY ROAD,
ALEXANDRIA, N.S.W. 2015.
AUSTRALIA.

Dated this Eleventh day of December 19 89

ALCATEL N.V.

FO13083 13/12/87

BY: .....
Signature of Applicant
B. O'Connor

To: The Commissioner of Patents

FORM 8

COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952 - 1969

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT OR A PATENT OF ADDITION

In support of the Convention application made for a patent ~~xxxxxxxxxxxx~~ for an invention entitled

"JITTER REDUCTION CIRCUIT IN A DEMULTIPLEXER"

I, BRIAN PATRICK O'CONNOR
of STANDARD TELEPHONES AND CABLES PTY. LIMITED, 252-280 Botany Road, Alexandria, 2015, N.S.W., Australia
do solemnly and sincerely declare as follows:-

1. I am authorised by ALCATEL N.V.
the applicant for the patent ~~xxxxxxxxxxxx~~ to make this declaration on its behalf.

2. The basic application as defined by Section 141 of the Act was/~~xxxxx~~ made in Germany

on 19 December 1988

by STANDARD ELEKTRIK LORENZ AG

3. DR. RAINER HEISS, a German citizen, of Lerchenstrasse 8, 7015 Korntal-Munchingen, Federated Republic of Germany, and THOMAS MICKE, a German citizen, of Christophstrasse 37, 7000 Stuttgart 1, Federated Republic of Germany

~~is~~/are the actual inventor of the invention, and the facts upon which the applicant is entitled to make the application are as follows:-

ALCATEL N.V. is the Assignee of STANDARD ELEKTRIK LORENZ AG who is is the Assignee of the SAID INVENTORS.

4. The basic application referred to in paragraph 2 of this Declaration was/~~xxxx~~ the first application in a Convention country in respect of the invention the subject of the application.

Declared at Sydney this 11th day of December 1989.

ALCATEL N.V.

.....
Signature of Declarant
B. O'Connor

To: The Commissioner of Patents.

(12) PATENT ABRIDGMENT (11) Document No. AU-B-46117/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 623458

(54) Title
JITTER REDUCTION CIRCUIT IN A DEMULTIPLEXER

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(71) Applicant(s)
ALCATEL N.V.

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DR. RAINER HEISS; THOMAS MICKE

(74) Attorney or Agent
ALCATEL AUSTRALIA LIMITED , BOX 525 G.P.O., SYDNEY N.S.W. 2001

(56) Prior Art Documents
AU 530661 61954/80 H03L 7/06 H04J 3/06 H04L 7/00

(57) Claim

1. A demultiplexer for a digital time-division multiplex communication system wherein a digital signal which is asynchronous with the pulse frame and comprises successive blocks whose beginnings are marked with sync words is inserted into the pulse frame, said demultiplexer comprising a circuit which derives from the clock of the received sync words a sync signal which exhibits less jitter than the clock of the received sync words, wherein the circuit contains a measuring device which measures the time intervals between the received sync words, a filter which takes the average of the time intervals between the sync words, and a signal generator which forms the sync signal from said average in such a manner that the pulse period of the sync signal is equal to said average.

623458

his document contains the amendments allowed under Section 83 (2) by the Supervising Examiner on

.....

and is correct for printing

: : .....

ORIGINAL

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PATENTS ACT 1952-1969

COMPLETE SPECIFICATION FOR THE INVENTION ENTITLED

"JITTER REDUCTION CIRCUIT IN A DEMULTIPLEXER"

The following statement is a full description of this invention, including the best method of performing it known to us:-

This invention relates to a demultiplexer for a digital time-division multiplex communication system wherein a digital signal which is asynchronous with the pulse frame and consists of successive blocks whose beginnings are marked with sync words is inserted into the pulse frame, comprising a circuit which derives from the clock of the received sync words a sync signal which exhibits less jitter than the clock of the received sync words.

Such a demultiplexer is disclosed in DE-A1-34 39 633. In a known demultiplexer, the sync signal is derived from the clock of the received sync words by correcting the word clock with the aid of additional information transmitted to the demultiplexer, such that the intervals between successive clock pulses are equal to the intervals between the sync words of the digital signal to be inserted into the pulse frame by the multiplexer at the transmitting end, which are asynchronous with the pulse frame. The jitter of the sync words caused by the asynchronous insertion of this signal, also referred to as "waiting-time jitter", is thus clearly reduced in the demultiplexer

This known arrangement has the disadvantage that a circuit for generating the additional information is required at the transmitting end, and that through the transmission of this additional information, the amount of useful information that can be transmitted is reduced.

It is, therefore, an object of the present invention to provide a demultiplexer which reduces the waiting-time jitter without any steps having to be taken in the associated multiplexer at the transmitting end.

According to the invention there is provided a demultiplexer of the aforementioned type, wherein the circuit contains a measuring device which measures the time intervals between the received sync words, a filter which takes the average of the time intervals between the sync words, and a signal generator which forms the sync signal from said average in such a manner that the pulse period of the sync signal is equal to said average. The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of the novel circuit for reducing waiting-time jitter;

Figure 2 shows a first embodiment of the filter F of Figure 1, and

Figure 3 shows a second embodiment of the filter F of Figure 1.

Referring to Figure 1, when a sync word has been detected in a sync-word detector (not shown), a pulse I generated in the sync-word detector in response thereto is applied to a measuring device M over two leads.

The measuring device M contains a counter 1 and a register 2.

After receipt of a pulse I, the counter 1, clocked by a word clock WT provided by the demultiplexer (not shown), counts from zero until the next pulse I. It has then reached a count N_n, which is a measure of the time interval between these two pulses, i.e. between the two successive sync words just received. Different counts N_i are possible, where i=0, 1, 2, ..., m, ..., n, ...

This count N_n is transferred into the register 2, which is enabled by said next pulse I.

From the register 2, the count N_n is transferred into a filter F, which is also controlled by the pulses.

The filter F takes the average N', rounded to an integer, of the last received count and a predetermined number of previously received counts.

This average N' is fed to a signal generator S consisting of a down counter 3 and a comparator 4. After receipt of the average N', the down counter 3, clocked at the repetition rate of the word clock WT or an integral multiple thereof, counts from the average N' down to zero. Each numerical value is fed to the comparator 4, which compares it with the numerical value zero. When zero has been reached, the comparator produces a sync signal SY, to be exact: the edge of a sync signal SY, whose pulse period is equal to the average N'. The sync signal SY serves as the input signal for a phase-locked loop (PLL). It is fed back to the down counter 3, so that the latter can receive the next average N' from the filter F.

Figure 2 shows a first embodiment of the filter F of Figure 1.

A count N_n is fed both to an adder 21, where it is added to the sum of the last m counts up to N_{n-1} received from the register 2, i.e.

$$\sum_{i=n-m}^{n-1} N_i + N_n = \sum_{i=n-m}^{n} N_i$$

and to a shift register 22 containing the last m counts N_{n-m} to N_{n-1}.

Each time a pulse I is applied to the shift register 22, the counts N_i are shifted by one cell, the new count N_n is inserted into the cleared cell of the count N_{n-1}, and the "oldest" count N_{n-m} is applied to a subtractor 23.

The latter has two inputs, which are connected to the output of the shift register 22 and to the output of the adder 21, respectively. It forms the difference between the sum

$$\sum_{i=n-m}^{n} N_i + N_n = \sum_{i=n-m}^{n} N_i$$

from the output of the adder 21 and the count N_{n-m} from the shift register 22:

$$\sum_{i=n-m}^{n} N_i - N_{n-m} = \sum_{i=n-m+1}^{n} N_i$$

The difference formed by the subtracter 23 is coupled into a register 24, which is also clocked by the pulses I. From this register, it is transferred, on the one hand, to an additional adder 25 and, on the other hand, back to the adder 21 to form the new sum

$$\sum_{i=n-m+1}^{n=1} N_i$$

The adder 25 forms the sum of the difference and a rounding error R. The sum is coupled into a computing circuit 26 with two outputs, which takes the average of the counts N_i and rounds it to an integer N', transfers the latter to the signal generator S (see Figure 1), and feeds the rounding error R to a register 27, which is clocked by the pulses I and feeds the error that results

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from the previous round-off to the adder 25 simultaneously with the arrival of a new sum.

The rounding errors R are used to maintain the clock rate constant on an average.

A further embodiment of the filter F is shown in Figure 3.

It includes an adder 31 at the input end which forms the sum of the respective last count N_n from the register 2 (Figure 1) and an error signal FS from a register 35.

This sum is fed to one input of a two-input comparator 32 and to a subtracter 34. The other input of the comparator 32 is fed with the count from the output of a counter 33. If the value from the adder 31 is less than the count of the counter 33, the comparator 32 will decrease the count of the latter by 1; if, conversely, the value from the adder 31 is greater than the count of the counter 33, the comparator 32 will increase the count of the counter 33. If the two values are equal, the comparator 32 will leave the count unchanged. Before the circuit is put into operation, the counter 33 is set to an assumed average count via a line L.

The counter 33 is clocked by the pulses I. Its output is connected to the input of the signal generator S of Figure 1 and to the subtracter 34.

The subtracter 34 forms the difference between the count of the counter 33 and the sum received from the adder 31. This difference represents the error signal FS, which is applied to the register 35, which is clocked by the pulses I and feeds the error signal FS to the adder 31 upon arrival of the next count N_{n+1} at the input of this adder. The latter then forms the sum of the count N_{n+1} and the error signal FS again.

In this manner, an average count N' can be set in the counter 33. The counts delivered by the counter to the signal generator S thus vary much less than the counts presented to the adder 31.

The claims defining the invention are as follows:

1. A demultiplexer for a digital time-division multiplex communication system wherein a digital signal which is asynchronous with the pulse frame and comprises successive blocks whose beginnings are marked with sync words is inserted into the pulse frame, said demultiplexer comprising a circuit which derives from the clock of the received sync words a sync signal which exhibits less jitter than the clock of the received sync words, wherein the circuit contains a measuring device which measures the time intervals between the received sync words, a filter which takes the average of the time intervals between the sync words, and a signal generator which forms the sync signal from said average in such a manner that the pulse period of the sync signal is equal to said average.

2. A demultiplexer as claimed in claim 1, wherein the filter takes the average of the time intervals between successive sync words successively over a predetermined period of time, and rounds it to an integer N′, the rounding error being taken into account for the subsequent averaging by error feedback.

3. A demultiplexer as claimed in claim 1, wherein the filter includes a counter in which an assumed mean distance between sync words is stored before the circuit is put into operation, that the counter can increase or decrease its count by a fixed amount only once during an interval between two sync words or leaves it unchanged, and that the change is determined by the result of a numerical comparison between the count of the counter and the sum of a subsequent count appearing at the input of the filter and an error signal.

4. A demultiplexer substantially as herein described with reference to Figures 1 of the accompanying drawings.

5. A demultiplexer substantially as herein described with reference to Figs. 1 and 2 of the accompanying drawings.

6. A demultiplexer substantially as herein described with reference to Figs. 1 and 3 of the accompanying drawings.

DATED THIS TWENTY-FIFTH DAY OF FEBRUARY 1992
ALCATEL N.V.

AUSTRALIAN PATENT OFFICE

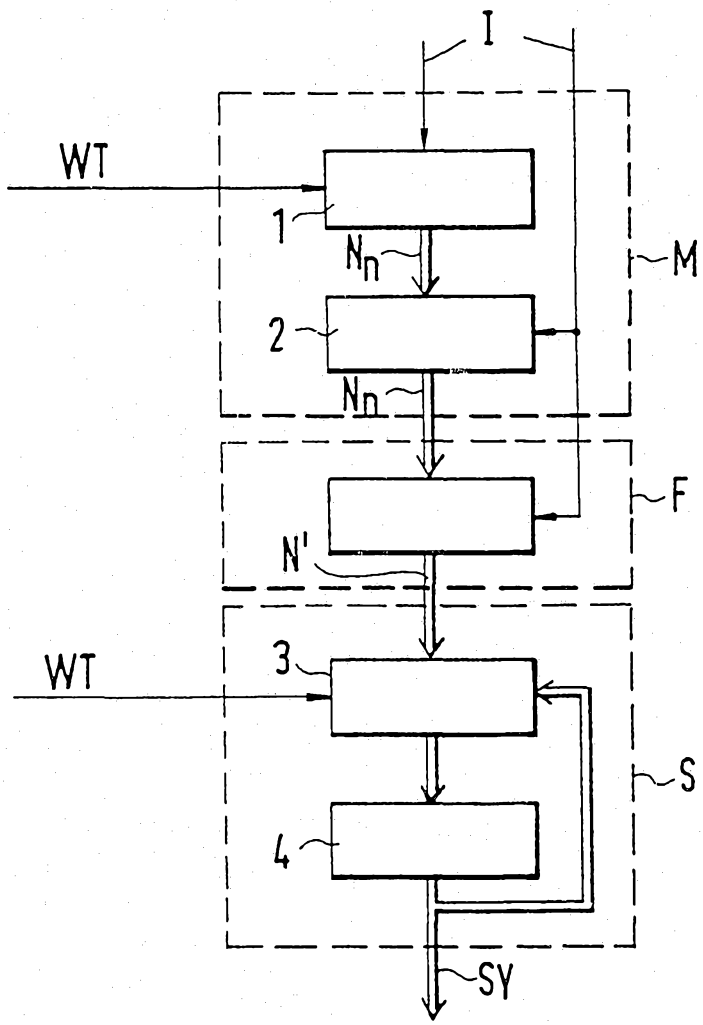

FIG.1

46117/89

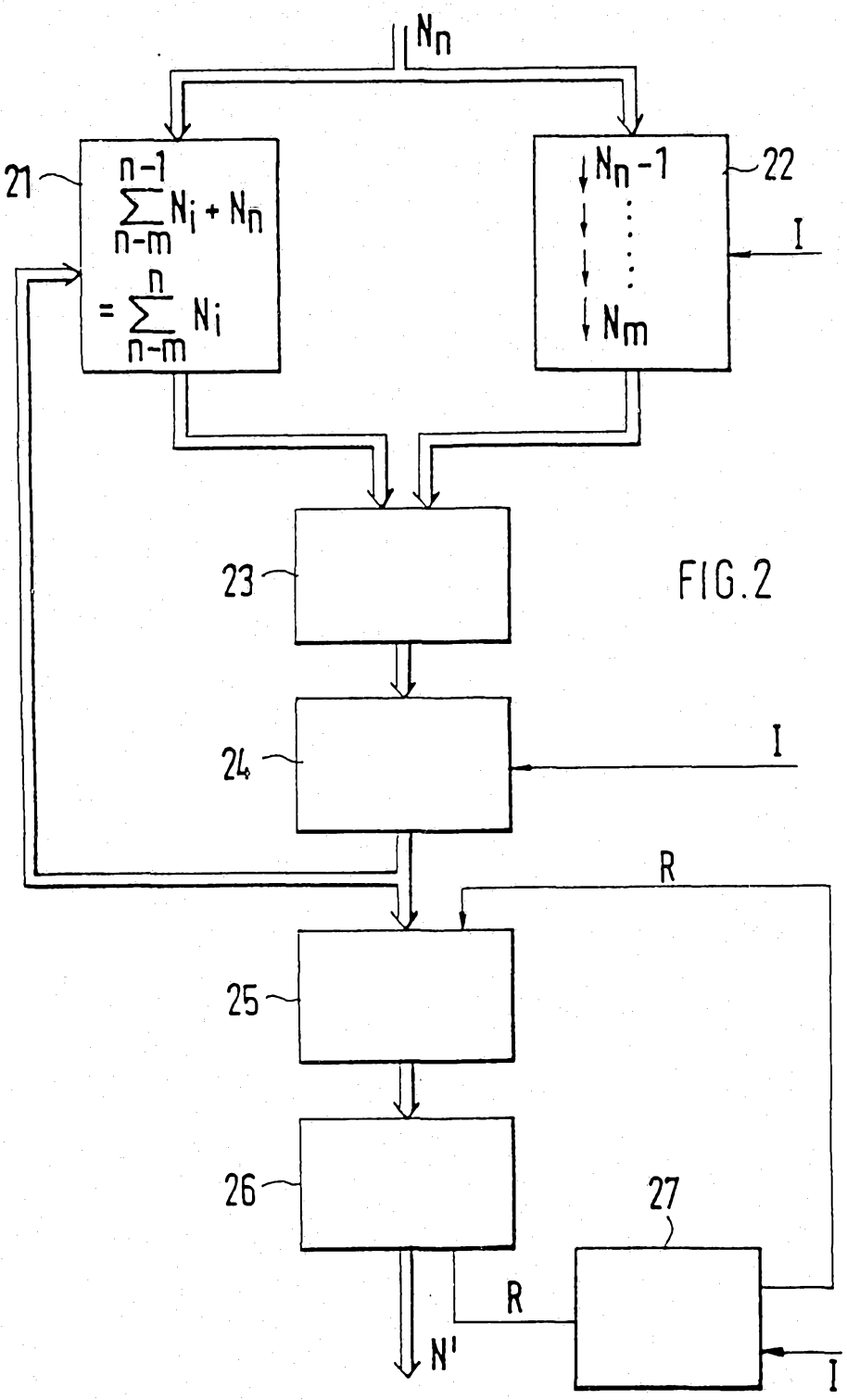

FIG.2

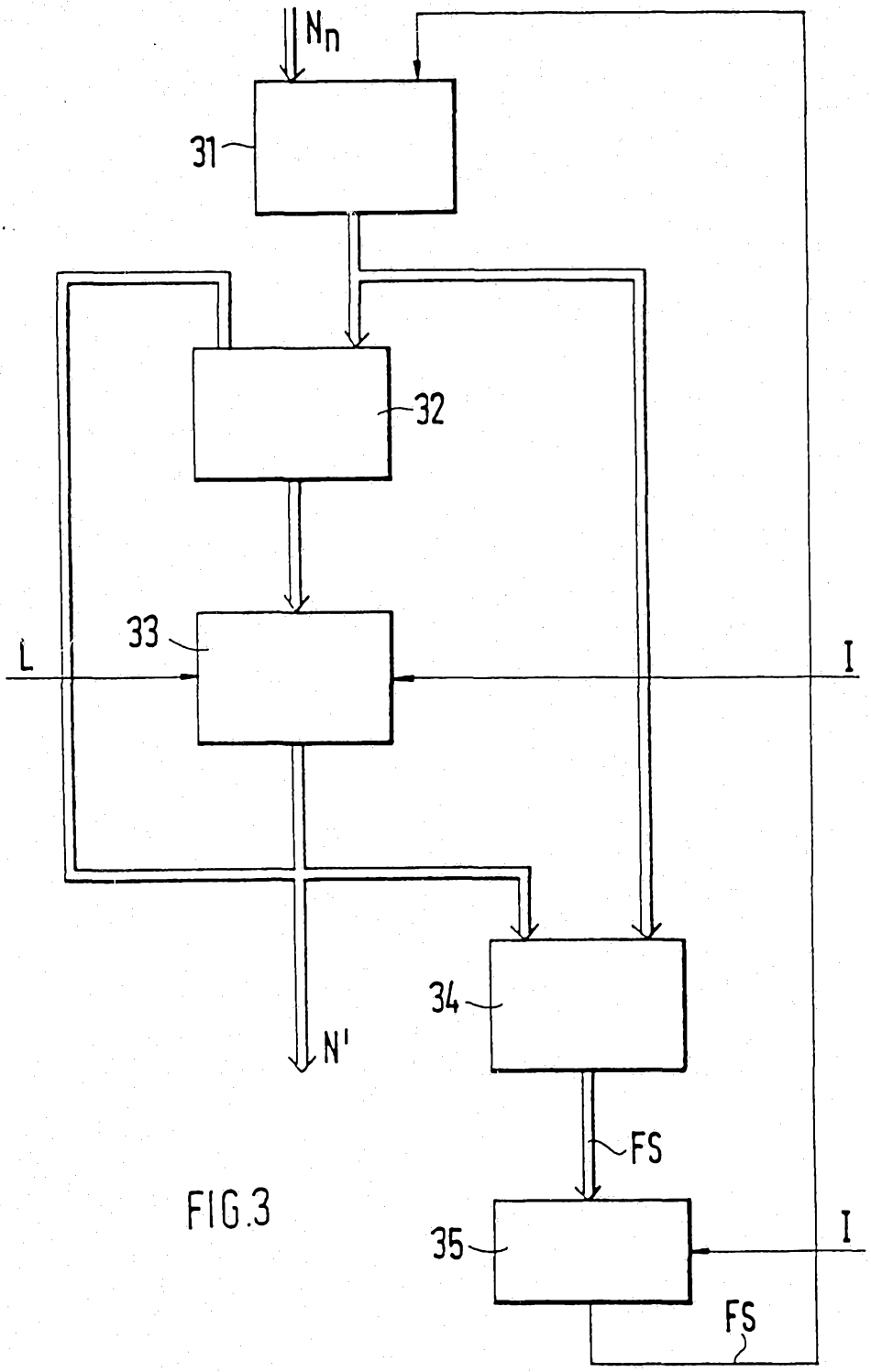

FIG.3