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(54) Title: TOP PACKAGE OF A PACKAGE-ON-PACKAGE FOR MEMORY DIES

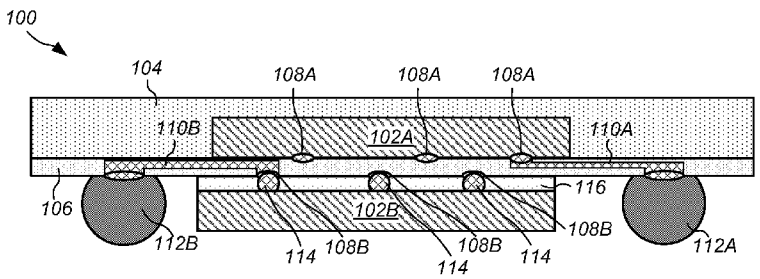


FIG. 3

(57) Abstract: A top package (100) used in a PoP (package-on-package) package includes two memory dies (102A, 102B) stacked with a redistribution layer (RDL) between the die. The first memory die (102A) is encapsulated in an encapsulant (104) and coupled to a top surface of the RDL (106). A second memory die (102B) is coupled to a bottom surface of the RDL. The second memory die is coupled to the RDL with either a capillary underfill material or a non-conductive paste. The RDL includes routing between each of the memory die and one or more terminals (112A, 112B) coupled to the RDL on a periphery of the die.

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TOP PACKAGE OF A PACKAGE-ON-PACKAGE FOR MEMORY DIES

BACKGROUND

Field of the Invention

[0001] The present invention relates to semiconductor packaging and methods for packaging semiconductor devices. More particularly, the invention relates to a top package of a PoP (package-on-package) for memory die.

Description of Related Art

[0002] Package-on-package ("PoP") technology has become increasingly popular as the demand for lower cost, higher performance, increased integrated circuit density, and increased package density continues in the semiconductor industry. As the push for smaller and smaller packages increases, the integration of die and package (e.g., "pre-stacking" or the integration of system on a chip ("SoC") technology with memory technology) allows for thinner packages. Such pre-stacking has become a critical component for thin and fine pitch PoP packages.

[0003] One limitation in reducing the size of a package (e.g., either the top package (the memory package) or the bottom package (the SoC package) in the PoP package) is the size of the substrate used in the package. Thin substrates and/or coreless substrates (e.g., laminate substrates) have been used to reduce the size of the packages to certain levels. Further reductions in size, however, may be needed in order to provide even smaller packages for next generation devices.

[0004] One or more memory die are typically placed in the top package of a PoP package. Using a single memory die (e.g., a single 8 GB (gigabyte) DDR (double date rate) memory die) in the top package is achieved relatively easy (e.g., connections to terminals on the package are reliable and simple to make and the top package has a relatively thin profile). The single memory die, however, may not provide sufficient capability for newer and more powerful devices. Thus, devices requiring larger memory capability typically need two or more die in the top package (e.g., two or more 8 GB DDR memory die).

[0005] A typical configuration for putting two memory die in a top package is to vertically stack the memory die (e.g., stack one memory die directly on top of another memory die). Vertically stacking the memory die reduces the overall thickness of the top package. Stacking the die vertically, however, creates problems with connecting both die to terminals on the package. Typically, the die are connected to the terminals using wire bonding between the top of the

memory die (with at least part of the bottom memory die in the stack protruding beyond the edge of the top memory die) and terminals on the substrate of the top package. Using wire bonding, however, increases the height of the top package as the wire bond paths are spaced to prevent shorting of the different wire bonds from each memory die. In addition, wire bonding may provide a high impedance path that reduces signal integrity and/or power integrity between the memory die and the terminals. A possible solution to overcome the problems with wire bonding is to provide through silicon vias (TSVs) from the memory die to the terminals in the top package. Providing TSVs, however, requires special memory die, adds several additionial process steps, and is relatively expensive.

SUMMARY

[0006] .In certain embodiments, a top package of a PoP package includes two memory die. A first memory die may be at least partially encapsulated in an encapsulant. A bottom surface of the first memory die may be coupled to a redistribution layer (RDL). A second memory die may be coupled to the bottom surface of the RDL. In some embodiments, the second memory die is coupled to the RDL using reflow of a capillary underfill material. In some embodiments, the second memory die is coupled to the RDL using thermal compression bonding with a non-conductive paste.

[0007] The RDL may include routing between the first memory die and one or more first terminals coupled to the RDL on a periphery of the die. The RDL may also include electrically separate routing between the second memory die and one or more second terminals coupled to the RDL on a periphery of the die. The routing between the first memory die and the first terminals may be electrically isolated from the routing between the second memory die and the second terminals. The RDL reduces the overall thickness of the top package and improves signal and power integrity in the top package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Features and advantages of the methods and apparatus of the present invention will be more fully appreciated by reference to the following detailed description of presently preferred but nonetheless illustrative embodiments in accordance with the present invention when taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 depicts a cross-sectional representation of an encapsulated memory die with a redistribution layer coupled to the memory die.

[0010] FIG. 2 depicts a cross-sectional representation of an embodiment of the encapsulated memory die of FIG. 1 being coupled to a second memory die.

[0011] FIG. 3 depicts a cross-sectional representation of an embodiment of a top package with two offset memory die coupled with a redistribution layer.

[0012] FIG. 4 depicts a bottom view representation of the embodiment depicted in FIG. 3.

[0013] FIG. 5 depicts a cross-sectional representation of another embodiment of a top package with two memory die coupled with a redistribution layer.

[0014] While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. The drawings may not be to scale. It should be understood that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but to the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF EMBODIMENTS

[0015] FIGS. 1-3 depict cross-sectional representations of steps of an embodiment of a process flow for forming a top package used in a PoP ("package-on-package") package. FIG. 1 depicts a cross-sectional representation of an encapsulated memory die with a redistribution layer coupled to the memory die used in forming top package 100. Memory die 102A is at least partially encapsulated in encapsulant 104. In certain embodiments, a bottom surface of die 102A is exposed (uncovered) by encapsulant 104. Die 102A may be, for example, a semiconductor chip such as a wire-bond die or a flip chip die. In certain embodiments, die 102A is a DDR (double data rate) die (e.g., an 8 GB DDR die). Encapsulant 104 may be, for example, a polymer or a mold compound such as an overmold or exposed mold.

[0016] In certain embodiments, redistribution layer (RDL) 106 is coupled to die 102A. RDL 106 may be coupled to a bottom surface of die 102A. RDL 106 may also be coupled to encapsulant 104. RDL 106 may include materials such as, but not limited to, PI (polyimide), PBO (polybenzoxazole), BCB (benzocyclobutene), and WPRs (wafer photo resists such as novolak resins and poly(hydroxystyrene) (PHS) available commercially under the trade name WPR including WPR-1020, WPR-1050, and WPR-1201 (WPR is a registered trademark of JSR Corporation, Tokyo, Japan)). RDL 106 may be formed on die 102A and encapsulant 104 using techniques known in the art (e.g., techniques used for polymer deposition).

[0017] In certain embodiments, die 102A and RDL 106 are coupled using one or more

connections 108A. Connections 108A may include landing pads or other terminals that couple die 102A to routing 110A in RDL 106. For example, connections 108A may include aluminum or copper landing pads or solder-coated or Sn-coated landing pads for coupling to routing 110A to die 102A.

[0018] After formation of RDL 106, terminals 112A, 112B may be coupled to the RDL, as shown in FIG. 1. Terminals 112A, 112B may be located on a periphery of die 102A. Terminals 112A, 112B may be used to couple top package 100 to a bottom package (e.g., a SoC package) to form a PoP package. Terminals 112A, 112B may include aluminum, copper, or another suitable conductive material. In some embodiments, terminals 112A, 112B are solder-coated or Sn-coated. In certain embodiments, terminals 112A are coupled to die 102A through routing 110A and connections 108A.

[0019] FIG. 2 depicts a cross-sectional representation of an embodiment of die 102B being coupled to die 102A and RDL 106. Die 102B may be, for example, a flip-chip semiconductor chip. In certain embodiments, die 102B is a DDR (double data rate) die (e.g., an 8 GB DDR die). In some embodiments, die 102B is identical to die 102A. Die 102B may be flipped so that terminals 114 (typically located on the bottom of the die) can be coupled to connections 108B on RDL 106. Terminals 114 may be copper or aluminum terminals. In some embodiments, terminals 114 are solder-coated or Sn-coated.

[0020] After terminals 114 are contacted to connections 108B, die 102B may be coupled to RDL 106 and die 102A with material 116, as shown in FIG. 3. Die 102B may be coupled to a bottom surface of RDL 106 (e.g., a surface of the RDL opposite the surface coupled to die 102A). Material 116 may be an electrically insulating material. In certain embodiments, material 116 is pre-applied to the surface of RDL 106 or die 102B before contacting the RDL and the die. Material 116 may be, for example, a polymer or epoxy material such as an underfill material or a non-conductive paste. For example, material 116 may be a capillary underfill material used in flip-chip bonding processes such as a snap cure underfill material or a low profile underfill material. Typically, material 116 is an electrically insulating material that cures at or lower than the melting temperatures of the materials used in terminals 114 and connections 108B (e.g., the solder melting temperature).

[0021] In some embodiments, if terminals 114 are copper, material 116 is a non-conductive paste and terminals 114 are coupled (bonded) to connections 108B using a thermal compressing bonding process (e.g., a flip-chip thermal compression bonding process). An example of a flip-chip thermal compression bonding apparatus that may be used is an FC3000 Flip Chip Bonder available from Toray Engineering Co., Ltd. (Tokyo, Japan). In some embodiments, material 116

is a capillary underfill material and terminals 114 are coupled (bonded) to connections 108B using a mass reflow process (e.g., using a solder reflow oven).

[0022] In some embodiments, terminals 112A, 112B are coupled to RDL 106 after coupling terminals 114 and connections 108B. The same process used to couple terminals 114 and connections 108B may be used to couple terminals 112A, 112B to RDL 106. For example, terminals 112A, 112B may be coupled using the same mass reflow process used to couple terminals 114 and connections 108B.

[0023] Coupling terminals 114 on die 102B to connections 108B in RDL 106 couples die 102B to routing 110B in the RDL. Routing 110B may provide connection to terminals 112B for die 102B while routing 110A provides connections between terminals 112A and die 102A. Routing 110A and routing 110B may be, for example, metal lines in RDL 106. In certain embodiments, routing 110B is electrically isolated from routing 110A in RDL 106. Electrically isolating routing 110A and routing 110B allows die 102A and die 102B to be individually connected to a bottom package through terminals 112A and terminals 112B, respectively.

[0024] Routing 110A and routing 110B, shown in FIGS. 1-3, are only shown for one terminal 112A coupled to die 102A and one terminal 112B coupled to die 102B for simplicity in the drawings. It is to be understood that additional routing exists for each of the terminals coupled to each memory die and that the routing may be in any configuration contemplated by one skilled in the art.

[0025] As shown in FIG. 3, die 102B is offset from die 102A. Offsetting die 102A and die 102B offsets connections 108A from connections 108B (e.g., creating a staggered bump pattern between the die). Offsetting connections 108A and connections 108B allows a single layer of routing (e.g., a single layer of metal lines that define routing 110A and routing 110B) in RDL 106 (e.g., RDL 106 is a single layer RDL). Single layer RDL 106 is possible because connections 108A and 108B do not overlap, which allows routing 110A and routing 110B to be in the same layer without any electrical connection between the individual routings for die 102A and die 102B.

[0026] FIG. 4 depicts a bottom view representation of the embodiment of top package 100 depicted in FIG. 3. Routing 110A couples connections 108A to terminals 112A and routing 110B couples connections 108B to terminals 112B. As shown in FIG. 4, the offset between die 102A and die 102B offsets connections 108A from connections 108B. Because connections 108A and connections 108B are offset (not overlapped), routing 110A and routing 110B may both be in the same layer in RDL 106 without the separate routings electrially connecting (shorting).

[0027] In some embodiments, die 102A and die 102B are not offset and connections 108A and connections 108B are aligned (e.g., the connections overlap). FIG. 5 depicts a cross-sectional representation of an embodiment of top package 100' with die 102A and die 102B coupled with no offset between the die. Because connections 108A and 108B overlap in top package 100', RDL 106' may include two or more layers of routing (e.g., RDL 106' is a 2L (two layer) RDL). The multiple layers of routing (e.g., routing 110A is in one layer and routing 110B is in another layer) may be used to inhibit electrical contact between the individual routings (e.g., electrically isolate routing 110A from routing 110B) and allow die 102A and die 102B to be individually connected to a bottom package through terminals 112A and terminals 112B, respectively.

[0028] As shown in FIGS. 3 and 5, the presence of RDL 106 (or RDL 106') in top package 100 allows for bonding and electrical coupling of die 102A, 102B to a bottom package through terminals 112A, 112B. Terminals 112A, 112B may be located on the periphery of die 102A, 102B. Using RDL 106 to couple die 102A, 102B to terminals 112A, 112B on the periphery of the die reduces an overall thickness of top package 100 by eliminating the use of wire bonding or other connection techniques that add height to the top package.

[0029] In addition, RDL 106 may be a relatively thin layer compared to substrates typically used for memory packages (e.g., top packages in PoP packages). For example, a single layer RDL may have a thickness of less than about 10 μm (e.g., about 5 μm) while typical organic substrates have thicknesses of about 200 μm or more. Thus, using RDL 106 in top package 100 reduces the overall thickness of the top package and a PoP package containing the top package, especially for the single layer RDL. For example, top package 100 may have a thickness between about 200 μm and 300 μm with a substantial majority of the thickness of the top package being due to the combined thickness of die 102A and die 102B. Reducing the thickness of top package 100 may allow increases in circuit density or package density and improve performance of a device using the top package.

[0030] Using routing 110A, 110B in RDL 106 may also decrease the impedance between die 102A, 102B and terminals 112A, 112B compared to connections made using wire-bonding techniques. The impedance may be decreased through the use of high conductivity metal lines in RDL 106 and/or reduced path lengths between the connections on the die and the terminals (e.g., shorter interconnects between the die and the terminals). Wire-bonding typically includes looped or rounded paths to allow for connections to upper surfaces of the dies and the substrate. Thus, the path length may be shorter using routing in the RDL because more direct connections between the die and the terminals are provided (e.g., no rounded or looped paths are needed). Additionally, couplings between die 102A, 102B, connections 108A, 108B, routing 110A, 110B,

and/or terminals 112A, 112B may be more robust than wire-bonding connections.

[0031] Reducing the impedance between die 102A, 102B and terminals 112A, 112B may provide better signal and power integrity in top package 100 (or top package 100') compared to top packages made using wire-bonding between the die and the terminals. Providing better signal and power integrity may improve device performance. In addition, utilization of RDL 106 in top package 100 may reduce yield losses (compared to top packages using wire-bonding) and potentially reduce manufacturing costs with the improved yield.

[0032] Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor device package, comprising:

a first memory die at least partially encapsulated in an encapsulant with at least one surface of the first memory die exposed;

a redistribution layer coupled to the exposed surface of the first memory die;

a second memory die coupled to the redistribution layer; and

a plurality of terminals coupled to the redistribution layer, wherein a first set of the terminals are coupled to the first memory die through the redistribution layer and a second set of the terminals are coupled to the second memory die through the redistribution layer.

2. The package of claim 1, wherein the terminals are coupled to the redistribution layer on a periphery of the first memory die and a periphery of the second memory die.

3. The package of claim 1, wherein the redistribution layer comprises a first routing between the first memory die and the first set of terminals and a second routing between the second memory die and the second set of terminals, and wherein the first routing and the second routing are electrically isolated.

4. The package of claim 1, wherein the second memory die is flip-chip coupled to the redistribution layer.

5. The package of claim 1, wherein the second memory die is coupled on an opposing surface of the redistribution layer from the first memory die.

6. The package of claim 1, further comprising a first set of connections between the first memory die and the redistribution layer and a second set of connections between the second memory die and the redistribution layer, wherein the first set of connections are offset from the second set of connections.

7. A semiconductor device package, comprising:

a mold material with a first memory die at least partially enclosed in the mold material;

a redistribution layer coupled to a bottom surface of the mold material;

a second memory die coupled to a bottom surface of the redistribution layer; and

a plurality of terminals coupled to the bottom surface of the redistribution layer on a periphery of the first memory die and a periphery of the second memory die;

wherein the redistribution layer comprises routing that couples the first memory die to a first set of the terminals and the second memory die to a second set of the terminals.

8. The package of claim 7, wherein the routing in the redistribution layer comprises a first routing between the first memory die and the first set of terminals and a second routing between the second memory die and the second set of terminals, and wherein the first routing and the second routing are electrically isolated.

9. The package of claim 7, wherein the routing comprise a single layer of routing in the redistribution layer.

10. The package of claim 7, wherein the first set of terminals are electrically isolated from the second set of terminals.

11. A method for forming a semiconductor device package, comprising:

providing a first memory die at least partially encapsulated in an encapsulant with at least one surface of the first memory die exposed;

coupling a redistribution layer to the first memory die;

coupling a plurality of terminals to the redistribution layer, wherein a first set of the terminals are coupled to the first memory die through the redistribution layer; and

coupling a second memory die to the redistribution layer, wherein a second set of the terminals are coupled to the second memory die through the redistribution layer.

12. The method of claim 11, further comprising providing routing in the redistribution layer, wherein the routing comprises a first routing between the first memory die and the first set of terminals and a second routing between the second memory die and the second set of terminals, and wherein the first routing and the second routing are electrically isolated.

13. The method of claim 11, further comprising coupling the redistribution layer to the encapsulant.

14. The method of claim 11, wherein the redistribution layer is positioned between the first memory die and the second memory die.

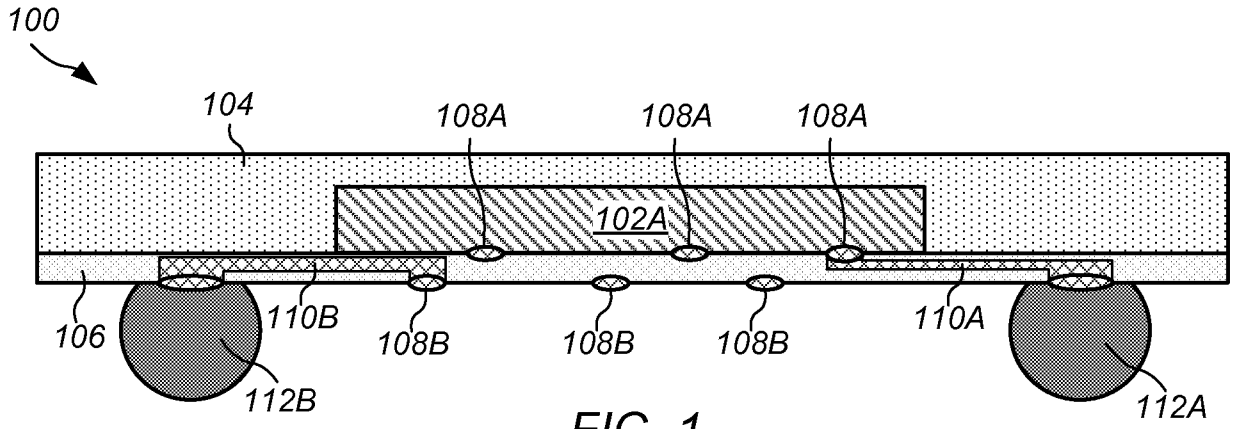


FIG. 1

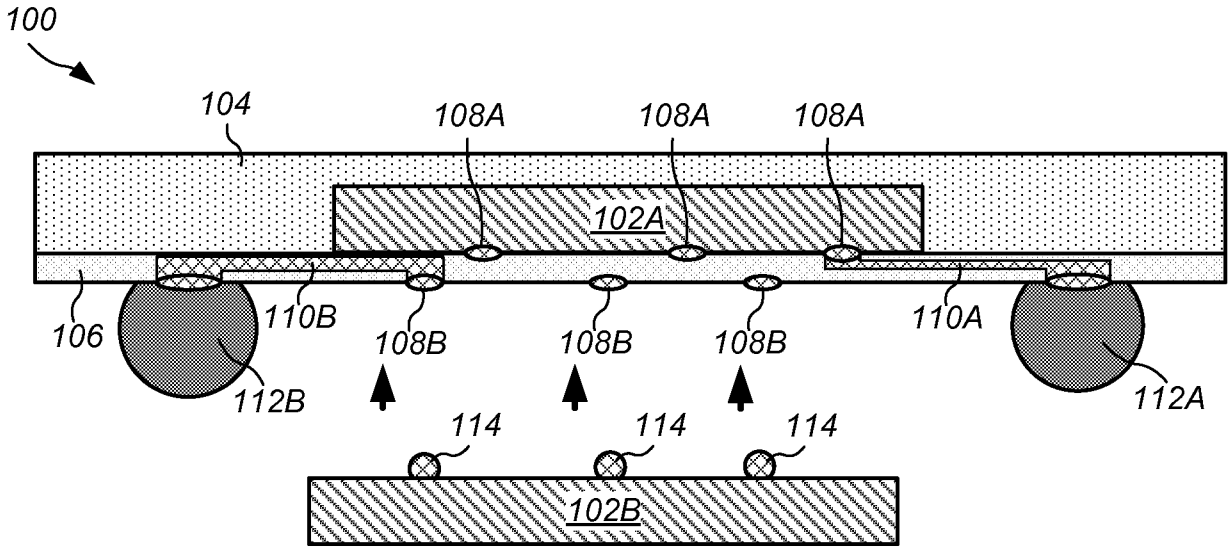


FIG. 2

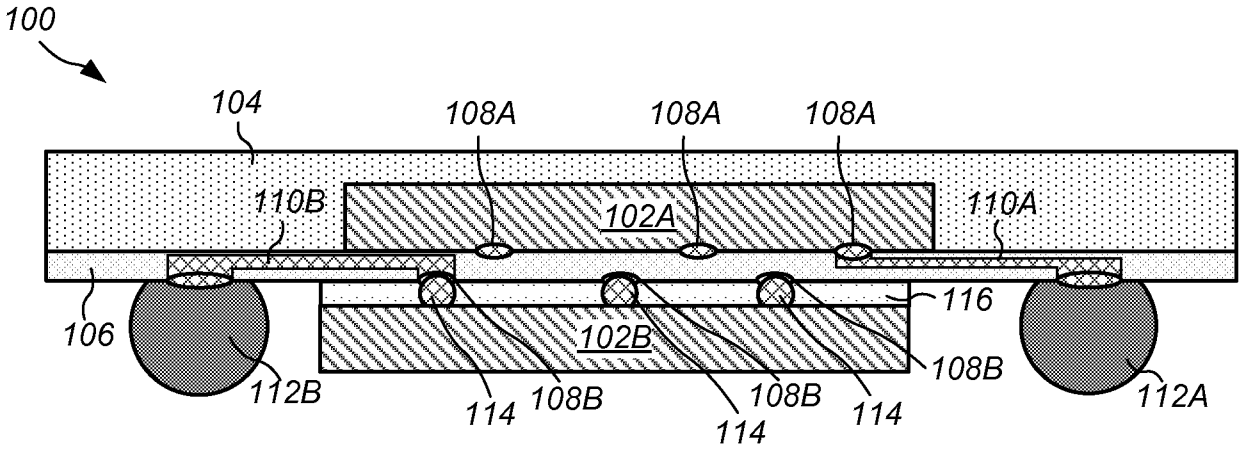


FIG. 3

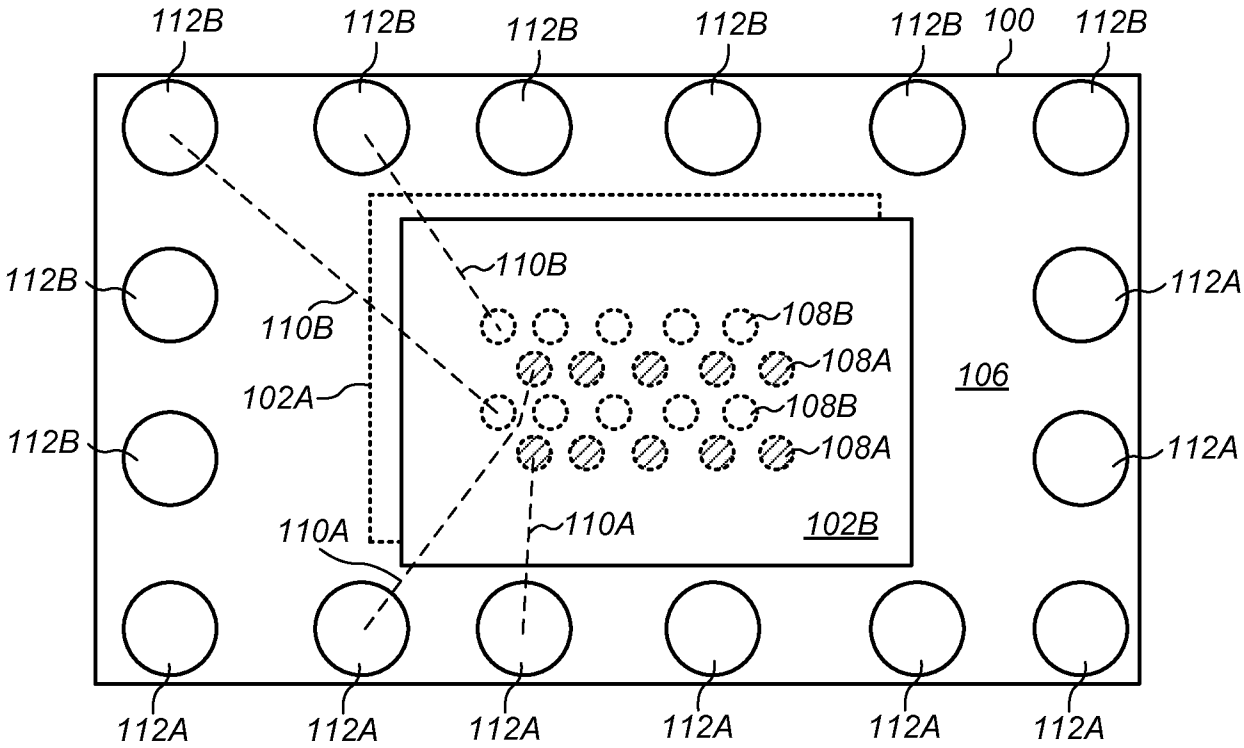

112B
112B
112B
112B
112B
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112B
112B
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110B
108B
108A
102A
106
108B
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112A

FIG. 4

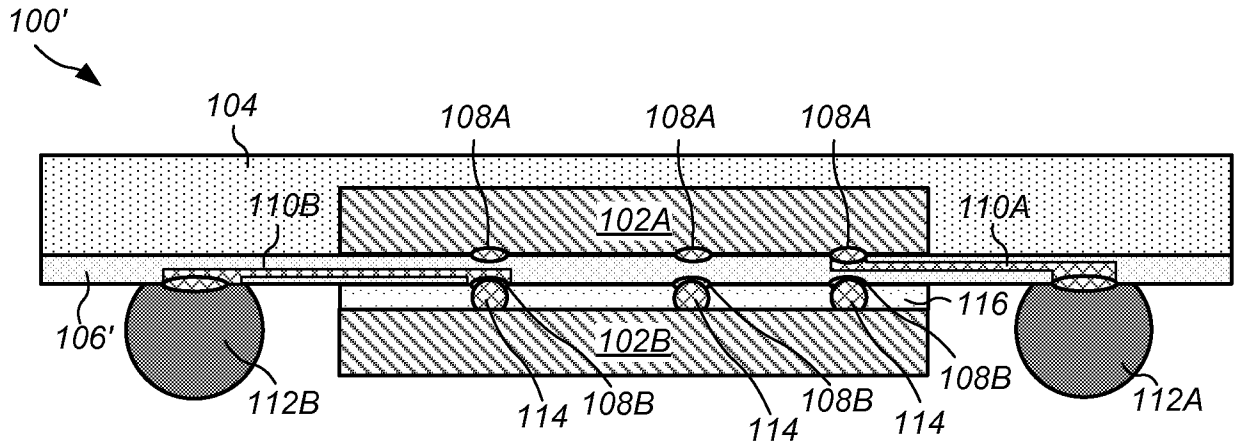

100'
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108A
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110A
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106'
102B
112B
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108B
108B
114
114
108B
112A

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/012072

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/03 H01L23/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/037169 A1 (PAGAILA REZA A [SG]) 17 February 2011 (2011-02-17) paragraph [0040] - paragraph [0050]; figures 3a-3h paragraph [0052] - paragraph [0054]; figures 5-7	1-5,7,8, 10-14
A	US 2011/101512 A1 (CHOI DAESIK [KR] ET AL) 5 May 2011 (2011-05-05) paragraph [0058] - paragraph [0059]; figures 6,7	2
X	US 2011/089561 A1 (KURITA YOICHIRO [JP] ET AL) 21 April 2011 (2011-04-21) figure 1 paragraph [0064] - paragraph [0076]; figures 3A-3D,4,5,6A,6B,7-9	1-5,7,8, 10

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 April 2014	18/06/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Gallo, Thomas

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/012072

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/272814 A1 (WACHTLER KURT [US] ET AL) 10 November 2011 (2011-11-10) abstract; figures 1,2	1-5,7,8, 10-14

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/012072

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-5, 7, 8, 10-14

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 7, 8, 10-14

   Semiconductor device package and method for forming a semiconductor device package

1.1. claims: 1, 2, 7, 11

   Position of the terminals in the semiconductor device package

1.2. claims: 3, 8, 10, 12

   Electrical routing in the redistribution layer and the terminals in the semiconductor device package

1.3. claims: 4, 5, 13, 14

   Relative position of the memory dies, the encapsulant and the redistribution layer in the vertical direction in the semiconductor device package

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2. claims: 6, 9

   Electrical routing of two memory dies with a single redistribution layer in a semiconductor device package

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/012072

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