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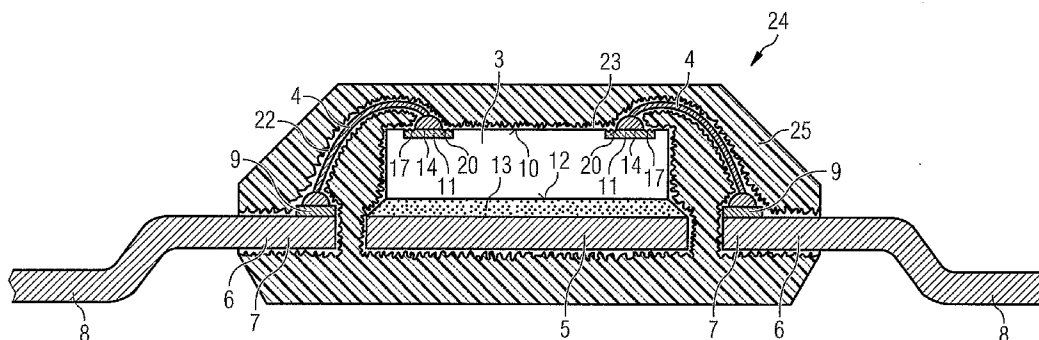
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(54) Title: SEMICONDUCTOR PACKAGE AND METHOD OF ASSEMBLING A SEMICONDUCTOR PACKAGE



(57) Abstract: A semiconductor package (24; 26) comprises a semiconductor component (1) including a circuit carrier (2; 27), a semiconductor chip (3) and a plurality of electrical connections (4). An adhesion promotion layer (22) is disposed on at least areas of the semiconductor component (1) and plastic encapsulation material (25) encapsulates at least the semiconductor chip (3), the plurality of electrical connections (4) and the plurality of the inner contact pads (9). Surface regions (17) of the semiconductor component (1) are selectively activated.

Description

Semiconductor package and method of assembling a semiconductor package

The invention relates to semiconductor packages and methods of the assembling a semiconductor package and, in particular, to an encapsulated semiconductor package and to a method of assembling an encapsulated semiconductor package.

It is known that encapsulated semiconductor packages which include a plastic encapsulation material as the package housing are susceptible to cracking during solder reflow. This phenomenon is commonly referred to as the "popcorn effect" and often results in the failure of the package.

This cracking is the result of the accumulation of moisture within the semiconductor package which, as the package is heated to a higher temperature during the solder reflow process, vaporizes, causing a build up of vapour pressure within the package resulting in cracking of the encapsulation material.

The mismatch in the coefficients of thermal expansion between dissimilar materials of the package, for example a metallic leadframe and plastic encapsulation material, can also lead to the formation of cracks, and even complete delamination, at the interfaces between these materials. Moisture is able to accumulate in these cracks and exacerbate the popcorn effect during solder reflow.

The problem of cracking is more severe for a so-called "green" packages, which use non-leaded solder requiring a higher solder reflow temperature of around 260°C, and for so-called "robust" packages which are required to withstand more extreme operating conditions such as packages for automotive applications

This problem has been addressed, for example in WO 00/74131 A1, by providing an additional adhesion promotion coating on the encapsulated elements of the semiconductor package. However, the improvements which are observed as a result of the additional adhesion promotion coating are limited and further improvements are desired.

It is an object of the invention to provide semiconductor packages and methods for assembling a semiconductor packages in which the adhesion between the embedded components and the plastic package material is improved and in which cracking during the solder reflow process is reduced. It is also desired that these improvements are suitable for use in "green" packages and "robust" packages.

It is a further object of the invention to provide methods for assembling the packages which are simple and which can be easily integrated into the manufacturing process.

These objects is provided by the subject matter of the independent claims. Further advantageous improvements are the subject matter of the dependent claims.

The invention provides a semiconductor package comprising a semiconductor component. The semiconductor component comprises

a circuit carrier, a semiconductor chip and a plurality of electrical connections. The circuit carrier comprises a die pad, a plurality of inner contact pads, a plurality of outer contact areas and a rewiring structure which electrically connects the plurality of inner contact pads and the plurality of outer contact areas. The semiconductor chip comprises an active surface with integrated circuit devices and a plurality of chip bond pads disposed on the active surface and a passive surface. The passive surface of the semiconductor chip is mounted on the die pad of the circuit carrier. The plurality of electrical connections extends between, and electrically connects, the plurality of chip bond pads with the plurality of inner contact pads of the circuit carrier.

The semiconductor package further comprises an adhesion promotion layer and plastic encapsulation material. The adhesion promotion layer is disposed on at least areas of the semiconductor component. The plastic encapsulation material encapsulates at least the upper surface of the die pad, the semiconductor chip, the plurality of electrical connections and the plurality of the inner contact pads. Surface regions of the semiconductor component are selectively activated.

The semiconductor package according to the invention comprises a semiconductor component with surface regions which are selectively activated. The semiconductor component also comprises surface regions which are not selectively activated. The selectively activated regions are surrounded by regions which are not selectively activated in an embodiment according to the invention. In an embodiment, the activated surface regions comprise an outer layer which has a different chemical composition to the underlying material of the region.

Defined regions which are to be activated are selected and the semiconductor component subjected to an appropriate treatment by which only the surface of the defined regions is activated. Other surface regions of the semiconductor component, which are not defined, are not activated. The selective activation of surface regions of the semiconductor components, therefore, differs from a cleaning process since a cleaning process affects all free-lying surfaces.

The surface regions are selectively activated after the passive surface of the semiconductor chip has been mounted on the die pad of the circuit carrier and after the plurality of electrical connections have been formed which electrically connect the chip bond pads with the inner contact pads of the circuit carrier. Therefore, the interfaces between the electrical connections and the chip bond pads and between the electrical connections and inner contact pads remain free from the adhesion promotion layer. The interfaces do not provide free surfaces of the semiconductor component and are, therefore, not selectively activated.

The semiconductor package according to the invention provides an improved moisture resistance and reliability upon soldering due to the provision of an adhesion promotion coating which covers at least regions of the surfaces of the semiconductor component. The adhesion promotion layer provides an improved adhesion between the plastic encapsulation material which provides the package housing and the surfaces of the semiconductor component coated by the adhesion promotion layer. This hinders the formation of cracks due to the mismatch in thermal expansion coefficient of the materials of the semiconductor

component and the plastic encapsulation material. Consequently, the accumulation of moisture in voids provided by cracks is prevented which eliminates one of the faults thought to result in the appearance of the popcorn effect during the solder reflow process. This has the advantage that the package is less likely to fail as a result of the solder reflow process performed by the customer in order to mount the package on a higher level substrate such as a printed circuit board.

The surface regions of the semiconductor component which are selectively activated provide a surface on which the adhesion promotion layer may be more reliably deposited than if these regions were to remain unactivated. Therefore, if the semiconductor component comprises different materials, for example, different metals, which have a different affinity for the material of the adhesion promotion layer, for example, different wetting characteristics, the regions containing materials with a poorer affinity for the adhesion promotion layer may be selectively activated.

The selectively activated surface regions have an improved affinity for the material of the adhesion promotion layer. The selectively activated surface regions are, therefore, covered by, and are directly in contact with, the adhesion promotion layer. The adhesion promotion layer can then be more reliably deposited on to the selectively activated regions so that the overall coverage of the adhesion promotion layer on the surfaces of the semiconductor component is improved. Therefore, the reliability of the semiconductor package is improved as poor or patchy coverage of the adhesion promotion layer is avoided and, therefore, isolated crack formation in the uncoated regions is prevented.

The surfaces which have been previously found to be poorly coated by the adhesion promotion layer can be provided with a activation treatment which activates only these regions, leaving other regions of the semiconductor component, which were previously found to be reliably coated by the adhesion promotion layer, unaffected and unactivated.

The semiconductor component comprises inner portions and outer portions. The inner portions are defined as those portions of the semiconductor component which are positioned within the package housing and are encapsulated by the plastic encapsulation material and covered by the adhesion promotion layer. Outer portions of the semiconductor component are defined as those portions of the semiconductor component which are positioned outside of the package housing and are not encapsulated by the plastic encapsulation material.

In an embodiment of the invention, the surface regions of the semiconductor component which are selectively activated are located on the inner portion of the semiconductor component. The inner portions of the semiconductor component also comprise regions which are unactivated. The selectively activated surface regions may be isolated regions disposed on the inner portion of the semiconductor component which are surrounded on all sides by unactivated regions.

In an embodiment of the invention, the exposed surfaces of the chip bond pads are selectively activated. In this context exposed surfaces denote those surfaces of the chip bond pads which are not occupied by the electrical connection disposed

on the chip bond pad. Exposed does not necessarily mean that these surfaces of the chip bond pads are uncovered.

The surface of the chip bond pads which is occupied by the bond wire and which forms an interface with the electrical connection remains unactivated as the activation of the exposed surfaces of the chip bond pads is performed after the electrical connections have been made between the chip bond pads and the inner contact areas of the circuits carrier.

It has been found that the chip bonding pads exhibit poor or no coverage by the adhesion promotion layer. Previous approaches to improve this problem have concentrated on treating the chip bond pads during the wafer fabrication stage, commonly referred to in the art as Front End. However, these methods have the disadvantage that analysis is difficult at the wafer level and the quality of the pad activation or conditioning only becomes apparent at a much later stage in the manufacture of the package after the chip has been coated with the adhesion promotion layer. Furthermore, some pad conditioning treatments have been found to contaminate gate areas of the integrated circuit devices present in the active surface of the semiconductor chip which has an unacceptable impact on the electrical robustness of the devices.

The production of a semiconductor package including a semiconductor chip is typically carried out in a different factory, commonly referred to as Back End, to that in which the semiconductor chip is manufactured. Therefore, if bond pad conditioning or activation is carried out at the wafer level, results from the packaging factory have to be relayed to the wafer manufacturer. Consequently, the optimization is time-

consuming and improvements to the package may be delayed. The invention enables the pad conditioning or activation to be performed in the packaging factory at a stage just before the adhesion promotion coating is applied. This enables a faster optimization of the activation process as the results of the adhesion promotion coating can be immediately used to optimize the activation treatment.

The disadvantages of wafer-level conditioning are avoided by activation of only the exposed surfaces of the chip bond pads during the package assembly process. The package and methods of the invention has the further advantage that the surfaces of the chip bond pads are activated only in those regions in which bond pad activation is actually necessary since the region of the chip bond pad occupied by the electrical connection is not coated by the adhesion promotion layer. A wider variety of activation processes are, therefore, in principle possible including the provision of non-electrically conductive or poorly electrically conductive activated surface regions.

The activated surface regions have an affinity for the material of the adhesion promotion layer which is to be included in the package and are suitable for the method by which the adhesion promotion layer is deposited. If electro-plating is used to deposit the adhesion promotion layer, the activated surfaces should be electrically conductive, for example.

In an embodiment, the chip bond pads comprise aluminium and the exposed surfaces of the chip bond pads comprise hydroxyl-enriched aluminium oxide. Hydroxy-enriched aluminium oxide is formed by treating the semiconductor component with boiling

water or steam. This process is typically carried out at approximately atmospheric pressure. The layer of aluminium oxide, present on the surface of the chip bond pads, reacts with the heated water or steam and forms a hydroxy-enriched aluminium oxide. Hydroxy-enriched aluminium oxide has the advantage that the chemical nature of the aluminium oxide changes and the transformation of the mainly hydroxyl-free aluminium oxide into a hydroxyl-enriched aluminium oxide results in the surface of the chip bond pad having a lower electrical resistance. Therefore, these exposed regions of the chip bond pads which include a surface layer of hydroxy-enriched aluminium oxide have a lower electrical resistance and, if the adhesion promotion layer is deposited by an electric chemical plating process, these regions can be more easily electroplated than untreated chip contact pads which comprise a outer surface layer of aluminium oxide.

In a further embodiment of the invention, the exposed surfaces of the chip bond pads comprise essentially fully hydroxylated aluminium oxide. The degree of the oxidation can be controlled by increasing the time to which the chip bond pads are exposed to steam or boiling water. By the creation of aluminium hydroxide bonds, the aluminium cation and partly loses its Lewis acidic character. The aluminium hydroxide bonds allow proton and charge transfer and increase the electrochemical reactivity. The adhesion promotion layer can, therefore, be more reliably deposited by electroplating on the activated exposed areas of the chip contact pads than is observed for non-activated exposed contact pads which include a native surface layer of aluminium oxide.

In a further embodiment, the exposed surfaces of the chip bond pads consist essentially of Boehmite (AlOOH) or Gibbsite ($\text{Al}(\text{OH})_3$).

In an embodiment of the invention, the adhesion promotion layer covers essentially the whole of the surfaces of the semiconductor component which are encapsulated by the plastic encapsulation material. The adhesion promotion layer covers, therefore, essentially the whole of the surfaces of the inner portion of the semiconductor component. The adhesion promotion layer covers, therefore, the activated surfaces and unactivated surfaces of the semiconductor component.

In an embodiment of the invention, the adhesion promotion layer comprises zirconium and chromium and may also comprise zirconium oxide and chromium oxides. The adhesion promotion layer may comprise a dendritic structure. A dendritic structure has the advantage that the surface area of the adhesion promotion layer is increased and a mechanical anchoring between the adhesion promotion layer and the plastic encapsulation material is provided. This further improves the adhesion between the embedded semiconductor components and the plastic encapsulation material.

In an embodiment of the invention, the circuit carrier comprises a leadframe strip. In this embodiment, the leadfingers of the leadframe strip provide the rewiring structure of the circuit carrier. The outer portion of each of the leadfingers provides the outer contact area of the rewiring structure.

In an alternative embodiment, the circuit carrier comprises a rewiring substrate. The rewiring substrate comprises a top

surface on which the die pad and inner contact areas are located. The lower surface of the rewiring substrate comprises outer contact areas which are electrically connected by conducting tracks and vias to the inner contact surfaces. The conductor tracks and vias provide the rewiring structure of the circuit carrier in this embodiment.

The plurality of electrical connections may be provided by a plurality of bond wires. One or more bond wires may extend between each of the chip contact pads and an inner contact pad.

The invention also relates to methods of assembling a semiconductor package. A method of assembling a semiconductor package comprises providing a semiconductor component. The semiconductor component comprises a circuit carrier, at least one semiconductor chip and a plurality of electrical connections. The circuit carrier comprises at least one device position. Each device position comprises a die pad, a plurality of inner contact pads, a plurality of outer contact areas and a rewiring structure which electrically connects the plurality of inner contact pads and the plurality of outer contact areas. The semiconductor chip comprises an active surface with integrated circuit devices and a plurality of chip bond pads and a passive surface. The passive surface of the semiconductor chip is mounted on the die pad of at least one device position of the circuit carrier. The plurality of electrical connections extends between and electrically connects the plurality of chip bond pads with the plurality of inner contact pads of the circuit carrier.

Surface regions of the semiconductor component are selectively activated and an adhesion promotion layer is deposited on at

least areas of the semiconductor component. At least the upper surface of the die pad, the semiconductor chip, the plurality of electrical connections and the plurality of the inner contact pads are encapsulated in plastic encapsulation material.

The method according to the invention has the advantage that surface regions of the semiconductor component are selectively activated after the semiconductor component has been assembled and, in particular, after the passive surface of the semiconductor chip has been mounted on the die pad of the circuit carrier and after the electrical connections have been made between the chip bond pads and the inner contact pads of the circuit carrier. Therefore, the electrically conductive interfaces between the portions of the semiconductor component, which are later encapsulated within the plastic encapsulation material of the package housing are formed before the selective activation of defined surface regions. Therefore, the contact resistance of the electrical connections and functionality of the package is not affected by the selective activation treatment.

As previously discussed, defined regions of the semiconductor component are selectively activated forming activated surface regions. Other regions of the semiconductor component remain unactivated and are unaffected by the activation treatment. The surface regions which are to be activated may be chosen on the basis of previous knowledge which shows that these particular surface regions are poorly or insufficiently covered by an adhesion promotion layer, for example. The selectively activated surface regions have a greater affinity for the adhesion promotion layer than these surface regions before the activation process.

In an embodiment of the invention, regions of the semiconductor component are selectively activated by chemical means. The chemical means may be chosen so as to activate only those regions which it is desired to activate. The chemical means may, for example, form reaction products only with one material and not with the other materials of the semiconductor component under the conditions at which the activated treatment is performed. In this embodiment, only those regions of the semiconductor component comprising this material will be activated by the chemical means.

Regions of the semiconductor component may be selectively activated by chemical reaction of at least the surfaces of the regions with the chemical means. At least the surfaces of the regions may comprise an outer activated layer of a material which is the reaction product of the material of the region and the chemical means.

In an embodiment, essentially the whole of the surfaces of the semiconductor component are exposed to the chemical means and are in direct contact with the chemical means during the activation treatment. However, selected and defined regions of the semiconductor component are selectively activated by appropriate selection of the chemical means. Regions in which no activation of the surface is desired, fail to be activated and fail to chemically react with the chemical means.

A selective activation of defined regions of the semiconductor component may be simply achieved in the method according to the invention without the use of masking steps. This greatly simplifies the assembly process and has the additional advan-

tage that very small regions may be selectively activated without the need for finely structured mask. Additional processing steps are, therefore, avoided. The selective activation of defined and desired regions occurs automatically by appropriate selection of the chemical means.

In one embodiment of the invention, regions of the semiconductor component are selectively activated by exposure to water in the liquid state or by water in the gaseous state. The water is preferably provided at a temperature in the range 60°C to 100°C and may be conveniently provided by boiling water or steam. Water has the advantage that complex handling conditions are not required and that materials costs are very low. In an embodiment, the semiconductor component is submerged in boiling water so that all the surfaces of the semiconductor component are in contact with the water for a certain time.

In an embodiment of the invention, exposed surfaces of the chip bond pads but selectively activated. Exposed surfaces of the chip bond pads are defined as those outer surfaces which are occupied by an electrical connection.

In an embodiment of the invention, the chip bond pads comprise aluminium and the activation process is carried out under conditions so that the exposed surfaces of the chip bond pads comprise hydroxy-enriched aluminium oxide. As previously discussed, the time to which the chip bond pads are exposed to water effects the extent of the reaction. The reaction kinetics also depend on the temperature of the water. Therefore, the conditions are adjusted until the exposed surfaces of the chip contacts comprise hydroxy-enriched aluminium oxide.

In further embodiment, the activation process is carried out under conditions so that the exposed surfaces of the chip bond pads comprise essentially fully hydroxylated aluminium oxide. Typically, the chip bond pads are exposed to water for a longer time to achieve a fuller transformation of the aluminium oxide into fully-hydroxylated aluminium oxide. The further embodiment, the activation process is carried out under conditions so that the exposed surfaces of the chip bond pads consist essentially of Boehmite or Gibbsite. In this embodiment of the invention, the chip bond pads comprise an outer layer of Boehmite or Gibbsite in the exposed areas. The region of the chip bond pad which is occupied by the electrical connection does not comprise Boehmite or Gibbsite.

The adhesion promotion layer may cover essentially the whole of the surfaces of the semiconductor component which are to be encapsulated by the plastic encapsulation material. These surfaces are defined as the inner portion of the semiconductor component. An essentially complete coverage of the surfaces ensures the best possible adhesion between the plastic encapsulation material and the embedded components.

In an embodiment of the invention, the adhesion promotion layer is deposited by an electrodeposition technique. This technique is advantageous in that a coating or layer is easily deposited on all surfaces of complex shapes. Since the semiconductor component is a three-dimensional object, electrodeposition and galvanic techniques are particularly advantageous.

In an embodiment of the invention, the adhesion promotion layer comprises zirconium and chromium and may also comprise

zirconium oxide and chromium oxides. The adhesion promotion layer may be deposited by a process known as A2 plating using a commercially available plating bath.

The adhesion promotion layer may be deposited under deposition conditions so as to produce a layer with a dendritic structure. The structure of an electrodeposit varies depending on the deposition conditions. Therefore, the conditions are chosen so as to produce a dendritic structure with the desired average thickness and surface roughness.

The encapsulation of at least the upper surface of the die pad, the semiconductor chip, the plurality of electrical connections and the plurality of inner contact pads may be performed by the transfer moulding process. This process is commonly used in the fabrication of encapsulated semiconductor packages and is, therefore, reliable and cost effectively used in the method of assembly according to the invention.

In an embodiment, the circuit carrier is provided in the form of the leadframe strip, each device position of the leadframe strip providing a leadframe for a single semiconductor package. In an alternative embodiment, the circuit carrier is provided in the form of the rewiring substrate. The to a plurality of electrical connections may be provided by producing a plurality of wire bonds using a known wire-bonding technique.

Embodiments of the invention will now be explained with reference to the diagrams.

Figure 1 depicts the selective activation of the chip bond pads of a semiconductor component,

Figure 2 illustrates the semiconductor component after the deposition of an adhesion promotion layer,

Figure 3 shows scanning electron micrographs comparing adhesion promotion layers deposited on non-activated and activated surface regions,

Figure 4 illustrates the chemical reaction by which the chip bond pads of Figure 1 are activated,

Figure 5 depicts an encapsulated semiconductor leadframe-based package including activated chip bond pads and an adhesion promotion layer, and

Figure 6 shows an encapsulated semiconductor package including a rewiring substrate, activated chip bond pads, an adhesion promotion layer.

Figure 1 illustrates a semiconductor component 1 which includes a leadframe 2, a semiconductor chip 3 and a plurality of bond wires 4. Figure 1 shows the cross-sectional view of a single device position of a leadframe strip. The leadframe strip comprises a plurality of device positions arranged in rows and columns. Each device position provides a leadframe 2 for a single semiconductor package.

The leadframe 2 includes a die pad 5 and a plurality of leadfingers 6. The die pad 5 is disposed in approximately the lateral centre of the leadframe 2 and is laterally surrounded by the plurality of leadfingers 6 which, in this embodiment of the invention, lie in essentially the same plane as the die

pad 5. Each leadfinger 6 comprises an inner portion 7, which will be encapsulated by the plastic encapsulation material of the package, and an outer portion 8 which extends outside of the plastic encapsulation material and provides the outer contact areas of the package. The inner portion 7 and outer portion 8 of the leadfingers 6 are illustrated with respect to the plastic encapsulation material in Figure 5 which depicts the assembled semiconductor package.

An inner contact pad 9 is positioned on the upper surface of each leadfinger 6 towards the innermost end of the inner portion 7. The plurality of inner contact pads 9 comprise a material which is suitable for wirebonding and, in this embodiment of the invention, comprise Ni/NiP.

The leadframe 2 provides the circuit carrier of the semiconductor package. The leadfingers 6 provide the rewiring structure between the inner pads 9 and outer regions 8 of the plurality of leadfingers 6 which provide the outer contact regions of the semiconductor package.

The semiconductor chip 2 has an active surface 10 which comprises integrated circuit devices (which are not illustrated in the figures) and a plurality of chip contact pads 11. The chip contact pads 11 comprise aluminium. The semiconductor chip 3 also comprises a passive rear surface 12. The passive surface 12 of the semiconductor chip 3 is mounted on the upper surface of the die pad 5 by a layer of adhesive 13.

A plurality of bond wires 4 are provided which comprise gold. A bond wire 4 extends between each chip contact pad 11 and an inner contact pad 9 disposed on the inner portion 7 of each of

the leadfingers 6. Typically, a chip bond pad 11 is electrically connected by a bond wire 4 to a leadfinger 6 which is laterally positioned adjacent the chip bond pad 11. The semiconductor component 1 consists of the leadframe 2, semiconductor chip 3 and the plurality of bond wires 4.

Each chip bond pad 11 comprises two types of region. A first region 14 is occupied by the interface formed between the end 15 of the bond wire 4 and the upper surface 16 of each bond pad 11. The first region 14 is, therefore, covered and unexposed. The second region 17 of each chip bond pad 11 is unoccupied by the end 15 of the bond wire 4. The upper surface 16 of each chip bond pad 11 is, therefore, in the second region 17 exposed. The plurality of chip bond pads 11 comprise aluminium which includes a native aluminium oxide layer 18 at the upper surface 16 in at least the exposed regions 17.

In the next stage of the method, the semiconductor component 1 is placed into boiling water for a certain time. During this stage, the exposed regions 17 of the chip bond pads 11 are selectively activated. This is indicated in Figure 1 by the arrows 19. According to the invention, at least the upper surface 16 the second exposed region 17 of each bond pad 11 is activated so as to provide an improved adhesion between the plurality of chip bond pads 11 and an adhesion promotion layer which is to be deposited on the exposed regions 17 of the plurality of bond pads 11.

Figure 2 illustrates the next stage in the method to assemble a semiconductor package. An adhesion promotion layer 21 is deposited on all of the free surfaces 22 or the semiconductor component 1 which are to be encapsulated by the plastic encap-

sulation material of the semiconductor package. The adhesion promotion layer 22 comprises zirconium and chromium and is deposited on the free surfaces 22 of the semiconductor component one by electroplating. This process is commonly referred to as an A2 plating process. A2 is the commercial name of the electroplating bath. The adhesion promotion layer 22 is deposited using electroplating conditions such that the layer 22 grows with a dendritic structure 23. The dendritic structure 23 provides a roughened surface, increasing the surface area of the layer 22, and providing an additional mechanical anchoring mechanism between the adhesion promotion layer 22 and the plastic encapsulation material of the package.

The adhesion promotion layer 22 is deposited on the semiconductor component 1 after the semiconductor chip 3 is mounted on the die pad 5 and after the bond wires 4 are formed between the chip contact pads 11 and inner contact pads 9 of the leadframe 2. This ensures that all of the surfaces 21 which are to be encapsulated within the plastic encapsulation material are coated with the adhesion promotion layer. This improves the adhesion between the plastic encapsulation material and the semiconductor component 1 and improves the reliability of the package.

The adhesion promotion layer 22 is typically deposited on a leadframe strip which comprises a plurality of device positions, each device position including a semiconductor component 1.

As can be seen in Figure 2, the adhesion promotion layer 22 is deposited on the inner portions 7 of the leadfingers 6, the die pad 5, the surfaces of the semiconductor chip 3 and the

bond wires 4. The exposed regions 17 of the chip bond pads 11 are also coated by the adhesion promotion layer 22. This is in contrast to semiconductor components which have not undergone the water treatment according to the invention. The exposed regions 17 have been activated by the water treatment and at least the surfaces of the exposed regions 17 have an improved affinity for the adhesion promotion layer 22.

The improvement in the deposition of the adhesion promotion layer 22 on the activated surfaces 20 in the exposed regions 17 of the aluminium chip bond pads 11 is illustrated by the comparison examples shown in Figure 3.

Figure 3 shows SEM micrographs of adhesion promotion layers 22 comprising zirconium and chromium, which were deposited using an A2 plating bath on the aluminium bond pads of power MOSFET devices.

Figure 3a shows an SEM Micrograph for an adhesion promotion layer 22 deposited on an aluminium bond pad 11 of a non-robust power MOSFET devices. The exposed regions of the aluminium bond pad 11 were activated using a water-based activation treatment according to the invention. The chip bond pad 11 was not subjected to any other pad activation treatment. As can be seen in Figure 3a, the adhesion promotion layer 22 was successfully deposited on the water activated chip bond pad 11.

Figure 3b shows an SEM Micrograph for a robust power MOSFET device in which the aluminium chip bond pads 11 were previously given an insufficient conventional pad activation treatment. Figure 3b shows that an adhesion promotion layer 22 was not deposited on the chip bond pad 11 and illustrates the

problem of the poor deposition of the adhesion promotion layer on conventional chip bond pads.

Figure 3c shows SEM Micrograph for a robust power MOSFET device in which the aluminium chip bond pads 11 were previously given an insufficient conventional pad activation treatment as in the device of Figure 3b. The chip bond pads 11 of the device of Figure 3c were then subjected to a water-based activation treatment according to the invention. As can be seen in Figure 3c, the adhesion promotion layer 22 was successfully deposited on the activated chip bond pad in contrast to the non-activated chip contact pad shown in Figure 3b.

The exposed regions 17 of the chip bond pads 11, according to an embodiment of the invention, are selectively activated by exposing all of the free surfaces of the semiconductor component 1 to boiling water for a given time. It is thought that the aluminium oxide layer 18 present at the surface 16 of the exposed regions 17 of the aluminium chip bond pads 11 reacts with the hot water forming hydroxy-enriched aluminium oxide at the outermost surface 16. The other free surfaces of the semiconductor component 1 which are also in contact with the hot water remain unaffected as no chemical reaction takes place. The reaction between the hot water and the aluminium oxide layer 18 in the exposed regions 17 of the chip bond pads 11 is illustrated in Figure 1 by the arrows 19.

The chemical reaction which is believed to take place is illustrated in Figure 4. The semiconductor component 1 is held in contact with the hot water until the aluminium oxide layer 18 has been transformed by chemical reaction into a fully hydroxylated aluminium oxide having a Gibbsite structure.

The use of the water-based procedure according to the invention alters the chemical nature of the aluminium oxide layer 18 present at the upper surface 16 of the chip bond pads 11. The fabricated aluminium chip bond pads 11 consist essentially of hydroxy-free aluminium oxide which, upon exposure to boiling water, is transformed into a hydroxy-enriched aluminium oxide AlOOH (Boehmite) and $\text{AlO}(\text{OH})_3$ (Gibbsite) which have a lower electrical resistance than aluminium oxide. Therefore, the activated surface areas 20 can be more easily plated by the adhesion promotion layer. The exposed regions 17 comprising the hydroxylated aluminium oxide are, therefore, activated.

Figure 4 shows, schematically, the increasing hydroxylation of the aluminium oxide layer 18. The aluminium oxide bonds are broken, the aluminium cation partly loses its Lewis acidic character and Al-OH bonds are created. These allow proton and, therefore, charge transfer throughout the aluminium-oxo-hydroxide layer. Consequently, the electrochemical reactivity of the upper surface 16 of the bond pads 11 in the exposed regions 17 increases and an activated upper surface 20 is formed in the exposed regions 17 of the chip bond pads 11. The exposed region 17 of the chip bond pads 11 comprise an outer layer of hydroxyl-enriched aluminium oxide which is disposed on the bulk aluminum of which provides the chip bond pad 11.

Figure 5 illustrates the semiconductor component 1 including the activated chip bond pads 20 and adhesion promotion layer 22, as shown in figure 3, after a mold transfer process to produce the semiconductor package 24. The surfaces 21 of the semiconductor component 1 which are located within the semi-

conductor package 24 are coated by the adhesion promotion layer 22 with a dendritic structure 23. The activated surface regions 20 of the chip bond pads 11 are coated with adhesion promotion layer 22. The plastic encapsulation material 25 which forms the semiconductor package 24 is, therefore, in contact with the adhesion promotion layer 22.

The adhesion promotion layer 22 along with its dendritic structure 23 improves the adhesion between the surfaces 21 or the semiconductor component 1 which are located within the package 24 and the plastic encapsulation material 25. This improved adhesion hinders the formation of cracks between the semiconductor component 1 and the plastic encapsulation material 25 and, consequently, hinders the accumulation of moisture at the interfaces which, during a later solder reflow process, vaporises, causing cracks in the package 24 and the phenomenon known as the popcorn effect.

Figure 6 illustrates an encapsulated semiconductor package 26 according to a second embodiment of the invention. The semiconductor package 26 comprises a circuit carrier, semiconductor chip and a plurality of bond wires 4.

In the second embodiment, the circuit carrier comprises a rewiring substrate 27. The rewiring substrate 27 has an upper surface 28 which includes a die pad 5 located in approximately the lateral centre which is surrounded by a plurality of inner contact pads 9. The lower surface of the rewiring substrate 27 comprises a plurality of outer contact areas 28 which are electrically connected to the inner contact areas 9 positioned on the upper surface 28 of the rewiring substrate 27 by conductor tracks 29 and vias 30.

The semiconductor package 26 was assembled by providing the rewiring substrate and mounting the passive surface 12 of the semiconductor chip 3 to the die pad 5. A plurality of bond wires 14 were then produced, each extending between a chip contact or bond pad 11 and an inner contact pad 9 to provide a semiconductor component 1. The chip bond pads 11 comprise aluminium.

The semiconductor component 1 was then subjected to boiling water which produced a selective activation of the exposed regions 17 of the chip contact pads 11 as described in conjunction with Figures 1 to 5. Therefore, the semiconductor package 26 also includes a chip contact pads 11 in which the exposed regions 17 of the chip contact pads in 11 which are not occupied by the ends 15 of the bond wires 4 comprise at least partially hydroxylated aluminium oxide. The exposed regions 17 comprise an outer layer 20 which is disposed on aluminium which comprises the chip bond pad 11 and which was formed as a result of the water-based activation treatment previously described. The activated layer 20 present in the exposed regions 17 of the chip bond pads 11 comprises hydroxy-enriched aluminium oxide.

The upper surface of the rewiring substrate 27, semiconductor chip 3, bond wires 4 and exposed regions 17 of the chip contact pads 11 were then coated by A2 electroplating with the adhesion promotion layer 22. A transfer moulding process was then carried out to embed the surfaces coated by the adhesion promotion layer 22 in epoxy resin 25 to provide the semiconductor package 26.

Reference numbers

1	semiconductor component	26	second semiconductor pack-
2	leadframe		age
3	semiconductor chip	27	rewiring substrate
4	bond wire	28	upper surface of rewiring
5	die pad		substrate
6	leadfinger	29	outer contact area
7	inner portion	30	conductor track
8	outer portion	31	via
9	inner contact pad		
10	active surface		
11	chip contact pad		
12	passive surface		
13	adhesive		
14	unexposed region		
15	end of bond wire		
16	upper surface of chip bond		
	pad		
17	exposed regions of chip		
	bond pad		
18	aluminium oxide layer		
19	activation		
20	activated surface		
21	free surface		
22	adhesion promotion layer		
23	dendritic structure		
24	semiconductor package		
25	plastic encapsulation mate-		
	rial		

Patent claims

1. Method of assembling a semiconductor package (24; 26), comprising:
 - providing a semiconductor component (1) comprising:
 - a circuit carrier (2; 27), the circuit carrier (2; 27) comprising at least one device position, each device position comprising a die pad (5), a plurality of inner contact pads (9), a plurality of outer contact areas (8, 29) and a rewiring structure electrically connecting the plurality of inner contact pads (9) and the plurality of outer contact areas (8; 29);
 - at least one semiconductor chip (3) comprising an active surface (10) with integrated circuit devices and a plurality of chip bond pads (11) and a passive surface (12), the passive surface (12) of the semiconductor chip (3) being mounted on the die pad (5) of at least one device position of the circuit carrier (2; 27); and
 - a plurality of electrical connections (4), the plurality of electrical connections (4) extending between and electrically connecting the plurality of chip bond pads (11) with the plurality of inner contact pads (9) of the circuit carrier (2; 27);
 - selectively activating surface regions (17) of the semiconductor component (1);
 - depositing an adhesion promotion layer (22) on at least areas of the semiconductor component (1), and
 - encapsulating at least the upper surface of the die pad (5), the semiconductor chip (3), the plurality of electrical connections (4) and the plurality of the inner

contact pads (9) in plastic encapsulation material (25).

2. Method of assembling a semiconductor package (24; 26) according to claim 1 characterised in that regions (17) of the semiconductor component (1) are selectively activated by chemical means.
3. Method of assembling a semiconductor package (24; 26) according to claim 2 characterised in that regions (17) of the semiconductor component (1) are selectively activated by chemical reaction of at least surfaces of the regions (17) with the chemical means.
4. Method of assembling a semiconductor package (24; 26) according to claim 2 or claim 3 essentially the whole of the surfaces (21) of the semiconductor component (1) are exposed to the chemical means.
5. Method of assembling a semiconductor package (24; 26) according to one of claims 2 to 4 characterised in that regions (17) of the semiconductor component (1) are selectively activated by exposure to boiling water or steam.
6. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that exposed surfaces (17) of the chip bond pads (11) are selectively activated.

7. Method of assembling a semiconductor package (24; 26) according to claim 6 characterised in that the chip bond pads (11) comprise aluminium and the activation process is carried out so that the exposed surfaces (17) of the chip bond pads (11) comprise hydroxy-enriched aluminium oxide.
8. Method of assembling a semiconductor package (24; 26) according to claim 7 characterised in that the activation process is carried out so that the exposed surfaces (17) of the chip bond pads (11) comprise essentially fully hydroxylated-aluminium oxide.
9. Method of assembling a semiconductor package (24; 26) according to claim 8 characterised in that the activation process is carried out so that the exposed surfaces (17) of the chip bond pads (11) consist essentially of Boehmite or Gibbsite.
10. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the adhesion promotion layer (22) covers essentially the whole of the surfaces (21) of the semiconductor component (1) which are to be encapsulated by the plastic encapsulation material.

11. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the adhesion promotion layer (229) is deposited by an electro-deposition technique.
12. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the adhesion promotion layer (22) comprises Zr and Cr.
13. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the adhesion promotion layer (22) is deposited under deposition conditions so as to produce a dendritic structure (23).
14. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the encapsulation of at least the upper surface of the die pad (5), the semiconductor chip (3), the plurality of electrical connections (4) and the plurality of the inner contact pads (9) is performed by a transfer molding process.
15. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the circuit carrier (2) is provided in the form of a lead-frame strip.

16. Method of assembling a semiconductor package (24; 26) according to one of claims 1 to 15 characterised in that the circuit carrier (27) is provided in the form of a re-wiring substrate.
17. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims characterised in that the plurality of electrical connections (4) are provided by a plurality of wire bonds.
18. Method of assembling a semiconductor package (24; 26) according to one of the preceding claims further comprising:
- providing a circuit carrier (2; 27), the circuit carrier (2; 27) comprising at least one device position, each device position comprising a die pad (5), a plurality of inner contact pads (9), a plurality of outer contact areas (8; 29) and a rewiring structure electrically connecting the plurality of inner contact pads (9) and the plurality of outer contact areas (8; 29);
 - providing a semiconductor chip (3) comprising an active surface (10) with integrated circuit devices and a plurality of chip bond pads (11) and a passive surface (12),
 - attaching the passive surface (12) of the semiconductor chip (3) to the die pad (5) of at least one device position of the circuit carrier (2; 27); and
 - producing a plurality of electrical connections (4), the plurality of electrical connections (4) extending between and electrically connecting the plurality of

chip bond pads (11) with the plurality of inner contact pads (9) of the circuit carrier (2; 27).

19. Semiconductor package (24; 26) comprising:

a semiconductor component comprising:

- a circuit carrier (2; 27) comprising a die pad (5), a plurality of inner contact pads (9), a plurality of outer contact areas (8; 29) and a rewiring structure electrically connecting the plurality of inner contact pads (9) and the plurality of outer contact areas (8; 29);
- a semiconductor chip (3) comprising an active surface (10) with integrated circuit devices and a plurality of chip bond pads (11) and a passive surface (12), wherein the passive surface (12) of the semiconductor chip (3) is mounted on the die pad (5) of the circuit carrier (2; 27); and
- a plurality of electrical connections (4), the plurality of electrical connections (4) extending between and electrically connecting the plurality of chip bond pads (11) with the plurality of inner contact pads (9) of the circuit carrier (2; 27);
- an adhesion promotion layer (22) disposed on at least areas of the semiconductor component (1); and
- plastic encapsulation material (25) encapsulating at least the upper surface of the die pad (5), the semiconductor chip (3), the plurality of electrical connections (4) and the plurality of the inner contact pads (9),

wherein surface regions (17) of the semiconductor component (1) are selectively activated.

20. Semiconductor package (24; 26) according to claim 19 characterized in that exposed surfaces (17) of the chip bond pads (11) are selectively activated.
21. Semiconductor package (24; 26) according to claim 19 or claim 20 characterized in that the chip bond pads (11) comprise aluminium and the exposed surfaces (17) of the chip bond pads comprise hydroxy-enriched aluminium oxide (20).
22. Semiconductor package (24; 26) according to claim 21 characterized in that the exposed surfaces (17) of the chip bond pads (11) comprise essentially fully hydroxylated-aluminium oxide (20).
23. Semiconductor package (24; 26) according to claim 22 characterized in that the exposed surfaces (17) of the chip bond pads (11) consist essentially of Boehmite or Gibbsite.
24. Semiconductor package (24; 26) according to one of claims 19 to 23 characterized in that the adhesion promotion layer (22) covers essentially the whole of the surfaces (21) of the semiconductor component (1) which are encapsulated by the plastic encapsulation material (25).
25. Semiconductor package (24; 26) according to one of claims 19 to 24

characterized in that
the adhesion promotion layer (22) comprises Zr and Cr.

26. Semiconductor package (24; 26) according to one of claims
19 to 25

characterized in that
the adhesion promotion layer (22) comprises a dendritic
structure (23).

27. Semiconductor package (24; 26) according to one of claims
19 to 26

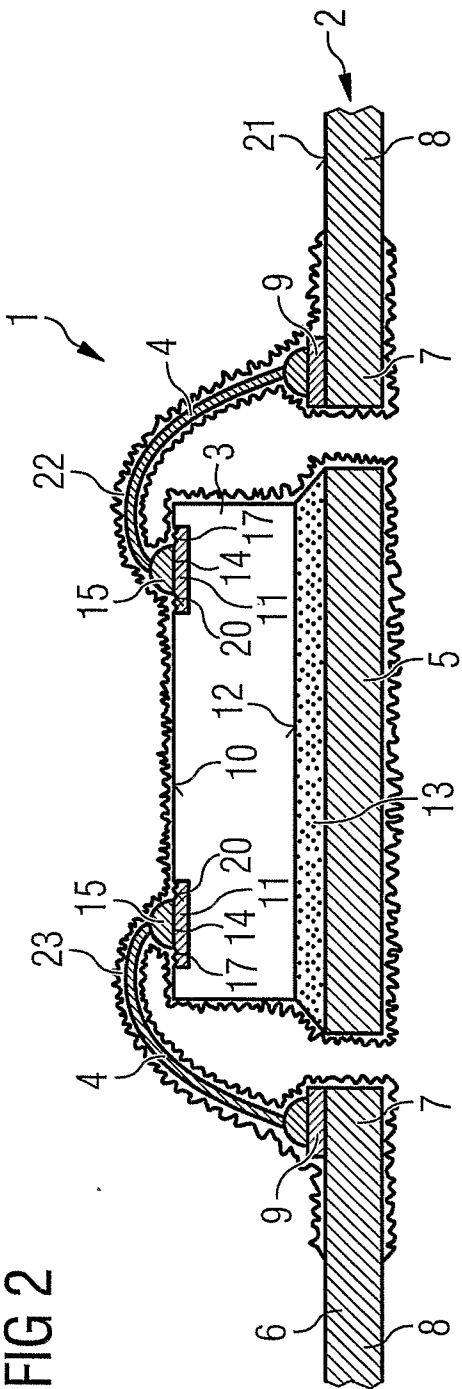
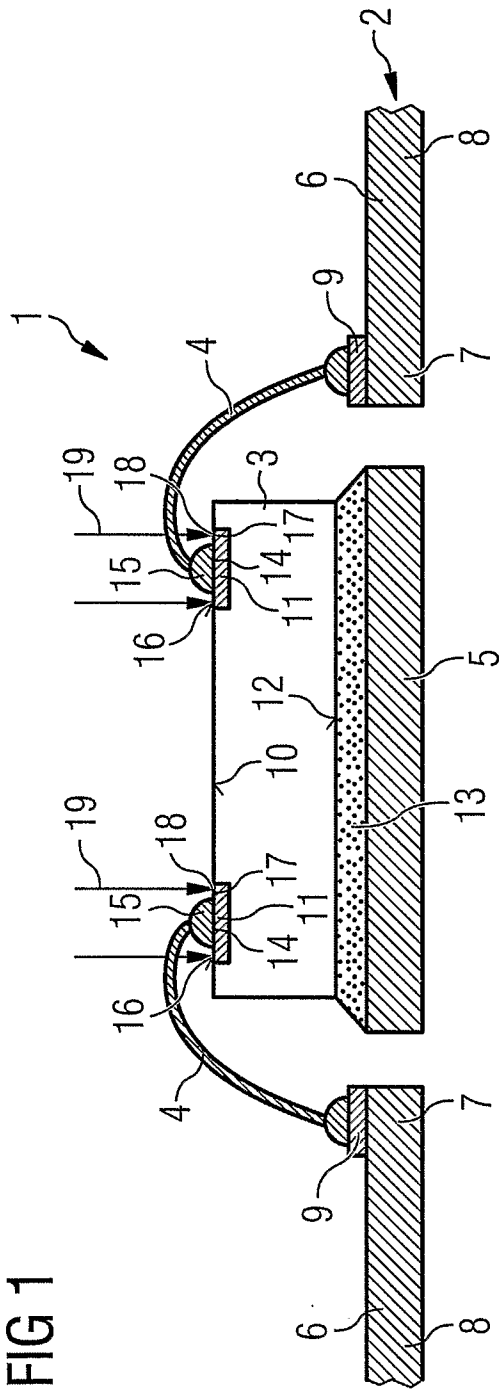
characterized in that
the circuit carrier (2) comprises a leadframe strip.

28. Semiconductor package (24; 26) according to one of claims
19 to 26

characterized in that
the circuit carrier (27) comprises a rewiring substrate.

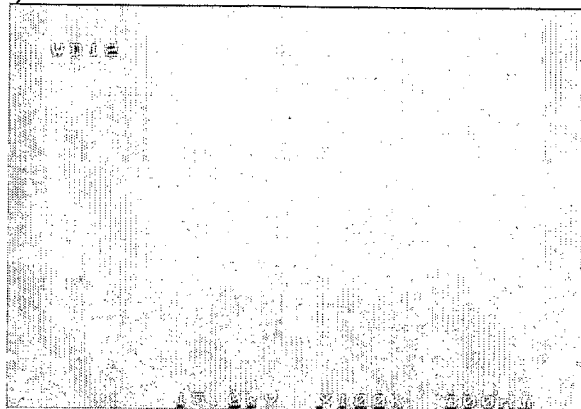
29. Semiconductor package (24; 26) according to one of claims
19 to 28

characterized in that
the plurality of electrical connections (4) are provided
by a plurality of wire bonds (4).

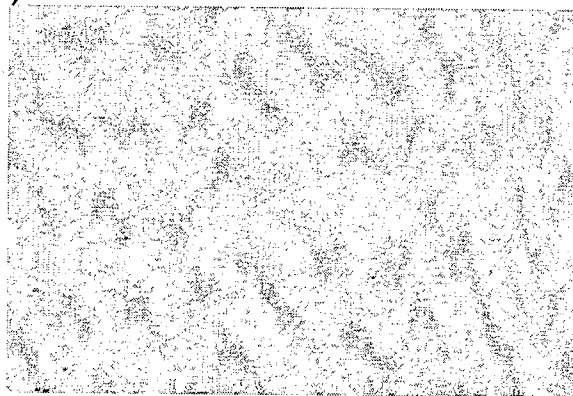


2/4

(a)



(b)



(c)

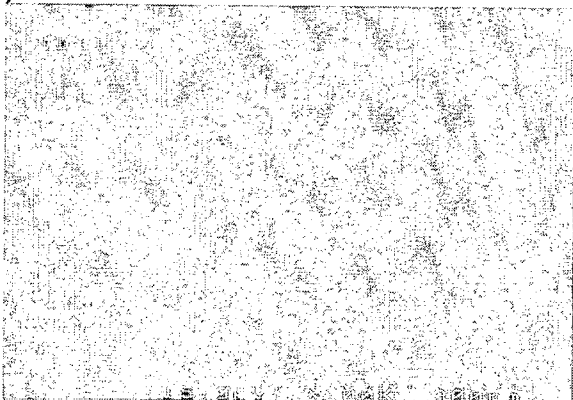


Fig. 3

FIG 4

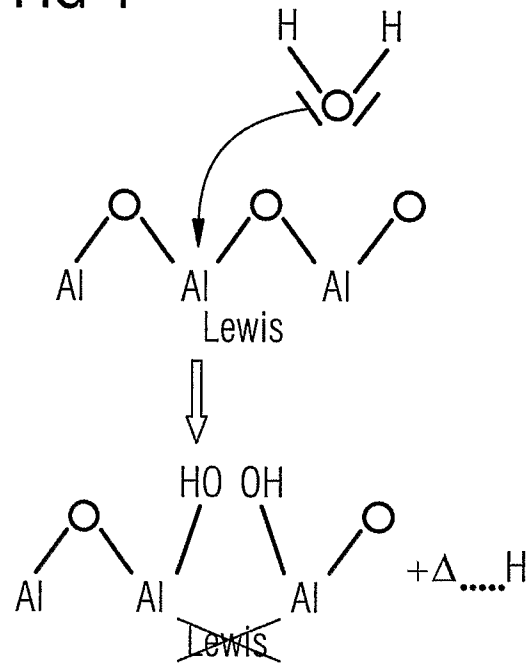


FIG 6

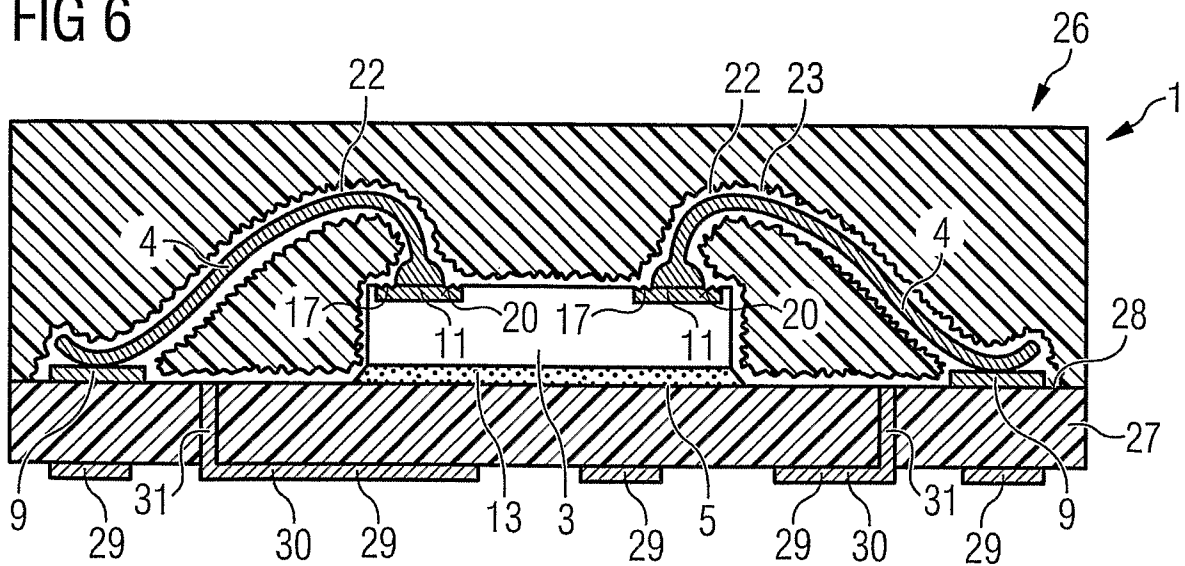
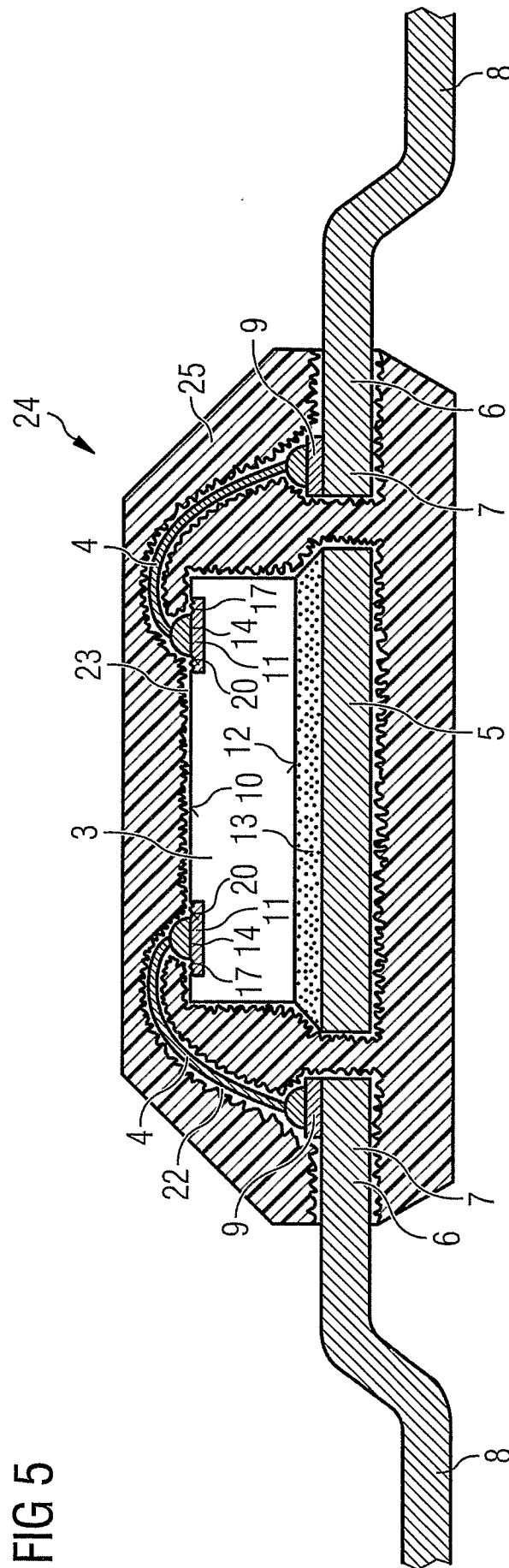


FIG 5



INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2006/001218

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H01L23/31 C25D7/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 C25D H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2005/008682 A (INFINEON TECHNOLOGIES AG [DE]; RIEDL EDMUND [DE]; SCHOBBER WOLFGANG [DE]) 27 January 2005 (2005-01-27) figure 9 page 1, line 7 - line 12 page 2, line 28 - line 30 page 7, line 28 - line 31 page 9, line 19 - line 20 page 12, line 4 - line 14 page 16, line 18 - line 22 page 25, line 15 - line 16	1-29
A	DE 101 24 047 A1 (INFINEON TECHNOLOGIES AG [DE]) 21 November 2002 (2002-11-21) figure 4 paragraph [0010] paragraph [0023] paragraph [0058] ----- -/--	1-29

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

16 January 2007

Date of mailing of the international search report

05/02/2007

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INTERNATIONAL SEARCH REPORT

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WO 2006/034682 A (INFINEON TECHNOLOGIES AG [DE]; KESSLER ANGELA [DE]; MAHLER JOACHIM [DE]) 6 April 2006 (2006-04-06) figures 1,2 page 2, line 25 - page 3, line 18 page 5, line 18 - line 23 page 8, line 24 - line 26 page 16, line 25 - line 29 -----	1-29

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Information on patent family members

International application No

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