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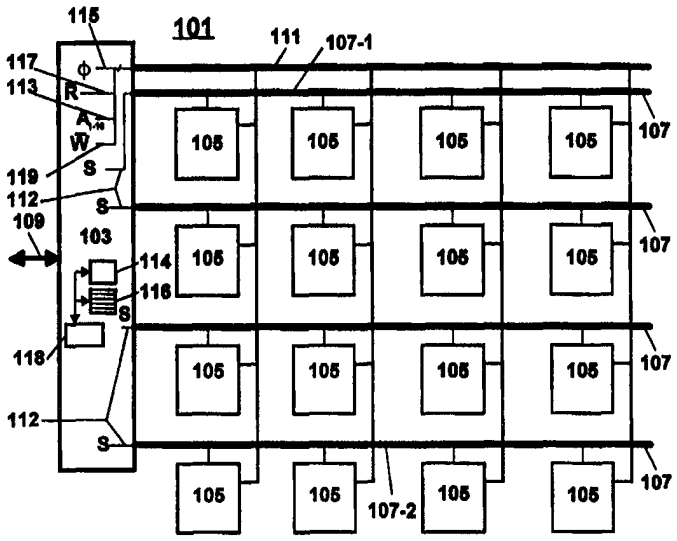

(57) Abstract

This disclosure provides a memory system and device for synchronizing response across multiple memory devices (105), whether arranged serially upon a single data bus, in parallel across multiple data busses (107), or both. A memory controller (103) periodically configures the system (101) by separately placing each memory chip (105) into a configuration mode. While in this mode, the chip (105) is polled by the controller (103) along the corresponding data bus (107), and the chip (105) responds with a reply. The controller (103) uses this reply to compute elapsed time between polling and the reply. Using all of the chips (105), the controller (103) determines the maximum response time, in termes of elapsed clock cycles. Based on this maximum time, and the individual response times for each chip, the controller (103) then programs each chip (105) with a number which defines chip–based delay (149) for responses to data read operations. In this manner, successive data reads can be performed on successive clock cycles without awaiting prior completion of earlier data reads. In addition, in a multiple data bus system, the controller (103) is not delayed by having to wait for all simultaneous data reads across a wide bus.

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MEMORY SYSTEM AND DEVICE

This disclosure relates to a memory system and device and, more particularly, provides a method of synchronizing response from memory chips.

BACKGROUND

As computers and their central processing units ("CPUs") become capable of executing instructions more rapidly, this ability carries with it a need for increased memory size and speed, and also bus size. The need has given rise to much design effort directed toward optimizing current and future memory device designs to provide quick memory response. Commonly-recognized current examples of memory devices include dynamic random access memories ("dRAMs"), read only memories ("ROMs") and synchronous random access memories ("SRAMs"), as well as mechanical and optical devices, such as CD-ROMs.

In performing a typical data read operation, a memory controller (usually the CPU or a dedicated memory controller in larger systems) sends a read command to a particular memory chip. This command is propagated to the chip along one or more lines of a command bus. When received by the particular chip, the command causes the chip to locate and direct an output from its internal memory array onto a data bus, as a return data signal intended for the memory controller. The output then propagates along the data bus, which may or may not travel the same route as the command bus. In the example just given, there are four sources of time delay, including the propagation time of a read command from the controller to the chip, the time required for the chip to power its

internal registers and channel the proper output onto the data bus, and the time required for propagation of the output back to the controller. The fourth source of time delay, present in systems which have split data busses (e.g., with separate, parallel data busses carrying bit-groups of different significance), is controller delay caused by slow retrieval along one of the parallel data busses. Typically, design efforts have focussed only on reducing the second of these times, that is, on improving internal routing and processing of instructions within memory chips.

The design efforts mentioned above, however, while continually providing more responsive memory devices, do not enable synchronization across multiple busses, nor do they eliminate the possibility of simultaneous bus contention among multiple memory chips, a problem explained with reference to FIGS. 1 and 2.

Bus Contention.

FIG. 1 illustrates a hypothetical memory system 21 which is accessed by a CPU 22. The memory system 21 includes a memory controller 23, a command bus 25, a data bus 27, and two memory devices 29 and 31 which are, in the example of FIG. 1, RAM chips. The command bus includes a system clock signal 33, issued by the controller, a data read signal 35, and an address bus 37. Each of the RAM chips 29 and 31 are presumed to be at different distances from the controller 23 from the standpoint of bus wiring, such that commands take a slightly different amount of time to reach each chip. FIG. 2 provides timing diagrams for purposes of explaining the problem of simultaneous bus contention.

It is desired for the memory system 21 to operate as quickly as possible, so the controller 23 will issue three data read commands on consecutive clock cycles; the first and third of these commands are directed to each of the aforementioned RAM chips 29 and 31, and the second command is unimportant to the present discussion and, so, it is indicated by a dash (-). It is presumed that the system clock has a frequency of 250 megahertz, so the width of each square pulse of FIG. 2A has an associated "high" time of 2 nanoseconds. FIG. 2B illustrates the issuance of two data read operations 39 and 41 by the memory controller, respectively labeled "X" and "Y," which then propagate along the command bus toward their intended RAM chip destinations.

FIG. 2C indicates timing of command "X" response by a first one 29 of the RAM chips, whereas FIG. 2D indicates timing of command "Y" response by the second one 31 of the RAM chips. The first chip 29, as indicated by FIG. 2C, receives its command "X" 8 clock cycles after it has been propagated, and beginning on the ninth clock cycle, takes 20 nanoseconds to retrieve and place its output "D-X" onto the data bus. By contrast, the second chip 31, as indicated by FIG. 2D receives its command "Y" only 7 clock cycles after it has been propagated, and it also takes 20 nanoseconds to place its output "D-Y" onto the data bus. If the output for each RAM chip 29 and 31 takes the same amount of propagation time to return to the controller as was the case for the commands to originally reach the RAM chips, then both outputs "D-X" and "D-Y" will arrive at the controller 23 at the same time, as indicated by a hatched block 43 of FIG. 2E. It will be noted that the address bus and data bus have been indicated, in this example, to have similar propagation times associated with them, though this result will not necessarily be the case in memory system

designs in which the command bus and data bus are separately routed. Further, while only two memory devices are indicated above, it will readily be seen that the problem of bus contention is particularly complicated as the number of memory devices is increased, and as CPUs become more and more efficient, operating at multi-hundred megahertz frequencies and greater.

There exists a definite need for a memory system which permits simultaneous response along multiple, parallel data busses. Also, there exists a definite need for a system that avoids simultaneous bus contention between multiple memory devices along one data bus. Preferably, such a system would address situations where propagation times for reaching individual chips may differ by an entire clock cycle or greater. By avoiding multiple device bus contention, it is hoped that memory controllers, such as CPUs and dedicated memory controllers, can perform data read and write operations on consecutive clock cycles, thereby keeping pace with CPU design, and the tendency toward increased computer speed and memory capacity. The present invention solves these needs and provides further, related advantages.

SUMMARY OF THE INVENTION

The present invention provides a memory system and device that fulfills the needs mentioned above; it provides a memory system where individual memory devices (such as micro-chips) can be delayed in operation to provide data outputs to a controller, such as a CPU or memory controller, a predetermined time after a request for data is made. Consequently, the CPU or memory controller does not have to wait until a first data read is completed prior

to beginning a second data read. Also, the system facilitates use of a scalable data bus, since memory chips feeding parallel 8-bit or other size data busses can be delayed to provide simultaneous response to a CPU, notwithstanding differences in wiring and bus routing. As can be seen therefore, the present invention provides a memory system with substantial utility.

A first form of the invention provides a memory system having a controller and at least two memory devices, with at least one data bus coupling the controller with each memory device. The controller sends a command to both of the memory devices, which provide a reply back to the controller. When sending a command, the controller begins timing, and awaits receipt of the reply, when the controller is able to determine an elapsed time. Once this is done for both memory devices, the controller determines a maximum travel time and adjusts the response time of at least one of the two memory devices.

In this manner, a device built according to the present invention can synchronize response for memory devices (1) across parallel data busses, for example, across four individual 16-bit data busses that make up a 64-bit data bus, to ensure simultaneous response, (2) serially, along one data bus, to avoid bus contention between multiple devices along the same data bus, such that data reads can be performed on successive clock cycles, or (3) both of the above.

To this effect, a second form of the invention provides a memory device having a buffer for delaying operations of the memory device. According to this form of the invention, the memory device receives a system clock and has stored in the buffer a number of clock cycles by

which it is to delay the device's output. When a data read command is then received, the device can first begin by counting until the number indicated by the buffer is reached, and then commence data fetch operations. Alternatively, the device can immediately fetch data from an internal memory storage area and delay latching its output onto the corresponding data bus by an amount responsive to the buffer's contents.

In more particular aspects of the invention, the memory device can include a configuration mode which the device is directed to enter by a system controller. The controller preferably writes a configuration command to a mode register of the memory device, which causes the device to monitor the data bus connecting the device to the controller; the device monitors the bus to detect both an input strobe and a predetermined data word from the controller. When the memory device detects this data word, it latches a reply word onto the data bus together with an output strobe, preferably derived locally by the device from the system clock. The controller uses the output strobe to notify it that incoming data on the data bus is valid, and consequently may be used to determine elapsed time. From this elapsed time, the controller determines the delay time suitable to the particular device, and loads it into the device's buffer. Preferably, this result is performed by detecting a maximum of all response times, and by loading into each buffer a number of clock cycles which delays latching of the corresponding chip's output to synchronize response to the maximum time.

In still more particular features of the invention, the device can perform correction to the buffer contents, by accepting a write command from the controller, by counting a difference between time of arrival of the write

command itself and write data, and by adjusting contents (the delay time) of the device's buffer, to thereby correct for differences in travel time between a command bus and a data bus.

Other forms of the invention are indicated below and in the claims, and include related systems and methods for performing memory synchronization related to the two forms of the invention discussed above.

The invention may be better understood by referring to the following detailed description, which should be read in conjunction with the accompanying drawings. The detailed description of a particular preferred embodiment, set out below to enable one to build and use one particular implementation of the invention, is not intended to limit the enumerated claims, but to serve as a particular example thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of one hypothetical memory system used to illustrate the prior art; a broken line separates a computer's central processing unit ("CPU"), which is above the line, and a memory system, located below the line.

FIG. 2 is a series of timing diagrams used to illustrate the problem of bus contention between multiple memory devices, in the hypothetical prior art system of FIG. 1.

FIG. 3 is a block diagram of the preferred embodiment, which uses both parallel data busses ("baby-

busses," which together make up a wide system bus) and simultaneous fetch of words (of 64, 132 or greater bit length) and shared data bus use among multiple memory devices.

FIG. 4 is a block diagram of a single memory device of FIG. 3; preferably, the device is a dynamic random access memory ("DRAM").

FIG. 5 is a series of timing diagrams corresponding to a portion of the system of FIG. 3; in particular, FIG. 5 illustrates synchronization of responses from two memory devices.

DETAILED DESCRIPTION

The invention summarized above and defined by the enumerated claims may be better understood by referring to the following detailed description, which should be read in conjunction with the accompanying drawings. This detailed description of a particular preferred embodiment, set out below to enable one to build and use one particular implementation of the invention, is not intended to limit the enumerated claims, but to serve as a particular example thereof. The particular example set out below is the specific implementation of a memory system, in particular, one that is used for to synchronize responses from multiple memory devices, whether arranged along a single data bus, or in across parallel data busses, or both.

In accordance with the present invention, the preferred embodiment is memory system 101, indicated in FIG. 3. A memory controller 103, which may be either a CPU or a dedicated memory controller, accesses numerous memory

chips 105 which are arranged both serially and in parallel. In other words, the system includes multiple, parallel data busses, preferably 16-bit data busses ("baby-busses") 107, with several memory devices on each baby-bus. This construction lends itself to a scalable bus system, e.g., in which the system data bus is 64-bits or 132-bits wide, or greater, with the least significant bits of data being retrieved along one baby-bus 107-1, and the most significant bits of data being retrieved along another baby-bus 107-2.

Implementing the features of the present invention, the controller synchronizes memory retrieval both amongst multiple chips 105 along each single baby-bus 107, as well as across the multiple baby-busses. Combined synchronization both across parallel busses and across serially-arranged chips is not necessary to practice the invention as defined by the claims below, and synchronization of memory devices either serially or in parallel, alone, is within the spirit of the present invention. Synchronization across multiple baby-busses 107 is performed in the preferred embodiment to ensure that the controller 103 is not delayed by a slow response along one of the baby-busses 107. Synchronization along each single baby-bus 107 is performed to reduce the possibility of bus contention by multiple chips 105, enabling the controller to perform multiple data reads from different chips 105 on consecutive cycles notwithstanding differences in propagation times along each baby-bus 107.

The controller 103, if it is a dedicated memory controller, receives memory requests along a master bus 109 which couples it to a system CPU (not illustrated). These requests are managed by the controller 103 across all of the baby-busses 107, each one of which may consist of

sixteen data lines and a strobe line 112 (to be discussed further below). The controller 103 also uses a single command bus 111 which connects the controller 103 with all memory chips 105. Typically, the command bus 111 will include each of an address bus 113, a system clock 115, a data read signal 117, a data write signal 119, and other lines as well (not shown) such as various interrupt lines, chip select circuitry and the like. Preferably, each memory chip 105 is a random access memory and, specifically, a dynamic random access memory, requiring periodic refresh. Since the memory devices can be affected by temperature, each device 105 is preferably configured both upon system power-up and also at periodic intervals for the purposes of synchonizing memory retrieval.

Each chip 105 includes an input buffer (not seen in FIG. 3) which is loaded with a number after the controller 103 has polled all of the memory chips. The number is derived from a number of elapsed system clock cycles, counted by the controller, corresponding to the slowest chip in the system 101 to respond. Preferably, the controller 103 during the configuration mode separately enables each memory chip 105, by programming a configuration command into a mode register of the chip (seen in FIG. 5, and described below), which then causes only that chip to be active and to enter a mode where it listens to its corresponding baby-bus. When a chip 105 in this mode detects an input strobe (including a predetermined data transmission to it along the data bus), it responsively transmits a predetermined response word back onto the data bus, together with the output strobe 112, which is then used to latch the predetermined response word into the controller 103. Receipt of the output strobe 112 and the predetermined response word indicates to a comparison mechanism 118 of the controller 103 that it

should freeze an internal timer, which has been incremented with each system clock pulse elapsed since the controller issued the input strobe, and load that counter's contents into memory internal to the controller, both into a memory spot 114 representing a maximum count (if the counter represents a maximum), and also into a slot 116 dedicated to the particular chip 105. Once the controller has polled all of the memory chips 105, it then calculates an offset for each chip by which each chip is to delay its output, such that data read operations provide data to the memory controller at the maximum response time. In other words, the controller 103 subtracts the response time for each chip from the maximum, to obtain the offset, and it then programs each chip 105 with the appropriate offset.

FIG. 4 is a block diagram a single chip 105 from FIG. 3. In particular, the preferred chip is a DRAM 123 which includes an internal delay mechanism 121 for synchronizing memory response with other chips; preferably, this delay mechanism includes an output latch and an internal counter and the internal buffer. The DRAM 123 is coupled to the memory controller 103 via a number of communication paths, including (a) the command bus 111, (b) a 16-bit baby-bus 107, (c) the strobe signal 117, (d) a command strobe 125, (e) the system clock 115 and (f) a chip select signal, not seen in FIG. 4. When the system clock 115 is received by the DRAM 123, an internal phase locking mechanism 127 is used to provide a locally-derived clock signal 129 for timing internal operations of the DRAM and for defining a local time zero for coordinating memory operations.

When it is desired to configure a particular chip, e.g., the DRAM 123, during a configuration mode, the controller 103 enables the specific DRAM, simultaneously

disabling all other memory chips along the same baby-bus 107. This enablement is achieved by causing the controller 103 to send a configuration command to the DRAM via the command bus 111, which together with a command strobe, causes the DRAM to latch the command into internal timing and control logic 131. Since the configuration command, as indicated by FIG. 4, must pass through a second latch 133 before it reaches the internal timing and control logic 131, its arrival will be synchronized with the local clock signal 129 of the DRAM 123. The configuration command, for example, may be indicated by the most significant bits only of the address bus, and it does not require transmission of data along the baby-bus 107. These most significant bits are then coupled by the internal timing and control logic 131 into a mode register 132 and used to direct the DRAM 123 to enter the configuration mode.

In the configuration mode, the DRAM will simply monitor the baby-bus 107 for a predetermined data word, which will be accompanied by an input strobe to strobe the data word into a sync detect register 137. In response to detection of the data word, the timing and control logic will immediately cause a predetermined response word to be fed to an output latch 139 from a memory space 141, which the timing and control logic will enable via a sync control line 143. The predetermined response word will thereby be immediately gated back onto the baby-bus 107 and sent to the controller, usually on the local clock pulse immediately subsequent to presentation of the response word to the output latch 139. Accompanied by an output strobe, the predetermined response word is latched into the controller immediately upon receipt, and used to stop the internal timer of the controller's comparison mechanism 118.

FIG. 5 is used to indicate the results of the controller's determination of a maximum delay time across all of the chips 105 of FIG. 3. In particular, as was the case in connection with FIG. 2, it is desired for the controller 103 of FIG. 3 to perform data reads on successive clock cycles. In this regard, the controller sends data reads "X" and "Y" (designated by the reference numerals 145 and 147 in FIG. 5B) to two different memory devices which are serially coupled to the controller. These devices may consist of single chips 105 along a single baby-bus 107-1, or alternatively, may consist of plural chips coupled to the controller via different baby-busses 107. The data reads 145 and 147 are the first and third reads of a train of three consecutive data reads, with the middle data read indicated by a dash "-" in FIG. 5B. As with FIG. 2, each data read operation has a propagation time associated with it, and the operations arrive at a corresponding memory device in accordance with the corresponding propagation time. However, implementing the principles of the present invention, the memory device associated with command "Y" is programmed with an offset 149 representing a two clock cycle delay. Thus, that memory device will use its local clock to impose a delay of two clock cycles to the output latch (139 in FIG. 4). The offset corrects each individual chip to respond in accordance with the maximum response time for all of the chips, e.g., each chip has its response slowed to be in sync with the slowest chip. Consequently, presuming that all three of the memory devices are configured in accordance with the present invention, each one of the three data reads will be received on successive clock cycles, as indicated by the reference numeral 151 in FIG. 5E.

Returning to FIG. 4, the controller programs delay by loading an offset into the DRAM 123; it performs this programming by writing a number of clock pulses into an internal buffer 153 of the DRAM. Subsequently, when the DRAM 123 receives a data read command outside of the configuration mode, it processes the command in the normal fashion. However, when the product of the read command is presented at the output latch, that product is not immediately gated onto the data bus on the subsequent local clock pulse. Rather, the internal timing and control logic 121 withholds enablement of the sync control line 143 to delay output by an amount indicated by the buffer. Preferably, the buffer is combined with a timer for this purpose, which begins a countdown upon the detection of each read command received by the chip.

Importantly, there are a number equivalent implementations of this delay structure that will readily occur to those of skill in the art; for example, offset could be achieved by designing each memory device and the system to provide output at a predetermined clock cycle, but to program a number to make the output available "early" in response to buffer contents. Alternatively, each memory device could have multiple modes, with delay achieved by selecting one of several modes. Alternatively, delay could be implemented by circuit external to each memory device. These environments, as well as other modifications that will occur to those having skill in memory system design, are contemplated as being within the spirit of the present invention.

After the DRAM 123 has been programmed with the offset, the controller preferably calculates a correction which is used to refine the offset. Specifically, in the system of FIG. 3, each data buss (each baby-bus 107) and

the corresponding command bus 111 may have different path lengths. Since the offset was originally calculated using polling and reply both over the data bus only (the baby-bus 107), and since read commands are normally issued along the command bus, the offset may not correctly reflect desired delay. Consequently, the correction for each chip is used to refine the delay time associated with each chip 105 to correct this discrepancy, and the correction may differ from chip-to-chip.

To calculate the correction, the controller 103 sends a follow-up write command to each DRAM; the write command includes both the actual command transmitted along the command bus 111, as well as data transmitted along the corresponding baby-bus 107. With reference to FIG. 4, as the command is received by the DRAM 123 from the command, it is provided to a first sync detect circuit 155, which provides an indication of a received command to a command state counter 157. The command state counter 157 then begins counting with each local clock pulse. The data corresponding to the command received from the corresponding baby-bus 107 is also fed to a second sync detect circuit 159, which similarly provides an indication of received data to a data state counter 161. This data state counter 161 also begins counting with each local clock pulse. Thus, receipt of either the write command, or its corresponding write data, will trigger one or the other of the counters 157 or 161 to begin counting. Receipt of both indications from the sync detect circuits 155 and 159 is used to gate, via a subtract circuit 163, a difference in number of clock cycles between command receipt, and an output reflecting this difference is provided to the timing and control logic 131 of the DRAM 123. This difference represents the correction to the offset in number of clock cycles. Thus, depending upon whether the command bus is

slower or faster than the data bus, in terms of propagation time, the timing and control logic 131 will modify the contents of the internal buffer 153 accordingly. Consequently, once the offset and correction are calculated, the contents of the internal buffer 153 will thereafter precisely reflect a desired number of offset clock cycles for achieving synchronization across multiple memory devices.

What has been described is a memory system and device for achieving synchronous data reply, at the controller, from many memory devices, such as from DRAM chips. Using the preferred embodiment described above, one may achieve substantially synchronous memory response either from parallel memory devices, e.g., as connected across multiple baby-busses 107, and providing bit groups of different significance for one data word fetch (e.g., for a 64-bit word fetch), or for avoiding bus contention between multiple memory devices coupled to the same data bus, as explained with reference to FIGS. 2 and 4. Notably, the system described herein performs correction for only integer clock cycles, and does not achieve phase correction between different memory chips. The system described herein, however, is compatible with systems for achieving phase synchronization, such as described in U.S. Patent No. 4,998,262, which is hereby incorporated by reference.

Having thus described an exemplary embodiment of the invention, it will be apparent that further alterations, modifications, and improvements will also occur to those skilled in the art. Such alterations, modifications, and improvements, though not expressly described or mentioned above, are nonetheless intended and implied to be within the spirit and scope of the invention.

Accordingly, the foregoing discussion is intended to be illustrative only; the invention is limited and defined only by the various following claims and equivalents thereto.

CLAIMS

1. In a digital memory system (101) having a controller (103) and at least two memory devices (105), with at least one data bus (107) coupling the controller (103) with each memory device (105), the controller (103) also having a (115) by which the controller (103) times its operations, an improvement comprising:

a buffer (153) in each memory device (105), each buffer (153) adapted to store a number (149) corresponding to an amount of time for which the corresponding buffer (153) is to delay data output;

a routine run by the controller (103) which causes the controller

to, for each memory device,

prompt the memory device for a response, and

count a number of clock pulses at the controller (103) between prompting of the memory device (105) and receipt of the corresponding response from the memory device (105),

to determine a maximum delay measured by the maximum number of clock pulses needed for response across the at least two memory devices (105), and

to cause the buffer (153) of each memory device (105) to store a number sufficient to cause data from the corresponding memory device (105)

to be received at the controller (103) at the maximum delay time; and

circuitry (121) in each memory device (105) that delays data output in response to the number stored in the corresponding buffer (153).

2. An improvement according to claim 1, wherein each memory device (105) receives the system clock (115) and generates a local clock (129) in response thereto, said improvement further comprising:

an output strobe (112) issued by each memory device (105) in response to being prompted, the output strobe (112) being locally derived from the system clock (115) at the location of the corresponding memory device (105) and coupled to the controller (103) so as to strobe arrival of the response from the particular memory device (105).

3. An improvement according to claims 1 or 2, wherein the system bus includes a data bus (107) and a command bus (111) having different path lengths, said improvement further comprising:

a delay configuration mode of each memory device (105), the delay configuration mode being instructed through the command bus (111) and causing the corresponding memory device (105) to

wait for presence of a data signal on the data bus (107) and an input strobe (125) to accept the data, the data signal forming at least part of the prompt from the controller (103), and

issue the response to the controller (103) in reply to the data signal.

4. An improvement according to claim 3, further comprising:

a delay adjustment mechanism within each memory device, the delay adjustment mechanism receiving a command from the command bus (111) and data from the data bus (107), and calculating a deviation in time to the number for the corresponding memory device (105), the number correcting for difference in travel time between the command bus (111) and the data bus (107).

5. An improvement according to claim 1, 2, 3 or 4, said improvement further comprising:

arrangement of at least two memory devices (105) on a single, shared data bus (107).

6. An improvement according to claim 1, 2, 3, 4 or 5, said improvement further comprising:

arrangement of at least two memory devices (105) on different, parallel data busses (107).

7. A method of synchronizing response in a memory system (101) which includes a plurality of memory devices (105) coupled to a controller (103) via at least one data bus (107), wherein the controller (103) performs data read operations from the memory devices (105) according to its own system clock (115), and the data read operations have an associated travel time between the controller (103) and corresponding memory devices (105), said method comprising:

individually enabling each memory device (105) along each data bus (107);

while a particular memory device (105) is enabled, sending a signal to the particular memory device (105) from the controller (103);

for each memory device (105), sending a reply to the controller (103) in response to the corresponding signal;

counting an elapsed time between sending the signal and receipt of the reply to obtain a response time, for each memory device (105);

in response to the response times for the memory devices (105), determining a maximum response time; and

causing each of the memory devices (105) to provide a data reads to the controller (103) at a predetermined time from command, selected in dependence upon the maximum response time.

8. A method according to claim 7, wherein each memory device (105) includes a buffer (153) and a delay mechanism (121) causing the memory device (105) to delay its output by an amount determined in response to contents of the buffer (153), wherein:

causing each of the memory devices (105) includes loading each buffer (153) with a corresponding number; and

delaying with the delay mechanism (121) an output of each memory device (105) in response to the contents of the corresponding buffer (153).

9. A method according to claims 7 or 8, wherein at least one memory device (105) accepts data write commands from the controller (103) and includes a mode register (132) that enables the at least one memory device (105) and causes it to await a polling command from the controller (103) along at least one data bus (107) associated with the at least one memory device (105), and the memory system (101) further includes at least one command bus (111) coupling the at least one memory device (105) to the controller (103), said method further comprising:

using the command bus (111) to command the mode register (132) to cause the at least one memory device (105) to await the polling command;

sending the polling command to the at least one memory device (105), the system controller (103), in association with sending the polling command, counting system clock cycles;

detecting the polling command at the memory device (105) and responsively sending the reply to the controller (103);

detecting the reply at the controller (103) and identifying a number of elapsed clock cycles; and

computing the number for the at least one memory device (105) therefrom.

10. A method according to claims 7, 8, or 9, further using a system clock signal (115) issued via the controller (103), wherein the at least one memory device (105) is coupled to the system clock signal (115) and provides an internal clock (129) based on the system clock signal (115), and further, provides a strobe signal (112) as an output, said method further comprising:

issuing the strobe signal (112) in synchronization with issuing the reply; and

using the strobe signal (112) to indicate to the system controller (103) that the reply is arriving at the system controller (103).

11. A method according to claims 7, 8, 9, or 10, wherein each memory device (105) further includes a predetermined data word stored internally, said method further comprising:

for each memory device (105), in response to the signal, coupling the predetermined data word to at least one associated data bus (107).

12. A method according to claim 7, 8, 9, 10 or 11, said method further comprising:

arranging at least two memory devices (105) on a single, shared data bus (107).

13. A method according to claim 7, 8, 9, 10, 11 or 12, said method further comprising:

arranging at least two memory devices (105) on different, parallel data busses (107).

14. A memory device (105) for use in a memory system (101) having a memory controller (103) and a system bus, wherein the memory controller (103) polls each of several memory elements (105) to determine an associated command response time and determines a desired response time, comprising:

a memory space (141) wherein data is stored;

an output path for coupling data from the memory space to the system bus in response to a data read command;

memory space drivers that accesses data locations within the memory space (141) and that couple contents of selected ones of the data locations to the output path in response to a data read command;

a clock mechanism (127) that provides a clock signal (129) to synchronize internal operations of said memory device (105);

a buffer (153) that stores a number of clock pulses; and

a delay mechanism (121) coupled to the buffer (153), the delay mechanism (121) causing delay of at least one of said output path and said memory space drivers by an amount corresponding the number of clock pulses;

wherein said device is adapted for synchronization with other memory elements (105), in response to the controller (103) causing the buffer (153) to be loaded with a number that causes equalization of command response time for said device to the desired response time.

15. A memory device according to claim 14, wherein the memory system (101) further includes a data bus (107) and a system clock (115) issued by the system controller (103), and wherein:

said device further comprises

a mode register (132) that is selectively programmed by command from the system controller (103) to cause said device to enter a calibration mode,

a predetermined response word stored within said device, the predetermined response word being coupled to the data bus (107) in response to a polling command from the system controller (103), and

an output strobe (112) of said device, the output strobe (112) being locally derived at said device from the system clock (115); and

the calibration mode causes said device to await the polling command and, in response to detection of the polling command by said device on the data bus (107), to couple the predetermined response word and the echo strobe onto the data bus (107).

16. A memory device according to claims 14 or 15, wherein the system bus further includes a command bus (111), and wherein:

said device further receives the number from the system controller (103) and stores it in the buffer (153); and

said device further comprises

a comparison mechanism (163) for comparing time of receipt of at least one signal along the command bus with time of receipt of a corresponding signal along the data bus, and for providing an output, and

an adder to which the output is coupled, the adder (131) modifying the number by the output to compensate for difference between travel time along the data bus and travel time along the command bus.

17. A memory device according to claims 14, 15, or 16, wherein the memory device is a random access memory.

18. A memory device according to claim 14, 15, or 16, wherein the memory device is a dynamic random access memory.

19. A memory system, comprising:

a memory controller (103);

a first memory device (105) having a buffer (153), and internal delay means (121) for delaying output in response to contents of the buffer (153);

a second memory device;

a system bus coupling one of commands and data between the memory controller (103) with each of the first memory device and second memory device, the system bus having difference in travel times between the memory controller with the first memory

device, and the memory controller with the second memory device;

a calibration mode of the controller (103), which causes the controller (103) to poll each of the first memory device and the second memory device and to time response from each of the first memory device and the second memory device; and

a comparison device of the controller (118), which compares during the calibration mode the timed response from each of the first memory device (105) and second memory device and calculates a number corresponding thereto;

wherein the calibration mode of the controller (103) causes the controller to store the number in the buffer (153), such that the internal delay means (121) delays output in response to the number.

20. A memory system according to claim 19 wherein:

both of the first and second memory devices are coupled to the controller (103) on a single, shared data bus (107).

21. A memory system according to claims 19 or 20, wherein:

both of the first and second memory devices are coupled to the controller (103) on different, parallel data busses (107).

22. A memory system according to claims 19 or 20 wherein:

both of the first and second memory devices are coupled to the controller (103) on a single, shared data bus (107);

said memory system (101) further comprises a third memory device which is coupled to the controller (103) on a second data bus, different from the shared data bus, the third memory also having a buffer (153);

the calibration mode of the controller (103) causes to poll the third memory device;

the comparison device (118) additionally compares a timed response from the third memory device with time response for at least one of the first and second memory devices;

the calibration mode of the controller (103) causes the controller to store a second number in the buffer (153) of the third memory, such that the third memory may be synchronized for simultaneous data delivery at the controller with one of the first and second memory devices.

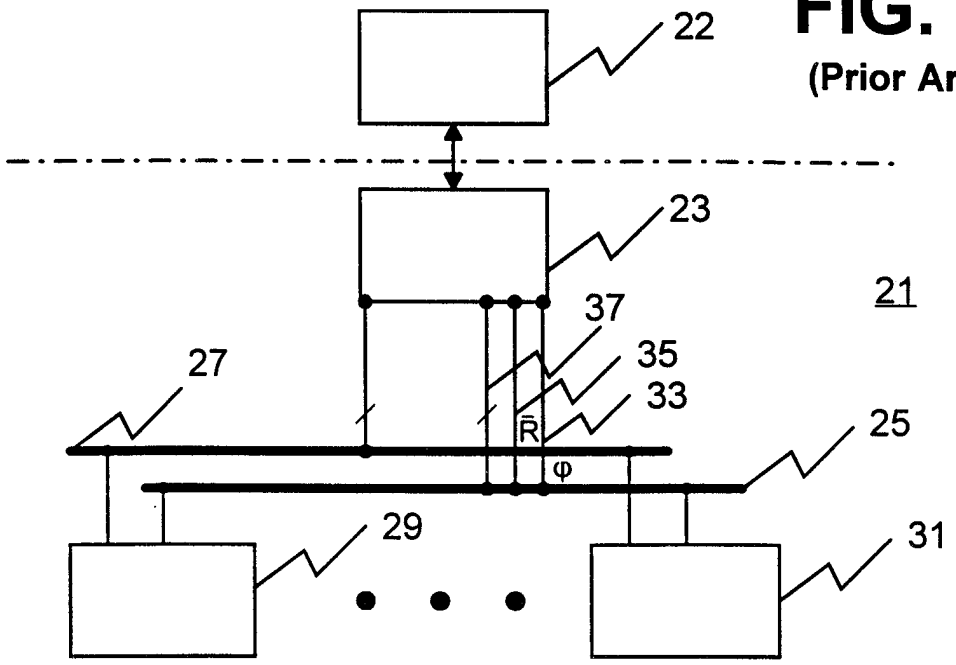

FIG. 1
(Prior Art)

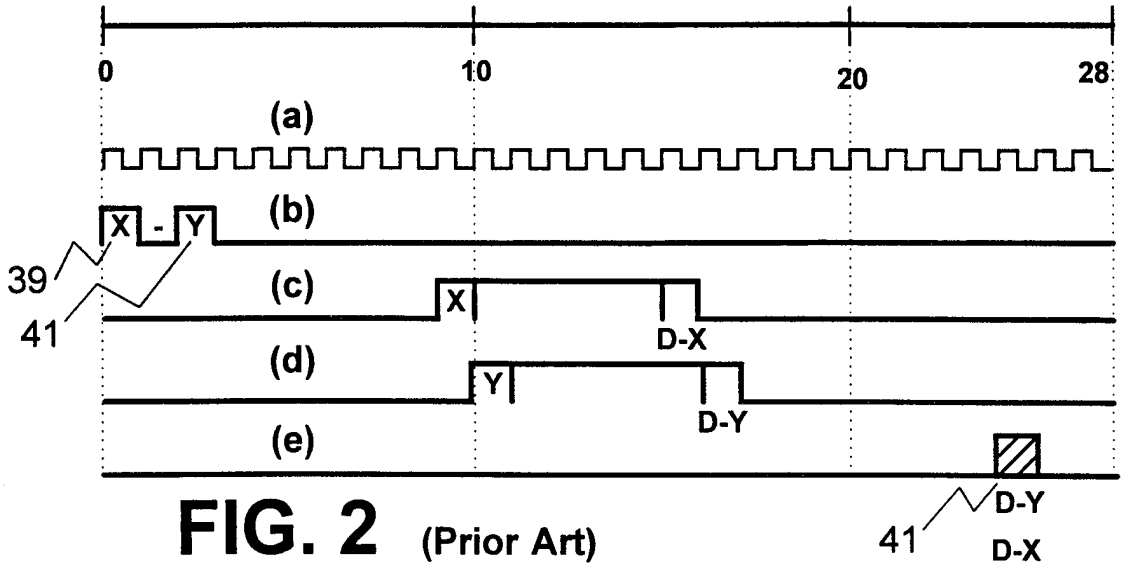

FIG. 2 (Prior Art)

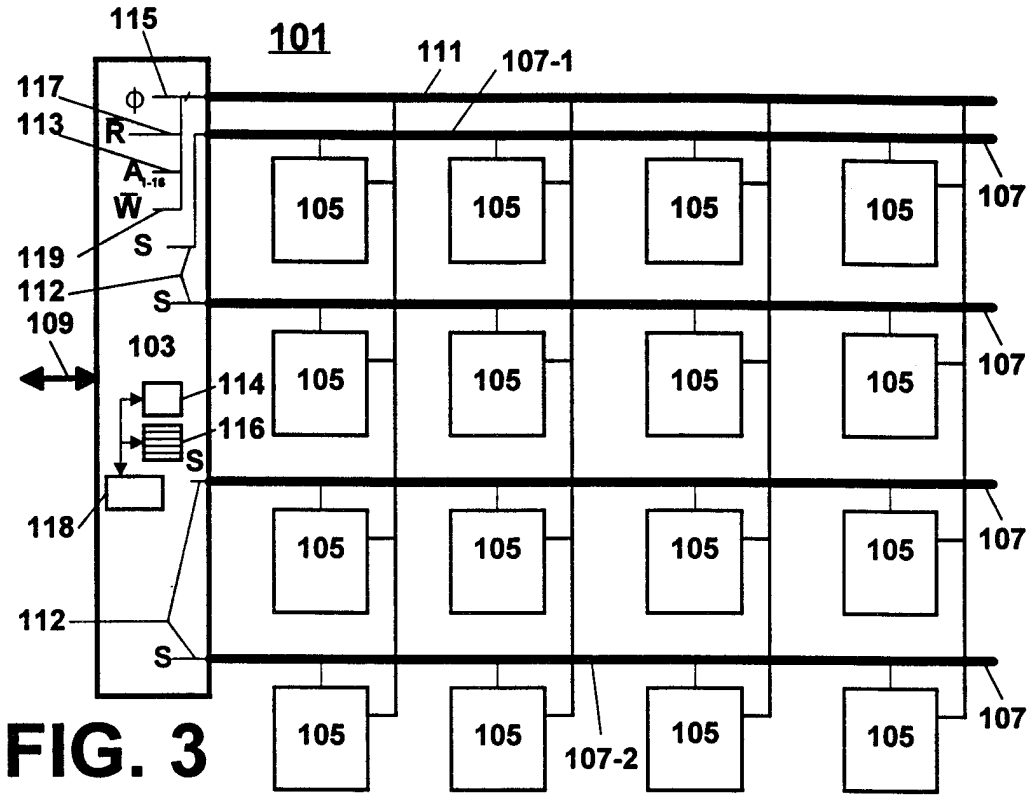
115
101
111
107-1
117
113
119
112
109
103
114
116
118
112
105
107
107-2

FIG. 3

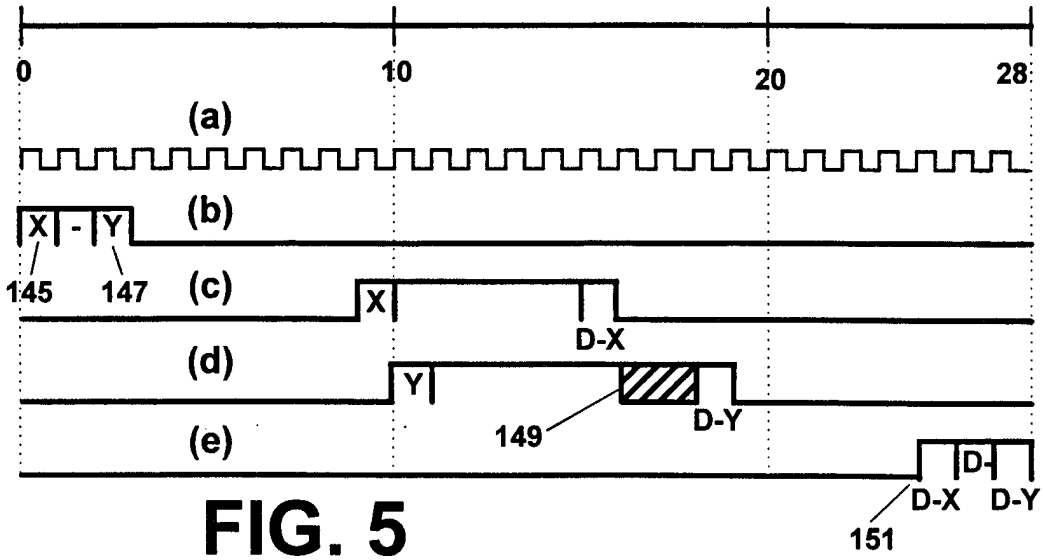
0
10
20
28
(a)
(b)
X
-
Y
145
147
(c)
X
D-X
(d)
Y
149
D-Y
(e)
D-X
D-Y
151

FIG. 5

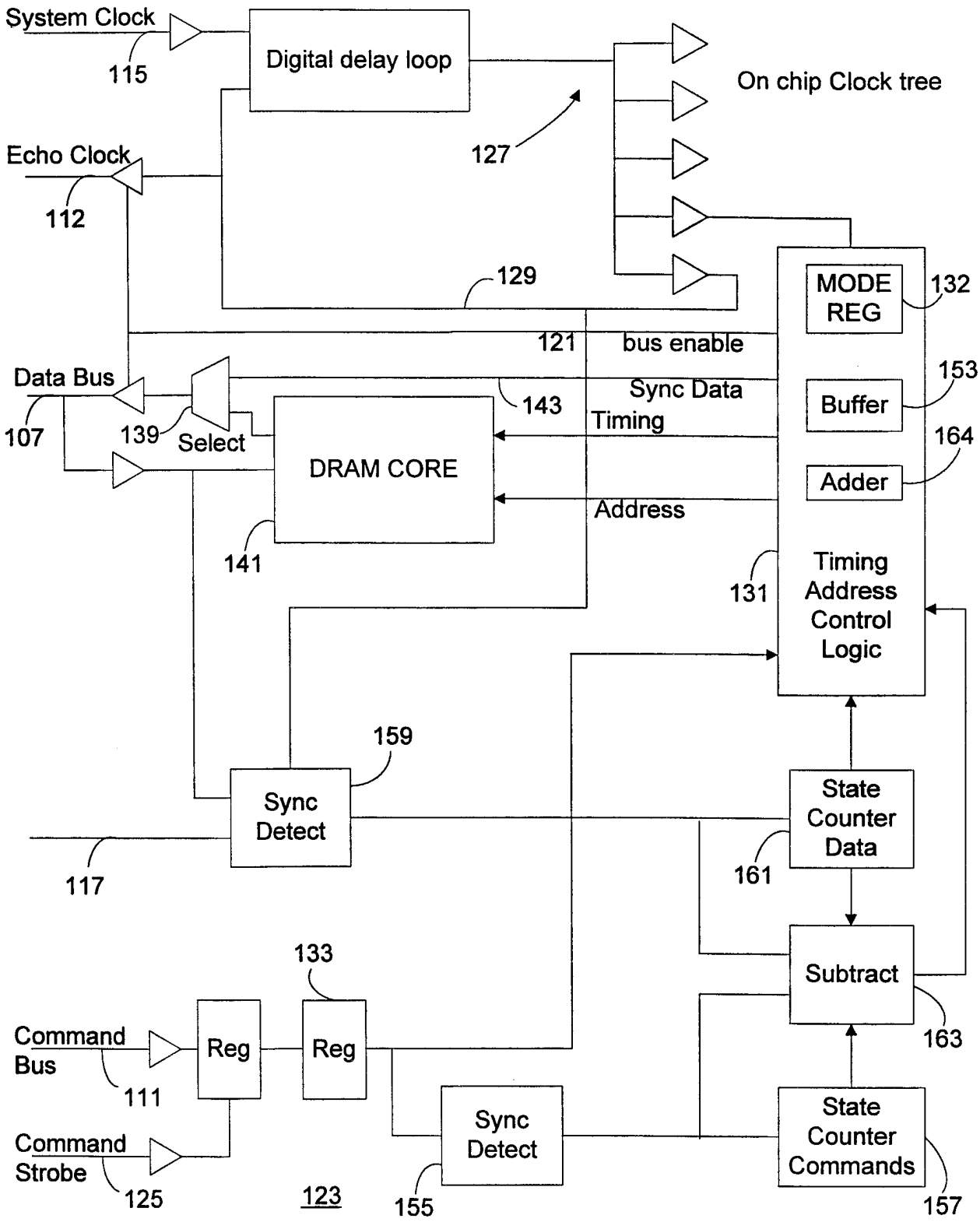
System Clock
115
Digital delay loop
On chip Clock tree
127
Echo Clock
112
129
MODE REG
132
121
bus enable
Data Bus
107
139
Select
143
Sync Data
Timing
153
Buffer
164
Adder
DRAM CORE
Address
141
131
Timing Address Control Logic
159
Sync Detect
117
State Counter Data
161
Subtract
133
163
Command Bus
111
Reg
Reg
Command Strobe
125
123
Sync Detect
155
State Counter Commands
157

FIG. 4

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 97/18128

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/16

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 339 224 A (I. B. M.) 2 November 1989 see page 3, line 15 - page 4, line 17 see page 5, line 19 - page 6, line 43; claims; figures 2,4	1,7,14, 19
A	US 5 509 138 A (CHRISTINE G. CASH) 16 April 1996 see column 2, line 26 - line 64 see column 8, line 65 - column 9, line 22; claims; figure 4	1,7
A	EP 0 238 090 A (NEC CORPORATION) 23 September 1987 see column 2, line 25 - column 3, line 7 see column 9, line 51 - column 11, line 57; claims; figures	1,7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 1998	25/02/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Soler, J

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int[illegible]ional Application No
PCT/US 97/18128

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