

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
15 February 2007 (15.02.2007)

PCT

(10) International Publication Number
WO 2007/018968 A1

(51) International Patent Classification:
H01L 21/283 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2006/027367

(22) International Filing Date: 13 July 2006 (13.07.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/195,174 2 August 2005 (02.08.2005) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US];
8000 South Federal Way, Boise, ID 83716 (US).

(72) Inventor: HU, Yongjun, Jeff; 2571 South Culpepper Avenue, Boise, ID 83709 (US).

(74) Agents: MATKIN, Mark, S. et al.; Wells St. John P.S.,
601 West First Avenue, Suite 1300, Spokane, WA 99201-3828 (US).

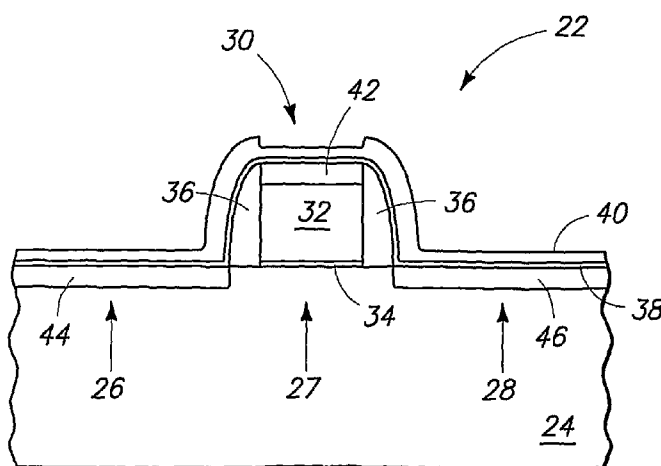
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS OF FORMING CoSi_2 , METHODS OF FORMING FIELD EFFECT TRANSISTORS, AND METHODS OF FORMING CONDUCTIVE CONTACTS



(57) Abstract: The invention included to methods of forming CoSi_2 , methods of forming field effect transistors, and methods of forming conductive contacts. In one implementation, a method of forming CoSi_2 includes forming a substantially amorphous layer comprising MSi_x over a silicon-containing substrate, where "M" comprises at least some metal other than cobalt. A layer comprising cobalt is deposited over the substantially amorphous MSi_x -comprising layer. The substrate is annealed effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with silicon of the silicon-containing substrate to form CoSi_2 beneath the substantially amorphous MSi_x -comprising layer. Other aspects and implementations are contemplated.

WO 2007/018968 A1

DESCRIPTION

METHODS OF FORMING CoSi_2 , METHODS OF FORMING FIELD EFFECT TRANSISTORS, AND METHODS OF FORMING CONDUCTIVE CONTACTS

5

TECHNICAL FIELD

This invention relates to methods of forming CoSi_2 , to methods of forming field effect transistors, and to methods of forming conductive contacts

10

BACKGROUND ART

Metal silicides are conductive metal compounds commonly used in the fabrication of integrated circuitry. Exemplary uses are as conductive interfaces to silicon-containing node locations, and as conductive contacts to and conductive strapping layers for field effect transistor gates.

15

One exemplary low resistance metal silicide is CoSi_2 . Cobalt silicide also occurs in the monosilicide form (CoSi), but it is the disilicide form which is of greater conductivity and that which is desired to be used in the fabrication of a conductive integrated circuit component. Cobalt silicide can be expressed as CoSi_x , where "x" typically ranges from 0.3 to 2.

20

One manner of forming cobalt silicide includes deposition of a layer of cobalt over a silicon-containing material, followed by subsequent high temperature anneal causing interdiffusion of the silicon and cobalt, thereby forming cobalt silicide. Typically and preferably, the cobalt layer is deposited directly on (with "on" in the context of this document meaning in at least some direct physical contact therewith) the silicon-containing material to facilitate diffusion of the cobalt and/or silicon to form the silicide. Less preferred, a very thin native oxide might be received intermediate the cobalt and silicon which disperses during the cobalt silicide formation typically still resulting in adequate cobalt silicide formation. Regardless, the typical annealing is conducted by rapid thermal processing (RTP).

25

30

The temperature at which the anneal occurs impacts the degree of formation of one or both of CoSi and/or CoSi_2 . For example, an annealing temperature of from 500°C to 550°C forms substantially all CoSi , and a temperature in excess of 800°C forms substantially all CoSi_2 . Intervening temperatures tend to form a mixture of CoSi and CoSi_2 including other quantities of silicon with respect to cobalt. Further, such different

35

temperatures are largely determinative of which species, cobalt or silicon, is the predominately moving species. For example at the lower temperatures, cobalt diffusion/movement predominates such that the CoSi which forms tends to form mostly in the silicon region of the substrate, for example
5 elevationally lower in the substrate where a cobalt layer is formed elevationally over silicon. On the other hand at the higher temperatures, silicon diffusion/movement predominates such that the CoSi₂ which is formed tends to form mostly in the region of the cobalt layer, for example elevationally higher in the substrate where a cobalt layer is deposited over
10 silicon. Further, where higher temperature anneals are conducted to predominately form CoSi₂, the silicon migration can tend to form voids within the underlying silicon-containing substrate beneath where the CoSi₂ is formed.

In many instances, it would be desirable to form the CoSi₂ in the
15 region prior to the annealing which is predominately composed of silicon and also in a manner which prevents void formation. One prior art manner of achieving this is to initially anneal at a lower temperature which forms CoSi lower within the substrate where desired, while also typically leaving some of the cobalt layer unreacted. The cobalt is then stripped by a wet etch, and
20 the substrate subsequently subjected to a high temperature anneal which converts the CoSi to CoSi₂. This of course requires two separate annealing steps and stripping of unreacted cobalt prior to conducting the second annealing step. Further, it is highly desirable that unreacted cobalt be stripped from the substrate prior to any subsequent exposure of the
25 substrate to temperatures higher than 650°C. This is because cobalt tends to react with underlying oxide at temperatures greater than 650°C and the resultant cobalt oxide which is formed can be difficult to remove.

While the invention was motivated in addressing the above identified issues, it is in no way so limited. The invention is only limited by the
30 accompanying claims as literally worded, without interpretative or other limiting reference to the specification, and in accordance with the doctrine of equivalents.

SUMMARY

35 The invention included to methods of forming CoSi₂, methods of forming field effect transistors, and methods of forming conductive contacts.

In one implementation, a method of forming CoSi_2 includes forming a substantially amorphous layer comprising MSi over a silicon-containing substrate, where "M" comprises at least some metal other than cobalt, and preferably a refractory metal. A layer comprising cobalt is deposited over the substantially amorphous MSi_x -comprising layer. The substrate is annealed effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with silicon of the silicon-containing substrate to form CoSi_2 beneath the substantially amorphous MSi_x -comprising layer.

In one implementation, a method of forming a field effect transistor comprises forming a polysilicon-comprising gate proximate a channel region of a semiconductor substrate. A gate dielectric is received between the gate and the channel region. The channel region is received between a pair of silicon-containing source/drain regions. A substantially amorphous layer comprising MSi_x is deposited over the polysilicon and over the silicon-containing source/drain regions, where "M" comprises at least some metal, and preferably a refractory metal, other than cobalt. A layer comprising cobalt is deposited over the substantially amorphous MSi_x -comprising layer. The substrate is annealed effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with polysilicon of the gate and with silicon of the source/drain regions effective to form a first region comprising CoSi_2 beneath the substantially amorphous MSi_x -comprising layer on the polysilicon-comprising gate and to form respective second and third regions comprising CoSi_2 beneath the substantially amorphous MSi_x -comprising layer on the silicon-containing source/drain regions. The first, second, and third regions are spaced from one another.

In one implementation, a method of forming a conductive contact comprises forming insulative material over a silicon-containing node location of a semiconductor substrate. An opening is formed through the insulative material to the silicon-containing node location. A substantially amorphous layer comprising MSi_x is deposited over the insulative material to within the opening and over the silicon-containing node location, where "M" comprises at least some metal, and preferably a refractory metal, other than cobalt. A layer comprising cobalt is deposited over the substantially amorphous MSi_x -comprising layer. The substrate is annealed effective to diffuse cobalt of the

cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with silicon of the node location effective to form CoSi_2 beneath the substantially amorphous MSi_x -comprising layer at the node location.

5 Other aspects and implementations are contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

10 Fig. 1 is a diagrammatic sectional view of a substrate fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 1.

15 Fig. 3 is a view the Fig. 2 substrate fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view the Fig. 3 substrate fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a diagrammatic sectional view of a substrate fragment in process in accordance with an aspect of the invention.

20 Fig. 6 is a view the Fig. 5 substrate fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view the Fig. 6 substrate fragment at a processing step subsequent to that shown by Fig. 6.

25 Fig. 8 is a view the Fig. 7 substrate fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view the Fig. 8 substrate fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view the Fig. 9 substrate fragment at a processing step subsequent to that shown by Fig. 9.

30 Fig. 11 is a diagrammatic sectional view of a substrate fragment in process in accordance with an aspect of the invention.

Fig. 12 is a view the Fig. 11 substrate fragment at a processing step subsequent to that shown by Fig. 11.

35 Fig. 13 is a view the Fig. 12 substrate fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view the Fig. 13 substrate fragment at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view the Fig. 14 substrate fragment at a processing step subsequent to that shown by Fig. 14.

5 Fig. 16 is a view the Fig. 15 substrate fragment at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a view of an alternate embodiment substrate processing in accordance with aspects of the invention.

10 Fig. 18 is a view of an alternate embodiment substrate processing in accordance with aspects of the invention.

Fig. 19 is a diagrammatic view of a computer illustrating an exemplary application of the present invention.

Fig. 20 is a block diagram showing particular features of the motherboard of the Fig. 15 computer.

15 Fig. 21 is a high-level block diagram of an electronic system according to an exemplary aspect of the present invention.

Fig. 22 is a simplified block diagram of an exemplary electronic system according to an aspect of the present invention.

20 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

A method of forming CoSi_2 in accordance with aspects of the invention is initially described with reference to Figs. 1-4. Fig. 1 depicts a substrate indicated generally with reference numeral 10. Substrate 10 typically and preferably comprises a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Substrate 10 is depicted as comprising a silicon-containing substrate 12, for example bulk monocrystalline silicon. Of course, silicon-on-insulator substrates are also contemplated as well as any other substrate which is at least somewhere silicon-containing. A substantially amorphous layer 14 comprising MSi_x has been formed over silicon-containing substrate 12, where "M" comprises at least some metal other than cobalt. "M" might comprise a mixture of metals

25

30

35

other than cobalt, or might comprise a single metal other than cobalt, for example Ta or other metal, with "M" most preferably comprising a refractory metal. Further, substantially amorphous MSi_x -comprising layer 14 might comprise/include some cobalt, or alternately and preferably might be void of detectable cobalt in the substrate of Fig. 1. Regardless, in one preferred implementation "x" of MSi_x ranges from 0.1 to 4.

In the context of this document, "substantially amorphous" does not preclude some degree of crystallinity, yet requires that the layer which is "substantially amorphous" be at least 65 percent by volume of an amorphous phase. Preferably, substantially amorphous MSi_x -comprising layer 14 is at least 70 volume percent amorphous, more preferably at least 90 volume percent amorphous, and even more preferably at least 95 percent amorphous. Further preferably, substantially amorphous MSi_x -comprising layer 14 is void of any crystalline grain boundaries extending completely through the thickness of layer 14. One reason for preclusion of any such crystalline grain boundaries is to restrict silicon diffusion as described below. Fig. 1 further depicts a preferred embodiment wherein substantially amorphous MSi_x -comprising layer 14 is formed on silicon or silicon-containing substrate 12. An exemplary preferred thickness range for layer 14 is from 5 Angstroms to 1,000 Angstroms, more preferably from 15 Angstroms to 100 Angstroms, and even more preferably from 20 Angstroms to 40 Angstroms.

Referring to Fig. 2, a layer 16 comprising cobalt has been deposited over, and preferably on as shown, substantially amorphous MSi_x -comprising layer 14. An exemplary preferred thickness range for cobalt-comprising layer 16 is from 20 Angstroms to 1,000 Angstroms. Cobalt-comprising layer 16 preferably comprises elemental-form cobalt. However, alloy, metal compound, and other cobalt-including materials are contemplated. Preferably if other than elemental-form cobalt, layer 16 is predominately comprised of cobalt or excess of a stoichiometric amount of cobalt in a cobalt compound. To prevent top surface oxidation of material 16 (if desired), a thin Ti and/or TiN layer (i.e., 30 Angstroms to 100 Angstroms) can be deposited atop material 16 (not shown).

Referring to Fig. 3, substrate fragment 10 has been annealed effective to diffuse cobalt of cobalt-comprising layer 16 through substantially amorphous MSi_x -comprising layer 14 and combine such cobalt with silicon of

silicon-containing substrate 12 to form CoSi_2 20 beneath substantially amorphous MSi_x -comprising layer 14. Such might also form some CoSi_2 above or within layer 14, but at least some will also form beneath layer 14. Most preferably, such annealing is conducted at a temperature of no greater than 650°C and at a temperature of no less than 450°C . One exemplary specific preferred annealing temperature range is from 500°C to 600°C . Any suitable annealing is contemplated, with RTP being but one specific example, for example having a temperature ramp rate of at least 10°C per second up to one or more desired annealing temperatures. A specific preferred example includes a rapid thermal processing temperature ramp at from 25°C per second to 75°C per second to 550°C , and maintaining temperature at 550°C for from 20 seconds to 30 seconds. The atmosphere during such annealing is preferably inert, for example consisting essentially of N_2 and/or one or more noble gases. Pressure can be atmospheric, subatmospheric, or greater than atmospheric pressure. A reduction to practice pressure was 10 Torr.

In one preferred example, the annealing forms no more than 5 atomic percent CoSi , if any, of a total of all cobalt silicide formed by the annealing, and preferably no more than 1 atomic percent CoSi , if any. Further in one preferred embodiment, the CoSi_2 is in crystalline form and the silicon of the silicon-containing substrate from which such is formed is also in crystalline form. Typically and preferably in such instance, the CoSi_2 formed will be of the same crystalline structure as the silicon of the silicon-containing substrate.

Figs. 2 and 3 depict excess cobalt material 16 being fabricated such that all of layer 16 is not consumed in forming CoSi_2 20 of Fig. 3. The invention also, of course, contemplates deposition of a cobalt-comprising material 16 to a suitably thin thickness and/or conducting the annealing under conditions such that all of cobalt-comprising layer 16 is consumed and converted to cobalt silicide. Regardless, any remaining of cobalt-comprising material 16 and MSi_x -comprising layer 14 might be desired to remain as part of the integrated circuitry being fabricated, or alternately be removed. Accordingly in one aspect, the invention contemplates removing all remaining of any of cobalt-comprising layer 16 and/or all remaining of any of MSi_x -comprising layer 14 from the substrate after the annealing. For example, Fig. 4 depicts all remaining of layers 16 and 14 having been

removed from the substrate. For example, elemental cobalt can be stripped utilizing a wet mixture of HCl, H₂O₂ and H₂O, while TaSi_x can be removed utilizing a mixture of H₂SO₄, H₂O₂, and H₂O, or with a dry chlorine based etch chemistry.

5 Aspects of the invention as described above in a method of forming CoSi₂ might be utilized in fabrication of any such layer or materials to be formed as part of integrated circuitry, or even as a sacrificial material not necessarily constituting part of integrated circuitry being fabricated. Regardless, an exemplary method of forming a field effect transistor
10 comprising CoSi₂ fabricated in accordance with an aspect of the invention is next described with reference to Figs. 5-10.

Fig. 5 depicts a substrate fragment 22 comprising a semiconductor substrate 24. Substrate 24 preferably has any of the above-described attributes of substrate 12 of the first-described embodiment, with
15 monocrystalline silicon being but one preferred example. Substrate 24 is depicted as comprising a pair of silicon-containing source/drain regions 26 and 28 having a channel region 27 received there between. Such regions may or may not be suitably doped at this point in the process but nevertheless constitute regions within which a channel region (27) and
20 source/drain regions (26, 28) will ultimately at least be partially received. A gate construction 30 is provided relative to semiconductor substrate 24. Such comprises a conductive polysilicon-comprising gate 32 received operably proximate channel region 27, and has a gate dielectric 34 received between gate 32 and channel region 27. The depicted exemplary
25 embodiment is with respect to a conventional horizontal, planar oriented field effect transistor. However of course, the invention contemplates fabrication relative to any field effect transistor orientation, and whether existing or yet-to-be developed. For example and by way of example only, constructions are contemplated where the gate is received beneath or
30 laterally of the channel region, including vertical and other oriented transistors. Gate construction 30 in the depicted preferred embodiment is also shown as comprising anisotropically etched insulative sidewall spacers 36 which have been formed over sidewalls of polysilicon-comprising gate 32. Exemplary preferred materials include one or a combination of silicon
35 dioxide and silicon nitride.

Referring to Fig. 6, a substantially amorphous layer 38 comprising MSi_x has been deposited over polysilicon 32 and over silicon-containing source/drain regions 26 and 28 (and preferably on polysilicon 32 and on source/drain regions 26 and 28), where "M" comprises at least some metal other than cobalt. Attributes of layer 38 are otherwise preferably as described above with respect to substantially amorphous MSi_x -comprising layer 14 of the first-described embodiment.

Referring to Fig. 7, a layer 40 comprising cobalt is deposited over (and preferably on) substantially amorphous MSi_x -comprising layer 38. Preferred attributes of layer 40 are otherwise preferably as described above in connection with cobalt-comprising layer 16 of the first-described embodiment.

Referring to Fig. 8, substrate 22 has been annealed effective to diffuse cobalt of cobalt-comprising layer 40 through substantially amorphous MSi_x -comprising layer 38 and combine such cobalt with polysilicon of gate 32 effective to form a first region 42 comprising CoSi_2 beneath substantially amorphous MSi_x -comprising layer 38 on polysilicon-comprising gate 32. Such annealing has also been effective to diffuse cobalt of cobalt-comprising layer 40 through substantially amorphous MSi_x -comprising layer 38 and combine such cobalt with silicon of source/drain regions 26 and 28 to form respective second and third regions 44 and 46 comprising CoSi_2 beneath substantially amorphous MSi_x -comprising layer 38 on silicon-containing source/drain regions 26 and 28, and wherein first region 42, second region 44, and third region 46 are spaced from one another. Preferred attributes of the annealing are preferably as described above in the fabrication of CoSi_2 region 20 in the first-described embodiment.

As in the first-described embodiment, some or all of any remaining cobalt and MSi_x material might remain or be removed from the substrate. Fig. 9, by way of example only, depicts complete removal of any remaining of cobalt-comprising material 40 (not shown) and MSi_x -comprising material 38 (not shown) from the substrate. Alternately and by way of example only, processing might be conducted whereby not all remaining of the MSi_x -comprising material is removed, and perhaps at least or only that portion of MSi_x -comprising layer which is received between spaced first region 42, second region 44 and third region 46 from substrate 22 after the annealing.

As referred to above, the invention contemplates ultimate fabrication of operable source/drain regions before or after any of the above-described processing. Accordingly in one implementation, and by way of example only, the invention contemplates implanting a highest concentration doped portion of the source/drain regions prior to the annealing, and in another exemplary implementation after the annealing. For example, Fig. 10 depicts formation of highest concentration doped portions 48 of the respective source/drain regions occurring by implanting of the Fig. 9 substrate. The implant species could, of course, be of "p" and/or "n" type as known by people of skill in the art. Further, LDD, halo, etc. implants might also be additionally be provided at any point in the fabrication of a field effect transistor.

By way of example only, aspects of the invention also encompass or contemplate methods of forming conductive contacts, for example as described below in connection with embodiments as shown in Figs. 11-17. Fig. 11 depicts a substrate fragment 50 comprising a silicon-containing substrate 52 having some insulative material 54 formed thereover. Exemplary preferred attributes for substrate 52 are those as described above in connection with substrate/material 12 of the first-described embodiment. Insulative material 54 might comprise one or more different insulative materials, with one or a combination of silicon dioxide (whether doped or undoped) and silicon nitride being but two examples. An exemplary preferred thickness for material 54 is from 400 Angstroms to 30,000 Angstroms. Fig. 11 can be considered as constituting some silicon-containing node location 56 over (preferably on as shown) which material 54 has been formed.

Referring to Fig. 12, an opening 58 has been formed through insulative material 54 to silicon-containing node location 56. By way of example only, an exemplary process comprises photolithographic patterning and etch. By way of example only, an exemplary minimum width for opening 58 is from 50 Angstroms to 900×10^4 Angstroms.

Referring to Fig. 13, a substantially amorphous layer 60 comprising MSi_x has been deposited over insulative material 54 to within opening 58 and over (preferably on) silicon-containing node location 56, where "M" comprises at least some metal other than cobalt. Preferred attributes for substantially amorphous MSi_x -comprising layer 60 are otherwise as

described above in connection with substantially amorphous MSi_x -comprising layer 14 of the first-described embodiment.

Referring to Fig. 14, a layer 62 comprising cobalt has been deposited over (preferably on) substantially amorphous MSi_x -comprising layer 60 within opening 58 as shown. Cobalt-comprising layer 62 might partially or completely fill remaining portions of opening 58, with less than complete filling being depicted in Fig. 14. Preferred attributes for cobalt-comprising layer 62 are preferably otherwise as described above with respect to cobalt-comprising layer 16 in the first-described embodiment.

Referring to Fig. 15, substrate 50 has been annealed effective to diffuse cobalt of cobalt-comprising layer 62 through substantially amorphous MSi_x -comprising layer 60 and combine such cobalt with silicon of node location 56 effective to form CoSi_2 64 beneath substantially amorphous MSi_x -comprising layer 60 at node location 56. Processing with respect to the annealing is preferably as described above in connection with fabrication of CoSi_2 -comprising region 20 in the first-described embodiment.

Fig. 16 depicts exemplary subsequent processing whereby a conductive contact 65 within opening 58 has been fabricated to node location 56. An exemplary manner of forming the same is by deposition of another conductive material 66 (i.e., any of one or more elemental metals, one or more alloys, one or more conductive compounds, and/or one or more conductively doped semiconductive materials) followed by a subsequent polishing (i.e., chemical mechanical polishing) or other removal of materials 60, 62 and 66 which were received elevationally outward of insulative material 54. Alternately of course, and by way of examples only, damascene-like processing is contemplated, or an exemplary subtractive patterning and etch of materials 60, 62 and 66 such that a conductive line is fabricated as part of the conductive contact elevationally outward of insulative material 54.

The invention also, of course, contemplates removal of some or all of materials 60 and 62 after the annealing, for example as depicted in Fig. 17 in connection with a substrate fragment 50a. Like numerals from the Figs. 11-16 embodiment have been utilized where appropriate, with differences being indicated with the suffix "a". Fig. 17 depicts materials 60 and 62 (not shown) as having been removed, and conductive material(s) 66a

formed within contact opening 58. An exemplary conductive material 66a includes a tungsten plug lined with TiN.

In fabricating an integrated circuit, such might comprise any circuit, or sub-circuit. Further by way of example only, such might comprise memory circuitry, for example DRAM circuitry. For example, Fig. 18 depicts the field effect transistor of Fig. 10 incorporated into a DRAM memory cell. Specifically, CoSi_2 region 44 is electrically connected to a storage device 150, and CoSi_2 region 46 is electrically connected to a bitline 152. Storage device 150 can comprise any suitable device, including a capacitor, for example. Bitline 152 can comprise any suitable construction. The field effect transistor can be considered to be part of an integrated circuit, for example the DRAM integrated circuitry just described.

Fig. 19 illustrates generally, by way of example, but not by way of limitation, an embodiment of a computer system 400 according to an aspect of the present invention. Computer system 400 includes a monitor 401 or other communication output device, a keyboard 402 or other communication input device, and a motherboard 404. Motherboard 404 can carry a microprocessor 406 or other data processing unit, and at least one memory device 408. Memory device 408 can comprise various aspects of the invention described above, including, for example, one or more of the wordlines, bitlines and DRAM unit cells. Memory device 408 can comprise an array of memory cells, and such array can be coupled with addressing circuitry for accessing individual memory cells in the array. Further, the memory cell array can be coupled to a read circuit for reading data from the memory cells. The addressing and read circuitry can be utilized for conveying information between memory device 408 and processor 406. Such is illustrated in the block diagram of the motherboard 404 shown in Fig. 20. In such block diagram, the addressing circuitry is illustrated as 410 and the read circuitry is illustrated as 412.

In particular aspects of the invention, memory device 408 can correspond to a memory module. For example, single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) may be used in the implementation which utilizes the teachings of the present invention. The memory device can be incorporated into any of a variety of designs which provide different methods of reading from and writing to memory cells of the device. One such method is the page mode operation. Page mode

operations in a DRAM are defined by the method of accessing a row of a memory cell arrays and randomly accessing different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed.

5 An alternate type of device is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on a
10 memory bus. Other alternative types of devices, by way of example only, include SDRAM, DDR SDRAM, SLDRAM, VRAM and Direct RDRAM, as well as others such as SRAM or Flash memories.

Fig. 21 illustrates a simplified block diagram of a high-level organization of various embodiments of an exemplary electronic system 700
15 of the present invention. System 700 can correspond to, for example, a computer system, a process control system, or any other system that employs a processor and associated memory. Electronic system 700 has functional elements, including a processor or arithmetic/logic unit (ALU) 702, a control unit 704, a memory device unit 706 and an input/output (I/O)
20 device 708. Generally, electronic system 700 will have a native set of instructions that specify operations to be performed on data by processor 702 and other interactions between processor 702, memory device unit 706 and I/O devices 708. Control unit 704 coordinates all operations of processor 702, memory device 706 and I/O devices 708 by
25 continuously cycling through a set of operations that cause instructions to be fetched from memory device 706 and executed. In various embodiments, memory device 706 includes, but is not limited to, random access memory (RAM) devices, read-only memory (ROM) devices, and peripheral devices such as a floppy disk drive and a compact disk CD-ROM drive. One of
30 ordinary skill in the art will understand, upon reading and comprehending this disclosure, that any of the illustrated electrical components are capable of being fabricated to include DRAM cells, wordlines and bitlines in accordance with various aspects of the present invention.

Fig. 22 is a simplified block diagram of a high-level organization of
35 various embodiments of an exemplary electronic system 800. The system 800 includes a memory device 802 that has an array of memory

cells 804, address decoder 806, row access circuitry 808, column access circuitry 810, read/write control circuitry 812 for controlling operations, and input/output circuitry 814. Memory device 802 further includes power circuitry 816, and sensors 820, such as current sensors for determining
5 whether a memory cell is in a low-threshold conducting state or in a high-threshold non-conducting state. The illustrated power circuitry 816 includes power supply circuitry 880, circuitry 882 for providing a reference voltage, circuitry 884 for providing the first wordline with pulses, circuitry 886 for providing the second wordline with pulses, and circuitry 888 for providing the
10 bitline with pulses. System 800 also includes a processor 822, or memory controller for memory accessing.

Memory device 802 receives control signals 824 from processor 822 over wiring or metallization lines. Memory device 802 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the
15 art that additional circuitry and control signals can be provided, and that memory device 802 has been simplified to help focus on the invention. At least one of processor 822 or memory device 802 can include a DRAM cell of the type described previously in this disclosure.

The various illustrated systems of this disclosure are intended to
20 provide a general understanding of various applications for the circuitry and structures of the present invention, and are not intended to serve as a complete description of all the elements and features of an electronic system using memory cells in accordance with aspects of the present invention. One of ordinary skill in the art will understand that the various
25 electronic systems can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device(s).

Applications for memory cells, wordlines and bitlines can include electronic systems for use in memory modules, device drivers, power
30 modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

CLAIMS

What is claimed is:

1. A method of forming CoSi_2 , comprising:
 - 5 forming a substantially amorphous layer comprising MSi_x over a silicon-containing substrate, where "M" comprises at least some metal other than cobalt; depositing a layer comprising cobalt over the substantially amorphous MSi_x -comprising layer; and
 - 10 annealing the substrate effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with silicon of the silicon-containing substrate to form CoSi_2 beneath the substantially amorphous MSi_x -comprising layer.
2. The method of claim 0 wherein the substantially amorphous
15 MSi_x -comprising layer is formed on silicon of the silicon-containing substrate.
3. The method of claim 1 wherein the substantially amorphous
20 MSi_x -comprising layer has a thickness of from 5 Angstroms to 1000 Angstroms.
4. The method of claim 3 wherein the substantially amorphous
25 MSi_x -comprising layer has a thickness of from 15 Angstroms to 100 Angstroms.
5. The method of claim 4 wherein the substantially amorphous
30 MSi_x -comprising layer has a thickness of from 20 Angstroms to 40 Angstroms.
6. The method of claim 1 wherein "M" comprises a refractory metal other than cobalt prior to the depositing.
7. The method of claim 6 wherein "M" comprises a mixture of refractory metals other than cobalt prior to the depositing.

8. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer comprises cobalt prior to the depositing.

9. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is void of detectable cobalt prior to the depositing.

10. The method of claim 1 wherein "M" comprises Ta.

11. The method of claim 1 wherein "x" ranges from 0.1 to 4.

12. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is at least 70% amorphous.

13. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is at least 90% amorphous.

14. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is at least 95% amorphous.

15. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is void of any crystalline grain boundaries extending completely through its thickness.

16. The method of claim 1 wherein the cobalt-comprising layer is deposited on the substantially amorphous MSi_x-comprising layer.

17. The method of claim 1 wherein the substantially amorphous MSi_x-comprising layer is formed on silicon of the silicon-containing substrate, and the cobalt-comprising layer is deposited on the substantially amorphous MSi_x-comprising layer.

18. The method of claim 17 wherein the substantially amorphous MSi_x-comprising layer has a thickness of from 15 Angstroms to 100 Angstroms.

19. The method of claim 1 wherein the cobalt-comprising layer comprises elemental-form cobalt.

20. The method of claim 1 comprising removing all remaining of the
5 MSi_x -comprising layer from the substrate after the annealing.

21. The method of claim 1 wherein the annealing is conducted at a temperature of no greater than 650°C.

10 22. The method of claim 21 wherein the annealing is conducted at a temperature of no less than 450°C.

23. The method of claim 1 wherein the annealing is conducted at a temperature of from 500°C to 600°C.

15

24. The method of claim 1 wherein the annealing comprises rapid thermal processing.

25. The method of claim 1 wherein the annealing forms no more
20 than five atomic percent CoSi, if any, of a total of all cobalt silicide formed by said annealing.

26. The method of claim 25 wherein the annealing forms no more than one atomic percent CoSi, if any, of a total of all cobalt silicide formed
25 by said annealing.

27. The method of claim 1 wherein the CoSi_2 is crystalline and the silicon of the silicon-containing substrate is crystalline, the CoSi_2 being of the same crystalline structure as the silicon of the silicon-containing
30 substrate.

28. A method of forming a field effect transistor, comprising:
forming a polysilicon-comprising gate proximate a channel region of a semiconductor substrate, a gate dielectric being received between the gate
35 and the channel region, the channel region being received between a pair of silicon-containing source/drain regions;

depositing a substantially amorphous layer comprising MSi_x over the polysilicon and over the silicon-containing source/drain regions, where "M" comprises at least some metal other than cobalt;

depositing a layer comprising cobalt over the substantially amorphous MSi_x -comprising layer; and

annealing the substrate effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x -comprising layer and combine with polysilicon of the gate and with silicon of the source/drain regions effective to form a first region comprising $CoSi_2$ beneath the substantially amorphous MSi_x -comprising layer on the polysilicon-comprising gate and to form respective second and third regions comprising $CoSi_2$ beneath the substantially amorphous MSi_x -comprising layer on the silicon-containing source/drain regions; the first, second, and third regions being spaced from one another.

15

29. The method of claim 28 comprising forming anisotropically etched insulative spacers over sidewalls of the polysilicon-comprising gate, the substantially amorphous MSi_x -comprising layer being deposited over such spacers.

20

30. The method of claim 28 comprising removing that portion of the MSi_x -comprising layer received between the spaced first, second, and third regions from the substrate after the annealing.

25

31. The method of claim 28 comprising removing all remaining of the MSi_x -comprising layer from the substrate after the annealing.

32. A method of forming a conductive contact, comprising:

forming insulative material over a silicon-containing node location of a semiconductor substrate;

forming an opening through the insulative material to the silicon-containing node location;

depositing a substantially amorphous layer comprising MSi_x over the insulative material to within the opening and over the silicon-containing node location, where "M" comprises at least some metal other than cobalt;

depositing a layer comprising cobalt over the substantially amorphous MSi_x-comprising layer; and

annealing the substrate effective to diffuse cobalt of the cobalt-comprising layer through the substantially amorphous MSi_x-comprising layer
5 and combine with silicon of the node location effective to form CoSi₂ beneath the substantially amorphous MSi_x-comprising layer at the node location.

33. The method of claim 32 wherein the cobalt-comprising layer is
10 deposited to within the opening.

1/11

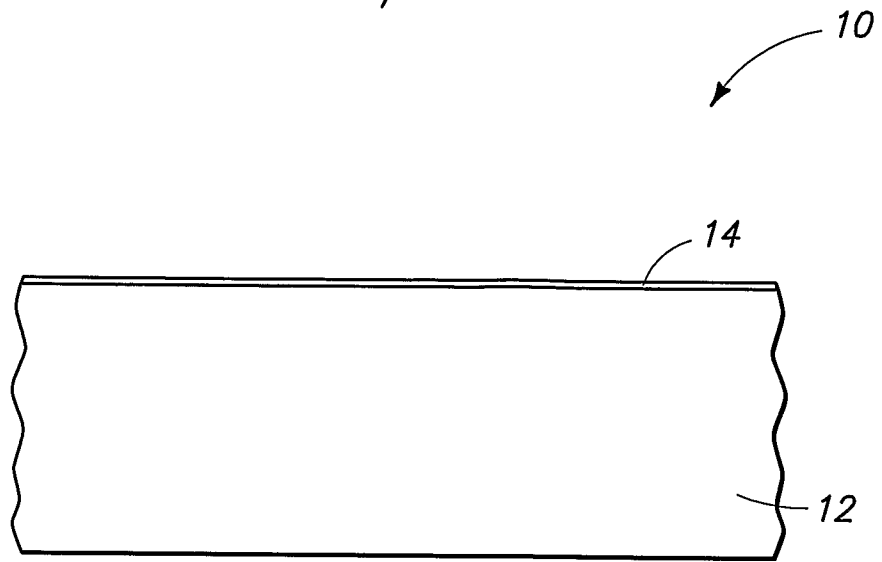


FIG. 1

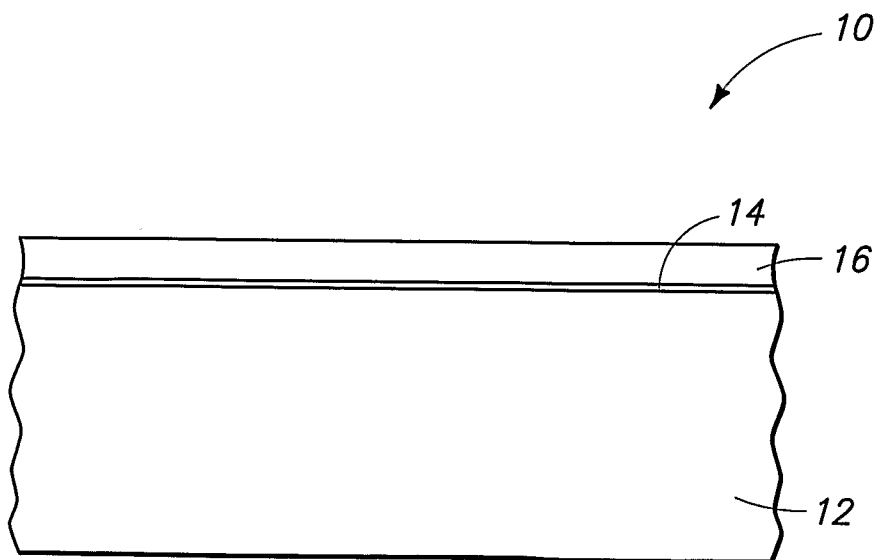


FIG. 2

2/11

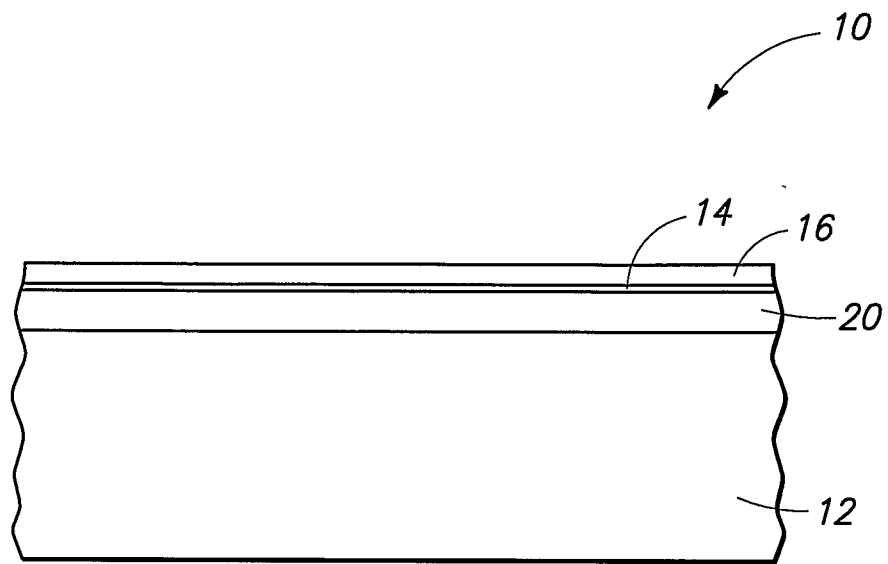


FIG. 2

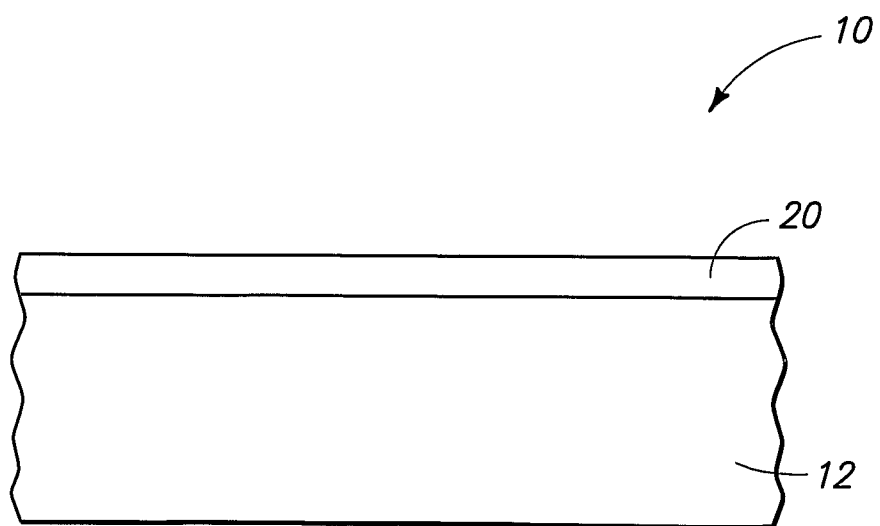
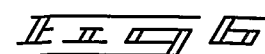
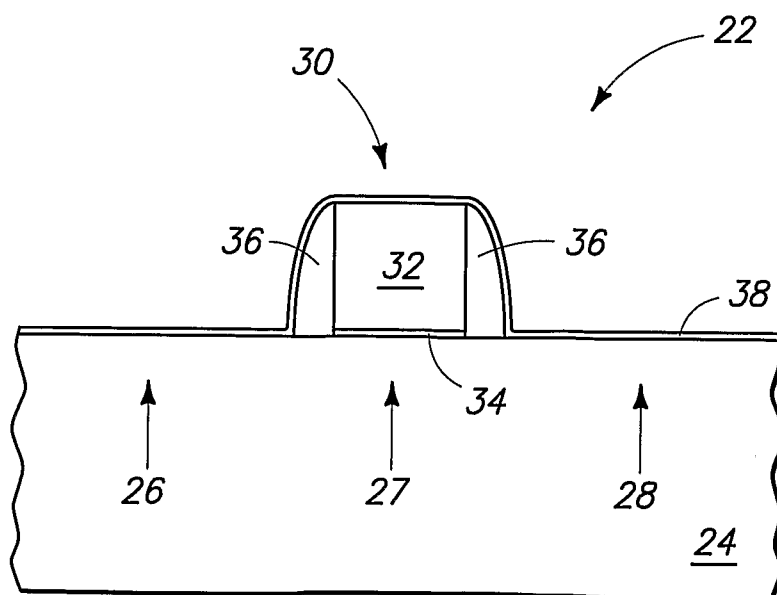
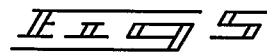
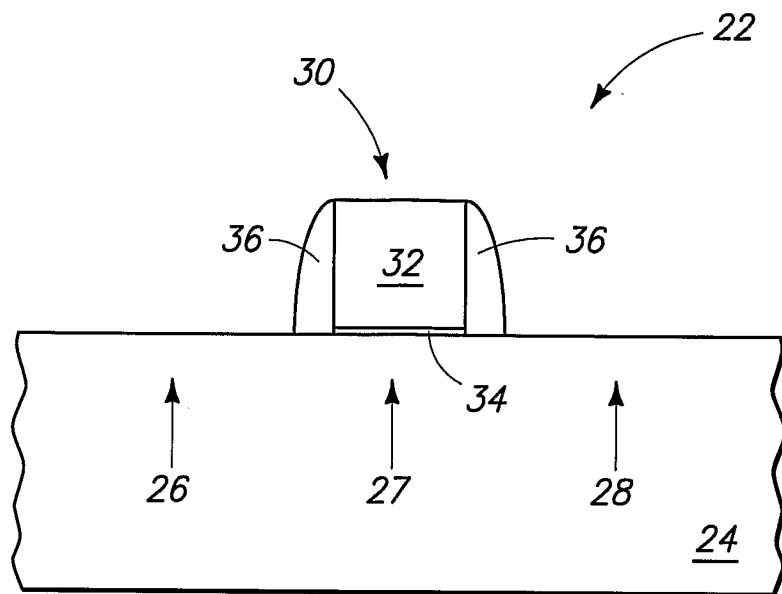
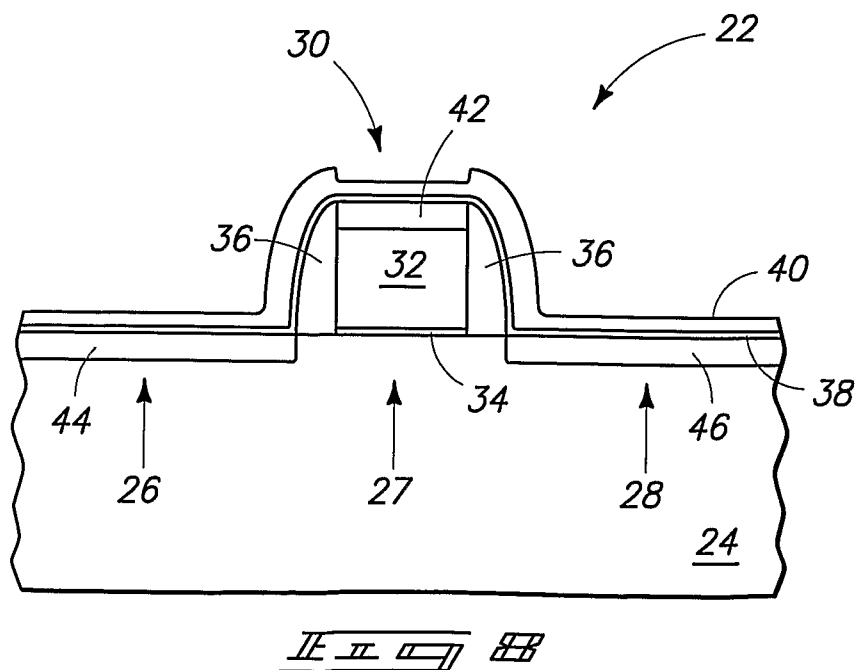
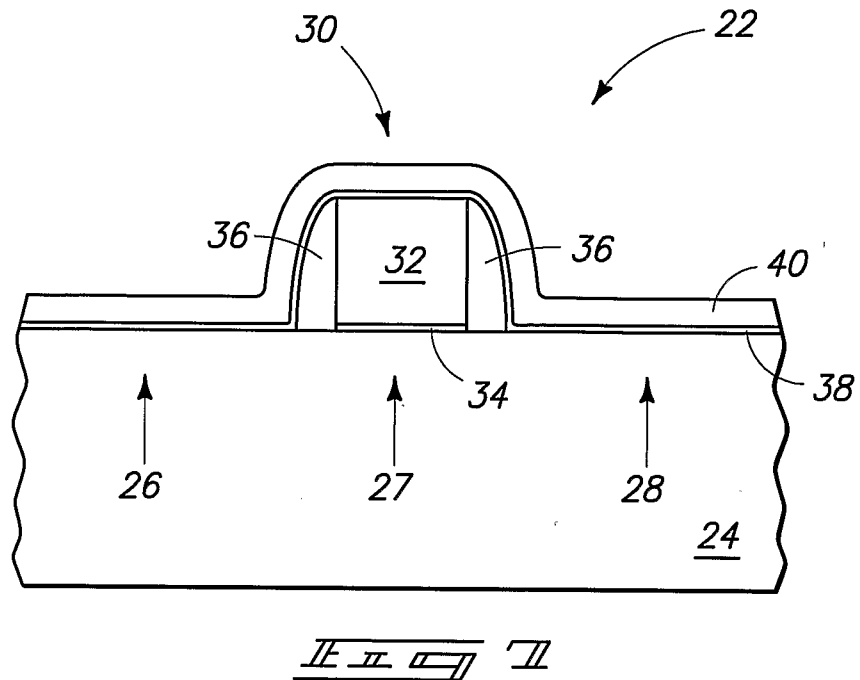


FIG. 3

3/11



4/11



5/11

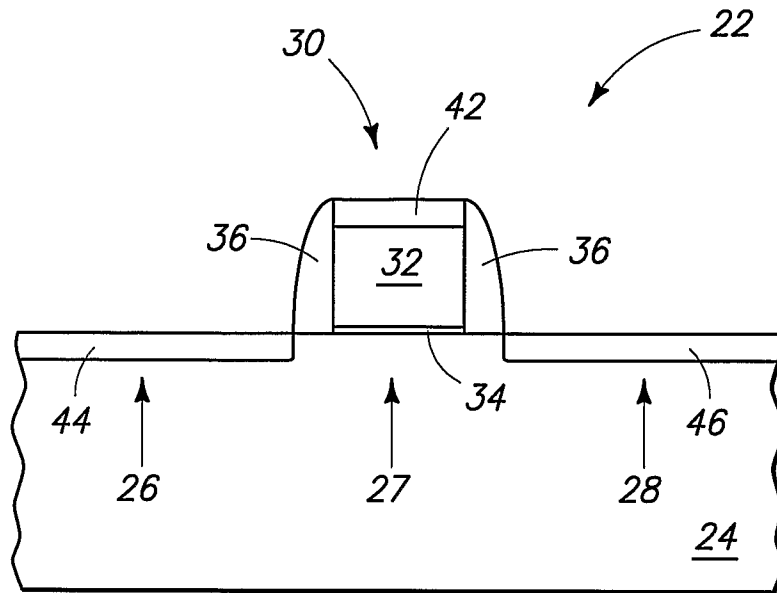


FIG. 5

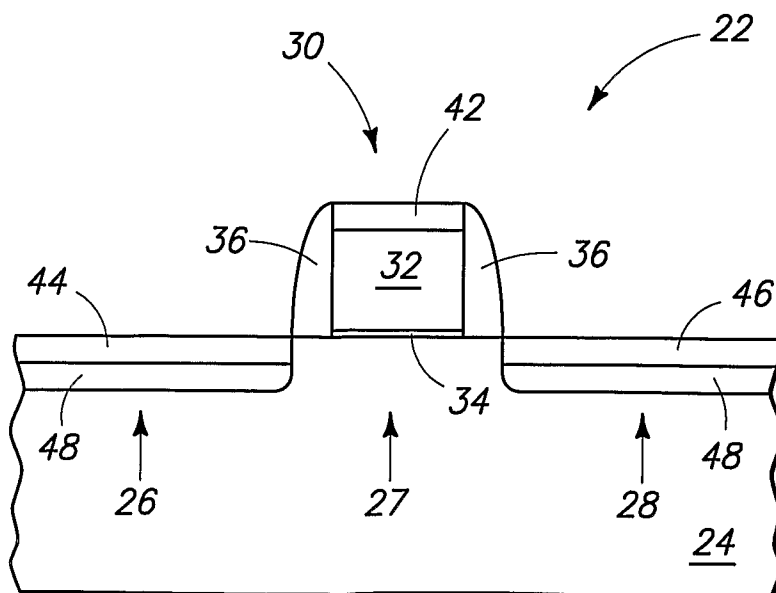
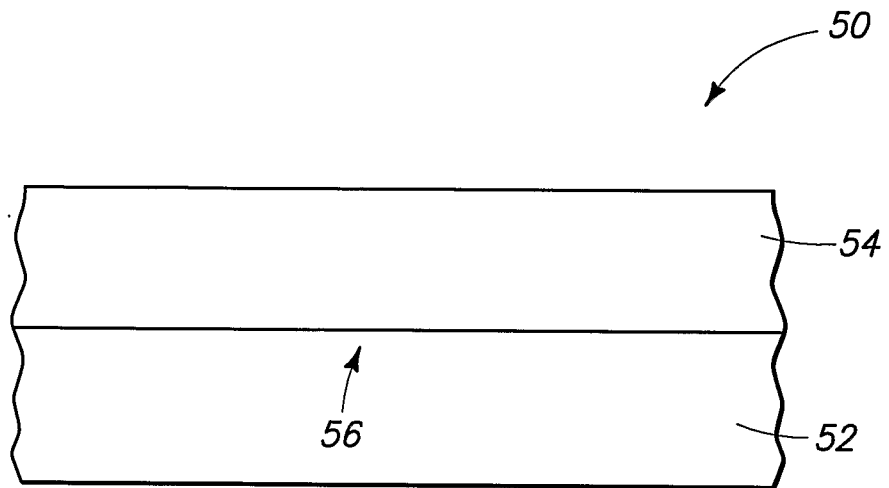
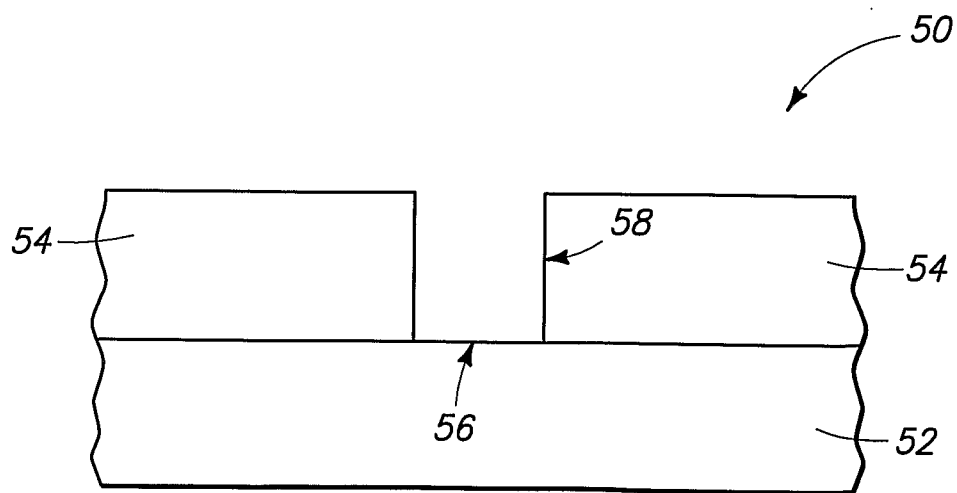


FIG. 6

6/11

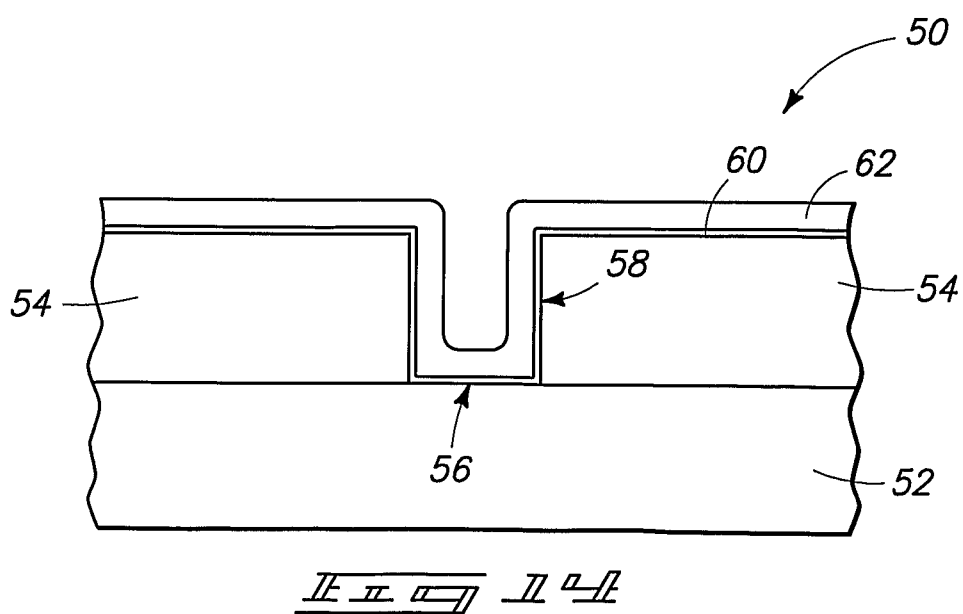
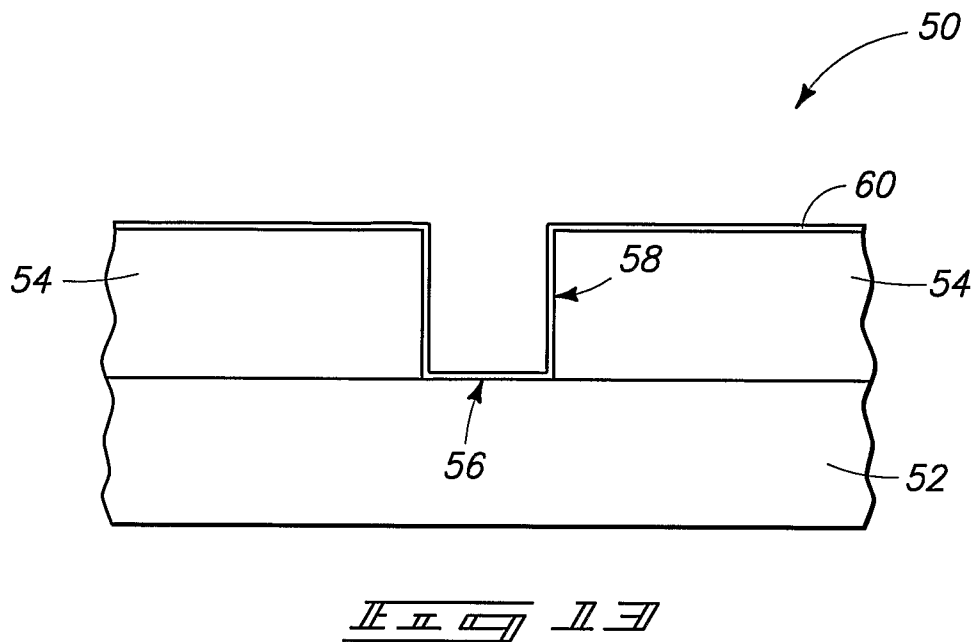


II II II II

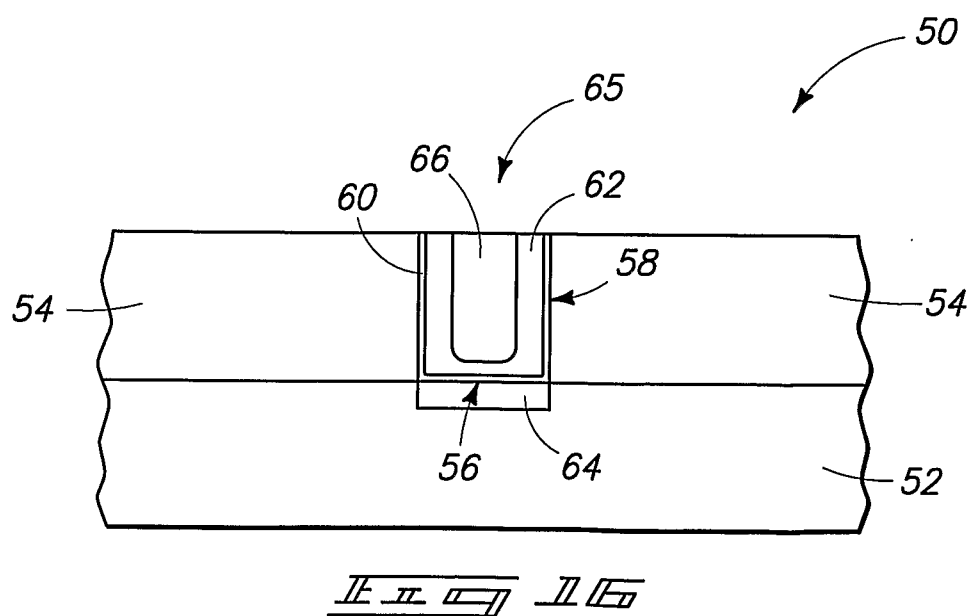
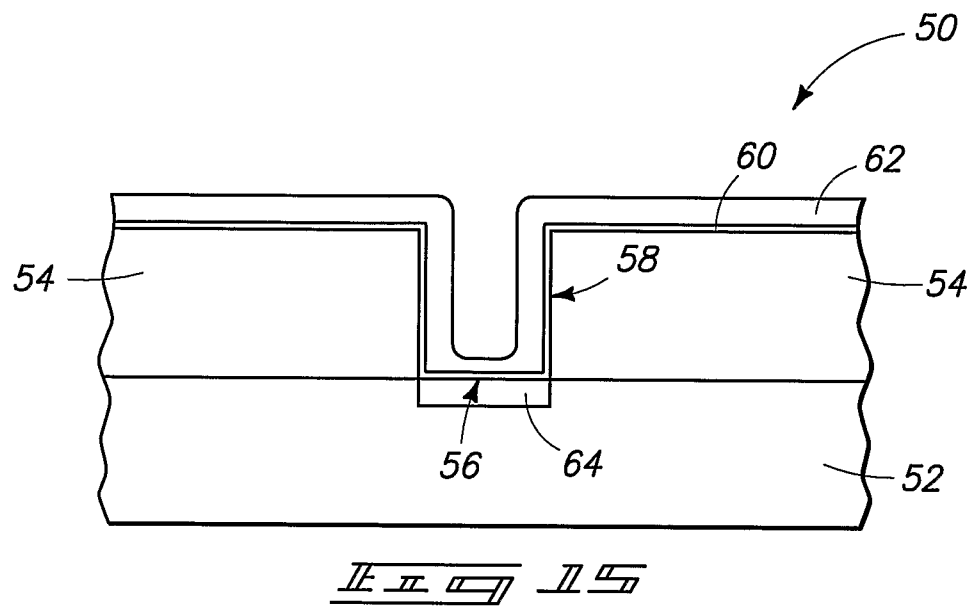


II II II II

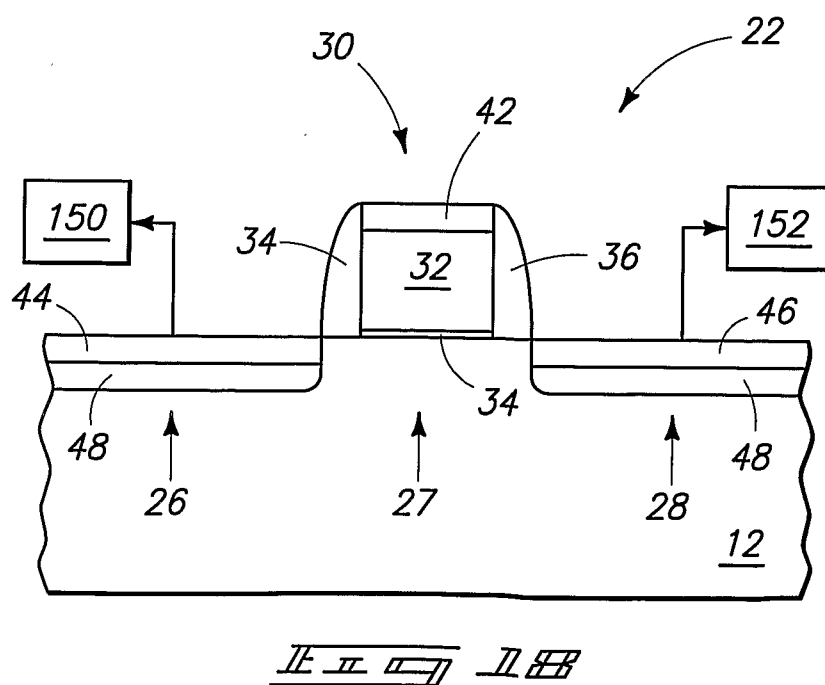
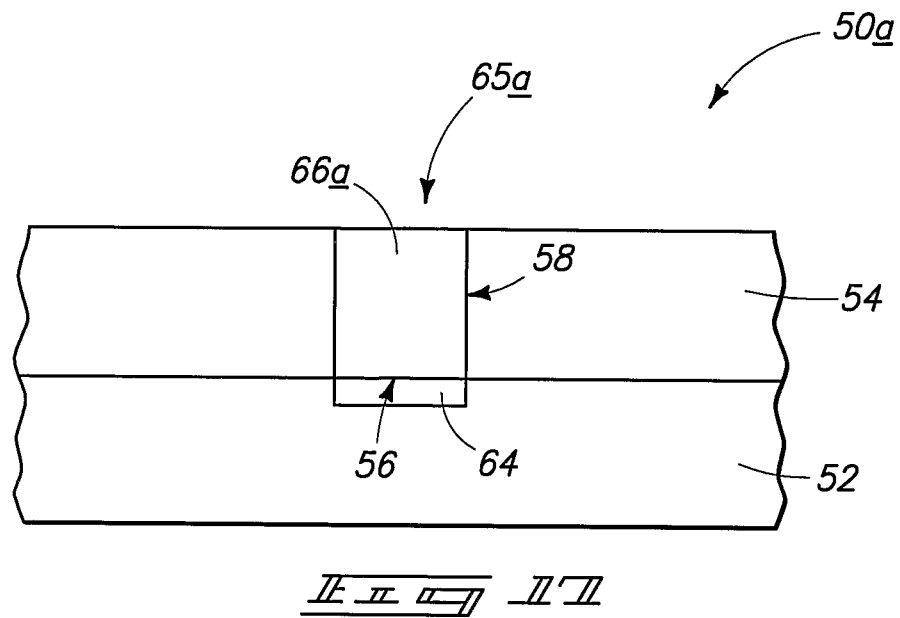
7/11



8/11



9/11



10/11

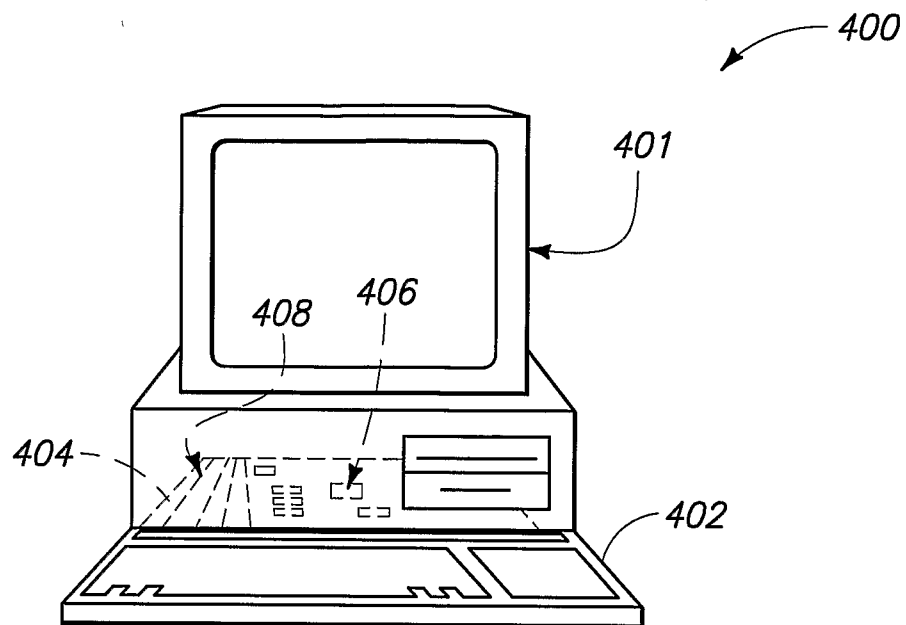


FIG. 11

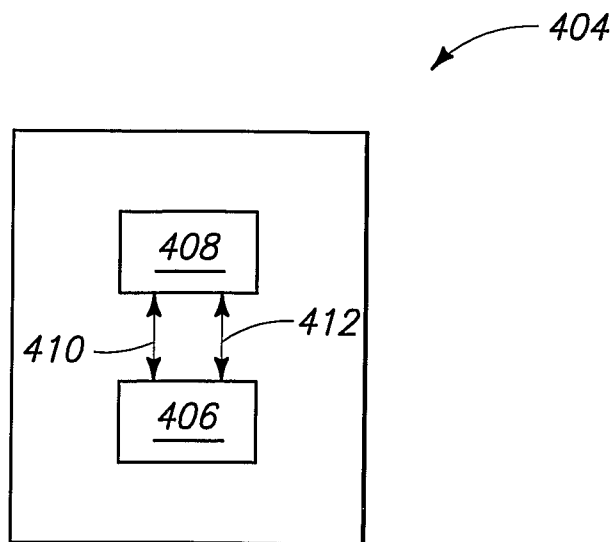


FIG. 12

11/11

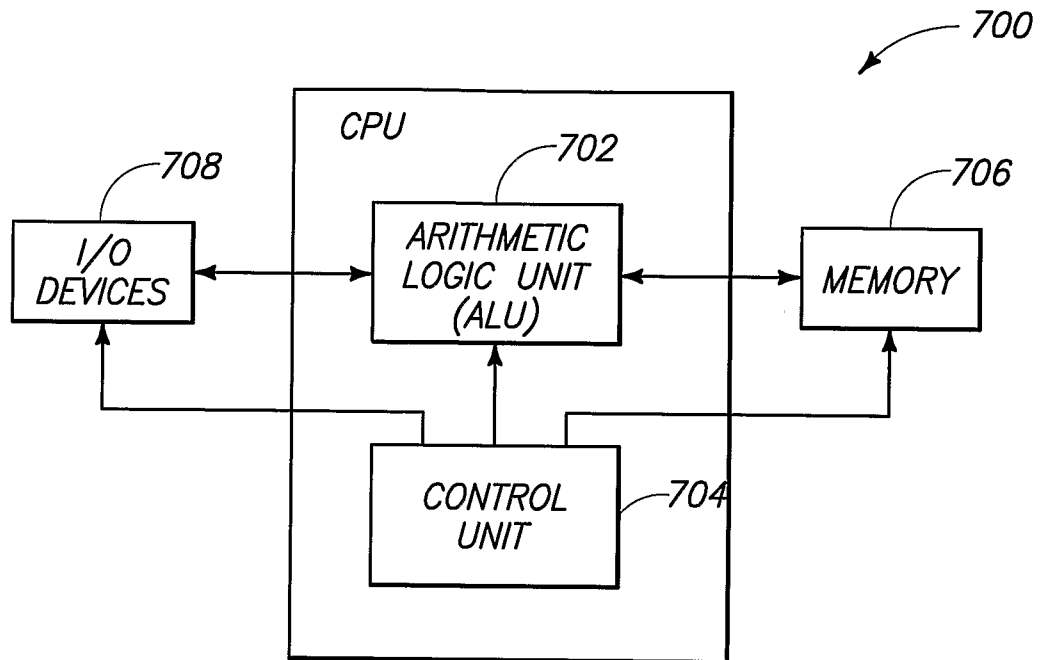


FIG. 11

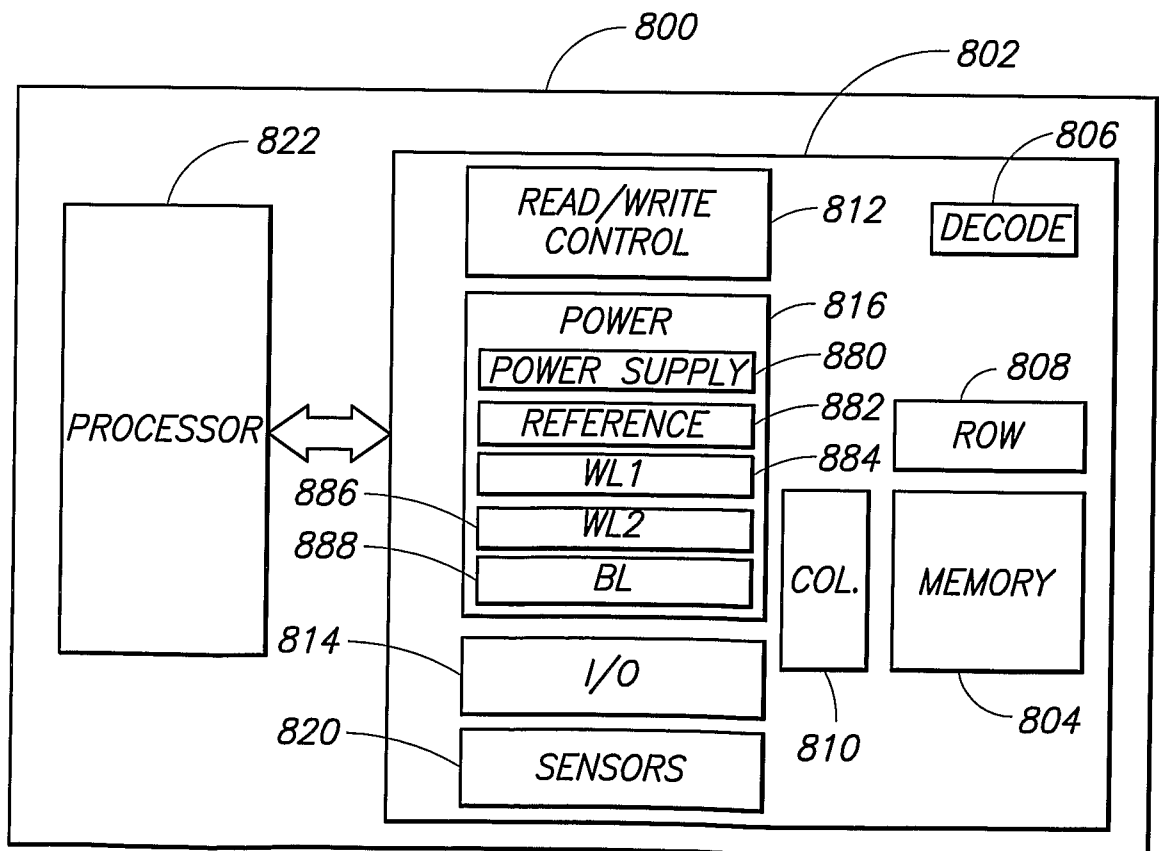


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/027367

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/283 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JEONG ET AL.: "Epitaxial Cobalt Silicide Formation Using a Co/TiSix Bilayer on Si (100) by Sputtering" SURFACE AND COATINGS TECHNOLOGY, vol. 171, 1 July 2003 (2003-07-01), pages 6-10, XP002405075	1,2,6,9, 16,17, 19,21, 22,24,27
Y	the whole document	28-33
Y	US 5 851 921 A (GARDNER MARK I [US] ET AL) 22 December 1998 (1998-12-22) column 5, line 37 - column 6, line 5; figures 1,2	28-31
Y	EP 0 905 752 A2 (LG SEMICON CO LTD [KR]) 31 March 1999 (1999-03-31) the whole document	32,33
	----- -/-- -----	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

31 October 2006

Date of mailing of the international search report

28/11/2006

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Ploner, Guido

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/027367

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 356 837 A (GEISS PETER J [US] ET AL) 18 October 1994 (1994-10-18) column 4, line 4 - column 5, line 59; figures 1,2	1-7,9, 16-19, 24,27
X	HONG F ET AL: "MECHANISMS OF EPITAXIAL COSI2 FORMATION IN THE MULTILAYER CO/TI-SI(100) SYSTEM" APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 64, no. 17, 25 April 1994 (1994-04-25), pages 2241-2243, XP000441267 ISSN: 0003-6951 page 2241, column 1	1-4,6,9, 15-19,27
A	DETAVERNIER C ET AL: "CoSi2 formation in the presence of Ti, Ta or W" PREPARATION AND CHARACTERIZATION, ELSEVIER SEQUOIA, NL, vol. 468, no. 1-2, 1 December 2004 (2004-12-01), pages 174-182, XP004579170 ISSN: 0040-6090 the whole document	1-33
A	QU XIN-PING ET AL: "Epitaxial growth of CoSi2 film by Co/a-Si/Ti/Si(100) multilayer solid state reaction" JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS, NEW YORK, US, vol. 89, no. 5, 1 March 2001 (2001-03-01), pages 2641-2648, XP012053022 ISSN: 0021-8979 the whole document	1-33
A	AKHAVAN ET AL.: "Single-Crystalline Growth of CoSi2 by Refractory-Interlayer-Mediated Epitaxy" APPLIED SURFACE SCIENCE, vol. 233, 30 June 2004 (2004-06-30), pages 123-128, XP002405076 the whole document	1-33
A	SUH Y-S ET AL: "Investigation of stress behaviors and mechanism of void formation in sputtered TiSix films" PREPARATION AND CHARACTERIZATION, ELSEVIER SEQUOIA, NL, vol. 450, no. 2, 1 March 2004 (2004-03-01), pages 341-345, XP004492154 ISSN: 0040-6090 the whole document	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2006/027367

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5851921	A	22-12-1998	NONE	
EP 0905752	A2	31-03-1999	CN 1213168 A	07-04-1999
US 5356837	A	18-10-1994	DE 69415476 D1	04-02-1999
			DE 69415476 T2	15-07-1999
			EP 0651077 A1	03-05-1995
			JP 2673104 B2	05-11-1997
			JP 7183253 A	21-07-1995