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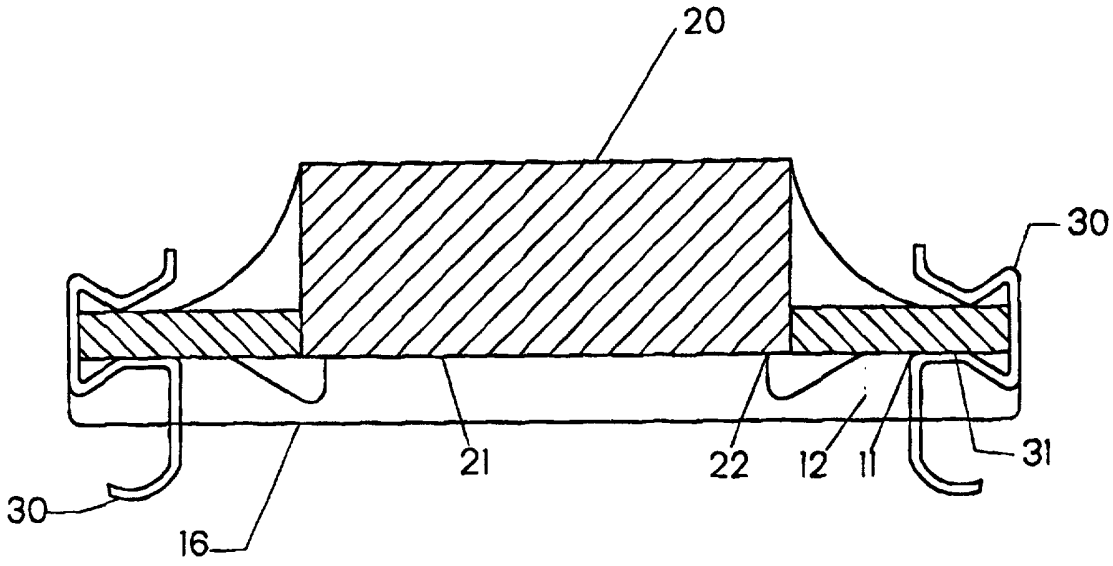

(57) Abstract

A semiconductor device package and method includes a thick, integrated circuit chip stack having a substantially planar bottom surface with a plurality of terminals. A carrier substrate is provided, also having a substantially planar surface, and being adapted to mount the chip stack. The substrate has a plurality of terminals and may preferably be made of a metallized ceramic. The terminals of the chip stack are adapted to be connected to the terminals of the substrate. Means are provided for mounting the chip stack on the substrate, as well as means for making electrical connections between the terminals of the chip stack and the terminals of the substrate. Finally, encapsulating means are used for supporting and maintaining the chip stack mounted on the carrier substrate. J leads connect the substrate to a circuit card.

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STACKED SEMICONDUCTOR DEVICE PACKAGE

TECHNICAL FIELD

The present invention relates to a semiconductor device package and method. More particularly, the present invention relates to a semiconductor device package and a method for making interconnections between a multi-layer "Chip Stack" to a printed circuit-board in a ceramic package.

Integrated circuits as fabricated on chips come in several different formats. These chips can be arranged in a "chip stack" and must be interconnected to a printed circuit card. Such stack can be much thicker than the common integrated circuit chip and comes in different heights.

BACKGROUND OF THE INVENTION

Various methods exist for packaging integrated circuit chips and mounting them on a printed circuit board. With a wire-bonding technique, the integrated circuit chip may be encapsulated, that is, as a molded plastic package or completely enclosed as a ceramic package. The chip is provided with wire-bonding pads onto which fine wires are bonded, which, in turn, have their opposite ends bonded to inner lead bond (ILB) pads contained in the package to be encapsulated. Thereafter, the chip and an end of each ILB are encapsulated in molding compound or enclosed in ceramic, with the outer lead (OL) exposed for further connections.

The integrated circuit chip's package very often has leads which are formed downwardly so that they may be soldered to the printed circuit board. In some cases, the integrated circuit chip's package plugs into a socket that makes the electrical connections on the printed circuit board.

Three-dimensional packaging techniques have been developed to increase such items as computer memory density. This can be done by stacking layers of ceramic containing multiple memory chips and stacked memory packages, such as in high-end computer memory subsystems. Such packaging methods have been carried out by mounting chips at an angle to a memory or a processor board in individual packages, or on a memory module known as a single-in-line memory module (SIMM). A dual-in-line package (DIP) is an example of such a memory package. The purpose is to put more memory into less volume. For a discussion of a three-dimensional memory cube system, see, "Evaluation of a Three-Dimensional Memory Cube System" in *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Volume 16, No. 8, December 1993, pp. 1006-1011, Claude L. Bertin, David J. Perlman, and Stuart N. Shanken.

This article indicates how a thin film metal layer is added to each chip surface to transfer signal and power input and output from the chip bond pads to the chip edges. The chips may be stacked and a right-angle joint is formed between the end of a transfer tab for transferring signals in and out of

each chip. Thus, it is possible to use electrical probing or to provide further interconnections on the face of the cube of the chip stack.

Accordingly, many problems exist when attempting to achieve a high density in a relatively small space. Various boundary conditions are presented when confronted with the problem of interconnecting different chip-stack heights to the printed circuit board. Such conditions include:

(1) minimum printed circuit card footprint;

(2) low cost for the package and the card attachment;

(3) there must be an opportunity for the provision of heat removal;

(4) the reliability of the devices on the silicon integrated circuit chip must be maintained;

(5) the chip stack must be protected during the bonding and assembling, the testing, and the use in the final assembly;

(6) if possible, a standard card footprint developed by the Joint Electronic Devices Engineering Council (JEDEC) should be used;

(7) the signal lines, power lines, and/or ground lines should be interconnected on the package's substrate, wherever possible; and

(8) compatibility should be maintained, when possible, with the appropriate test and burn-in equipment.

SUMMARY OF THE INVENTION

In order to solve the high-density stacking problem, and meet as many of the established boundary conditions as possible, the present invention provides a semiconductor device package which includes a thick, integrated circuit chip stack having a substantially planar bottom surface and a plurality of terminals. A metallized ceramic (MC) carrier substrate is provided, having a substantially planar surface adapted to mount the chip stack and having a plurality of terminals adapted to be electrically connected to the terminals of the chip stack. Means are provided for mounting the chip stack to the substrate. Means are further provided for making electrical connections between the terminals of the chip stack and the terminals of the substrate. Finally, when desired, encapsulating means for supporting and maintaining the chip stack mounted to the carrier substrate must be provided.

In a preferred embodiment of the present invention, the semiconductor package includes a chip stack with a bottom surface having a preselected physical configuration. The carrier substrate has a cutout portion corresponding substantially to the physical configuration of the chip stack's bottom surface. In this way, the chip stack may be mounted in the cutout portion in a substantially coplanar arrangement, with the bottom surface of the chip stack being coplanar with the bottom surface of the substrate.

In a further embodiment of the present invention, solder-laden J lead clips can be coupled to the substrate to permit further electrical connection to the printed circuit board (PCB).

In further embodiments, other types of connections may be used such as pin-in-hole (PIH), card edge Zero Insertion Force (ZIF), gull wing and lead frame.

In yet another preferred embodiment of the present invention, the carrier is a metallized ceramic substrate, and the electrically connecting means include solder pads on the substrate for connection to the terminals on the chip stack.

In a method incorporating the principles of the present invention, the semiconductor package is assembled utilizing the steps of forming a thick integrated circuit chip stack having a substantially planar bottom surface with a plurality of terminals, mounting the chip stack on a carrier substrate having a substantially planar surface and having a plurality of terminals adapted to be electrically connected to the terminals of the chip stack, making electrical connections between the terminals of the chip stack and the terminals of the substrate, and encapsulating the chip stack and the carrier substrate to support and maintain the chip stack mounted on the carrier substrate, and to provide protection from the environment.

In a preferred method, the carrier substrate has a cutout portion and during the step of mounting the chip stack on the carrier substrate, the

bottom surface of the chip stack protrudes through the cutout portion of the carrier substrate.

In a further preferred method, the carrier substrate is a metallized ceramic substrate. Solder is deposited on the substrate, whereby the mounting of the chip stack on the substrate and the making of electrical connections between the terminals of the chip stack and the terminals of the substrate is accomplished via the deposited solder.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of a wire-bond metallized ceramic (MC) embodiment of the present invention;

Figure 2 is a cross-sectional view of a ceramic-soldered-to-ceramic version of the present invention;

Figure 3 is a cross-sectional view of a pin-in-hole connector;

Figure 4 is a cross-sectional view of a leadframe connector;

Figure 5 is a cross-sectional view of a Zero Insertion Force connector; and

Figure 6 is a cross-sectional view of a gullwing connector.

DESCRIPTION OF THE INVENTION

Referring to the drawings and, more particularly to Figure 1, a metallized substrate 10 is provided, having a cutout portion into which a chip stack 20 is mounted. The bottom portion of the chip stack 20, as shown in Figure

1, has a preselected configuration which corresponds to the cutout portion of the ceramic substrate 10. It can be seen that the bottom surface 21 of the chip stack 20 protrudes into and is substantially coplanar with the bottom surface 11 of the ceramic substrate 10.

The substrate 10 can be patterned (circuitized) with a photolithographic process and plated in the standard wire-bond flat pack (WBFP) construction. That is, the construction and manufacturing processes for providing the electrical connections on the surfaces of the substrate 10 are done in a conventional manner, and need not be detailed at this time. For example, see Williams, M. E., et al., "Enabling Fine-Pitch Wire Bonding Through the Use of Thin Film Metal on Ceramic," *Proceedings of the 1995 International Symposium on Microelectronics*, October 24-26, 1995, Los Angeles, California, pp. 290-295.

Note that the terminals 22 on the bottom surface of the chip stack 20 may be connected to the terminals 12 on the bottom surface of the substrate 10, as viewed in Figure 1. It can be seen that this design is not limited in height, so that the chip stack may be made any height desired to fit into the physical dimensions of the particular requirements. Since the terminals 22 of the chip stack 20 and the terminals 12 of the substrate 10 are in substantially the same plane, the wire-bonding equipment for making the connections between these terminals can make bonds to the chip stack and the substrate in the same plane. The procedures for such wire bonding can be of the type described by Christian

Val in "The 3D Interconnection—An Enhanced Densification Approach with Bare Chips," Eighth IEMT: International Electronics Manufacturing Conference, IEEE No. CH2833-2/90/0000-0082, 1990, pp 82–91.

The wire bond 15 connects the terminals 22 to the terminals 12. After the chip stack 20 has been assembled by mounting on the substrate 10 and the desired interconnections made between the chip stack and the substrate, the package can be protected with encapsulants 16 and 17, as shown. Again, the encapsulating process and the material are well-known and need not be specifically discussed at this time.

The advantages of the preferred embodiment, shown in Figure 1, are manyfold. Note that the chip stack may be mounted through the ceramic, so that the wire-bond process is a simple one for connecting the pads on the chip stack to the terminals of the substrate. The arrangement can stay substantially fixed and a taller chip stack 20 can be accommodated since there is unlimited height in this version of the present invention. A heat sink can be attached directly to the top of the uppermost chip stack. Even without such heat sink, there would be good heat dissipation due to the exposure of the chip stack to the air in the stacked position. There is no metal cap in this arrangement to limit the height of the integrated circuit package.

J lead clips 30 may be connected to the substrate 10 by a solder joint 31 to permit further interconnection to other electrical devices, such as a circuit card.

The design shown in Figure 1 is very flexible and can incorporate a variety of options. Thus, gullwing leads may be used, as well as J leads. Referring to Figure 6, a gullwing connector 60 is shown connecting the substrate 10.

It is also possible to dispense additional epoxy 17 to coat the metal on the side of the chip stack, when desired, and to match the stack wire-bond pitch to the ceramic carrier pad pitch to simplify assembly. There are also, with this arrangement, expandable lead counts and overmold plastic encapsulation is available.

A plastic, metal, or ceramic cap, can be used in place of encapsulation. Rather than using a ceramic substrate, it is possible to use an organic carrier, such as an FR4 printed circuit board. A multi-layer ceramic (MLC) substrate or a "flexible" base (such as stamped metal) may also be used in place of the MC substrate. The chip stack-to-ceramic geometry can be flush, underflush, or "overflush," as needed for optimizing the wire bond process. The process can also be compatible with cutouts provided by dry pressing, laser cutting, or other ceramic fabrication techniques.

The arrangement shown in Figure 1 satisfies substantially all of the eight boundary conditions set forth above. The package provides a reliable chip-to-card interconnect arrangement for a "taller than typical" chip or chip stack. The package shown in Figure 1 also maintains reliability of silicon by

protecting the chip stack during the bonding and assembly, the test, the burn-in, the card assembly, as well as the testing and use in final assembly.

As mentioned above, the package arrangement can be extended to a variety of different chip-stack heights. Also, the substrate allows interconnection of signals, power, and ground connections. The arrangement may interconnect with the existing stack without modifying such stack.

The arrangement shown in Figure 1 may meet the JEDEC or de facto card footprint standard. As mentioned above, this arrangement provides an opportunity for heat removal by means of a bonded heat sink on the top or on the side of the stack. The technique shown in Figure 1 is expandable to different industry formats, such as the SIMM, with ceramic-to-ceramic or ceramic stack to organic, such as in the FR4, wire-bond connections. Other card connections, such as pin-in-hole (PIH), card edge Zero Insertion Force (ZIF) connector, and lead frame, are also possible.

Referring to Figure 3, a PIH connector is shown having pins 70 connected to the substrate 10.

In Figure 4 is shown a lead frame connector 80 connected to the substrate 10, while in Figure 5, a ZIF connector 90 is shown connected to the substrate 10. Figures 3-6 clearly illustrate the flexibility of the design shown in Figure 1.

Referring now to Figure 2, a second preferred embodiment of the semiconductor device package incorporating the principles of the present

invention is shown. As mentioned above, this embodiment is a ceramic-soldered-to-ceramic version of the package, and is also based on metallized ceramic substrate processing. In this arrangement, the ceramic substrate 40 has no cutout portion, but has a substantially planar upper and bottom surface.

The chip stack 50 is mounted on the substrate 40 by using the flip-chip-like chip connection. This connection utilizes solder pads 41 meeting with solder-wettable terminals 53 on the chip stack. The solder is dispensed on the substrate where it meets with the terminal 53 of the stack 50.

The screened solder can be near-pear-shaped to allow processing on existing solder-dispensing equipment, yet it can be matched to a tight-knit pad pattern on the existing stack. The solder is provided on the MC substrate rather than the chip stack. This permits the chip-stacking process the freedom to gang process stacks 50 without interspersed layers of solder. Solder can be plated onto the MC substrate instead of screening. Solder injection onto the MC substrate can also be used.

Similarly, solder on the ceramic is desirable because separating the ganged chip stacks and adding solder to one stack at a time will not be cost effective. The chip-stack-to-carrier assembly processes used are similar to the bond and assembly process currently practiced for the controlled-collapse-chip-connection (C4) or flip-chip, Flat Pack (C4FP). These processes are used to connect the stack to the ceramic substrate 40. J lead clips 51 are provided to make contact between the substrate and the printed circuit card, as before.

J lead clips 51 may be connected to the substrate 10 by a solder joint 55 to permit further interconnection to other electrical devices, such as a circuit card. Also, the overall package is again protected by encapsulant 52 in the conventional manner. An underfill epoxy or similar material 54 can be dispensed under the stack.

The metallized ceramic substrate 40 is provided with a circuitry pattern using current metallized ceramic (MC) photolithographic processes. This version of Figure 2 has additional wiring flexibility when compared to the wire-bond version of Figure 1. Since there is no cutout in the embodiment of Figure 2, it is possible to provide additional interconnecting lines in the area under the stack. These electrical lines can be used to jumper signal lines, power buses, and ground lines. The package will provide a reliable chip-to-card interconnect method for the chip stack.

Similar to the wire-bond embodiment, the embodiment of Figure 2 is extendable to a variety of heights of chip stacks. This design concept is also flexible and provides a variety of options which can also be incorporated. This semiconductor device package, arranged in the manner illustrated in Figure 2, provides a reliable chip-to-card interconnect arrangement for the "taller than typical" chip or chip stack. This package also maintains the reliability of the device by protecting the chip stack during the bond and assembly process, the test, burn-in, card assembly, testing, and use in the final assembly. The solder, as noted above, is provided with the ceramic rather than with the chip stack. This

allows the chip-stacking process the freedom to stack chips without adding solder to the stack. This would be very desirable to a chip-stack manufacturer.

The ceramic-to-ceramic interconnection by means of solder pads will have a significantly reduced CTE mismatch; therefore, the assembly will have a higher reliability than an assembly with a silicon-to-ceramic interconnect. The embodiment of Figure 2 has additional wiring flexibility compared to the embodiment of Figure 1, as indicated above, since there is no cutout and it permits more interconnecting lines to be run under the stack area. The arrangement of Figure 2 can interconnect existing stacks without modifying such stacks. The technique used in the embodiment of Figure 2 is expandable to the industry format, such as the SIMM, with ceramic-on-ceramic or ceramic stack on organic, such as FR4. MLC or stamped metal may be used in place of MC. The embodiment of Figure 2 may also meet the JEDEC or de facto card footprint standard. An electrically conductive adhesive may be used in place of solder.

Gull Wing, PIH, lead frame, or card edge ZIF may be used instead of J leads. Figures 3-6 again illustrate the flexibility of this design wherein the substrate 40 of Figure 2 may be substituted for the substrate 10 shown in these Figures. The Figure 2 embodiment makes transition to packaging C4 stacks straightforward. The embodiment of Figure 2 also provides good surface area for heat removal by means of a bonded heat sink either on top of or on the side of the stack.

While the present invention has been described with respect to two specific embodiments, it is clear that these are examples provided by way of explanation only, and not by way of limitation. Thus, the invention is not intended to be limited in scope, except as by the following claims.

What is claimed is:

1. A semiconductor device package comprising:

a thick integrated circuit chip stack having a substantially planar bottom surface with a plurality of terminals;

a carrier substrate having a substantially planar surface adapted to mount said chip stack and having a plurality of terminals adapted to be electrically connected to said terminals of said chip stack;

means for mounting said chip stack on said substrate;

means for making electrical connections between said terminals of said chip stack and said terminals of said substrate; and

encapsulating means for supporting and maintaining said chip stack mounted on said carrier substrate, and providing protection from the environment.

2. A semiconductor package, as claimed in claim 1, wherein said bottom surface of said chip stack has a preselected physical configuration and said carrier substrate has a cutout portion corresponding substantially to said physical configuration of said chip stack bottom surface whereby said chip stack is mounted in said cutout portion with said bottom surface of said chip stack substantially coplanar with said surface of said substrate.

3. A semiconductor package, as claimed in claim 2, wherein wire bonds are coupled to said substrate to permit further electrical connection to said chip stack.

4. A semiconductor package, as claimed in claim 1, wherein a means is provided to connect the substrate to a next level of assembly

5. A semiconductor package, as claimed in claim 4, wherein said means to connect said substrate to said next level of assembly include a plurality of J lead clips.

6. A semiconductor package as claimed in claim 4, wherein said means to connect said substrate to said next level of assembly includes a plurality of gullwing connectors.

7. A semiconductor package as claimed in claim 4, wherein said means to connect said substrate to said next level of assembly includes a plurality of pin-in-hole connectors.

8. A semiconductor package as claimed in claim 4, wherein said means to connect said substrate to said next level of assembly includes a plurality of leadframe connectors.

9. A semiconductor package as claimed in claim 4, wherein said means to connect said substrate to said next level of assembly includes a plurality of Zero Insertion Force connectors.

10. A semiconductor package, as claimed in claim 1, wherein said carrier substrate is a metallized ceramic substrate and said electrical connecting means includes solder pads on said substrate for connection to said terminals on said chip stack.

11. A semiconductor package, as claimed in claim 10, wherein underfill is used between said chip stack and said substrate.

12. A semiconductor package, as claimed in claim 10, wherein an electrically conductive adhesive is used for connection to said terminals on said chip stack.

13. A semiconductor package, as claimed in claim 1, wherein said carrier substrate is a metallized ceramic substrate.

14. A semiconductor package, as claimed in claim 1, wherein multiple stacks are interconnected to each other and/or the next level of assembly.

15. A semiconductor package, as claimed in claim 10, wherein multiple stacks are connected together and/or to the next level of assembly.

16. A method for assembling a semiconductor device package comprising the steps of:

forming a thick integrated circuit chip stack having a substantially planar bottom surface with a plurality of terminals;

mounting said chip stack on a carrier substrate having a substantially planar surface and having a plurality of terminals adapted to be electrically connected to said terminals of said chip stack;

making electrical connections between said terminals of said chip stack and said terminals of said substrate; and

encapsulating said chip stack and said carrier substrate to support said chip stack mounted on said carrier substrate, and to provide protection from the environment.

17. A method as claimed in claim 16, wherein said carrier substrate has a cutout portion and during said step of mounting said chip stack on said carrier substrate, said bottom surface of said chip stack protrudes through said cutout portioin of said carrier substrate.

18. A method as claimed in claim 17, wherein said protruding bottom surface of said chip stack is assembled substantially coplanar with said planar surface of said substrate.

19. A method as claimed in claim 1, wherein said carrier substrate is a metallized ceramic substrate and including the step of depositing solder on said substrate, whereby said mounting of said chip stack on said substrate and said making of electrical connections between said terminals of said chip stack and said terminals of said substrate is accomplished via said deposited solder.

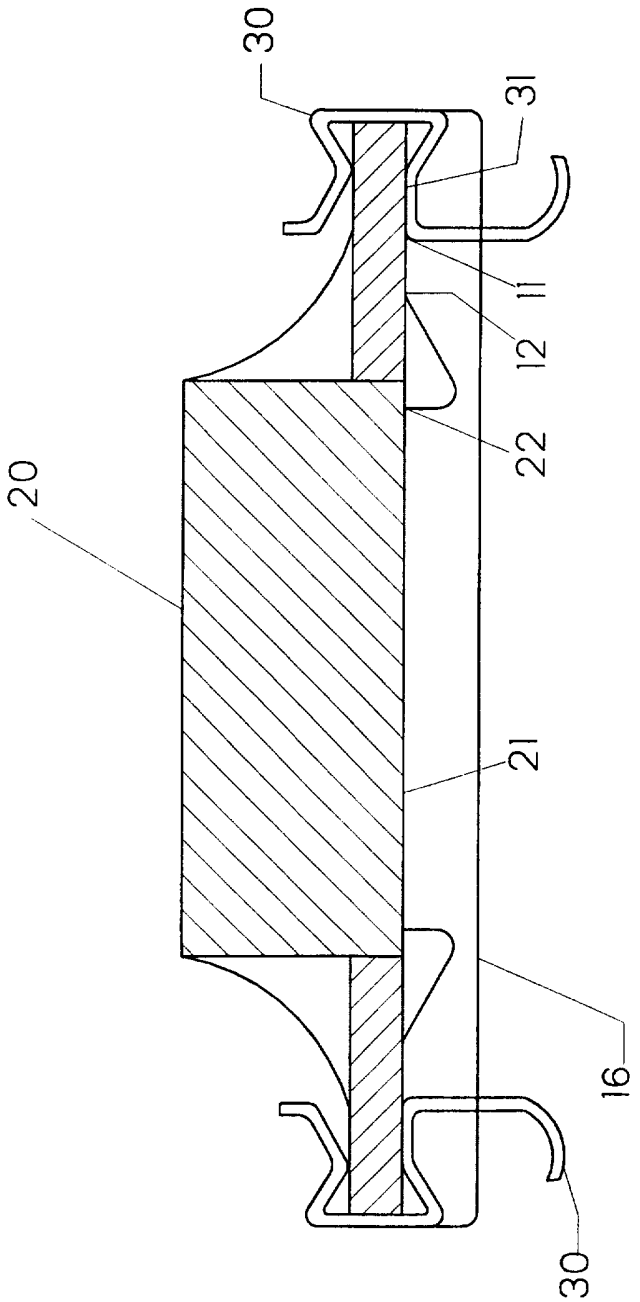

FIG. 1

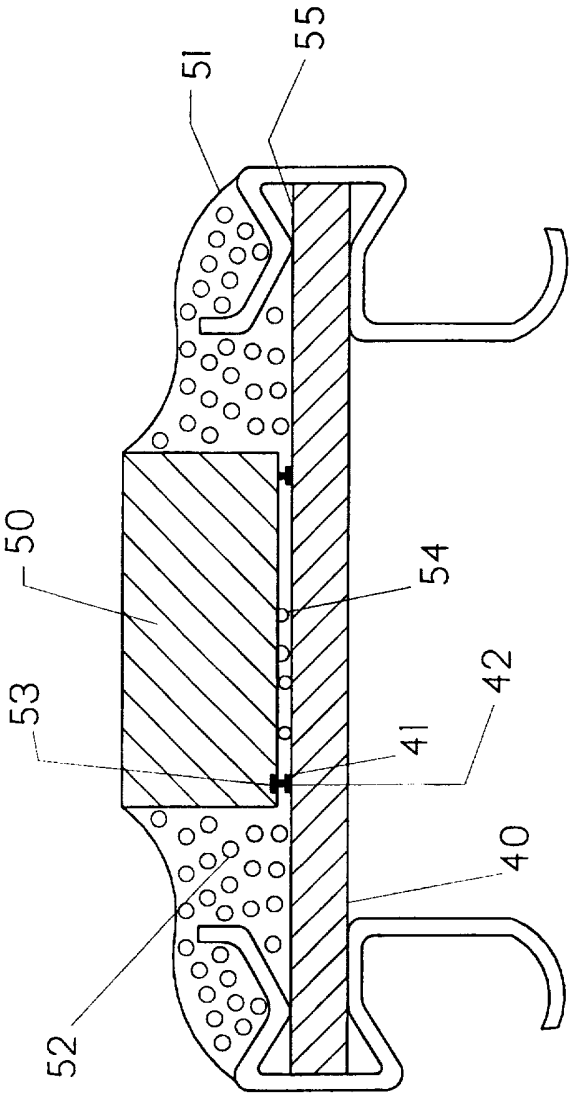

FIG. 2

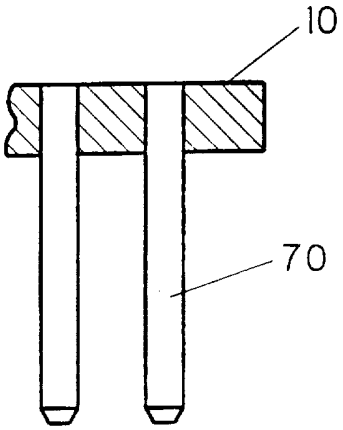

FIG. 3

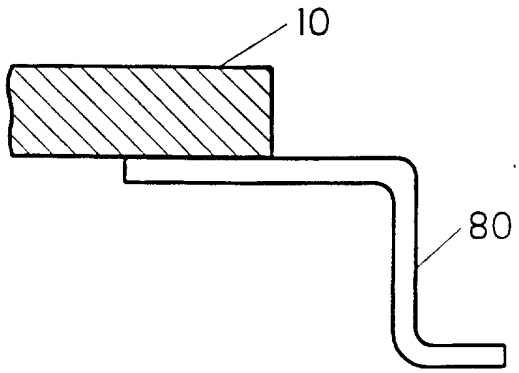

FIG. 4

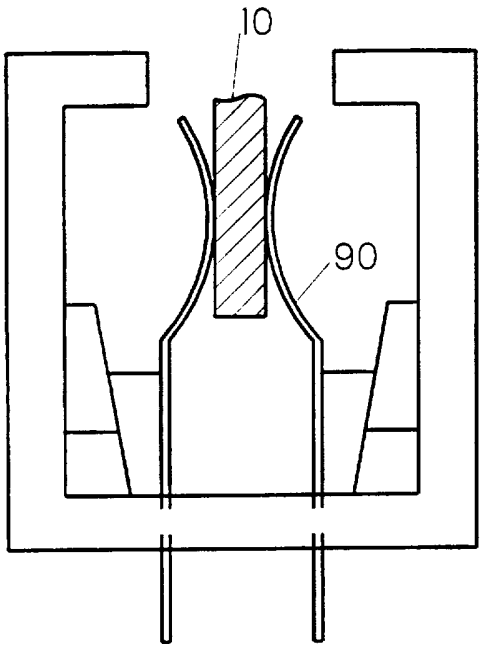

FIG. 5

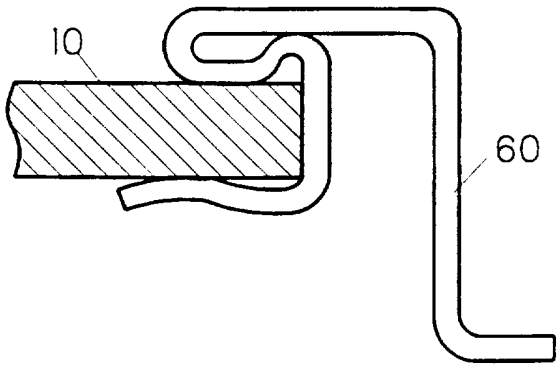

FIG.6

INTERNATIONAL SEARCH REPORT

Intern al Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L25/065 H01L23/31 H01L23/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 712 157 (IBM) 15 May 1996 see figures ---	1,4-6, 10,11, 13,16
X Y	EP,A,0 637 839 (IBM) 8 February 1995 see figures ---	1,4,6, 10,11, 13,16 2,3,14, 15,17-19
Y	PATENT ABSTRACTS OF JAPAN vol. 96, no. 002 & JP,A,08 031869 (NEC CORP), 2 February 1996, see abstract --- -/--	2,3,14, 15,17-19

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A,4 706 166 (GO TIONG C) 10 November 1987 see figure W	2,3,14, 15,17-19
A	US,A,4 850 105 (NAKAJIMA KAZUO ET AL) 25 July 1989 see figures 1-4	2,3,13
A	WO,A,95 29506 (HITACHI LTD) 2 November 1995 see figures 80,81,93,94 see figures 101,102,111 see figures 112,126,127	4-9
A	EP,A,0 486 829 (SEIKO EPSON CORP) 27 May 1992	

1

INTERNATIONAL SEARCH REPORT

Inter ıal Application No
PCT/US 96/10883

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0712157	15-05-96	US-A-	5561322	01-10-96
		JP-A-	8213510	20-08-96
EP-A-0637839	08-02-95	US-A-	5390082	14-02-95
		BR-A-	9402986	18-07-95
		CA-A-	2126121	04-02-95
		CN-A-	1103734	14-06-95
		JP-A-	7078914	20-03-95
US-A-4706166	10-11-87	NONE		
US-A-4850105	25-07-89	JP-A-	1011357	13-01-89
		JP-B-	8021672	04-03-96
WO-A-9529506	02-11-95	NONE		
EP-A-0486829	27-05-92	JP-A-	4158565	01-06-92
		US-A-	5376825	27-12-94