



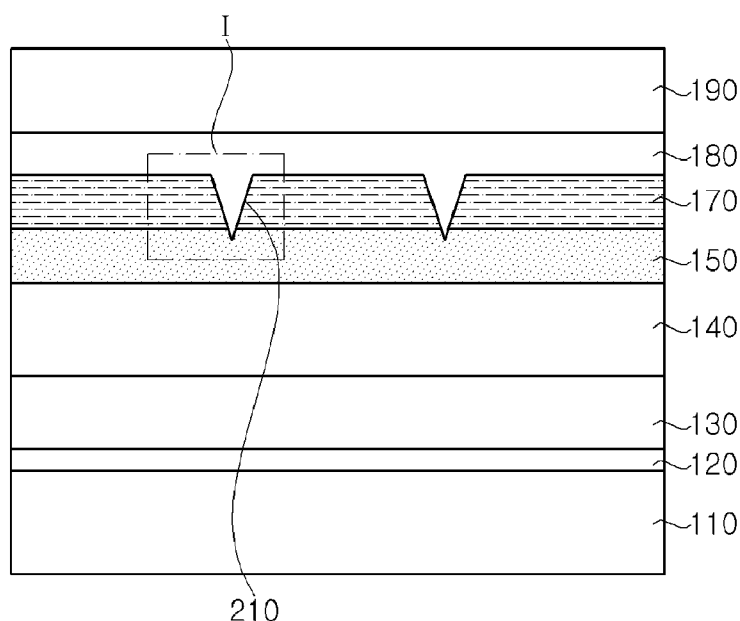
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(54) **Title:** LIGHT EMITTING DEVICE



(57) **Abstract:** A light emitting device is disclosed. The light emitting device includes an n-type nitride semiconductor layer; a V-pit creation layer; an active layer; a p-type nitride semiconductor layer; a V-pit; a high resistance embedment layer; and an n-type doped region overlapping at least part of the active layer, wherein the active layer includes a multi-quantum well structure including pluralities of barrier layers and well layers, at least one of interfaces between the barrier layers and the well layers is disposed within the n-type doped region, the n-type doped region includes a lower surface and an upper surface, and at least one of the upper and lower surfaces of the n-type doped region does not overlap the interfaces between the barrier layers and the well layers.

Description

Title of Invention: LIGHT EMITTING DEVICE

Technical Field

- [1] Exemplary embodiments of the present disclosure relate to a light emitting device, and more particularly, to a light emitting device having improved efficiency in current spreading and current leakage prevention.

Background Art

- [2] Recently, a nitride-based semiconductor broadly used as a base material of a light emitting device such as a light emitting diode is grown on a homogeneous substrate such as a gallium nitride substrate or on a heterogeneous substrate such as a sapphire substrate. Some factors affecting crystallinity and luminous efficacy of the nitride-based semiconductor are related to characteristics of a growth substrate.
- [3] A nitride-based semiconductor grown on a heterogeneous substrate used as a growth substrate has high defect density due to differences in lattice parameter and coefficient of thermal expansion between the growth substrate and the nitride-based semiconductor. For example, a nitride-based semiconductor grown on a sapphire substrate has a high dislocation density of about $1 \times 10^9/\text{cm}^2$ or more.
- [4] Dislocations provide electron trap sites to cause non-emissive recombination or spatial separation between electrons and holes, or act as a path of current leakage. Particularly, dislocations propagated to a surface of a semiconductor layer and contacting electrodes thereon act as a main path of current leakage to generate reverse current at reverse voltage, and become a main cause of failure of a light emitting device due to electrostatic discharge.
- [5] In order to prevent failure of the light emitting device due to electrostatic discharge, a separate Zener diode may be provided to the light emitting device or crystallinity of the light emitting device may be improved to enhance durability with respect to electrostatic discharge. However, such a separate Zener diode requires an additional space, thereby increasing volume of the light emitting device and process costs. In addition, existing techniques have a limit in improvement of crystallinity of the light emitting device and it is substantially impossible to form a dislocation-free epitaxial layer.

Disclosure of Invention

Technical Problem

- [6] Exemplary embodiments of the present disclosure provide a light emitting device having good current spreading efficiency and high electrical reliability.

Solution to Problem

- [7] In accordance with one exemplary embodiment, a light emitting device includes: an

n-type nitride semiconductor layer; a V-pit creation layer disposed on the n-type nitride semiconductor layer; an active layer disposed on the V-pit creation layer; a p-type nitride semiconductor layer disposed on the active layer; a V-pit formed through the active layer; a high resistance embedment layer at least partially filling the V-pit; and an n-type doped region overlapping at least part of the active layer, wherein the active layer includes a multi-quantum well structure including pluralities of barrier layers and well layers, at least one of interfaces between the barrier layers and the well layers is disposed within the n-type doped region, the n-type doped region includes a lower surface and an upper surface, and at least one of the upper and lower surfaces of the n-type doped region does not overlap the interfaces between the barrier layers and the well layers.

- [8] The n-type doped region may include Ge as a dopant and have a thickness of 10 nm to 100 nm.
- [9] The n-type doped region may have a greater thickness than at least one of the barrier layers and the well layers, and at least one of the barrier layers and the well layers may be disposed within the n-type doped region.
- [10] The n-type doped region may include a region modulation-doped with an n-type dopant.
- [11] The n-type doped region may include a first doped region and a second doped region having a lower doping concentration than the first doped region, and the first doped region may be closer to the V-pit creation layer than the second doped region.
- [12] The light emitting device may further include a V-pit enlargement layer interposed between the active layer and the V-pit creation layer, and the n-type doped region may be disposed over the active layer and the V-pit creation layer.
- [13] The V-pit creation layer may include a superlattice layer, and at least one of interfaces between layers within the superlattice layer may be disposed within the n-type doped region.
- [14] In accordance with another aspect of the present invention, a light emitting device includes: an n-type nitride semiconductor layer; a V-pit creation layer disposed on the n-type nitride semiconductor layer; an active layer disposed on the V-pit creation layer and including a well layer and a barrier layer; a p-type nitride semiconductor layer disposed on the active layer; a V-pit formed through the active layer and the V-pit enlargement layer; a high resistance embedment layer at least partially filling the V-pit; and an n-type doped region overlapping at least part of the active layer, wherein at least one of upper and lower surfaces of the n-type doped region corresponds to an interface between the well layer and the barrier layer, and a thickness of the n-type doped region is equal to integer times the thickness of the barrier layer or the well layer.

- [15] The light emitting device may further include a V-pit enlargement layer disposed on the V-pit creation layer, wherein the V-pit enlargement layer includes a superlattice layer in which first nitride layers and second nitride layers having different band-gap energies are alternately stacked one above another, and at least one of interfaces between the first and second nitride layers is disposed within the n-type doped region.
- [16] The n-type doped region may have an average Ge doping concentration of 5×10^{19} atoms/cm³ or more.
- [17] The n-type doped region may have a thickness of 10 nm to 100 nm.
- [18] The n-type doped region may have a greater thickness than at least one of the first nitride layers and the second nitride layers.
- [19] The n-type doped region may include a region modulation-doped with Ge dopants.
- [20] The n-type doped region may include at least one first nitride layer and at least one second nitride layer disposed therein.
- [21] The n-type doped region may include a first doped region and a second doped region having a lower doping concentration than the first doped region, and the first doped region may be closer to the V-pit creation layer than the second doped region.
- [22] The n-type doped region may be disposed over the active layer and the V-pit creation layer.

Advantageous Effects of Invention

- [23] According to exemplary embodiments, the light emitting device includes an n-type doped region disposed independently of other layers formed in the light emitting device to achieve sufficient electron concentration while effectively enlarging V-pits. Accordingly, the light emitting device has improved electrical reliability and current spreading effects.

Brief Description of Drawings

- [24] Figure 1 and Figure 2 are a side-sectional view and an enlarged sectional view of a light emitting device according to one exemplary embodiment of the present disclosure.
- [25] Figure 3a to Figure 3e are graphs depicting band-gap energy of an active layer and an n-type doped region according to exemplary embodiments of the present disclosure.
- [26] Figure 4 and Figure 5 are a side-sectional view and an enlarged sectional view of a light emitting device according to another exemplary embodiment of the present disclosure.
- [27] Figure 6 is an enlarged sectional view of a light emitting device according to a further exemplary embodiment of the present disclosure.
- [28] Figure 7a to Figure 7e are graphs depicting band-gap energy of a V-pit enlargement layer and an n-type doped region according to exemplary embodiments of the present disclosure.

disclosure.

- [29] Figure 8 is a graph depicting a location of an n-type doped region according to yet another embodiment of the present disclosure.

Mode for the Invention

- [30] Hereinafter, exemplary embodiments will be described in more detail with reference to the accompanying drawings. The following embodiments are provided by way of example so as to fully convey the spirit of the present disclosure to those skilled in the art to which the present disclosure pertains. Accordingly, the present disclosure is not limited to the embodiments disclosed herein and can also be implemented in different forms. In the drawings, widths, lengths, thicknesses, and the like of elements can be exaggerated for clarity and descriptive purposes. When an element or layer is referred to as being "disposed above" or "disposed on" another element or layer, it can be directly "disposed above" or "disposed on" the other element or layer or intervening elements or layers can be present. Throughout the specification, like reference numerals denote like elements having the same or similar functions.

- [31] In order to address problems caused by dislocations described above, there is suggested a technique in which V-pits are formed through enlargement of the dislocations and are then filled with a high resistance semiconductor material to suppress current leakage through the dislocations by increasing resistance of a path through which current enters the dislocations. However, the dislocations are not blocked simply by forming the V-pits and it is necessary to enlarge the V-pits so as to achieve resistance effects. In addition, interfaces between semiconductor layers contacting inclined surfaces of the enlarged V-pits are required to have good crystal quality in order to prevent additional current leakage. Hereinafter, a light emitting device includes a semiconductor layer capable of reducing current leakage using V-pits while securing good crystal quality will be described.

- [32] It should be understood that compositions, growth methods, growth conditions, thicknesses, and the like of nitride-based semiconductor layers described below are provided by way of example and the present disclosure is not limited thereto. For example, in expression of AlGa_N, a composition ratio of Al to Ga may be modified in various ways by a person having ordinary knowledge in the art (hereinafter, "those skilled in the art") as needed. In addition, the nitride-based semiconductor layers described below may be grown by various methods known to those skilled in the art, for example, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or hydride vapor phase epitaxy (HVPE). Herein, in the following exemplary embodiments, semiconductor layers will be described as being grown within a growth chamber by MOCVD. For growth of the nitride-based semiconductor

layers, any sources known to those skilled in the art may be supplied into the growth chamber, and for example, TMGa or TEGa may be used as a Ga source, TMAI or TEAI may be used as an Al source, TMIIn or TEIn may be used as an In source, and NH_3 may be used as an N source. However, it should be understood that the present disclosure is not limited thereto.

- [33] Figure 1 is a side-sectional view of a light emitting device according to one exemplary embodiment of the present disclosure, and Figure 2 is an enlarged sectional view of 'region I' in Figure 1.
- [34] Referring to Figure 1 and Figure 2, the light emitting device includes an n-type nitride semiconductor layer 140, a V-pit creation layer 150, an active layer 170, a high resistance embedment layer 180, a p-type nitride semiconductor layer 190, and an n-type doped region 310. The light emitting device may further include a growth substrate 110, a buffer layer 120, and an undoped nitride layer 130.
- [35] For the growth substrate 110, any substrate may be used without limitation so long as the substrate allows growth of a nitride-based semiconductor layer thereon and may include, for example, a sapphire substrate, a silicon substrate, a silicon carbide substrate, an aluminum nitride substrate, and a gallium nitride substrate. In addition, the growth substrate 110 may include a growth plane on which the nitride-based semiconductor layer is grown, and the growth plane may be a crystalline plane having polar, non-polar or semi-polar characteristics.
- [36] The buffer layer 120 may include AlGaIn and/or GaN, and may be grown on the growth substrate 110 at a temperature of about 500°C to 600°C. The buffer layer 120 can serve to relieve stress and strain caused by lattice mismatch between the growth substrate 110 and a nitride-based semiconductor grown on the buffer layer. Alternatively, the buffer layer 120 may be omitted.
- [37] The undoped nitride layer 130 may be disposed on the growth substrate 110 and may include a nitride semiconductor such as (Al, Ga, In)N. For example, the undoped nitride layer 130 may include u-GaN. The undoped nitride layer 130 is free from dopants and thus can exhibit good crystallinity. As a result, the undoped nitride layer 130 can improve crystallinity of other semiconductor layers disposed on the undoped nitride layer 130, as described below.
- [38] Here, it should be understood that the growth substrate 110, the buffer layer 120 and the undoped nitride layer 130 can be omitted from the light emitting device depending on the structure of the light emitting device. When the light emitting device according to this exemplary embodiment is applied to a flip-chip type light emitting device or a vertical type light emitting device, the growth substrate 110 can be omitted together with at least some of the buffer layer 120 and the undoped nitride layer 130.
- [39] Herein, detailed descriptions of well-known technical features related to the growth

substrate 110, the buffer layer 120 and the undoped nitride layer 130 are omitted.

[40] The n-type nitride semiconductor layer 140 may include a nitride-based semiconductor such as (Al, Ga, In)N, and may further include an n-type dopant to exhibit n-type conductivity. For example, the n-type nitride semiconductor layer 140 may include Si, Ge, C, or the like as dopants. As the n-type dopant for the n-type nitride semiconductor layer 140, Si may be doped in a concentration of 1×10^{17} atoms/cm³ to 5×10^{19} atoms/cm³. The n-type nitride semiconductor layer 140 may have a thickness of several micrometers and may include a single layer or multiple layers. The n-type nitride semiconductor layer 140 may be grown through MOCVD by introducing Group III element sources such as Al, Ga and In, Group V element sources such as N, and a Si dopant source such as silane into a growth chamber.

[41] The V-pit creation layer 150 may be disposed on the n-type nitride semiconductor layer 140.

[42] The V-pit creation layer 150 may include a nitride-based semiconductor such as (Al, Ga, In)N. The V-pit creation layer 150 can act as a seed for creation of V-pits 210 through various methods. For example, upon growth of the V-pit creation layer 150, growth conditions may be adjusted such that the V-pit creation layer 150 has a higher vertical growth speed with respect to a lateral growth speed than the n-type nitride semiconductor layer 140, whereby the V-pit creation layer 150 can be grown as a semiconductor layer with a rough surface through three-dimensional growth. For example, the V-pit creation layer 150 may be grown at a lower temperature, for example, at about 900°C, than the n-type nitride semiconductor layer 140. As the V-pit creation layer 150 is grown at a relatively low temperature, three-dimension growth is promoted in the course of growing the V-pit creation layer 150, whereby the V-pit creation layer 150 can be grown as a semiconductor layer with a rough surface. As the V-pit creation layer 150 is grown at a relatively low temperature, the V-pits 210 may be formed at least some of portions in which dislocations propagated from the semiconductor layers (including the n-type nitride semiconductor layer 140) under the V-pit creation layer 150.

[43] Here, it should be understood that intentional reduction in crystallinity of the V-pit creation layer 150 is not limited to growth of the V-pit creation layer 150 under low temperature conditions as described above. For example, some exemplary embodiments may include intentional reduction in crystallinity of the V-pit creation layer 150 through adjustment of the ratio of III/V elements supplied into the growth chamber, growth pressure, and flow rates of Group III element sources and Group V element sources upon growth of the V-pit creation layer 150.

[44] The V-pits 210 may be created in the V-pit creation layer 150 and may be formed over other semiconductor layers additionally grown by other processes described

below. Alternatively, V-pit seeds are formed in the V-pit creation layer 150 and V-pits created from the V-pit seed may be formed over semiconductor layers additionally grown by other processes described below. Locations of the V-pits 210 created in the V-pit creation layer may be adjusted through change of growth conditions and the like in various ways, and may be adjusted through an additional process. For example, after completion of growth of the V-pit creation layer 150, an annealing process may be additionally performed to adjust the location of the V-pits 210 created therein. For example, the annealing process may be performed by increasing an inner temperature of the growth chamber to about 1050°C, followed by decreasing the temperature. By the annealing process, the V-pits 210 can be created at a relatively high location in the V-pit creation layer. Accordingly, the locations of the V-pits 210 created can be arbitrarily determined depending upon time and temperature of the annealing process.

[45] The V-pits 210 may be enlarged in a radial shape and a surface of each of the V-pits 210 may correspond to one plane of a nitride semiconductor. For example, the V-pits 210 may be formed in a reverse hexagonal pyramid shape and the surface of each of the V-pits 210 may correspond to one crystal plane of the nitride semiconductor.

[46] The V-pit creation layer 150 may include a single layer or multiple layers. For example, the V-pit creation layer 150 may include InGaN, AlGaIn, GaN, AlInGaIn, InAlN, and the like, and may have a structure in which AlInGaIn layers and AlGaIn layers are alternately stacked one above another. Further, the V-pit creation layer 150 may include a nitride semiconductor having a higher lattice parameter than the average lattice parameter of the n-type nitride semiconductor layer 140. For example, the V-pit creation layer 150 may include indium, the atomic radius of which is greater than those of Ga and Al. As the V-pit creation layer 150 has a relatively high lattice parameter, the V-pit creation layer 150 is subjected to compressive strain, which promotes radial enlargement of dislocation defects into the shape of the V-pits 210, so that boundary planes of the V-pits 210 can become more clear and the size of the V-pits 210 can be increased.

[47] The active layer 170 may be disposed on the V-pit creation layer 150. Further, the V-pits 210 may be formed through the active layer 170, whereby a portion of the active layer 170 adjoining each of the V-pits 210 may have an inclined surface. That is, the V-pits 210 may be enlarged in a radial shape together with growth of the active layer 170, and may have a V-shaped cross-section, as shown in the drawings. Further, as the V-pits 210 are enlarged together with growth of the active layer 170, the V-pits 210 may be formed through the active layer 170.

[48] The active layer 170 may include a nitride-based semiconductor such as (Al, Ga, In)N, and may be formed in a multi-quantum well structure including barrier layers 171 having relatively high band-gap energy and well layers 173 having relatively low

band-gap energy. The active layer 170 may include indium (In) and, particularly, the barrier layer 171 may include AlInGaN which contains In. Accordingly, as the active layer 170 is grown, the V-pits 210 are further enlarged, thereby increasing the size of the V-pits 210. Specifically, when nitride layers having relatively large lattice parameters and including indium (In) are grown on a region in which the V-pits 210 are created, compressive strain can be exerted on the V-pits 210 enlarged. When the V-pits 210 are subjected to compressive strain, stress and strain are exerted outwards within the V-pits 210, thereby increasing the size of the V-pits 210. However, it should be understood that the present disclosure is not limited thereto.

[49] Elements and the composition of the well layer 173 may be determined depending upon the peak wavelength of light to be emitted from the light emitting device 100, and considering the band-gap energy of the well layer 173, the elements and the composition of a nitride-based semiconductor for the barrier layer 171 may be determined such that the barrier layer 171 has relatively high band-gap energy.

[50] Further, the light emitting device includes an n-type doped region 310 overlapping at least part of the active layer 170. Next, the n-type doped region 310 according to exemplary embodiments will be described in more detail with reference to Figure 1 to Figure 3e. Figure 3a to Figure 3e are graphs depicting band-gap energy of active layers and n-type doped regions according to exemplary embodiments of the present disclosure. Although the n-type doped region 310 will be described as being doped with Ge in the following exemplary embodiments, the present disclosure is not limited thereto. The n-type doped region 310 may further include other n-type dopants such as Si or C in addition to Ge.

[51] The n-type doped region 310 may be a region including Ge as a dopant, and thus semiconductor layers thereof exhibit n-type conductivity. When the nitride semiconductor includes the n-type doped region 310, three-dimensional growth of the nitride semiconductor is predominantly carried out such that vertical growth of the nitride semiconductor is predominant to lateral growth of the nitride semiconductor. That is, when Ge is doped into the nitride semiconductor during growth of the nitride semiconductor, a possibility that a bond between Ge and N is broken is increased due to relatively low bonding energy between Ge and N. Accordingly, when Ge is doped into the nitride semiconductor during growth of the nitride semiconductor, three-dimensional growth of the nitride semiconductor becomes predominant to two-dimensional growth thereof. It should be understood that the n-type doped region 310 may further include other dopants as well as Ge, as described above.

[52] As described above, the V-pits 210 are more enlarged through three-dimensional growth of the nitride semiconductor than through two-dimensional growth thereof. Thus, as three-dimensional growth becomes predominant by forming the n-type doped

region 310 that overlaps at least part of the active layer 170, the size of the V-pits 210 can be further increased during growth of the active layer 170. Particularly, although the composition ratio of In can be increased in order to enlarge the V-pits 210, there is a limit in increase of the composition ratio of In in the active layer 170 in consideration of emission wavelengths. Therefore, by forming the n-type doped region 310 to overlap at least part of the active layer 170, it is possible to increase the size of the V-pits 210 without increasing the composition ratio of In.

- [53] Although enlargement of the V-pits 210 can be achieved using Si as a dopant, Si can deteriorate crystallinity of the active layer 170. On the contrary, the n-type doped region 310 including Ge as a dopant causes less deterioration in crystallinity of the semiconductor layer than the doped region including Si alone as a dopant. In addition, Ge used as a dopant can permit greater enlargement of the V-pits 210 than Si used as a dopant.
- [54] More specifically, when Si is used as a dopant, Si is substituted into sites of Group III elements (Ga, Al, In). However, since Si is not in the same period as Ga, the diameter of a Si atom is smaller than the diameter of a Ga atom. Accordingly, when Si is doped into GaN or into AlGa_N, InGa_N, or AlInGa_N having a relatively high mole fraction of Ga, one Ga site is substituted with a Si atom, thereby increasing the possibility of generating defects due to lattice mismatch. Further, since the Si atom has a small size, tensile stress and strain are exerted on lattices surrounding the site into which the Si atom is substituted, thereby obstructing enlargement of the V-pits 210. On the contrary, since Ge is in the same period as Ga, there is no significant difference in atom size therebetween. Accordingly, when Ge is used as a dopant, since stress and strain exerted on surrounding lattices due to lattice mismatch are insignificant upon substitution of a Ge atom into the Ga site, deterioration in crystallinity due to lattice mismatch can be relieved even when Ge is substituted as a dopant into the nitride-based semiconductor. Furthermore, Ge has a larger atomic radius than Si and causes compressive stress and strain on lattices around a Ge substituted site, thereby causing further enlargement of the V-pits 210.
- [55] On the other hand, although the doping concentration of the n-type doped region 310 is not particularly limited, the n-type doped region 310 may have a doping concentration of 5×10^{19} atoms/cm³ or more, specifically in the range of 5×10^{19} atoms/cm³ to 8×10^{20} atoms/cm³, to promote three-dimensional growth, thereby further improving enlargement of the V-pits 210. Further, although the thickness of the n-type doped region 310 is not particularly limited, the n-type doped region 310 having an excessively thin thickness provides an insignificant effect in enlargement of the V-pits 210, and the n-type doped region having an excessively thick thickness can deteriorate crystallinity within the n-type doped region 310, thereby deteriorating luminous

efficacy of the light emitting device. Accordingly, it is desirable that the thickness of the n-type doped region 310 be determined within a predetermined range, and for example, the n-type doped region 310 may have a thickness of about 10 nm to 100 nm. However, it should be understood that the present disclosure is not limited thereto.

[56] Referring again to Figure 2, the n-type doped region 310 may overlap at least part of the active layer 170 and may be disposed over at least two layers within the active layer 170. Thus, at least one of interfaces between the barrier layers 171 and the well layers 173 may be disposed within the n-type doped region 310. Further, the n-type doped region 310 may be disposed independently of the barrier and well layers of the active layer 170. In other words, when the n-type doped region 310 has an upper surface and a lower surface, locations of the upper surface and/or the lower surface of the n-type doped region 310 may not correspond to the locations of the interfaces between the barrier layers 171 and the well layers 173.

[57] The reason for formation of the n-type doped region 310 to be disposed independently of semiconductor layers within the light emitting device is to achieve a sufficient doping thickness for securing the V-pits. Table 1 shows surface roughness depending upon doping thickness upon Ge doping in a concentration of 1×10^{19} atoms/cm³ or more, as measured through atomic force measurement (AFM). As can be seen from Table 1, in order to form a semiconductor layer having surface roughness of a predetermined RMS value or more, it is necessary to form the semiconductor layer to a predetermined thickness or more. For example, from Table 1, it could be seen that surface roughness was rapidly increased when the thickness of the semiconductor layer was 40 nm or more, and further rapidly increased when the thickness of the semiconductor layer was 100 nm or more.

[58] [Table 1]

Light emitting device sample	Sample A	Sample B	Sample C	Sample D
Thickness of Ge doped layer (nm)	10	40	100	300
RMS (nm)	3.32	8.96	8.48	14.6

[59] As such, although the n-type doped region 310 may have a thickness of dozens of nanometers or more, each of the layers within the active layer 170 has a thickness of several nanometers and thus formation of the n-type doped region 310 to be disposed over plural layers within the active layer 170 enables more effective enlargement of the V-pits.

[60] Further, each n-type doped region 310 may have various doping concentrations, for

example, a constant doping concentration, a gradually increasing or decreasing doping concentration in the thickness direction thereof, or a modulated doping concentration in which the doping concentration repeatedly increases and decreases. At least one of n-type doped region 310 may include a modulation-doped region. For example, the n-type doped region 310 may include a region modulated-doped with Ge dopants.

- [61] Furthermore, the light emitting device may include a plurality of n-type doped regions 310, which may have different doping concentrations. At this point, the doping concentrations of the plural n-type doped regions 310 may gradually decrease with increasing distance from the n-type nitride semiconductor layer 140.
- [62] Next, referring to Figure 2 and Figure 3a to Figure 3e, examples of the n-type doped region 310 according to various embodiments of the present disclosure will be described. Here, it should be understood that the present disclosure is not limited thereto.
- [63] First, as shown in Figure 2 and Figure 3a, the n-type doped region 310 may be disposed over two layers to twenty layers within the active layer 170, and, for example, the n-type doped region 310 may be disposed over three barrier layers 171 and two well layers 173. Further, the upper surface and the lower surface of the n-type doped region 310 may not overlap interfaces between the barrier layers 171 and the well layers 173. As shown in the drawings, the lower surface of the n-type doped region 310 may be disposed at the middle of one barrier layer 171 and the upper surface of the n-type doped region 310 may be disposed at the middle of another barrier layer 171. In addition, the n-type doped region 310 may be formed in plural within the active layer 170.
- [64] In another exemplary embodiment, as shown in Figure 3b, one of the upper and lower surfaces of the n-type doped region 310 may be disposed corresponding to an interface between the barrier layer 171 and the well layer 173. For example, the lower surface of the n-type doped region 310 may overlap a lower surface of one barrier layer 171. This structure can be obtained by introducing a Ge dopant source into the growth chamber in the course of growing the corresponding barrier layer 171.
- [65] When the thickness of the n-type doped region 310 is equal to integer times the thickness of the well layer 173 or the barrier layer 171 so as to correspond to the interface therebetween, the doping concentration of the n-type doped region 310 can also be changed in an atmosphere ramping period between the respective layers upon growth to provide a clear interface between doped regions, thereby reducing thickness tolerance.
- [66] In a further exemplary embodiment, as shown in Figure 3c, both the upper and lower surfaces of the n-type doped region 310 may be disposed corresponding to the interfaces between the barrier layers 171 and the well layers 173. For example, the lower

surface of the n-type doped region 310 may overlap a lower surface of one barrier layer 171 and the upper surface of the n-type doped region 310 may overlap an upper surface of another barrier layer 171. In this exemplary embodiment, the n-type doped region 310 is also formed independently of the barrier layers 171 and the well layers 173 instead of having a relationship therewith.

[67] As described above, when the interface between the barrier layer 171 and the well layer 173 is not coincident with a time point of dopant introduction, despite an adverse effect on tolerance of the interface, compressive strain can be sufficiently exerted on the interface as described above and then three-dimensional growth can be achieved, thereby enabling more effective enlargement of the V-pits. According to yet another exemplary embodiment, as shown in Figure 3d, the doping concentration may differ in one n-type doped region 310. For example, Ge dopants may be included in one n-type doped region 310 through modulation doping. Modulation doping of the Ge dopants can relieve deterioration of crystallinity of the active layer 170 by the n-type doped region 310.

[68] Although Ge doping can relieve creation of crystal defects as compared with Si doping, Ge doping also causes creation of the crystal defects and compromises enlargement of the V-pits, and is thus required to be performed in a suitable cycle and to a suitable thickness so as to achieve both effects. Thus, modulation doping as in the above exemplary embodiment is performed for the purpose of preventing creation of crystal defects while securing a sufficient doping thickness.

[69] In some exemplary embodiments, as shown in Figure 3e, the light emitting device may include a plurality of n-type doped regions 311, 312. For example, the n-type doped region 310 may include a first n-type doped region 311 and a second n-type doped region 312. The first n-type doped region 311 may have a higher Ge doping concentration than the second n-type doped region 312. In these embodiments, the first n-type doped region 311 may be closer to the V-pit creation layer 150 than the second n-type doped region 312. By the first n-type doped region 311 disposed relatively close to the V-pit creation layer 150, the V-pits 210 can be enlarged. Further, the second n-type doped region 312 has a lower Ge doping concentration than the first n-type doped region, thereby relieving deterioration in crystallinity of the active layer 170 while further enlarging the size of the V-pits 210.

[70] Exemplary embodiments obtained through combination of technical features described in the above exemplary embodiments are also included in the present disclosure.

[71] In this way, the n-type doped region 310 is formed independently of the barrier layers 171 and the well layers 173 within the active layer 170, thereby enabling easy control of enlargement of the V-pits 210 through the n-type doped region 310. Namely,

considering the composition of the active layer 170, growth conditions, and the size of the V-pits 210, the n-type doped region 310 is set regardless of the barrier layers 171 and the well layers 173, thereby optimizing luminous efficacy and reliability of the light emitting device.

- [72] The V-pits 210 serve to achieve more efficient current spreading and to reduce current leakage while improving durability to electrostatic discharge by blocking propagation of dislocations through the V-pits 210. Accordingly, formation of the V-pits 210 in the light emitting device results in improvement of luminous efficacy and electrical reliability of the light emitting device. According to the exemplary embodiments, the V-pits 210 can be created in a relatively large size, thereby maximizing advantageous effects of the V-pits 210. As such, the exemplary embodiments provide a light emitting device having improved luminous efficacy and reliability.
- [73] The light emitting device may further include an electron injection layer (not shown) under the active layer 170 and an electron blocking layer (not shown) on the active layer 170. The electron injection layer and the electron blocking layer can increase electron density in the active layer 170, thereby improving luminous efficacy.
- [74] The V-pits 210 are at least partially filled with the high resistance embedment layer 180. The high resistance embedment layer 180 may be disposed on the active layer 170.
- [75] The high resistance embedment layer 180 may include a nitride-based semiconductor such as (Al, Ga, In)N and may have relatively high resistance. Thus, the high resistance embedment layer 180 may be doped in a low concentration or may be in an undoped state. Further, the high resistance embedment layer 180 may have higher band-gap energy than the active layer 170. As the V-pits 210 are at least partially filled with the high resistance embedment layer 180 having relatively high resistance, the high resistance embedment layer 180 can block leaked current from flowing in a downward direction through dislocations residing at lower ends of the V-pits 210. Thus, the light emitting device has improved durability with respect to electrostatic discharge.
- [76] The p-type nitride semiconductor layer 190 may include a nitride-based semiconductor such as (Al, Ga, In)N, and may be disposed on the high resistance embedment layer 180 and/or the active layer 170. The p-type nitride semiconductor layer 190 may include a p-type dopant, for example, Mg. All of technical features known in the art may be applied to the p-type nitride semiconductor layer 190, and detailed descriptions thereof will be omitted herein.
- [77] The light emitting device may further include a V-pit enlargement layer (not shown) disposed between the active layer 170 and the V-pit creation layer 150. The V-pits 210 can be further enlarged by the V-pit enlargement layer. When the light emitting device

further includes the V-pit enlargement layer, the n-type doped region 310 may overlap at least part of the V-pit enlargement layer. In this case, the n-type doped region 310 may be disposed over the active layer 170 and the V-pit enlargement layer. Furthermore, the V-pit enlargement layer may include a superlattice layer, and at least one of interfaces between layers in the superlattice layer may be disposed within the n-type doped region 310. The V-pit enlargement layer will be described in more detail in description of an exemplary embodiment shown in Figure 4 and Figure 5.

[78] Although the V-pit enlargement layer is illustrated as overlapping at least part of the n-type doped region 310 in the exemplary embodiment shown in Figure 4 and Figure 5, it should be understood that this feature is not necessary in the present embodiment. That is, in this embodiment, the overlapping structure between the V-pit enlargement layer and the n-type doped region 310 may be optionally selected.

[79] This exemplary embodiment provides a light emitting device which includes the V-pits 210 at least partially filled with the high resistance embedment layer 180. Particularly, the light emitting device includes the n-type doped region 310, so that the V-pits 210 can be further enlarged, thereby improving current spreading and reliability. The light emitting device described in this exemplary embodiment may be used as various types of light emitting devices such as vertical type, flip-chip type or lateral type light emitting devices through an additional process.

[80] Figure 4 is a side-sectional view of a light emitting device according to another exemplary embodiment of the present disclosure, and Figure 5 is an enlarged sectional view of region II of Figure 4. Figure 6 is an enlarged sectional view of a portion of a light emitting device according to a further exemplary embodiment of the present disclosure, corresponding to region II of Figure 4.

[81] The light emitting device according to this exemplary embodiment is different from the light emitting device shown in Figure 1 and Figure 2 in that the light emitting device according to this exemplary embodiment further includes a V-pit enlargement layer 160 and has a structure wherein an active layer 170 selectively overlaps an n-type doped region 310. Herein, different features of the light emitting device according to this exemplary embodiment will be mainly described, and detailed descriptions of the same features will be omitted.

[82] Referring to Figure 4 and Figure 5, the light emitting device according to this exemplary embodiment includes an n-type nitride semiconductor layer 140, a V-pit creation layer 150, a V-pit enlargement layer 160, an active layer 170, a high resistance embedment layer 180, a p-type nitride semiconductor layer 190, and an n-type doped region 310. The light emitting device may further include a growth substrate 110, a buffer layer 120, and an undoped nitride layer 130.

[83] The V-pit enlargement layer 160 may be disposed on the active layer 170, and V-pits

220 may be formed through the V-pit enlargement layer 160 and the active layer 170. That is, the V-pits 220 may be created from the V-pit creation layer 150 and then enlarged in a radial shape through the V-pit enlargement layer 160 and the active layer 170.

[84] The V-pit enlargement layer 160 may include a nitride semiconductor such as (Al, Ga, In)N and may be grown from an upper surface of the V-pit creation layer 150. The upper surface of the V-pit creation layer 150 acts as seeds for growth of the V-pit enlargement layer 160, which can be grown while enlarging the V-pits 220. For example, the V-pit enlargement layer 160 may have a higher average lattice parameter than the V-pit creation layer 150, so that compressive stress and strain are continuously generated during growth of the V-pit enlargement layer 160. Accordingly, the size of the V-pits 220 can be increased together with growth of the V-pit enlargement layer 160. In this exemplary embodiment, the V-pit enlargement layer 160 may include, for example, indium (In).

[85] The V-pit enlargement layer 160 includes first nitride layers 161 and second nitride layers 163 having smaller band-gap energy than the first nitride layers 161. Each of the first nitride layers 161 and the second nitride layers 163 has a thickness of about dozens of nanometers. Furthermore, the first nitride layers 161 and the second nitride layers 163 may be repeatedly stacked one above another in two cycles or more to form a superlattice structure. For example, the first nitride layers 161 may be represented by $\text{In}_x\text{Ga}_{(1-x)}\text{N}$ ($0 < x < 1$) and the second nitride layer 163 may be represented by $\text{In}_y\text{Ga}_{(1-y)}\text{N}$ ($0 < y < 1$, $x < y$), without being limited thereto. The V-pit enlargement layer 160 is formed in the superlattice structure, thereby improving crystallinity of the active layer 170 while enlarging the V-pits 220. Furthermore, upon operation of the light emitting device, the superlattice structure of the V-pit enlargement layer 160 can facilitate injection of electrons into the active layer 170.

[86] The light emitting device according to this exemplary embodiment includes the n-type doped region 310 overlapping at least part of the V-pit enlargement layer 160. Next, the n-type doped region 310 will be described in more detail with reference to Figure 4, Figure 5 and Figure 7a to Figure 7e. Figure 7a to Figure 7e are graphs depicting band-gap energy of V-pit enlargement layers and n-type doped regions according to exemplary embodiments of the present disclosure.

[87] The n-type doped region 310 may be a region including Ge as a dopant, and thus semiconductor layers thereof exhibit n-type conductivity. When the nitride semiconductor includes the n-type doped region 310, three-dimensional growth of the nitride semiconductor is predominantly carried out such that vertical growth of the nitride semiconductor is predominant to lateral growth of the nitride semiconductor. That is, when Ge is doped into the nitride semiconductor during growth of the nitride

semiconductor, a possibility that a bond between Ge and N is broken is increased due to relatively low bonding energy between Ge and N. Accordingly, when Ge is doped into the nitride semiconductor during growth of the nitride semiconductor, three-dimensional growth of the nitride semiconductor becomes predominant to two-dimensional growth thereof.

- [88] As described above, the V-pits 220 are more enlarged through three-dimensional growth of the nitride semiconductor than through two-dimensional growth thereof. Thus, as three-dimensional growth becomes predominant by forming the n-type doped region 310 that overlaps at least part of the V-pit enlargement layer 160, the size of the V-pits 220 can be further increased during growth of the V-pit enlargement layer 160. Particularly, although the composition ratio of In can be increased in order to enlarge the V-pits 220, there is a limit in increase of the composition ratio of In in the V-pit enlargement layer 160 in consideration of a difference in lattice parameter between the n-type doped region and other semiconductor layers grown by a subsequent process. Therefore, by forming the n-type doped region 310 to overlap at least part of the V-pit enlargement layer 160, it is possible to increase the size of the V-pits 220 without increasing the composition ratio of In.
- [89] Although enlargement of the V-pits 220 can be achieved using Si as a dopant, Si can deteriorate not only crystallinity of the V-pit enlargement layer 160 but also crystallinity of the active layer 170. On the contrary, the n-type doped region 310 including Ge as a dopant causes less deterioration in crystallinity of the semiconductor layer than the doped region including Si alone as a dopant. In addition, Ge used as a dopant can permit more enlargement of the V-pits 220 than Si used as a dopant. This is generally similar to the aforementioned effect.
- [90] Although the doping concentration of the n-type doped region 310 is not particularly limited, the n-type doped region 310 may have a doping concentration of 5×10^{19} atoms/cm³ or more to promote three-dimensional growth, thereby further improving enlargement of the V-pits 220. Further, although the thickness of the n-type doped region 310 is not particularly limited, the n-type doped region 310 having an excessively thin thickness provides an insignificant effect in enlargement of the V-pits 220, and the n-type doped region having an excessively thick thickness can deteriorate crystallinity within the n-type doped region 310, thereby deteriorating luminous efficacy of the light emitting device. Accordingly, it is desirable that the thickness of the n-type doped region 310 be determined within a predetermined range, and for example, the n-type doped region 310 may have a thickness of about 10 nm to 100 nm. However, it should be understood that the present disclosure is not limited thereto.
- [91] Furthermore, the n-type doped region 310 may be formed to overlap at least part of the V-pit enlargement layer 160 such that the V-pit enlargement layer 160 formed at a

lower end of the active layer 170 can also act as an electron injection layer. Thus, the size of the V-pits 220 can be increased through the V-pit enlargement layer 160 without forming a separate electron injection layer, while improving luminous efficacy through improvement in efficiency of electron injection into the active layer 170.

- [92] Referring to Figure 4 and Figure 5, the n-type doped region 310 may overlap at least part of the V-pit enlargement layer 160 and may be disposed over at least two layers within the V-pit enlargement layer 160. Thus, at least one of interfaces between the first nitride layers 161 and the second nitride layers 163 may be disposed within the n-type doped region 310. Further, the n-type doped region 310 may be disposed independently of the layers within the V-pit enlargement layer 160. In other words, when the n-type doped region 310 has an upper surface and a lower surface, locations of the upper surface and/or the lower surface of the n-type doped region 310 may not correspond to the locations of the interfaces between the first nitride layers 161 and the second nitride layers 163.
- [93] Further, each n-type doped region 310 may have various doping concentrations, for example, a constant doping concentration, a gradually increasing or decreasing doping concentration in the thickness direction thereof, or a modulated doping concentration in which the doping concentration repeatedly increases and decreases.
- [94] Furthermore, the light emitting device may include a plurality of n-type doped regions 310, which may have different doping concentrations. At this point, the doping concentrations of the plural n-type doped regions 310 may gradually decrease with increasing distance from the n-type nitride semiconductor layer 140
- [95] Next, referring to Figure 4, Figure 5 and Figure 7a to Figure 7e, examples of the n-type doped region 310 according to various embodiments of the present disclosure will be described. Here, it should be understood that the present disclosure is not limited thereto.
- [96] First, as shown in Figure 4, Figure 5 and Figure 7a, the n-type doped region 310 may be disposed over two layers to twenty layers within the V-pit enlargement layer 160, and, for example, the n-type doped region 310 may be disposed over three first nitride layers 161 and two second nitride layers 163. Further, the upper surface and the lower surface of the n-type doped region 310 may not overlap interfaces between the first nitride layers 161 and the second nitride layers 163. As shown in the drawings, the lower surface of the n-type doped region 310 may be disposed at the middle of one first nitride layer 161 and the upper surface of the n-type doped region 310 may be disposed at the middle of another first nitride layer 161. In addition, the n-type doped region 310 may be formed in plural within the V-pit enlargement layer 160.
- [97] In another exemplary embodiment, as shown in Figure 7b, one of the upper and lower surfaces of the n-type doped region 310 may be disposed corresponding to an

interface between the first nitride layer 161 and the second nitride layer 163. For example, the lower surface of the n-type doped region 310 may overlap a lower surface of one first nitride layer 161. This structure can be obtained by introducing a Ge dopant source into the growth chamber in the course of growing the corresponding first nitride layer 161.

- [98] In a further exemplary embodiment, as shown in Figure 7c, both the upper and lower surfaces of the n-type doped region 310 may be disposed corresponding to the interfaces between the first nitride layers 161 and the second nitride layers 163. For example, the lower surface of the n-type doped region 310 may overlap a lower surface of one first nitride layer 161 and the upper surface of the n-type doped region 310 may overlap an upper surface of another first nitride layer 161. In this exemplary embodiment, the n-type doped region 310 is also formed independently of the first nitride layers 161 and the second nitride layers 163 instead of having a relationship therewith.
- [99] In yet another exemplary embodiment, as shown in Figure 7d, the doping concentration may differ in one n-type doped region 310. For example, Ge dopants may be included in one n-type doped region 310 through modulation doping. Modulation doping of the Ge dopants can relieve deterioration of crystallinity of the V-pit enlargement layer 160 by the n-type doped region 310. As a result, the active layer 170 formed on the V-pit enlargement layer 160 can have further improved crystallinity.
- [100] In some exemplary embodiments, as shown in Figure 7e, the light emitting device may include a plurality of n-type doped regions 311, 312. For example, the n-type doped region 310 may include a first n-type doped region 311 and a second n-type doped region 312. The first n-type doped region 311 may have a higher Ge doping concentration than the second n-type doped region 312. In these embodiments, the first n-type doped region 311 may be closer to the V-pit creation layer 150 than the second n-type doped region 312. By the first n-type doped region 311 disposed relatively close to the V-pit creation layer 150, the V-pits 210 can be enlarged. Further, the second n-type doped region 312 has a lower Ge doping concentration than the first n-type doped region, thereby relieving deterioration in crystallinity of the V-pit enlargement layer 160 while further enlarging the V-pits 210.
- [101] Exemplary embodiments obtained through combination of technical features described in the above exemplary embodiments are also within the scope of the present disclosure.
- [102] According to exemplary embodiments of the present disclosure, the n-type doped region 310 may be disposed to overlap the V-pit enlargement layer 160 and the active layer 170. As shown in Figure 6 and Figure 8, some of the n-type doped region 310 may overlap the V-pit enlargement layer 160, and the other portion thereof may be disposed to overlap the active layer 170. Furthermore, when the light emitting device

includes a plurality of n-type doped regions 310, one of the plural n-type doped regions 310 may be disposed to overlap the V-pit enlargement layer 160, another n-type doped region 310 may be disposed to overlap the active layer 170, and a third n-type doped region 310 may be disposed over the V-pit enlargement layer 160 and the active layer 170. In this way, the n-type doped region 310 may be disposed in various ways.

[103] According to the exemplary embodiments, the light emitting device further includes the V-pit enlargement layer 160, so that the size of the V-pits 220 can be further increased, thereby improving electrical reliability of the light emitting device. Furthermore, the n-type doped region 310 overlaps the V-pit enlargement layer 160 such that the V-pit enlargement layer 160 also acts as the electron injection layer, thereby improving luminous efficacy of the light emitting device.

[104] Although some exemplary embodiments have been described herein, it should be understood by those skilled in the art that these embodiments are given by way of illustration only, and that various modifications, variations, and alterations can be made without departing from the spirit and scope of the invention.

Claims

- [Claim 1] A light emitting device comprising:
an n-type nitride semiconductor layer;
a V-pit creation layer disposed on the n-type nitride semiconductor layer;
an active layer disposed on the V-pit creation layer;
a p-type nitride semiconductor layer disposed on the active layer;
a V-pit formed through the active layer;
a high resistance embedment layer at least partially filling the V-pit;
and
an n-type doped region overlapping at least part of the active layer,
wherein:
the active layer includes a multi-quantum well structure including pluralities of barrier layers and well layers;
at least one of interfaces between the barrier layers and the well layers is disposed within the n-type doped region; and
the n-type doped region includes a lower surface and an upper surface, and at least one of the upper and lower surfaces of the n-type doped region does not overlap the interfaces between the barrier layers and the well layers.
- [Claim 2] The light emitting device of claim 1, wherein the n-type doped region includes Ge as a dopant and has a thickness of 10 nm to 100 nm.
- [Claim 3] The light emitting device of claim 1, wherein the n-type doped region has a greater thickness than at least one of the barrier layers and the well layers, and at least one of the barrier layers and the well layers is disposed within the n-type doped region.
- [Claim 4] The light emitting device of claim 1, wherein the n-type doped region includes a region modulation-doped with an n-type dopant.
- [Claim 5] The light emitting device of claim 1, wherein the n-type doped region includes a first doped region and a second doped region having a lower doping concentration than the first doped region, and the first doped region is disposed to be closer to the V-pit creation layer than the second doped region.
- [Claim 6] The light emitting device of claim 1, further including:
a V-pit enlargement layer interposed between the active layer and the V-pit creation layer,
wherein the n-type doped region is disposed over the active layer and

- the V-pit creation layer.
- [Claim 7] The light emitting device of claim 6, wherein the V-pit creation layer includes a superlattice layer, and at least one of interfaces between layers within the superlattice layer is disposed within the n-type doped region.
- [Claim 8] A light emitting device comprising:
an n-type nitride semiconductor layer;
a V-pit creation layer disposed on the n-type nitride semiconductor layer;
an active layer disposed on the V-pit creation layer and including a well layer and a barrier layer;
a p-type nitride semiconductor layer disposed on the active layer;
a V-pit formed through the active layer and the V-pit enlargement layer;
a high resistance embedment layer at least partially filling the V-pit;
and
an n-type doped region overlapping at least part of the active layer, wherein at least one of upper and lower surfaces of the n-type doped region corresponds to an interface between the well layer and the barrier layer, and a thickness of the n-type doped region is equal to integer times the thickness of barrier layer or the well layer.
- [Claim 9] The light emitting device of claim 8, further including:
a V-pit enlargement layer disposed on the V-pit creation layer, wherein the V-pit enlargement layer includes a superlattice layer in which first nitride layers and second nitride layers having different band-gap energies are alternately stacked one above another, and at least one of interfaces between the first and second nitride layers is disposed within the n-type doped region.
- [Claim 10] The light emitting device of claim 8, wherein the n-type doped region has an average Ge doping concentration of 5×10^{19} atoms/cm³ or more.
- [Claim 11] The light emitting device of claim 8, wherein the n-type doped region has a thickness of 10 nm to 100 nm.
- [Claim 12] The light emitting device of claim 11, wherein the n-type doped region has a greater thickness than at least one of the first nitride layers and the second nitride layers.
- [Claim 13] The light emitting device of claim 8, wherein the n-type doped region includes a region modulation-doped with Ge dopants.
- [Claim 14] The light emitting device of claim 9, wherein the n-type doped region

includes at least one first nitride layer and at least one second nitride layer disposed therein.

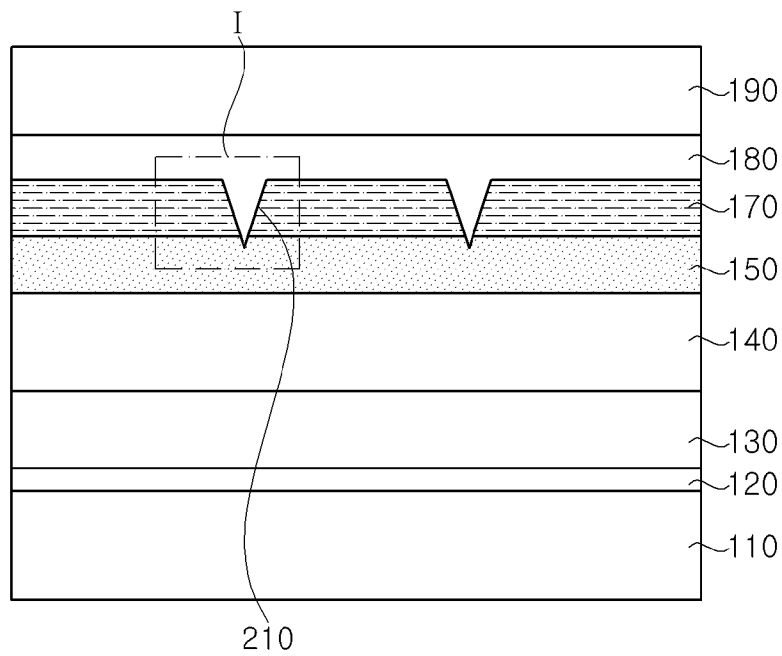
[Claim 15]

The light emitting device of claim 8, wherein the n-type doped region includes a first doped region and a second doped region having a lower doping concentration than the first doped region, the first doped region being closer to the V-pit creation layer than the second doped region.

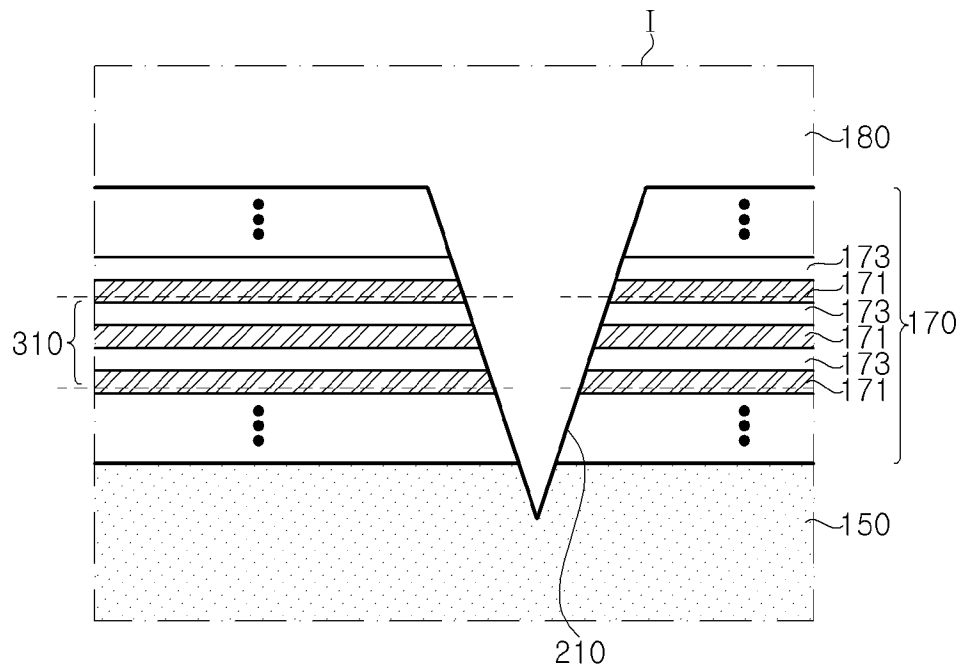
[Claim 16]

The light emitting device of claim 8, wherein the n-type doped region is disposed over the active layer and the V-pit creation layer.

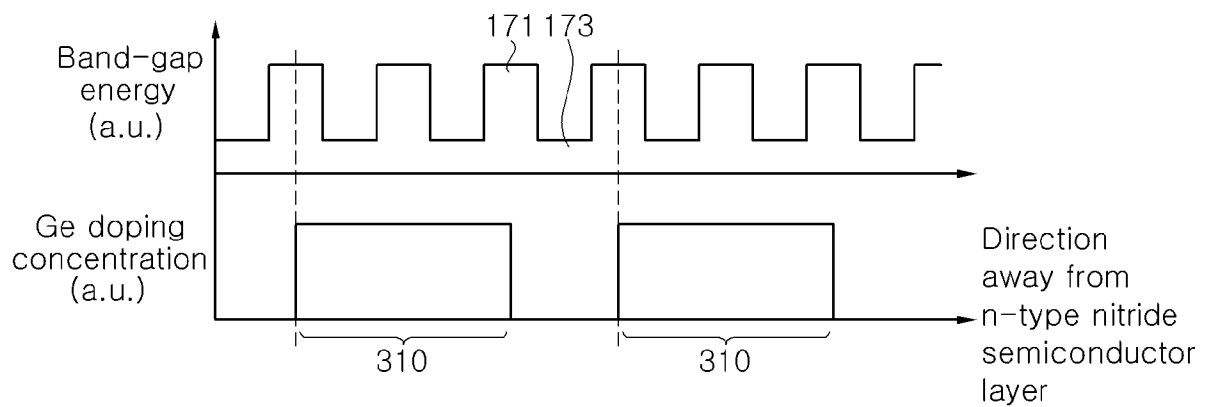
[Fig. 1]



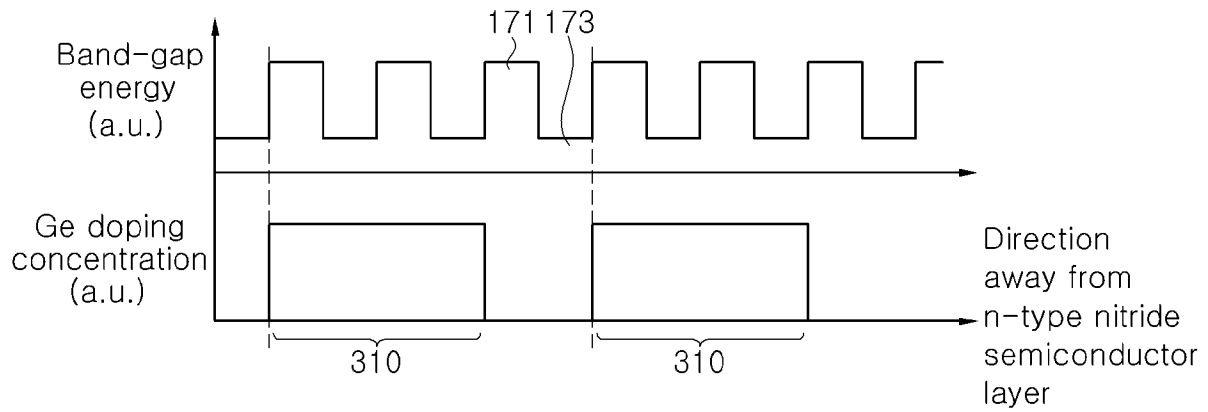
[Fig. 2]



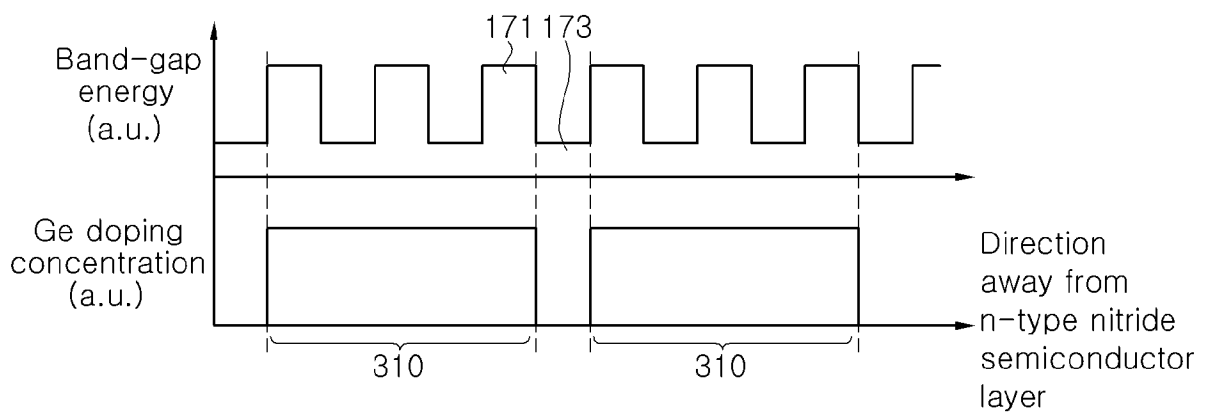
[Fig. 3a]



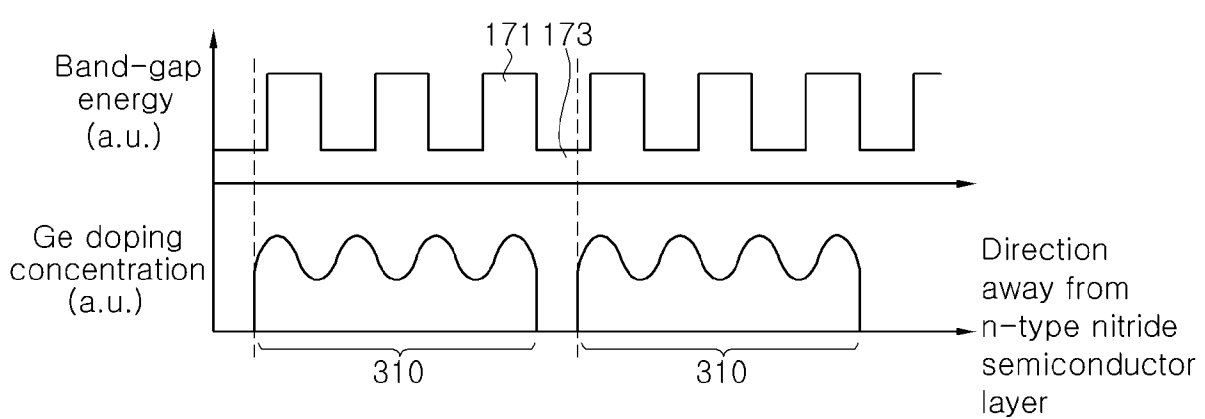
[Fig. 3b]



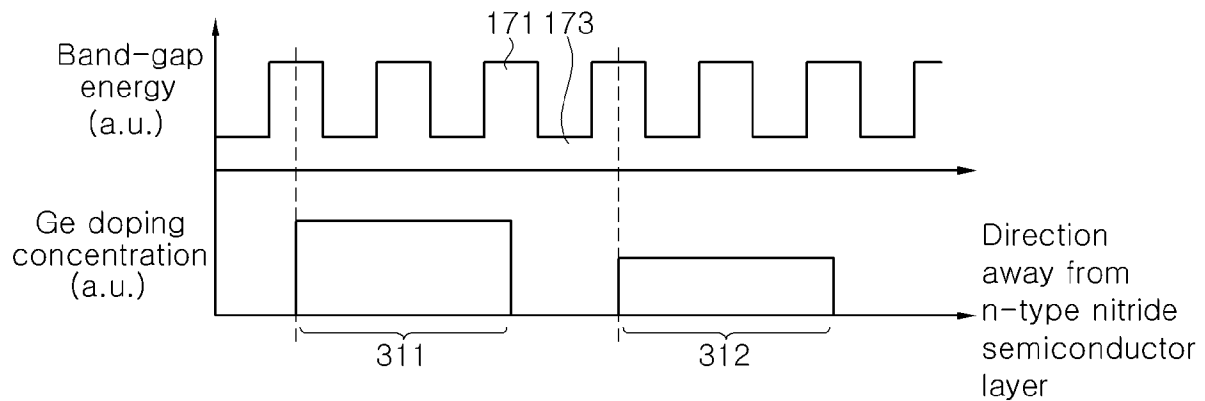
[Fig. 3c]



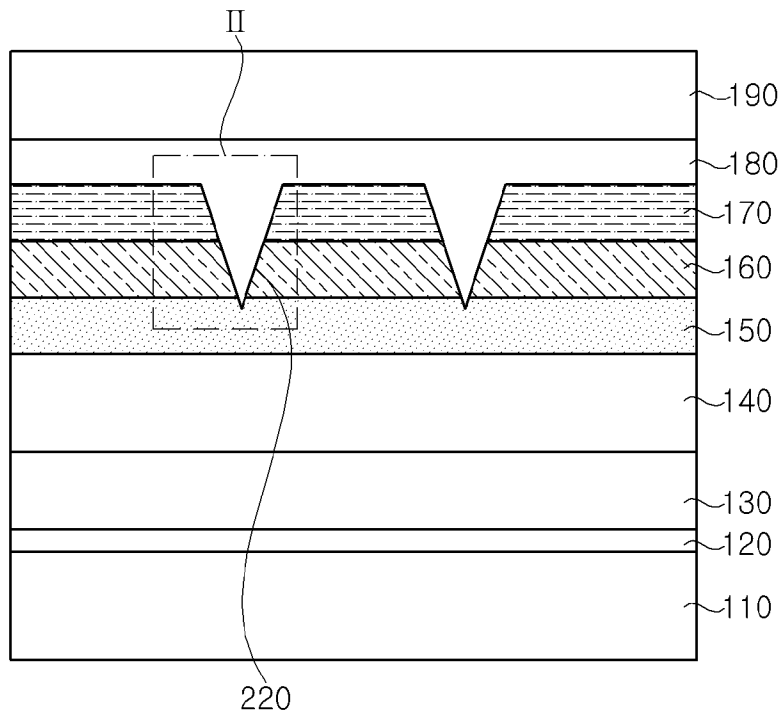
[Fig. 3d]



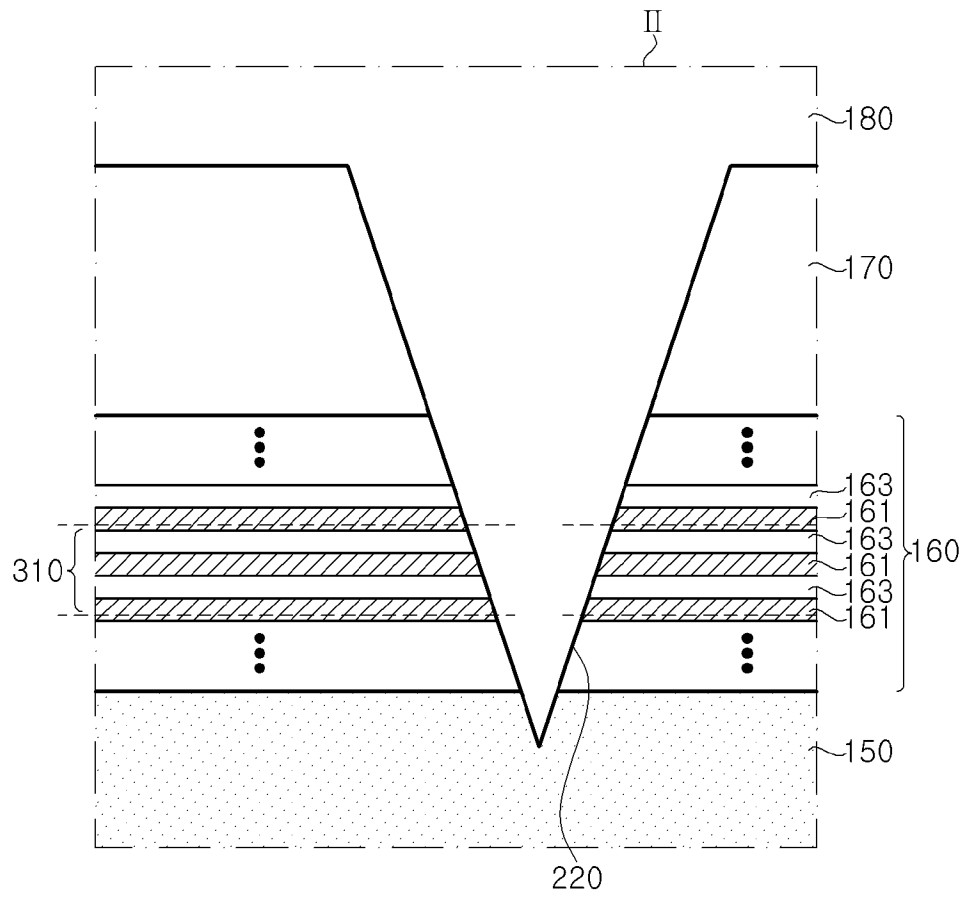
[Fig. 3e]



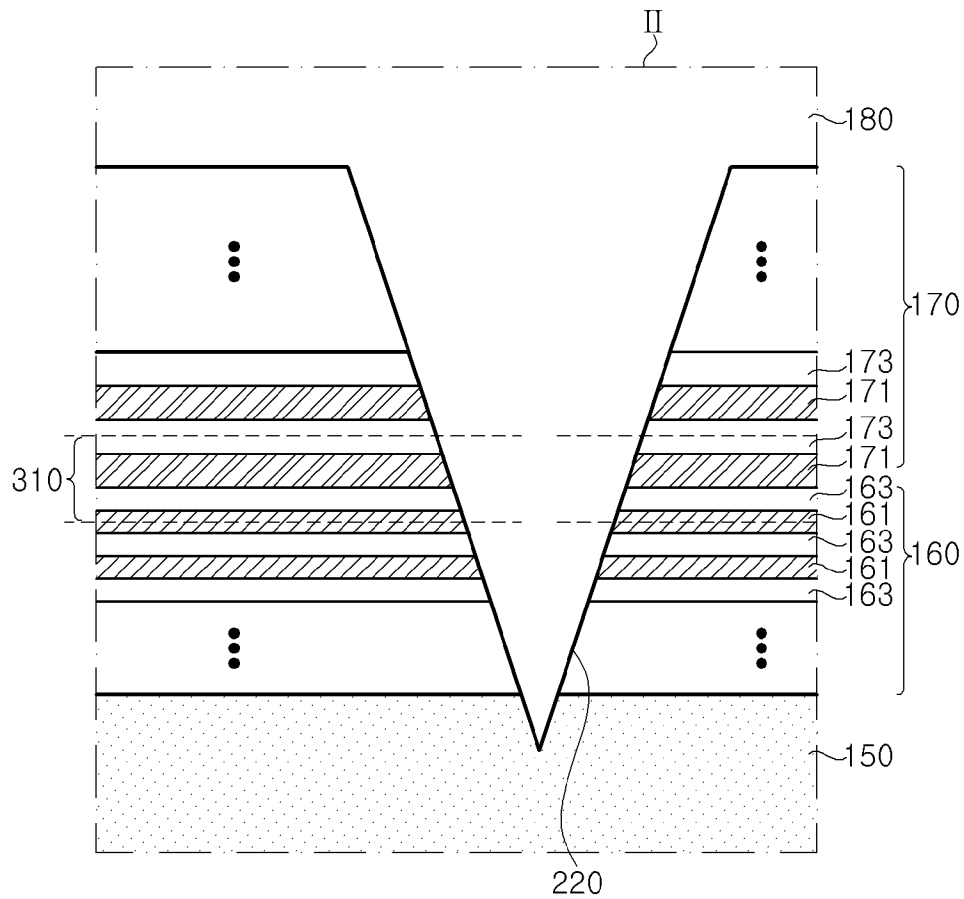
[Fig. 4]



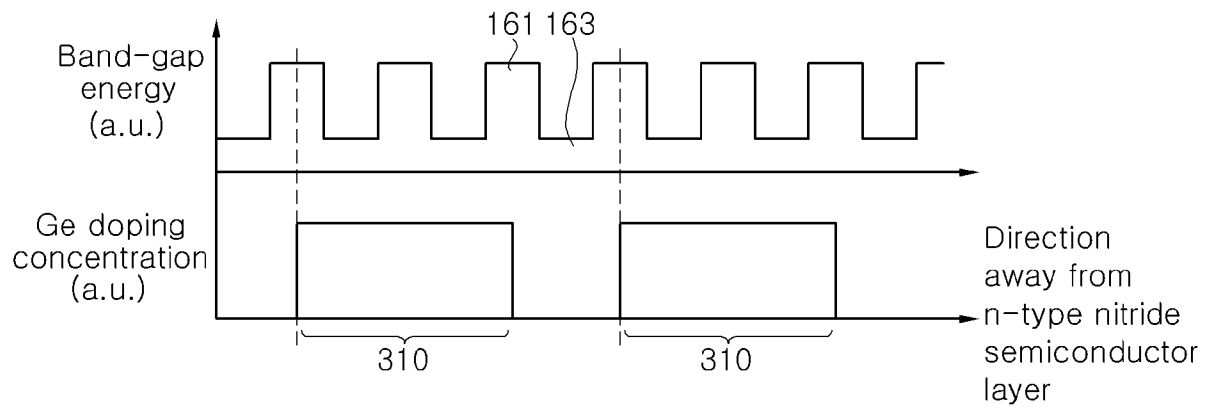
[Fig. 5]



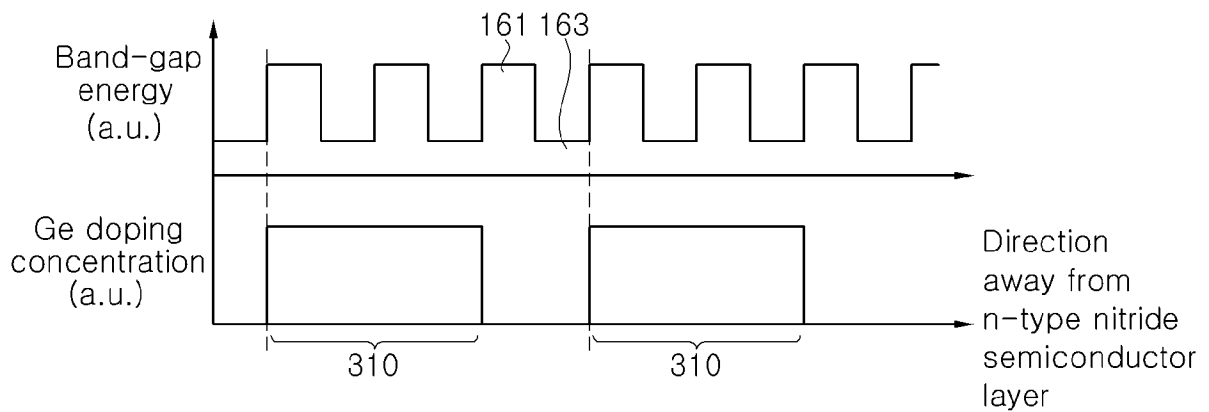
[Fig. 6]



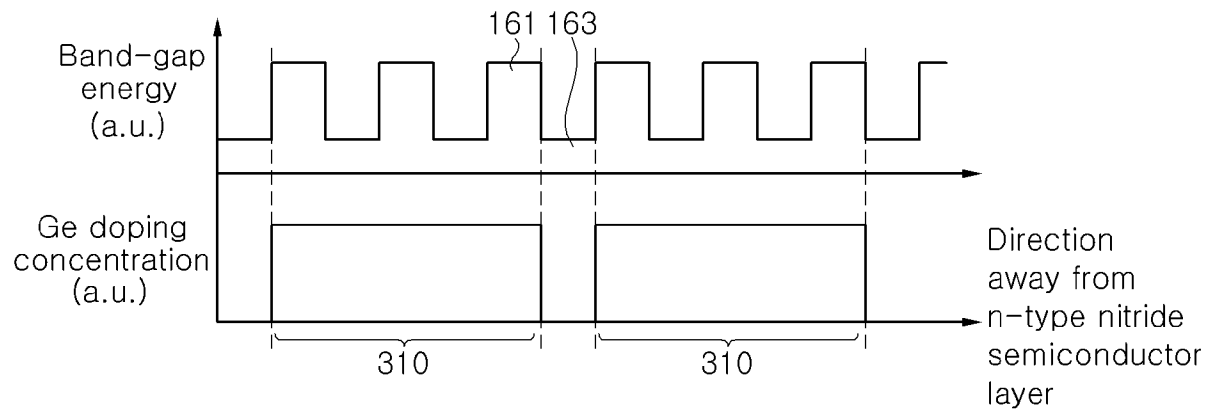
[Fig. 7a]



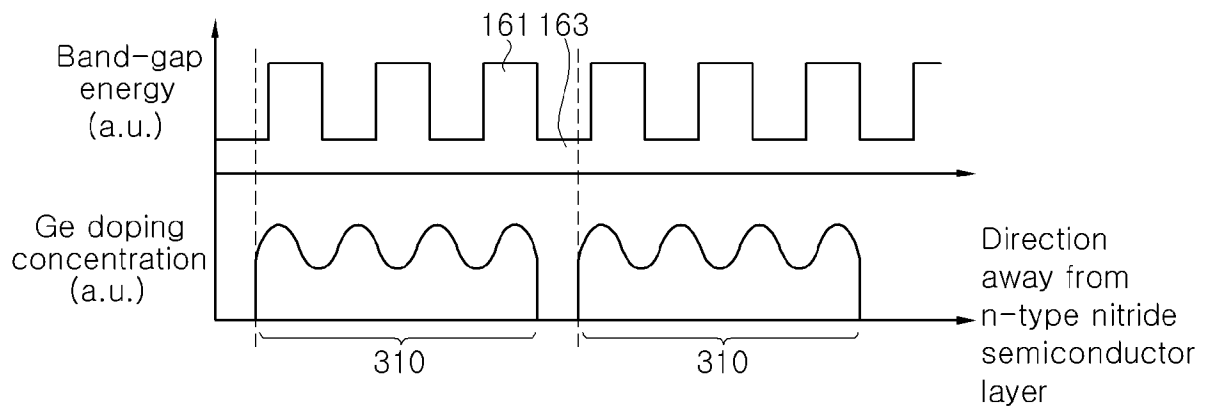
[Fig. 7b]



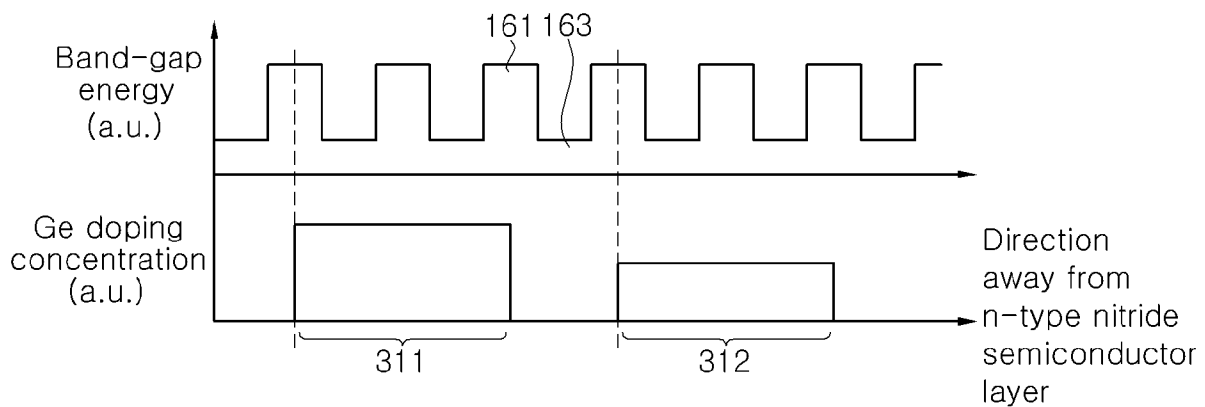
[Fig. 7c]



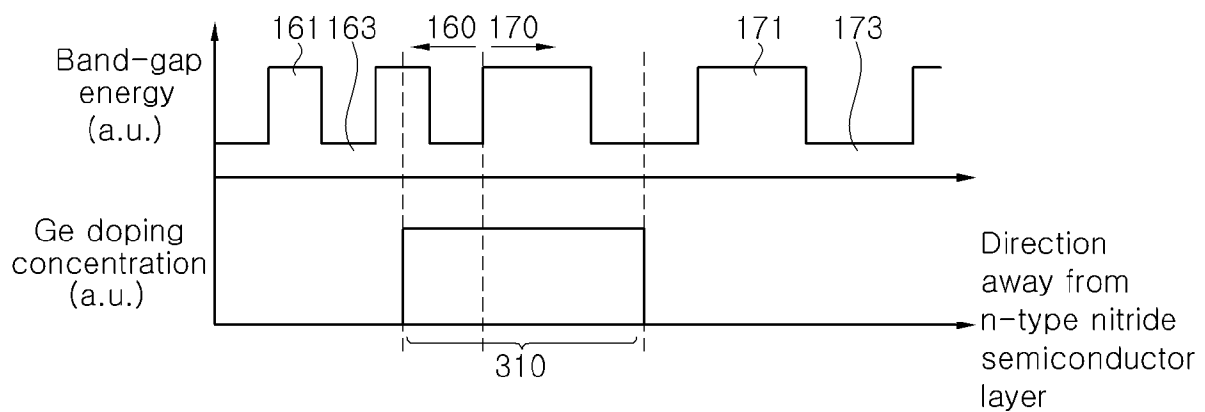
[Fig. 7d]



[Fig. 7e]



[Fig. 8]



A. CLASSIFICATION OF SUBJECT MATTER**H01L 33/22(2010.01)i, H01L 33/06(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/22; H01L 33/20; H01L 33/30; H01L 33/32; H01L 33/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: current spreading, LED, n-type doped layer, V-pit, active layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-1026031 B1 (SAMSUNG LED CO., LTD.) 30 March 2011 See abstract, paragraphs 22-27, claims 1-8 and figures 2-3.	1-16
A	JP 2013-041930 A (SHARP CORP.) 28 February 2013 See paragraphs 41-42, claims 1-2 and figure 1.	1-16
A	KR 10-2012-0095652 A (SAMSUNG ELECTRONICS CO., LTD.) 29 August 2012 See abstract, paragraphs 22-27, claim 1 and figure 1.	1-16
A	US 2013-0082273 A1 (STEVE TING) 04 April 2013 See abstract, paragraphs 36-72, claim 1 and figures 1-4.	1-16
A	KR 10-2006-0019043 A (LG INNOTEK CO., LTD.) 03 March 2006 See abstract, paragraphs 60-67 and figures 5-6.	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 February 2016 (26.02.2016)

Date of mailing of the international search report

26 February 2016 (26.02.2016)

Name and mailing address of the ISA/KR

International Application Division

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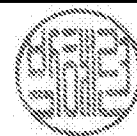
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-1026031 B1	30/03/2011	KR 10-2010-0054590 A	25/05/2010
JP 2013-041930 A	28/02/2013	CN 102956769 A	06/03/2013
		TW 201314947 A	01/04/2013
		TW I479683 B	01/04/2015
		US 2013-0037779 A1	14/02/2013
		US 8816321 B2	26/08/2014
KR 10-2012-0095652 A	29/08/2012	None	
US 2013-0082273 A1	04/04/2013	CN 103460409 A	18/12/2013
		JP 2014-518014 A	24/07/2014
		KR 10-2014-0010064 A	23/01/2014
		TW 201330315 A	16/07/2013
		US 2014-0106493 A1	17/04/2014
		US 2015-0024531 A1	22/01/2015
		US 8698163 B2	15/04/2014
		US 8828752 B2	09/09/2014
		WO 2013-049415 A2	04/04/2013
		WO 2013-049415 A3	11/07/2013
KR 10-2006-0019043 A	03/03/2006	CA 2578443 A1	02/03/2006
		CA 2578443 C	05/08/2014
		CN 101027791 A	29/08/2007
		CN 101027791 B	10/08/2011
		EP 1790017 A1	30/05/2007
		EP 1790017 B1	15/08/2012
		JP 2008-511153 A	10/04/2008
		JP 5048497 B2	17/10/2012
		KR 10-0670531 B1	16/01/2007
		US 2008-0093610 A1	24/04/2008
		US 2010-0320441 A1	23/12/2010
		US 7808010 B2	05/10/2010
		US 8193545 B2	05/06/2012
		WO 2006-022497 A1	02/03/2006