United States Patent

Jamieson

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[54] VARIABLE FREQUENCY SYSTEM

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[73] Assignee: **Lorain Products Corp.**, Lorain, Ohio

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[21] Appl. No.: **33,343**

[52] **U.S. Cl.** ..... **328/44**, 235/92 EV, 328/130

[51] **Int. Cl.** **H03k 21/30**

[58] **Field of Search** ..... 328/39, 41, 42, 44, 129, 186, 328/130; 307/222; 235/92 EV

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[57] **ABSTRACT**

A digital timing system of high precision and stability is provided with a selectively variable frequency and phase by employing a variable frequency dividing circuit that is responsive to a highly accurate precision crystal clock generator. The variable divider includes a fixed modulus counter which in turn triggers a variable modulus counter. High frequency precision clock pulses are fed first to the fixed counter which upon completion of its count, switches the clock pulses to the variable counter. The latter, when it completes its count, provides an output pulse that (a) constitutes one element of the system output, (b) resets the fixed counter, and (c) switches the clock pulses to the fixed counter whereby the above cycle is repeated. To vary the frequency or repetition rate of the described cycle of operation, the magnitude of the count provided by the variable counter is changed to thereby change the total interval or period of a single cycle. To control the phase of the output signal, the count of the fixed counter is changed during but one of its counts. The variable counter is formed of a pair of reversible, up-down counters each of which provides an output upon reaching the count of one when counting down. The frequency of the output is changed by controllably varying the number to which these variable reversible counters count.

27 Claims, 19 Drawing Figures

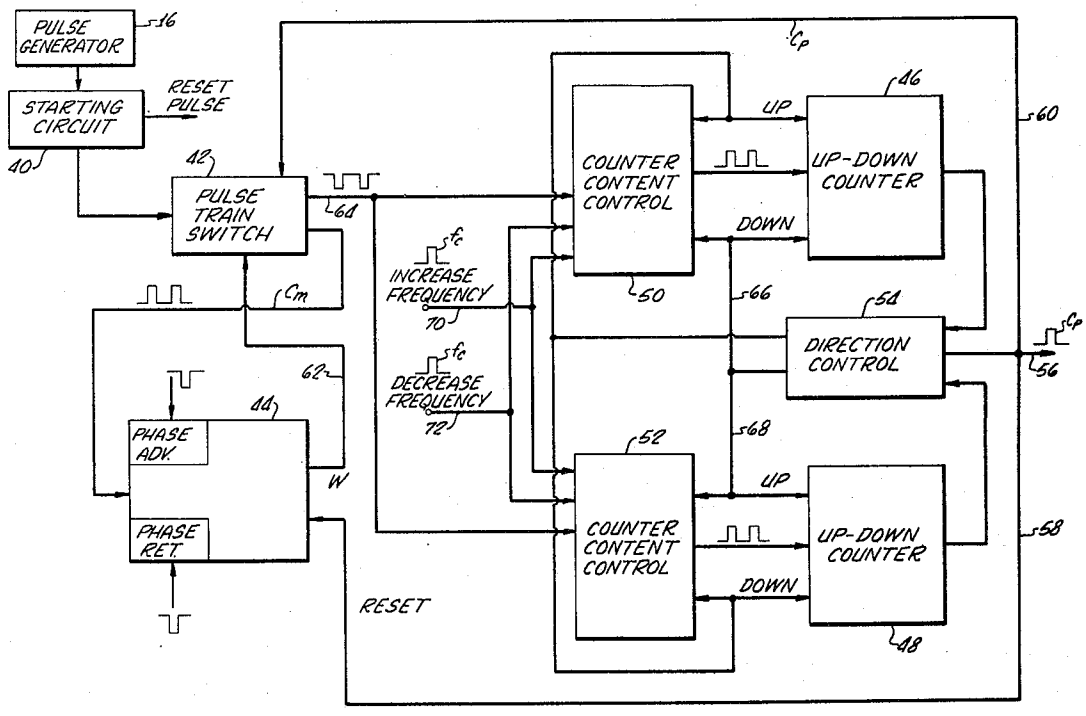
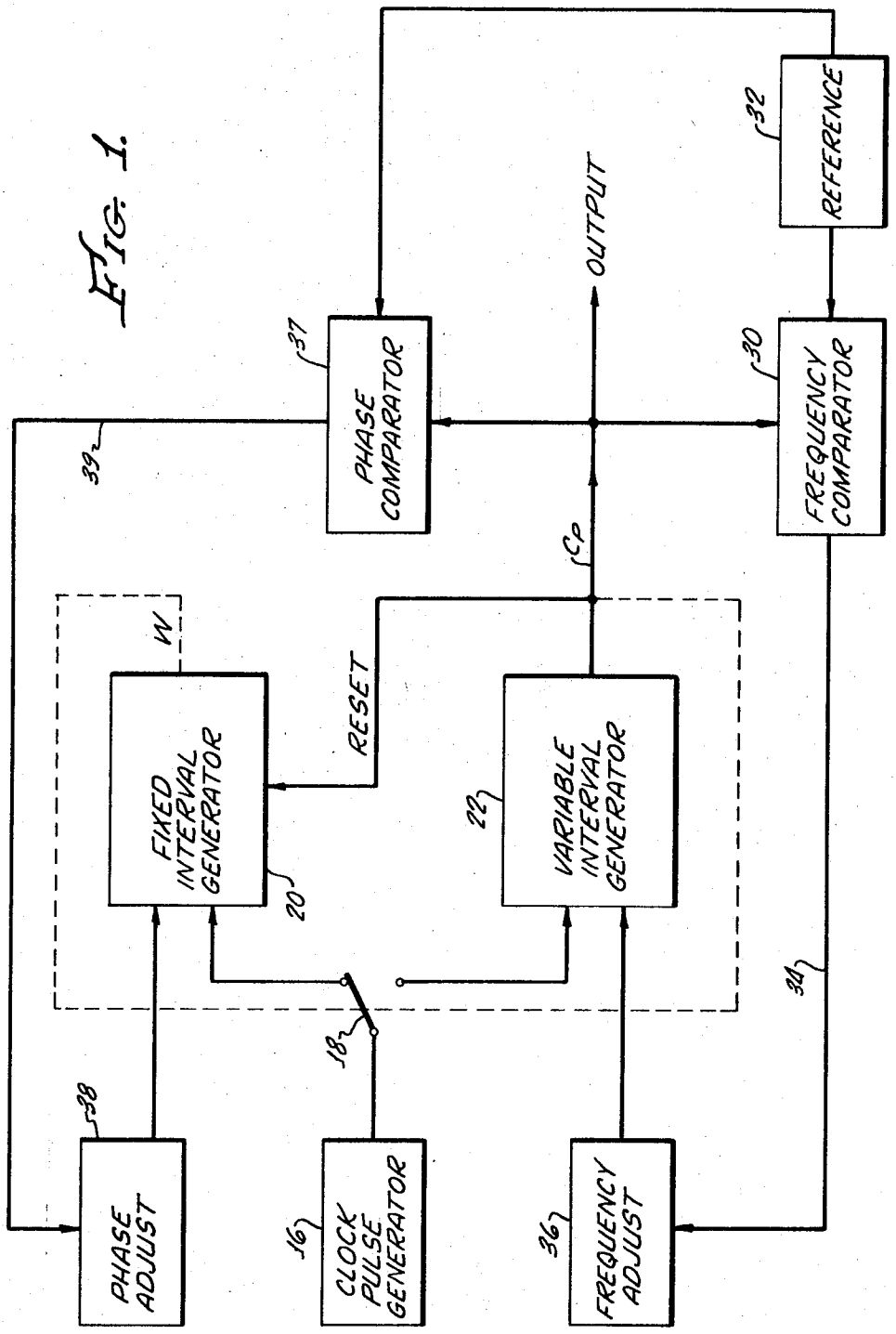


FIG. 1.



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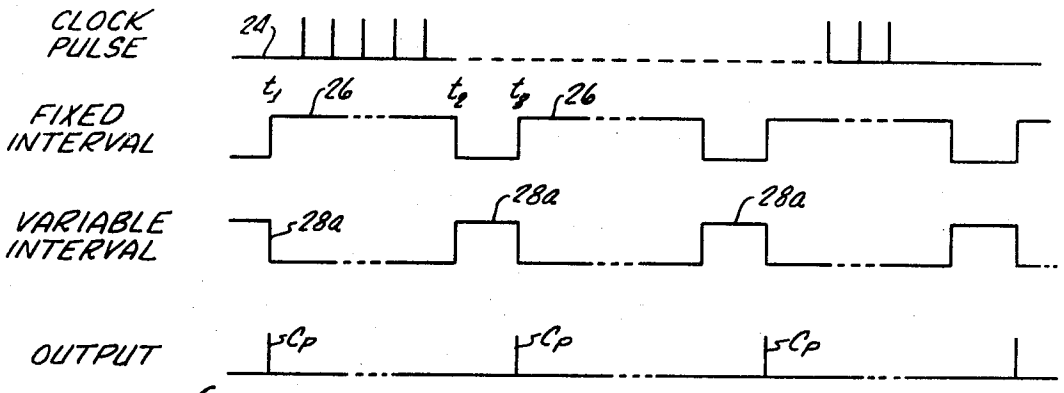

FIG. 2a.

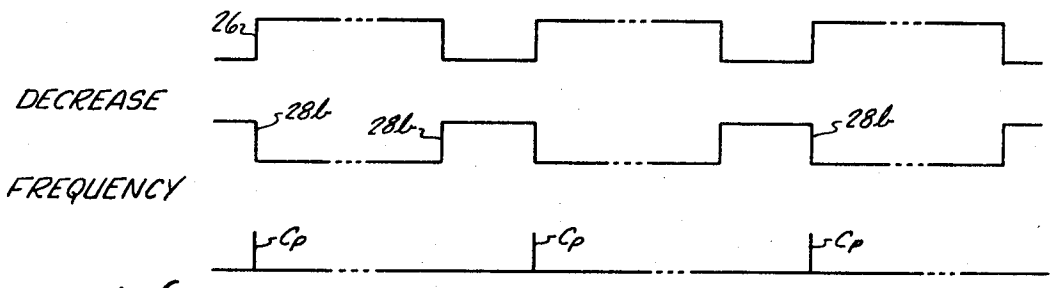

FIG. 2b.

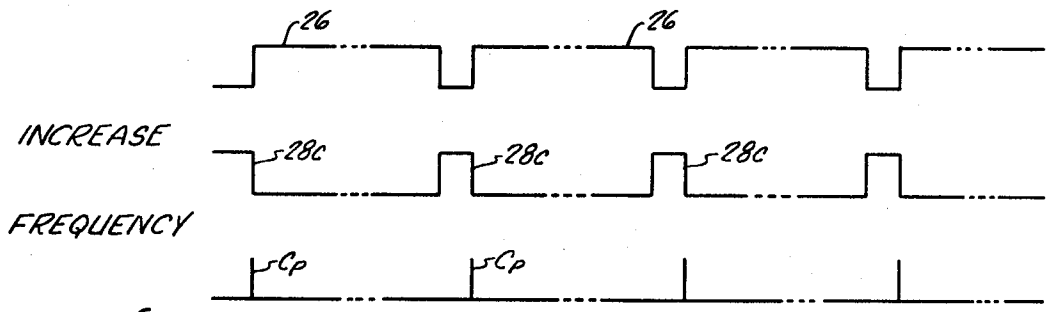

FIG. 2c.

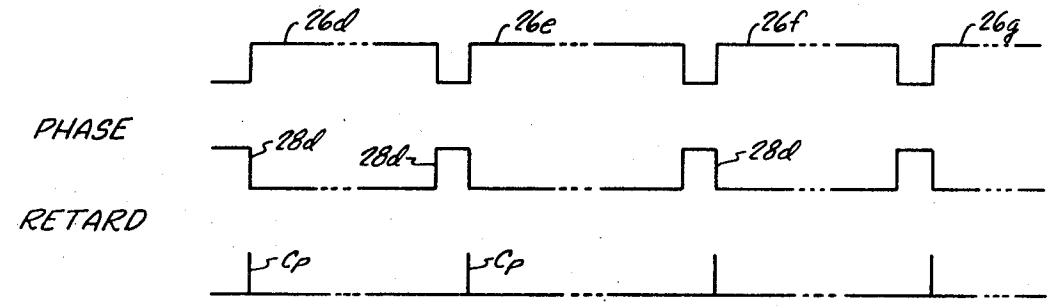

FIG. 2d.

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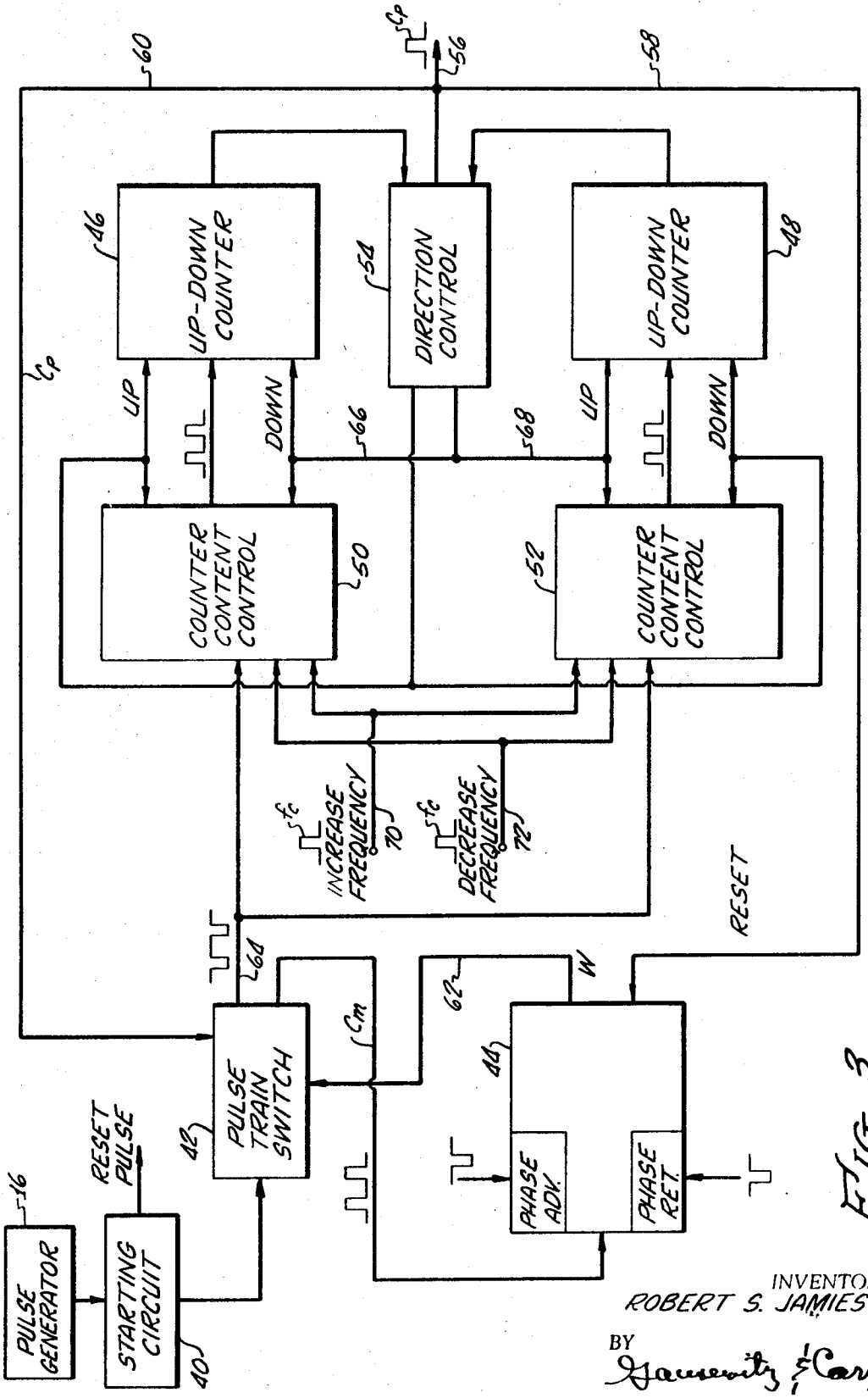

FIG. 3.

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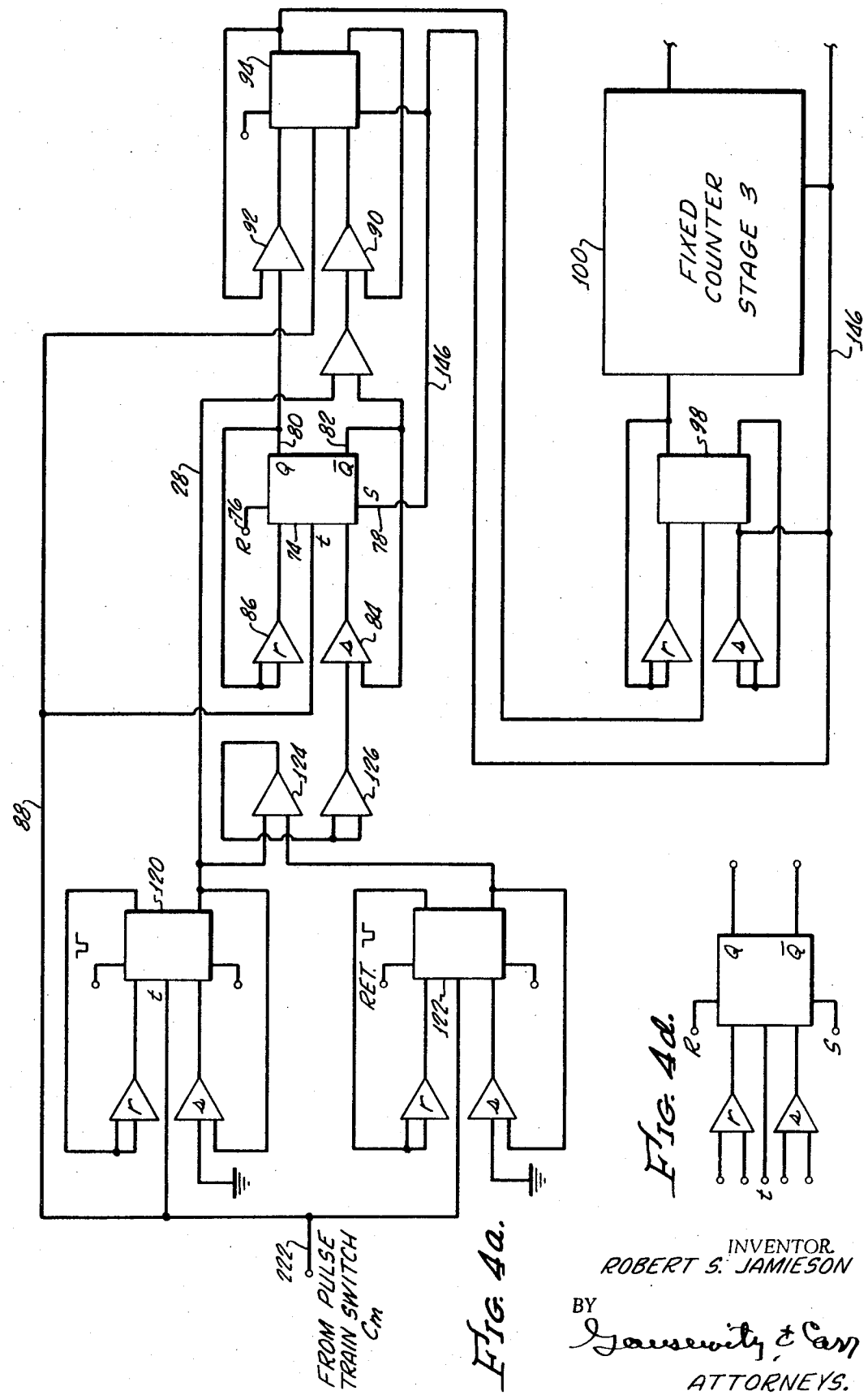

FIG. 4a.

FIG. 4d.

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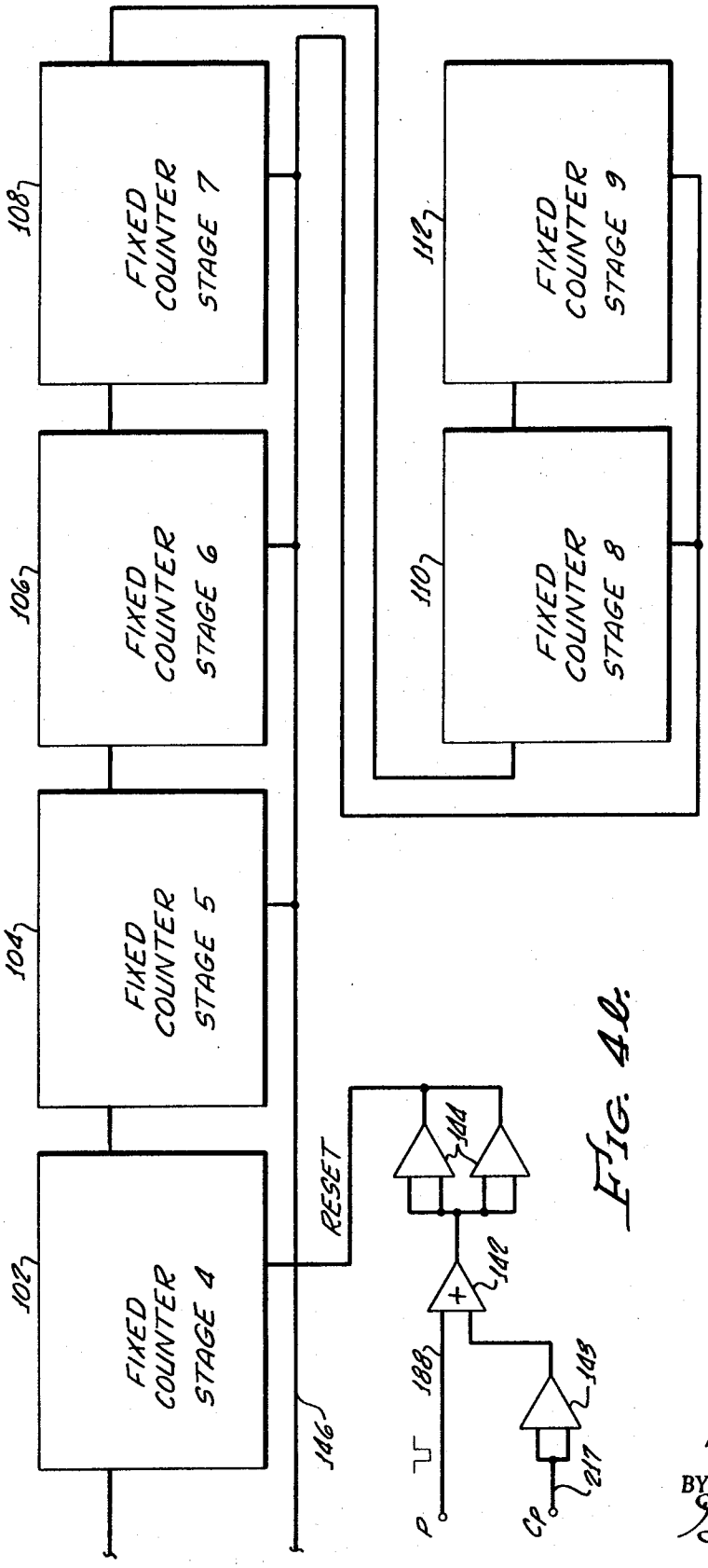

FIG. 4B.

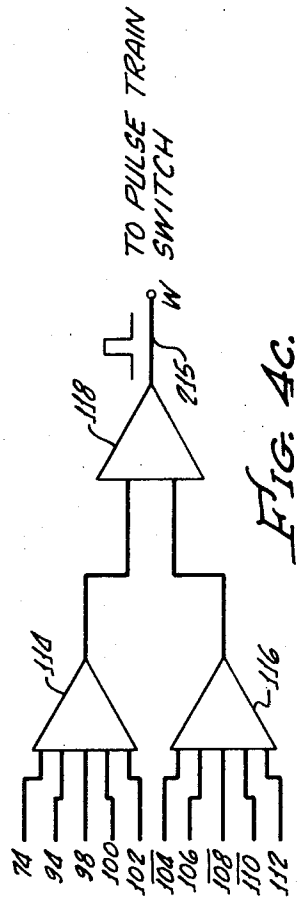

FIG. 4C.

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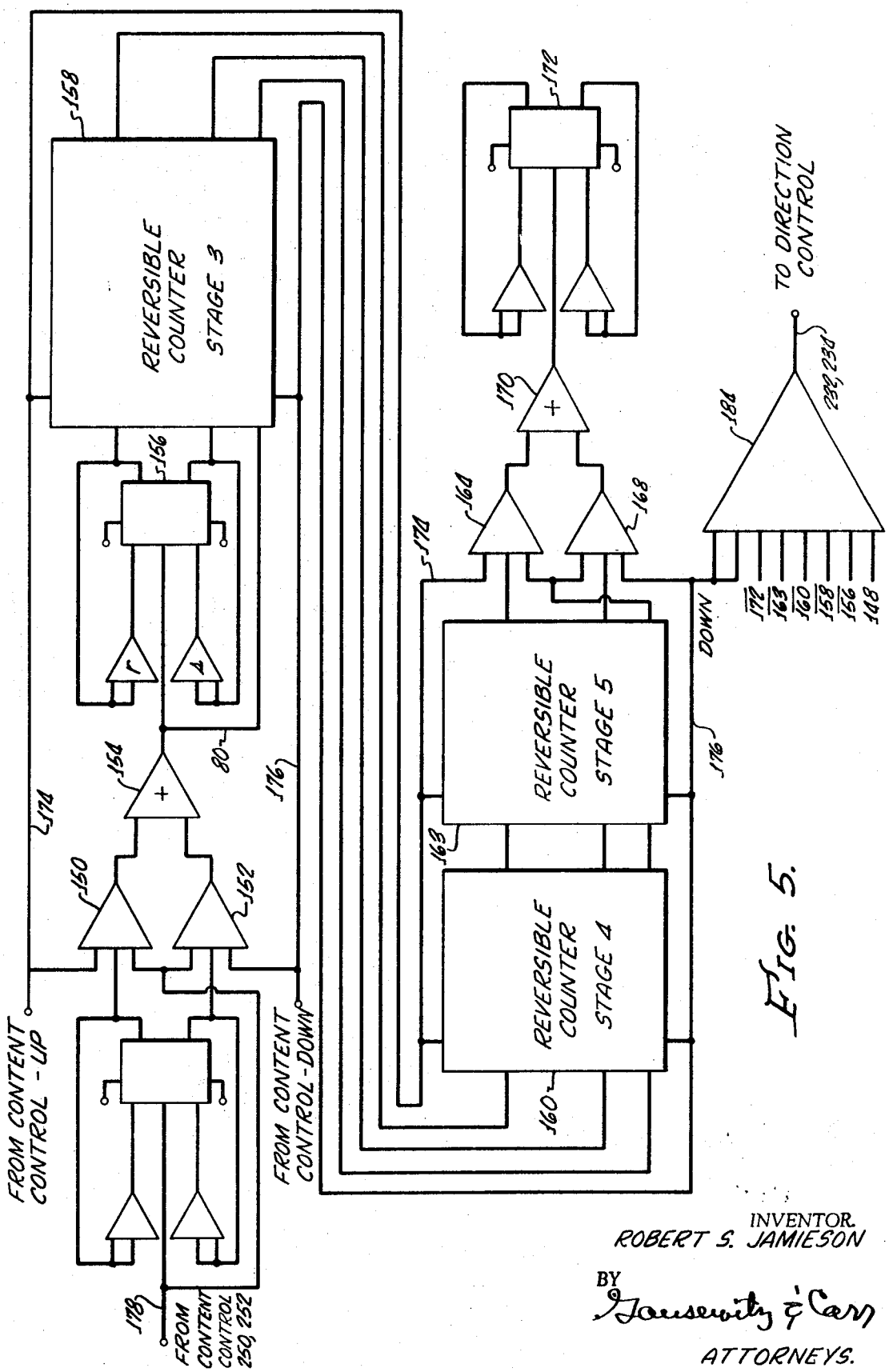

FIG. 5.

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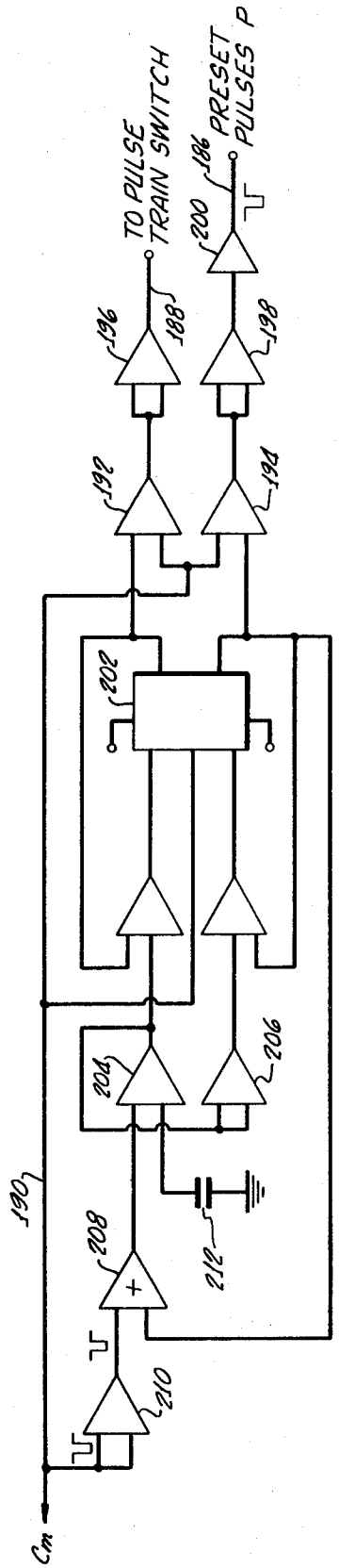

FIG. 6.

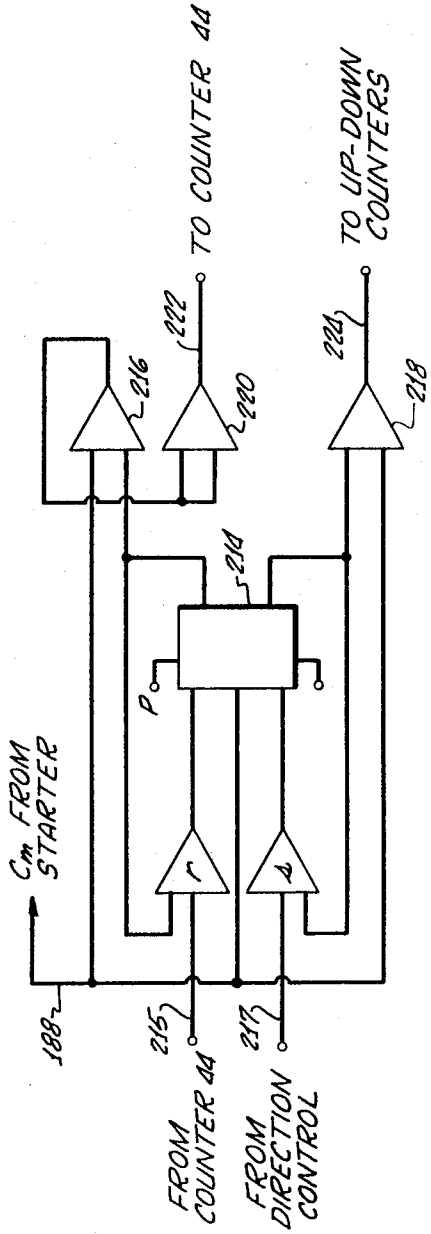

FIG. 7.

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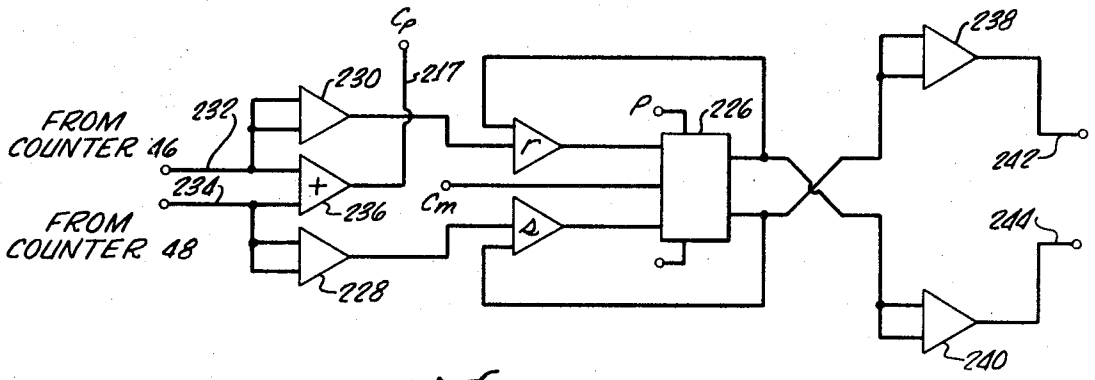

FIG. 8.

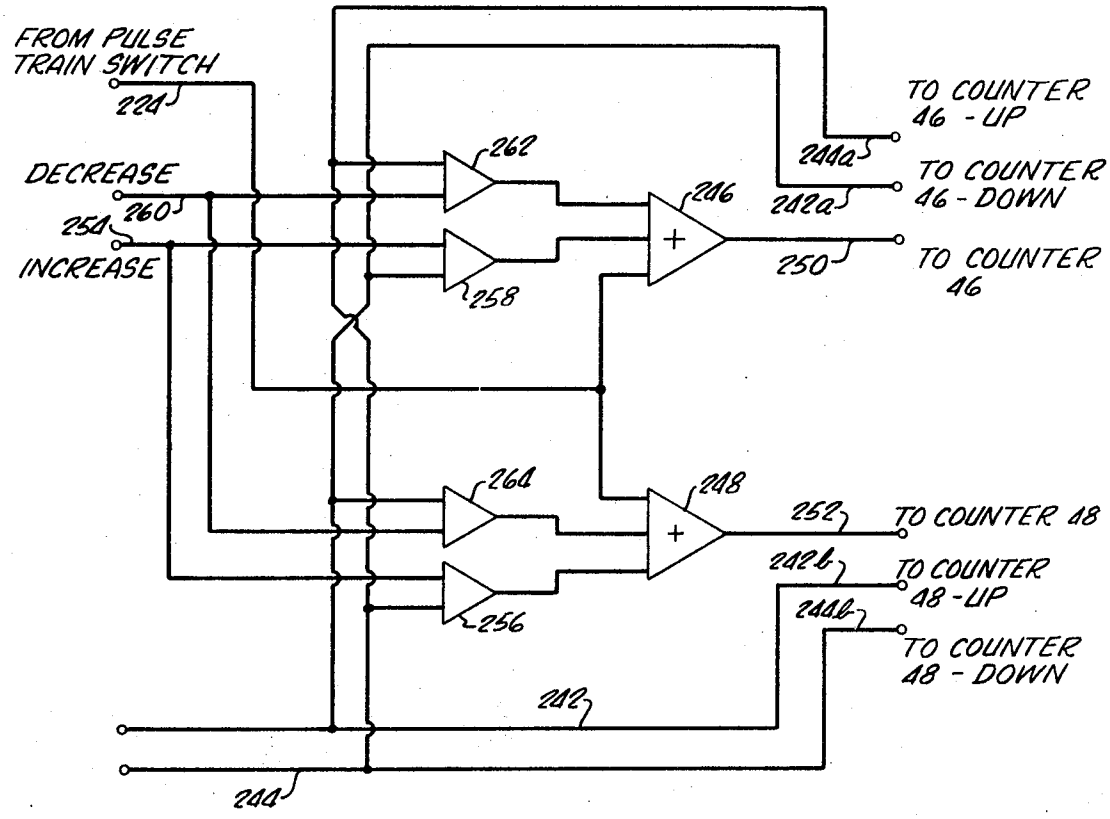

FIG. 9.

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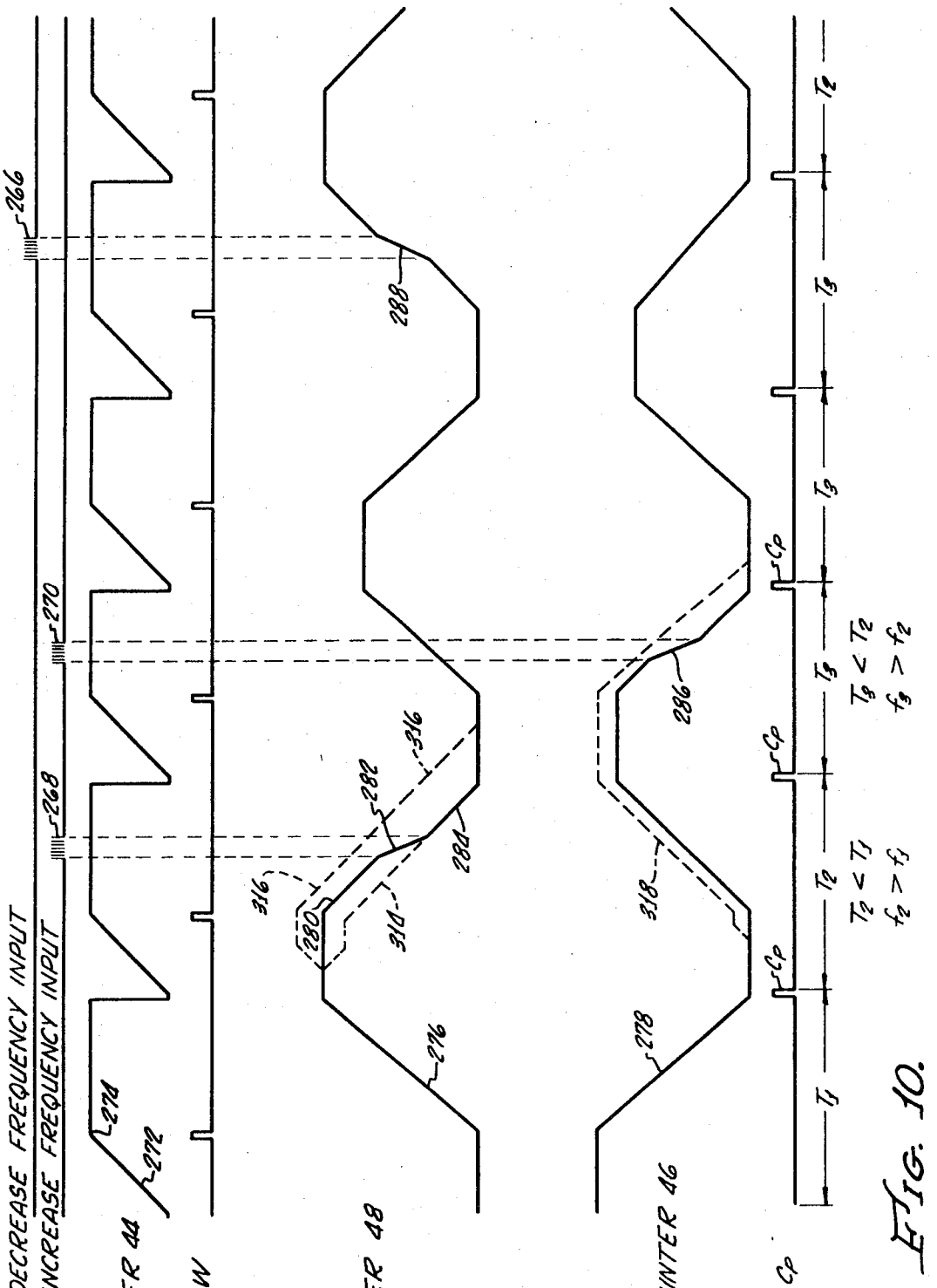

FIG. 10.

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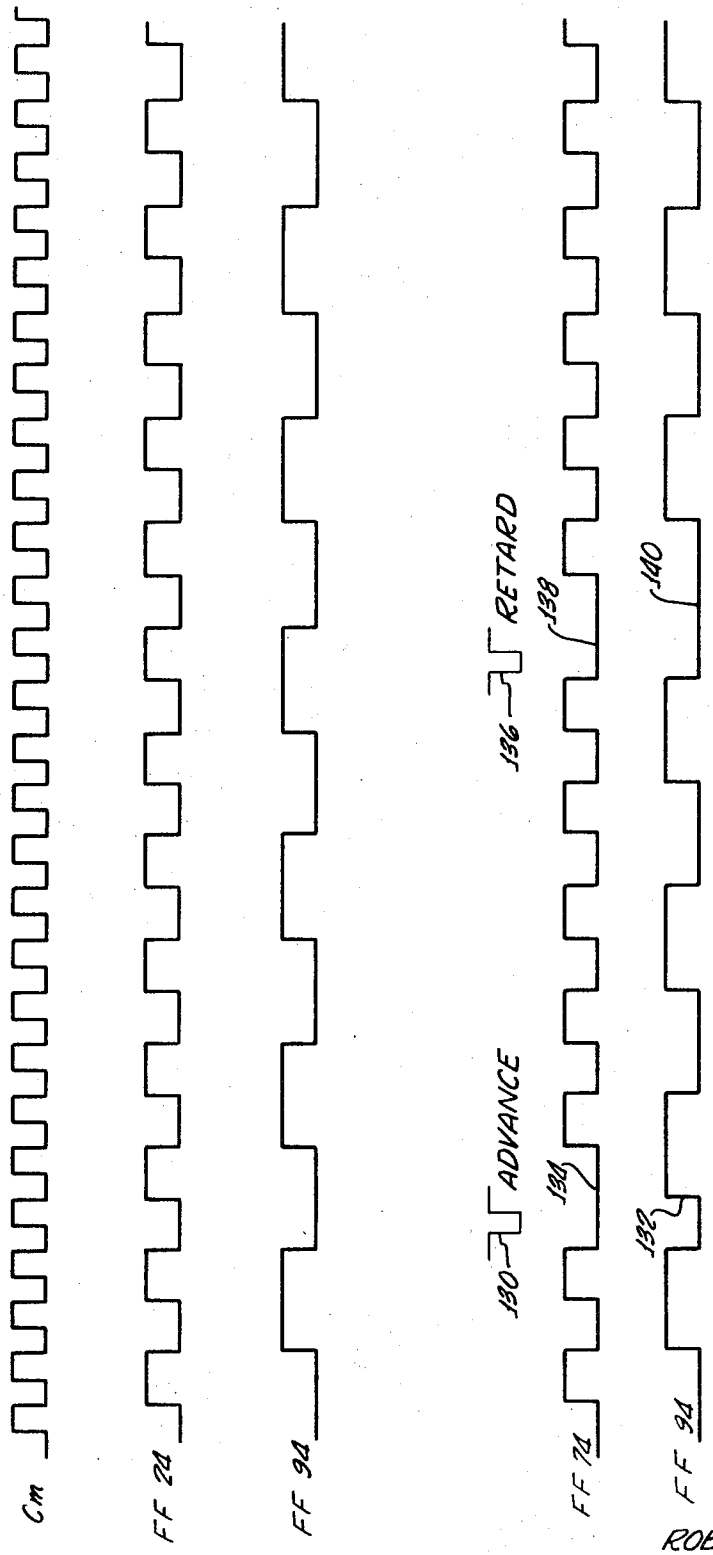

FIG. 11.

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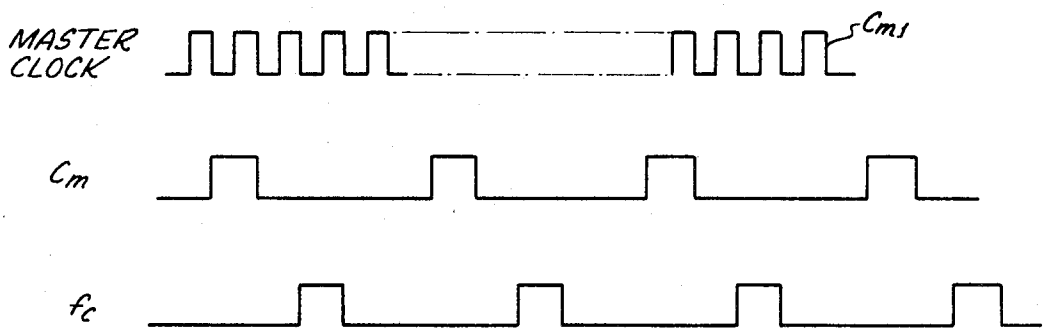

FIG. 12.

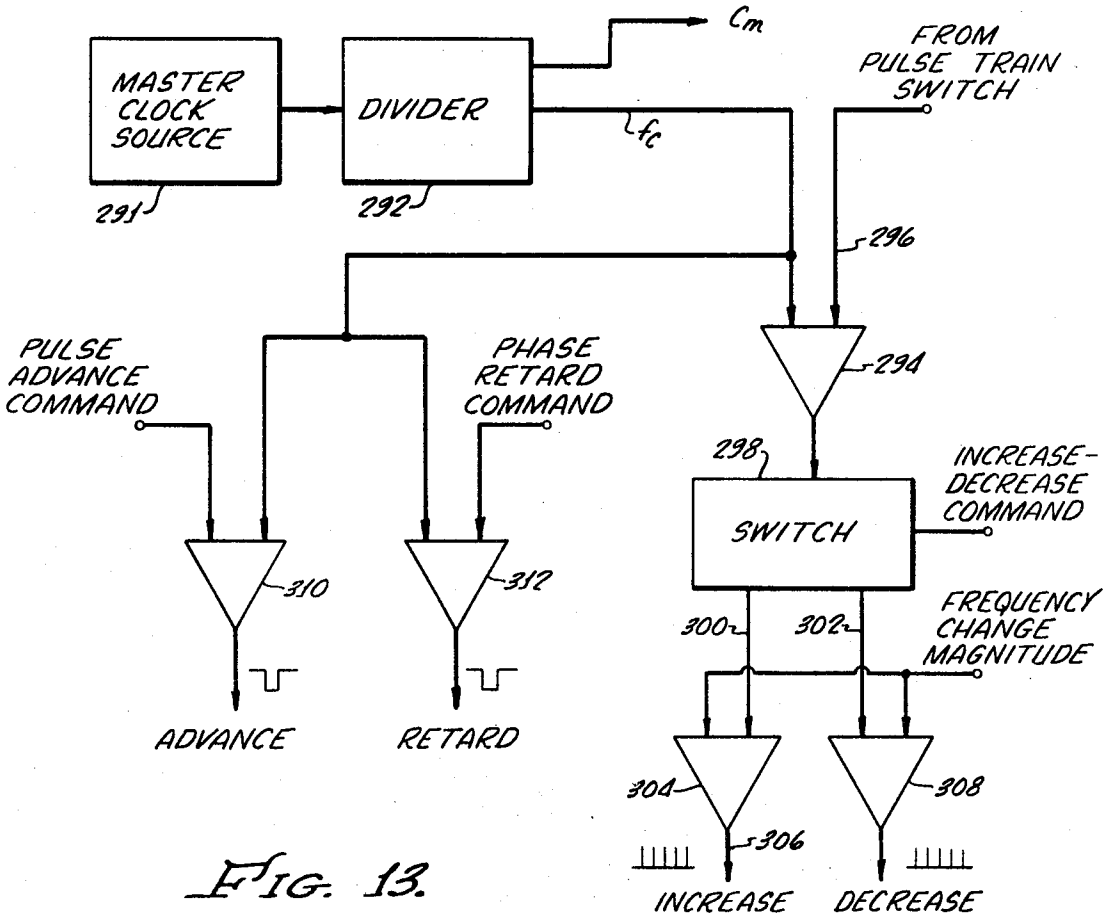

FIG. 13.

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VARIABLE FREQUENCY SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to timing systems and more particularly concerns a source of stable high precision timing signal that may be selectively varied in frequency and/or phase. In implementation of the timing aspect of the invention improved dividing circuits are employed.

2. Description of Prior Art

Arrangements for controlling phase and frequency of oscillating circuits have long been employed in a variety of forms and involving many different techniques. Most commonly, an oscillator has its frequency varied by changing certain reactive elements in the circuit. Thus, a variable capacitor or inductor may be employed for frequency control. Many types of oscillators lend themselves to ready control by application of external synchronizing signals. Such oscillators, because of the variable element required for frequency control, are inherently subject to drift and lack suitably high tolerance, stability and precision of frequency output. For optimum precision of oscillator frequency, circuits are generally controlled by crystals which have a natural frequency that remains relatively stable and unaffected by environmental changes or aging. However, unless one goes to use of harmonic modes, the frequency of the crystal cannot be changed whereby the only way to change the frequency of a crystal controlled oscillator is by alternatively switching into the circuit one of a number of oscillators or crystals. This arrangement, of course, can provide but a limited number of frequency variations and does not readily lend itself to external synchronization or phase control.

Precision timing systems required in various power supplies, such as, for example, the uninterruptible power supply system employed in large digital computing machines, must be capable of being synchronized both in frequency and phase to an outside power source and yet, in the absence of such outside power source, must have an extremely stable frequency. Further, since a computer such as, for example, the IBM 360 computer, requires a power source that stays within a frequency band of ±½ Hz., there is a maximum frequency variation that can be tolerated. Accordingly, it is desirable to provide a timing system of controllably variable frequency which, nevertheless, has set frequency limits so that it cannot be inadvertently varied in frequency to an extent that would cause damage to the system being powered thereby. No system meeting all of the above requirements has heretofore been available.

SUMMARY OF THE INVENTION

In carrying out the principles of this invention in accordance with a preferred embodiment thereof, a fixed frequency clock providing basic frequency stability and accuracy is arranged to drive a variable divider that provides a system output that is selectively variable in phase and/or frequency. The variable divider may include means repetitively generating first and second chronologically successive time intervals, frequency control means for changing the duration of one of the intervals, phase control means for changing the duration of one of the intervals, and output means responsive to a predetermined point of one of the intervals. More specifically, the output of the fixed frequency clock is counted by a substantially fixed interval counter which upon termination of its count, switches the fixed frequency clock pulses to be counted by a variable counter. The latter upon reaching a predetermined point in its count provides an element of the frequency variable system output and initiates a repetition of the cycle of counting pulses of the train by the fixed counter and then by the variable counter. A significant aspect of the invention is the mutually opposite phase operation of a pair of oscillatory circuits, each operable in positive and negative half cycles, provided with means responsive to termination of one of the half cycles of the first circuit for terminating a concurrent half cycle of the second circuit, and wherein said means comprises means for initiating the next half cycle of the second circuit. In a preferred embodiment the oscillatory circuits are reversible, up-down, counters.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a timing system according to principles of the present invention,

FIGS. 2*a a–2d*, collectively, comprise a synchrograph illustrative of the operation of FIG. 1,

FIG. 3 is a block diagram illustrating the fixed and variable modulus counters and their control,

FIGS. 4*a*, 4*b*, 4*c* and 4*d* illustrate details of the fixed modulus counter of FIG. 3,

FIG. 5 shows details of one of the reversible counters of FIG. 3,

FIG. 6 illustrates a starting circuit for the system,

FIG. 7 shows the details of the pulse train switch,

FIG. 8 shows the circuit of the direction control of the reversible counters,

FIG. 9 illustrates content control circuitry for the reversible counters,

FIG. 10 comprises an analog representation of the counter operation including increase and decrease frequency operation,

FIG. 11 is a synchrograph illustrating operation of phase advance and phase retard functions of the fixed modulus counter,

FIG. 12 is a synchrograph illustrating phasing of the frequency control signal, and

FIG. 13 is a block diagram of an arrangement for generating frequency and phase control command signals.

DESCRIPTION OF THE PREFERRED EMBODIMENT

General System

Advantages of digital integrated circuits, whether in timing devices, power systems, or other arrangements, are many and well known. Digital systems are not seriously affected by DC gains, drifts, temperature effects or the like. In most cases, noise is considerably less of a problem in a digital system. One can obtain greater precision of control in digital modes than in analog modes. Feedback is less of a problem. High feedback analog systems are subject to undesired oscillation problems requiring complex and sophisticated compensatory circuits. In a system such as an uninterruptible power supply requiring a crystal oscillator having a stability of ±100 parts per million it is highly desirable to be able to synchronize the system in both frequency and phase to an outside power source. Notwithstanding such capability for synchronization, the system must exhibit extremely stable frequency in the absence of or upon failure of the outside power source. Such requirements of stability and accuracy can be met by employing a crystal clock as the basic frequency source. Suitable crystal controlled frequency sources are described in a copending application for Frequency Comparator, Ser. No. 33,208, filed on Apr. 30, 1970 by L. C. Butler, Jr. and R. S. Jamieson, and in copending application for Multi-Channel Control Circuit, Ser. No. 8,877, filed on Feb. 5, 1970, by L. C. Butler, Jr., T. W. Grasmehr and R. S. Jamieson, both applications being assigned to the assignee of the present application and incorporated herein by reference. Such crystal clocks, although exhibiting high precision, are themselves subject to but a small tuning range. Accordingly, a fundamental advantage derived from use of the crystal clock, namely extreme stability, is antithetical to the presently identified requirement of a variable frequency and phase system that can be synchronized with another source. The two contradictory requirements, the first being for stable frequency, and the second being for external frequency and phase synchronization, are satisfied in the present invention by employing a fixed frequency clock to establish the basic frequency stability and accuracy and, in addition, a variable divider to provide the desired output signal of variable frequency and phase. The described embodiment

of the present invention is particularly arranged for use in an uninterruptible power supply of the type referred to in the aforementioned application of Butler and Jamieson and of the type also referred to in copending application of L. C. Butler, Jr., Ser. No. 8,875, filed on Feb. 5, 1970 for Majority Logic System, assigned to the assignee of the present application and incorporated herein by reference. For reasons discussed in the above-identified applications, it is desirable to start with a precision clock signal of, for example, 230.4 kHz. and divide this down into a 360 Hz., six phase signal for driving inverters of an uninterruptible power system. Although these frequencies are employed in the illustrated embodiment by reason of the designed application for a specified system, it will be readily appreciated that the specific values of the various frequencies employed, the various moduli of the several counters, and particular details of magnitude of timing parameters all may be varied to suit particular needs and applications and are illustrated herein as being of the identified values solely for the purposes of exposition.

In order to provide a fixed frequency clock and a variable divider, one could simply employ a variable modulus counter, a counter whose division ratio could be changed at will and make such counter responsible to a fixed frequency clock. However, in accordance with a preferred embodiment of the present invention, a pair of interval generators are used. A fixed interval generator is followed by a variable interval generator as will be described more particularly hereinafter. The fixed interval generator is caused to actuate a variable interval generator which, in a preferred mechanization, is formed of a pair of up-down or reversible counters which exchange counts between them. As illustrated in FIG. **1**, a clock pulse generator **16** provides a train of high stability and high precision pulses at a fundamental frequency, at a frequency in this example of 230.4 kHz. The pulses from the clock pulse generator are fed via a switch **18**, when in the illustrated position, to a fixed time interval generator **20** which initiates generation of a fixed interval when the switch **18** is moved to the illustrated position. Upon termination of the interval provided by the generator **20**, an output signal W is produced to cause the switch to move to the other position thereof which initiates operation of a variable interval generator **22**. In the described embodiment both generators **20** and **22** are digital counters. When generator **22** times out, it produces an output signal C_p which comprises one element of a train of pulses that forms the output of the described system. The output C_p performs two other functions. First, it is fed back to the fixed interval generator **20** to reset the latter and place it in condition to initiate another of its time intervals. Second, it is fed back to operate the switch **18** and return it to the illustrated position thereof whereby operation of the fixed interval generator is once again initiated. Completion of this interval again operates the switch to initiate the timing of the second interval generator **22** and so on in continued cyclical steady-state operation.

The steady-state operation is illustrated in FIG. **2***a* wherein the first line illustrates the train of clock pulses **24** which comprise the units that are counted by the generators **20** and **22** for creation of their timed intervals. Upon first operation of the switch **18** into the position illustrated in FIG. **1**, the fixed timed interval of generator **20** is initiated at time *t*, as indicated at **26**. The interval of **26** terminates at time t_2 and thereupon operates switch **18** to effect initiation of the interval of the variable timer **22** as indicated in FIG. **2***a* at **28***a*. Interval **28***a* terminates at a time t_3 to thereupon operate switch **18** and initiate a subsequent fixed interval **26**. Upon termination of the interval **28***a* there is produced the output pulse C_p and upon the termination of the subsequent interval **26**, a second interval **28***a* is initiated. Thus a steady-state cyclic operation continues with the two interval generators timing out alternately, one after the other, and an output pulse C_p being generated at a fixed point in the cycle of one of the interval generators, specifically in this instance, upon the termination of the interval **28***a*. It will be readily appreciated that the train of pulses C_p comprises a fixed frequency timing signal that may be taken from any readily identifiable point in the timing interval of either of the interval generators, but is suitably obtained at the fall of the interval designated as **28***a* in FIG. **2***a*.

In order to vary the frequency of the output of pulse train C_p, these pulses are fed as illustrated in FIG. **1** to a frequency comparator **30** which receives as a second input thereto a reference frequency pulse train from a reference source **32**. The difference in frequencies between the pulse train C_p and the output of the reference frequency source **32** is fed via line **34** to a frequency adjust or command circuit **36** which produces a signal that is fed to the variable generator **22** to change the timing thereof in accordance with the sense of the frequency difference as determined by frequency comparator **30**. A variety of methods and mechanisms may be used to change such timing as will be described hereinafter. Where the described system is to be employed as a standby power supply for an uninterruptible system, the reference system **32** may comprise the line frequency to which it is desired to synchronize the described system. It is not necessary to distinguish the magnitude of frequency difference, since it is necessary only to determine the sense of such difference, that is, to determine which of the two frequencies compared by comparator **30** is the higher. One such circuit that may be employed for this purpose is shown in the aforementioned application for Frequency Comparator of Butler and Jamieson and is described as a frequency difference sense detector. Other arrangements are readily available including the conventional frequency modulation servo that provides the sense of the frequency difference by means of a shaft output rotation to thereby operate one of two switches depending upon which frequency is the higher and upon the direction of such a shaft rotation.

Functionally, operation of the frequency adjustment is illustrated in FIG. **2***b* wherein the situation for decrease of frequency is shown. The fixed interval pulse **26** remains the same, but for frequency decrease it is preferred to increase the variable interval to provide a longer period for the complete cycle whereby the repetition rate of the pulses C_p is decreased. The relative timing of the various components of the system remains the same. That is, upon termination of interval **26**, interval **28***b* is initiated and upon termination of the latter, the interval **26** is again initiated and the output pulse C_p is generated. The difference resides in the fact that one of the intervals, interval **28***b*, has been lengthened.

As shown in FIG. **2***c* for increase of output frequency, the fixed interval **26** again remains the same. The output pulse C_p still is produced upon the termination of the shorter variable interval, but the latter in this situation for increased frequency has been decreased as illustrated at **28***c*. Again the relative sequences remain the same, but the total period has been decreased to provide the commanded frequency increase.

For phase adjustment, output pulses C_p are fed as one input to a phase comparator **37** (FIG. **1**) which receives its reference input from the reference **32**. Comparator **37** produces a signal that represents a phase error and is fed via line **39** to a phase adjust circuit **38**. The latter produces signals that temporarily change the interval of the fixed interval generator **20** although temporary change of the variable interval generator may also control output phase. Illustrated in FIG. **2***d* are representations of the fixed and variable intervals and output pulse train C_p for the condition of retarding of the phase of the output signals with respect to the phase of the pulse train illustrated in FIG. **2***c*. The first of the intervals **26***d* and the shorter interval **28***d*, again remain the same as compared with the arrangement of FIG. **2***c* so that the interval between the first two output pulses C_p shown in FIG. **2**d remain unchanged. However in this situation, after the occurrence of the second output pulse C_p a phase retard signal from the phase adjustment circuit **38**, FIG. **1**, is fed to the fixed interval generator **20** to temporarily, or for one cycle of the output signal, increase its time period. Thus, the relatively fixed

interval **26***e* has been lengthened for this one cycle. For subsequent cycles indicated at **26***f* and **26***g* this relatively fixed time interval goes back to its original length where it remains for subsequent steady-state operation. In each case, as before, the variable interval **28***d* is initiated upon termination of the fixed interval **26***d* or **26***e*, etc., and upon termination of interval **28***d*, the output pulse C_p is generated and the fixed interval **26***e* or **26***f* is initiated. Thus, the fixed interval is changed but once in order to change the phase, and thereafter, the system returns to an unvarying steady-state operation. The magnitude of the phase change can be varied by controlling the amount of lengthening of interval **26** or by repeating a selected lengthening. It will be readily appreciated that for a phase advance the fixed interval **26** would be shortened rather than lengthened during one (or several) of its occurrences to thereby advance the train of output pulses C_p.

In the illustrations of FIGS. **2***a* through **2***d*, the fixed interval period **26** is shown to be of considerably greater duration than the nominal length of the variable interval **28**. A significant advantage of employing both a fixed and variable interval generator resides in the protection afforded to the timed circuit. It was pointed out above that certain sensitive systems such as computing devices cannot tolerate a frequency variation beyond a certain amount such as plus or minus three percent, for example. For such a tolerance, it is possible with the illustrated arrangement to provide the fixed interval generator with a period equal to 97 percent of the desired period of the output frequency and to provide the variable interval generator with a nominal period equal to 3 percent of the desired output period. Accordingly, for a plus or minus 3 percent variation, the period of the variable interval may be varied from zero to an amount equal to a total of 6 percent of the desired output frequency. No greater variation can be achieved since even in the total absence of the variable interval generator, the fixed interval generator will still provide 97 percent of the output interval. Thus, the use of the fixed interval generator provides, in effect, a set of stops or limits for the frequency variation selection. It is not possible to inadvertently cause or command a frequency variation greater than the frequency tolerance of the system.

A number of different types of interval generators or timers, both analog and digital, are known and readily available for use in the practice of the invention as described in the system of FIG. **1**. For example, relaxation oscillators, one-shot or monostable multi-vibrators may be employed with one triggering the other, and with various arrangements for effecting a temporary (in the case of the fixed interval generator **20**) or relatively a steady-state (in the case of variable interval generator **22**) variation in the time interval thereof. Where conventional circuits such as one-shot multi-vibrators are employed, the clock pulse generator **16** need perform no function other than to initially trigger the interval generator. However, for high precision systems, the fixed interval generators are preferably made in the form of the more accurate counters which also perform the division of the high frequency clock pulse train of 230.4 kHz. down to a desired nominal 360 Hz. output timing signal.

A mechanization of the system of FIG. **1** employing a substantially fixed modulus counter and a pair of variable modulus reversible counters is illustrated in FIG. **3**.

DIGITAL SYSTEM

As indicated in FIG. **3**, the clock pulse generator **16** which may be a source of high precision, high frequency train of clock pulses produced by equipment such as that more particularly described in the aforesaid copending applications, feeds the pulses thereof to a starting circuit **40** and thence through a pulse train switch **42** from which the pulses C_m are fed alternately to a fixed interval counter **44**, or to both of a pair of reversible counters **46**, **48** through counter content control circuits **50**, **52**, respectively. The reversible or up-down counters **46**, **48** are substantially identical to each other and are arranged to operate under the control of a direction control circuit **54** to count in mutually opposite directions. Stated in another fashion, each of the counters is a cyclical counter or an oscillatory circuit that operates in a positive half cycle, say the up direction, for example, and thence in a negative half cycle, or down direction. When the counter **46** is counting up, the direction control for both counters is such as to cause counter **48** to be counting down and vice versa. When either counter reaches a predetermined point in its cycle or count, it feeds a signal to the direction control circuit **54** which thereupon performs three separate functions. First, the direction control circuit **54** produces the system output pulse indicated as C_p on output line **56**. Second, via line **58**, the output pulse C_p is fed back to the fixed modulus counter **44** to reset this counter to **0**. Third, via line **60** the output pulse C_p is fed back to the pulse train switch **42** to cause this switch to feed the pulses from the pulse generator **16** through starting circuit **40** to the fixed modulus counter **44** once again. The output pulse C_p comprises one element or one pulse of the train of output pulses of the system. Initially, upon starting of the system, the pulse train switch **42** is in a position to feed pulses C_m from the pulse generator to the input of the fixed modulus counter **44**, which, accordingly, begins to count up from its zero count. When this counter attains its full count, it provides an output signal W on line **62** which is fed to the pulse train switch **42** to operate this switch into a position wherein the pulses from pulse generator **16** are now fed via line **64** to both of the content control circuits **50** and **52** of the two reversible counters. These counters then proceed to count the pulses of pulse train C_m, one counter counting up and the other counting down under direction control of a signal provided on lines **66** and **68** from the direction control circuit **54**. As previously indicated, when one of these counters reaches a preselected count, the counting direction of the two are switched, the fixed modulus counter is reset to zero, the pulse train switch is operated to switch the train C_m to the fixed modulus counter and another output pulse C_p is provided as a second element of the system output pulse train. Thus, the system will continuously recycle, counting a fixed interval by means of counter **44**, and then a second interval by means of one half cycle of the reversible counters **46**, **48**.

The several periods and counts available from the fixed counter **44** and up-down counters **46**, **48** are readily selected to meet a specific application. For example, for use in an uninterruptible power supply wherein a train of 360 Hz. pulses C_p is required to drive the power supply inverters, the pulse generator may provide a pulse train of 230.4 kHz. Thus, it is convenient to employ a fixed modulus counter **44** that will achieve a divide by **608** operation. In such an operation, the reversible counters are set to provide a nominal count of **32** and a maximum count of **64** so that the sum of the divisors, **608** and **32** total **640**, which is the proper divisor of 230.4 kHz. to obtain the desired 360 Hz. For the exemplary counters indicated, the tolerable frequency variation is from about

$$343\left(=\frac{230400}{608+64}\right) \text{ to about } 378\left(=\frac{230400}{608}\right) \text{ Hz.,}$$

whereby the nominal **360** Hz. pulse train C_p may vary by ±32 clock pulses C_m for each repetition thereof. In most cases, however, the range of frequency variation is less important than the value of the nominal frequency, although either may be readily selected to suit a given application.

In order to vary the output frequency of the system, one or a group of increase or decrease frequency pulses f_c may be provided via line **70** to each of the counter content control circuits **50**, **52**. The addition of these pulses to the counters during the up or down counts thereof is but one of several ways to change the time required for either of these reversible counters to attain its selected count. Details of the counter and frequency control circuits thereof will be described hereinafter. Nevertheless, as previously described in connection with FIGS. **1** and **2**, it will be understood that addition of pulses f_c to the up-down counters will cause these to increase

or decrease the total count thereof and thereby change the second of the two intervals that makeup the total period between output pulses C_p. Furthermore, any change in the total count of these counters effects a steady-state change in the interval provided by these circuits whereby there is a relatively steady-state frequency change commanded. For phase control, on the other hand, it is convenient to provide a temporary change in the count of the fixed modulus counter **44** by adding or inhibiting a count of this counter. The addition of one or several pulses to this counter over and above the pulses received via the pulse train switch **42** will cause the fixed modulus counter to achieve its maximum count earlier whereby the entire cycle of the system is advanced. Conversely, inhibiting one or several pulses fed to the counting input of this counter causes it to reach its total count at a later time, thereby retarding the cycle of the system. This operation is temporary since it affects only a single cycle of the fixed modulus counter. On the next cycle of the system, the counter will receive the usual number of pulses and count to its predetermined value in the same time. Accordingly, there are two independent arrangements for controlling first, the phase by means of the fixed modulus counter, and second, the frequency by means of the reversible counters. It will be readily understood, however, that opposite sense variation of the frequency of the system on successive or different cycles thereof could also achieve a phase variation of the output. In other words, if input pulses f_c are fed in such a manner as to increase the frequency of the system at one instant and then a like number of such pulses are subsequently fed to decrease the frequency of the system, there will have been achieved no net change in frequency although the phase of the output will have been advanced. Similarly, although it is preferred to employ the fixed modulus counter **44** for phase control only, it may be repetitively employed to achieve relatively small amounts of frequency control. It is well known that phase modulation is, from one point of view, simply another form of frequency modulation.

Before a detailed description of the mode of operation of the digital system is presented, it will be convenient to describe the details of the fixed modulus and reversible counters and control circuitry therefor.

FIXED MODULUS COUNTER

The fixed modulus counter **44** is a conventional arrangement of inter-connected flip-flops of JK type which are operated to provide mutually exclusive outputs in any one condition. The flip-flops are conventional circuits which provide mutually exclusive outputs in any one condition as is well known. Each flip-flop as typically shown in FIG. 4*d* has direct set and reset terminals S and R which, when low, will shift and hold the flip-flop in its set or reset state respectively providing at the two flip-flop output terminals Q and $\overline{Q}$, respectively, high and low outputs for the set condition of the flip-flop and respectively low and high outputs for the reset condition of the flip-flop. In addition to the direct set and reset terminals responsive to low signals, each flip-flop has a clock or toggle input *t* and a set and reset input gate indicated at *s* and *r*. Each of the set and reset input gates has two inputs which, when high, enable the input gates and allow the flip-flop to be toggled or to change its state when the clock or toggle input goes low. That is, the set or reset gate that is enabled by a high at its two inputs will provide a signal that allows the flip-flop to be set or reset upon the fall of the toggle if it is not already in such condition. Thus, the direct set and reset terminals are responsive to steady-state low signals, and the set and reset input gates are enabled by high signals to cause the flip-flop to be toggled on the fall of the toggle signal thereto. Typical flip-flops of the type described are sold as microcircuit chips designated MC945FG, MC845F, P,G, MC948F,G, MC848F,P,G, and described in "Integrated Circuit Data Book," First Edition, Aug. 1968, Motorola Semi-Conductor Products, Inc. All of the flip-flops described herein are of the type described so that a detailed description of only one is necessary. As shown in FIG. 4*a*, flip-flop **74**, which comprises the first or input stage of the fixed modulus counter, has direct set and reset terminals **76** and **78** which, when low, will shift and hold the flip-flop to or in its set or reset state respectively which provide at the output terminals generally referred to as Q and $\overline{Q}$, but more specifically for flip-flop **74**, leads **80** and **82** thereof, high and low outputs for the set condition of the flip-flop and low and high outputs respectively for the reset condition. In addition to the direct set and reset terminals, responsive to low signals, each flip-flop has a set and reset gate indicated at **84, 86** for flip-flop **74**. Each of the set and reset gates has two inputs. These gates selectively enable the toggle input to the flip-flop. That is, upon the fall of the triggering input **84***a*, the set or reset gate that is enabled by a high on its two inputs will allow the flip-flop to be set or reset if it is not already in such condition. Thus, the direct set and reset terminals are responsive to steady-state low signals and force their respective output states independent of the condition of the other inputs whereas the set and reset gates of the flip-flops are enabled by high signals, thereby permitting a specific state change upon the fall of the clock signal thereto. The first stage flip-flop **74** of the fixed modulus counter receives a triggering input via line **88** on which appears the pulse train C_m from the pulse train switch. This pulse train is also fed as the toggle input of flip-flop **94** of the second stage of the counter. All of the flip-flops employed herein and described in connection with other circuits of this system are substantially identical to the flip-flop **74**, its set and reset gates **84, 86**, and its direct set and reset terminals **76, 78**. Thus, it will be seen that when flip-flop **74** is set, its output terminal **80** provides a first enabling signal to the reset gate **92** of flip-flop **94**, the latter when set provides a second enabling input to its reset gate so that upon the fall of a toggle or clock signal on lead **88**, flip-flop **94** will be reset. The $\overline{Q}$ output of flip-flop **74** is fed via lead **82** and an OR gate **96** to one of the enabling inputs of the set input gate **90** on flip-flop **94**. Note that the OR gates described herein are structurally the same as the NAND gates, providing the logical OR function for low signals, with polarity inversion. Understanding of operation of the system is facilitated by referring to the various gates by their logical functions although the gate circuits are the same for OR and NAND. The Q output of flip-flop **94**, the second stage of this counter, is fed as the toggle input of a third stage of the counter including a flip-flop **98**. Additional counter stages including their set and reset gates as indicated at **100, 102, 104, 106, 108, 110** and **112** (see also FIG. 4*b*) provide this counter with a total count that produces the desired dividing ratio. Each of the counter stages is identical with all of the others and each is connected to the preceding stage in the same manner as counter flip-flops **94** and **98**. The OR gate **96** between the zero or $\overline{Q}$ output of flip-flop **74** and the set input gate **90** of flip-flop **94** is provided uniquely for the first two stages in order to provide for the advance retard feature functionally described above but yet to be described in detail. In order to provide the output signal W indicating attainment of the desired count by the fixed modulus counter, there is provided a pair of five input inverting AND or NAND gates **114, 116**(FIG. 4*c*) having inputs (via leads not shown) as indicated in the drawing from the various flip-flops or counter stages **74, 94, 98, 100, 102, $\overline{104}$, 106, $\overline{108}$, $\overline{110}$** and **112**. It will be understood that the bar over the indicated counter stage indicates that the output is taken from the $\overline{Q}$ output terminal of the specific stage, whereas the number without a bar indicates an output derived from the Q side. The outputs of the two NAND gates **116** are fed to a second NAND gate **118** to provide the positive going pulse W that is the output of this counter, and which is fed to operate the pulse train switch to be described in detail below. The NAND gate is a conventional circuit that provides a low output when and only when all of its inputs are high. When any one or more of its inputs is low, its output is high.

In order to cause the fixed modulus counter to attain its output count earlier or later in time, there is provided a pair of ad-

vance and retard flip-flops **120** and **122** (FIG. 4*a*) having set and reset input gates and direct set and reset input terminals all as described in connection with the other flip-flops employed herein. Each of the advance and retard flip-flops has a clock or toggle input via line **88** in the form of the clock pulses C_m, and each is adapted to receive a negative retard or advance pulse applied to its direct set terminal from the phase advance or phase retard circuit as indicated in FIG. **2**. The $\overline{Q}$ outputs of both of the advance and retard flip-flops are fed as the inputs to NAND gate **124** which has its output inverted in a second NAND gate **126**, that, in turn, provides an input to the set gate **84** of the first counter stage. The $\overline{Q}$ output of the advance flip-flop is also fed via line **128** as the second of the two inputs of OR gate **96**.

With a symmetrical square wave train of clock pulses C_m as indicated in FIG. **11**, the first stage **74** of the fixed modulus counter of FIG. 4*a* sets and resets upon each fall of pulse train C_m to provide a train of square wave pulses, essentially a divide by two pulse train as indicated in the drawing. The second counter stage **94** sets and resets upon each fall of the Q output of the first counter stage as illustrated in the drawing. Upon occurrence of a negative going advance pulse **130** as indicated in the second row of output pulses of flip-flop **74**, the advance flip-flop **120** has a low on its direct set terminal and is set to provide a low output at its $\overline{Q}$ terminal, thereby disabling the NAND gate **124** and set gate **84**. Concurrently, the low signal at the $\overline{Q}$ output terminal of advance flip-flop **120** is fed through the OR gate **96** and inverted thereby to provide an enabling input to the set gate **90** of the second counter stage. Accordingly, the second stage flip-flop **94** will set on the next fall of a clock pulse as indicated at **132**, whereas flip-flop **74**, its set gate disabled, will remain low as indicated at **134**. Flip-flop **120** is reset or cleared by the next clock pulse whereby the relative phasing of flip-flops **74** and **94** thereafter continues exactly as it was prior to the occurrence of the advance pulse **130**, except that both of these have now been advanced by one full cycle of the clock pulse C_m and, accordingly, the attainment of the desired total count of the fixed modulus counter is likewise advanced by one full clock pulse interval.

Upon occurrence of negative going retard pulse **136**, also illustrated in FIG. **11**, the direct set terminal of flip-flop **122** goes low whereby this flip-flop **122** is set and its $\overline{Q}$ output is low, disabling NAND gate **124** and set gate **84** of the first flip-flop stage **74**. Accordingly, the Q output of this flip-flop remains low as indicated in the drawing at **138**, upon occurrence of the next clock pulse. No additional input pulse is fed to input gates of the second stage flip-flop **94**, although flip-flop **74**, its Q output remaining low and its $\overline{Q}$ output high, provides a high output to the input of OR gate **96** which appears as a low input to the set gate **90** of flip-flop **94**. Accordingly, the latter cannot be set upon occurrence of the next clock pulse and simply retains its low state for an additional clock pulse interval as indicated at **140**. Retard flip-flop **122** is reset or clear upon the fall of the following clock pulse. Thereafter, in the absence of additional advance or retard pulses, the first two stages of the counter, stages **74** and **94**, continue their cyclic operation as illustrated in the drawing and both have been retarded in phase by the period of one full clock pulse interval. Accordingly, the output pulse W has been delayed by such interval.

Illustrated in FIG. 4*b* is the starting gating for the fixed modulus counter. The output pulse C_p which is provided by the reversible counter direction control circuit, is fed as the first input to an OR gate **142** which receives as a second input thereto a plurality of starting pulses identified as P. These pulses are fed via a pair of NAND gates **144** to a common reset line **146** connected to the direct reset terminal of all of the flip-flop stages except the advance and retard flip-flops, whereby each of the counter stages may be reset to zero upon start of the operation and upon each occurrence of an output pulse of C_p. Although the output pulse C_p is not fed to the advance/retard flip-flops **120**, **122**, it is not necessary to place these in condition initially because they are immediately reset by clock pulses C_p on line **88**. The set gates of these flip-flops **120**, **122** are disabled by the fixed ground or low input thereto.

REVERSIBLE COUNTERS

Illustrated in FIG. **5** is an exemplary one of the two reversible counters, each of which is identical to the other, receiving only different control signals so that the two will always operate in mutually opposite phase relation during their reversible cyclical counting period. Direction and content control of the counters will be described below in connection with FIGS. **8** and **9**. The various stages of the reversible counters each comprises a JK or a set and reset flip-flop having direct set and reset input terminals, and set and reset gates which permit the flip-flop to toggle upon fall of a clock input thereto just as described in connection with the corresponding flip-flops and gating of the fixed modulus counter. Accordingly, each reversible counter, having in this expository arrangement a nominal counting half cycle of **32** and a total counting capacity of **64**, comprises six stages of which the first two and last one are illustrated in detail with the three intermediate stages being illustrated in block. To cause these counters to reversibly count either up or down, the output terminals of each flip-flop are fed as toggling inputs to the input of the succeeding flip-flop stage via suitable gating which is identical for the interstage coupling of all of the counters as illustrated in FIG. **5**. Thus, the first stage includes a flip-flop **148** that is followed by interstage gating comprising first and second NAND gates **150**, **152** having the outputs thereof fed via an OR gate **154** to the clock or toggling input of the succeeding stage. Similarly, the Q and $\overline{Q}$ outputs of the second stage flip-flop **156** are fed through similar gating to toggle the third stage **158**. Similar connections are made to and between fourth and fifth stages **160** and **163**, with the outputs of the fifth stage **163** from the Q and $\overline{Q}$ terminals thereof being fed via NAND gates **164**, **168**, respectively, and OR gate **170** to the toggle input of the final stage **172**. Each of the NAND gates such as **150** and **164** that has a first input directly from the Q output terminal of the preceding stage flip-flop, also has a second input from a line **174** on which appears the up command signal. Whenever the signal on this line is high, the counter is counting in the up mode. Each of the NAND gates such as NAND gates **152** and **168** having a first input directly from the $\overline{Q}$ side of the output terminal of the preceding stage flip-flop has a second input from a down command line **176**. The signal on this line is high whenever the counter is commanded to count in the down direction. The third input to the interstage NAND gates, whether counting up or down, is provided for the first pair of NAND gates **150** and **152** from a counting input line **178** at which appears the pulse train C_m that is to be counted. The succeeding pairs of interstage NAND gates receive as their third inputs, the output of the OR gate of the preceding stage. Thus, NAND gates **150**, **152** provide first and second inputs to OR gate **154**. The latter provides its output as the clock input to the toggle terminal of the succeeding stage and also provides via line **180** the same output as a third input to both of the interstage NAND gates, (not shown) that follow the second stage flip-flop **156**. Likewise, the third input on line **182** to the final stage NAND gates **164**, **168** is provided by the output of the OR gate (not shown) that follows the fourth flip-flop **160**. Accordingly, with the arrangement of interstage gating illustrated in FIG. **5**, each counter will count up or down in straight binary code depending upon the state of the signal on lines **174** and **176**, respectively. Whenever the signal on line **174** is high, the signal on line **176** is low and vice versa, as will be described below with reference to FIG. **8**.

As previously explained, the output of each of the reversible counters is provided when the counter attains a preselected count. In the embodiment illustrated herein, the preselected count for each of the counters is the count of one in the down counting mode. Accordingly, there is provided an eight input NAND gate **184** having a first pair of inputs from the down command line **176** and having six additional inputs from the

various counter output stages as indicated. It is noted that identical input signals to plural terminals of certain of the gates are shown only because of the particular number of input terminals that are provided in the standard circuits that have been employed in mechanization of the described embodiment. All of the inputs to output gate **184** are provided from the $\overline{Q}$ sides of the flip-flops except that output which is obtained from the first stage **148**. Thus the input to gate **184** comprises the binary number 000001, the count of one. NAND gate **184** will provide a negative going output pulse when all of the inputs thereto are high. This negative going pulse is a pulse that is fed via line **232** for counter **46** and via line **234** for counter **48** through the direction control circuit of FIG. **8** to provide therefrom the output pulse C_p as will be described more particularly below.

The counter of FIG. **5** will count input pulses provided on line **178** in straight binary notation, and will count in one direction until the control signals on the up-down command lines **174** and **176** are interchanged at which time the counter will start to count in the opposite direction. Accordingly, simply by changing the signal on lines **174** from high to low and concommitantly changing the signal on line **176** from low to high, the counter may be made to terminate a particular half cycle and initiate the succeeding half cycle, that is, to change the direction of its count. Further, by terminating the application of input pulses to the counter, the counter will stop its count, performing a memory function to store the particular count that had been reached when the input pulses are stopped.

STARTING CIRCUIT

Illustrated in FIG. **6** is the starting circuit that has the function of initially providing on a line **186** the train of negative going preset pulses P which are fed to the various stages of the several counters and to other circuits to be described more particularly hereinafter to establish the several flip-flops in appropriate conditions for start of system operation. After a short start interval, the starting circuit of FIG. **6** operates to provide the clock train pulses C_m at an output terminal **188** thereof. The clock pulses C_m are fed to the starting circuit from the clock pulse generator **16** (FIGS. **1** and **3**) on a line **190** and also fed via a pair of NAND gates **192**, **194**, to a second pair of NAND gates **196**, **198**. At the output of gate **196** appears the train of positive going clock pulses C_m. These are fed to the pulse train switch which directs these pulses to the several counters. The output of NAND gate **198** is further inverted in a gate **200** at the output of which appears the starting pulses P on line **186**.

When the circuit is first turned on, NAND gate **192** is disabled by the low input provided from the Q output of a starting flip-flop **202** which has the $\overline{Q}$ output terminal thereof connected to enable the second starting gate **194**. Initially, flip-flop **202** is in reset condition and is arranged to receive a toggling input in the form of the clock pulses C_m on line **190**. This flip-flop also receives enabling inputs to its reset and set gates from the output of a series of starting NAND gates **204** and **206**, respectively. Initially, the $\overline{Q}$ output side of flip-flop **202** is high, providing a high input to an OR gate **208** which provides a low input to gate **204** whereby both inputs to gate **206** (from the output of gate **204**) are high. The output of gate **206** is low and the set input gate of the flip-flop **202** is disabled. When the clock pulse generator is turned on, pulses C_m are fed through an input gate **210** through the OR gate **208** and to the NAND gate **204** to provide a first input thereto. A second input to the NAND gate **204** is provided by a capacitor **212** connected to an input diode (not shown) of NAND gate **204** substantially as described in connection with the timing flip-flop T described in FIG. **8** of the aforesaid copending application for Frequency Comparator. NAND gate **204** provides no output until a series of pulses are received via the OR gate **208** sufficient to charge the capacitor **212** to a value at which the capacitor provides the second input to the NAND gate **204**. Thus, after a delay of several clock pulse intervals, the capacitor provides one input and one of the clock pulses C_m provides the other input to the NAND gate **204**. This gate then provides a low output to gate **206** which enables the set input gate of flip-flop **202**. The flip-flop is then set upon the fall of the next clock pulse. When the flip-flop **202** is set, its Q output terminal goes high to enable gate **192**. Gate **194** is disabled to cut off the starting pulses P and the clock pulses C_m are fed to the rest of the system from line **188**.

PULSE TRAIN SWITCH

The pulse train switch, as illustrated in FIG. **7**, comprises a flip-flop **214** having direct set and reset input terminals and set and reset input gates connected and arranged as are all of the corresponding circuits of the other flip-flops employed herein. The clock train pulses C_m are fed from line **188** of the start circuit as the toggle input to flip-flop **214** and also fed as a first input to each of NAND gates **216** and **218**. The reset input gate of pulse train switch flip-flop **214** is enabled by a positive going pulse W on line **215** received from the output of gate **118** of FIG. **4c**. The set input gate of pulse train switch flip-flop **214** is enabled by occurrence of the system output pulse C_p appearing on line **217** from one of the outputs of the direction control circuit illustrated in detail in FIG. **8**. The direct set input terminal of flip-flop **214** receives the preset starting pulses from line **186** and, accordingly, upon turn-on of the system flip-flop **214** is in the set condition. An output from its Q terminal is fed to gate **216** which is, accordingly, enabled to receive and pass the clock train pulses C_m. The output of gate **216** is inverted a second time in the NAND gate **220** which provides at an output terminal **222** the train of pulses C_m that is fed to the fixed modulus counter illustrated in detail in FIG. **4***a*, **4***b* and **4***c*. Accordingly, the fixed modulus counter proceeds to count to its selected value and when attaining such count, provides the output signal W on line **215** which enables the reset gate of flip-flop **214** whereby upon the fall of the next clock pulse C_m, the flip-flop is reset. Since the fixed counter flip-flops are reset by starting pulses P, counting will commence only after start flip-flop **202** has been toggled. With flip-flop **214** reset gate **216** is no longer enabled and clock pulses no longer appear on output line **222**. However, the $\overline{Q}$ terminal of the pulse train switch flip-flop is now high whereby gate **218** is enabled and may pass to its output line **224** the clock pulses C_m that appear on line **188**. Negative pulses on line **224** are fed to the content control circuits (FIG. **9**) of the reversible counters which proceed to count. When that one of the reversible counters that is counting in the down mode reaches the count of one, an output pulse C_p appears from the direction control circuit (FIG. **8**) which enables the set input gate of flip-flop **214**, whereby the latter will once again be set upon the fall of the following clock pulse. As previously described with the flip-flop **214** in set condition, the clock pulses are no longer fed to the up-down counters but are instead fed to the fixed modulus counter **44**. Thus, the system recycles itself, alternately counting clock pulses in the fixed and reversible counters.

DIRECTION CONTROL CIRCUIT

Illustrated in FIG. **8** are details of the direction control circuit which basically comprises a flip-flop **226** substantially identical to all of the other flip-flops described herein. The flip-flop receives a clock input from the clock train pulses C_m and is initially placed in set condition by receipt of starting pulses P which are applied to its direct set input terminal. With flip-flop **226** in set condition, its Q output terminal is high and the circuit, as will be more particularly described below, is in condition to command counter **46** to count in the down mode and to command counter **48** to count in the up mode. The set and reset input gates of the direction control flip-flop **226** are enabled by the outputs of NAND gates **228** and **230**, respectively, which receive outputs from the "one" count of the reversible counters **48** and **46**, respectively, on lines **234** and

232. Upon start up, the starting pulses P are fed to the various counter input stages so that initially counter **46**, which is to start counting in the down mode, is at its nominal high count of **32**, and counter **48** which will start counting in the up mode, is at its lowest count. This initial condition is obtained by feeding the starting pulses to the appropriate direct set and reset terminals of the several counter flip-flops. For example, counter **46** is initially established with a count of 32 by feeding start pulses to the direct reset terminals of all but the last of its stages. The starting pulses are fed to the direct set input of flip-flop **172** of this counter uniquely. Although, a "one" output from counter **48** would normally be fed to enable the set input gate of the direction flip-flop **226**, the latter is initially in set condition. The selected count outputs from the reversible counters which occur when each of these reaches the count of "one" when counting down, appear on input lines **232** and **234** of the direction control circuit and are also fed as inputs to an OR gate **236** which, accordingly, provides at its output line **217**, the system output pulse C_p. It will be recalled that this is the pulse which (a) provides an individual element of the output pulse train of the system, (b) is fed to the pulse train switch to put the latter in condition to pass pulses C_m to the fixed modulus counter and (c) provides an input to the OR gate **142** (via a NAND gate **143**) of FIG. 4a to reset the fixed modulus counter to its condition wherein it may initiate its fixed count. The Q and $\overline{Q}$ outputs of the direction control flip-flop **226** are fed to NAND gates **238** and **240**, respectively, which invert the inputs thereto and provide on output lead **242** a high signal to command counter **46** to count down and counter **48** to count up, or on output lead **244** a high signal to command counter **48** to count down and counter **46** to count up.

REVERSIBLE COUNTER CONTENT CONTROL

Referring to FIG. **9**, the inputs to the two reversible counters are provided via OR gates **246** and **248** as a train of positive going pulses on lines **250** and **252** which are fed to the inputs of the first stage of each of reversible counters **46**, **48**, respectively. These reversible counter input lines **250**, **252** correspond to the input line **178** of the exemplary counter illustrated in FIG. **5**. The OR gates are arranged to pass one of three possible input pulse trains as counting inputs to the reversible counters. The first of these pulse trains is that provided on output line **224** of the pulse train switch. This is the clock pulse train C_m. As a second of the three possible inputs, each of the OR gates may receive an increase frequency command in the form of a series of positive going pulses fed from an increase frequency command line **254** via a down count NAND gate **256** for counter **48** (enabled only when counter **48** is in down mode) and via a down count NAND gate **258** for counter **46** (enabled only when counter **46** is in down mode). The third input to the OR gates **246** and **248** is provided by a series of decrease frequency command pulses on a line **260** which are fed to an up count NAND gate **262** for counter **46** and to an up count NAND gate **264** for counter **48**. Up count gates **262** and **264** are enabled only when the respective counters are in up counting mode. Thus, the increase or decrease frequency command pulses are applied to the reversible counter input only when it is operating in an appropriate one of its two half cycles of operating.

As will be described in detail below, the count of the reversible counters may be varied to change frequency or to change phase in any one of a number of ways. There is selected for purposes of illustration an arrangement wherein frequency or repetition rate of the output signal C_p is increased by feeding additional counting pulses to that counter which is counting down and decreased by feeding additional pulses to be counted by that counter which is counting up. Only two of the NAND gates **256**, **258**, **262**, and **264** will be enabled at any one time and only one of the enabled pair receives a frequency change command signal. To command an increase of frequency, a group of increase frequency pulses is fed from line **254** to be passed through NAND gates **258** and **256** only when these NAND gates are enabled. For the method of frequency control illustrated, these are enabled only when the respective counters are counting down. A down direction command signal, appearing as a high on line **244**, is fed as an enabling input to gate **256** when counter **48** is counting down and also fed as an enabling input to gate **262** when counter **46** is counting up. Similarly, for a down counting operation of counter **46**, line **242** is high and enables the down counting gate **258** of the content control of counter **46** and simultaneously enables the up counting gate **264** of the content control of counter **48**. Thus, the arrangement allows pulses to be added only to that counter counting down for a commanded frequency increase and only to that counter counting up for a commanded frequency decrease. The up-down count command signals on lines **242** and **244** are provided as outputs of the counter content control at output lines **242*b*** and **244*b*** which command counter **48** to count up and down respectively, and at output lines **244*a***, **242*a***, which command counter **46** to count up and down respectively. Up-down lines **174**, **176** of FIG. **5** correspond to content control lines **244*a***, **242*a***, respectively, for counter **46** and to content control lines **242*b***, **244*b***, respectively, for counter **48**.

FREQUENCY CONTROL OPERATION

From the foregoing description and the following discussion it will be appreciated that the described reversible counters and control circuits therefore comprise an arrangement having exceeding flexibility of control that readily enables operation for a variety of applications in addition to that specifically described herein, including use as a variable divider, a time modulator or an externally controllable oscillator.

Illustrated in FIG. **10** is an heuristic representation of the operation of the digital frequency control system described above. The first line of this synchro-graph illustrates a group of decrease frequency command pulses **266**. The second line indicates two groups **268**, **270** of increase frequency command pulses. The third line of the graph schematically represents the operation of the fixed modulus counter **44**. The next line shows the output pulses W of the fixed counter. The following two lines graphically represent the operation of the up-down X and Y counters **46** and **48**. The final line illustrates the clock pulses C_p provided at the count of "one" by each of the reversible counters in the down counting mode. The analog representations of counter contents are employed in FIG. **10** solely to facilitate understanding of operation since the counter contents are digital, actually changing in discrete amounts. When the system is turned on and the preset pulses P have operated, the several counters are in the initial states ad indicated with the fixed counter being initially at the count of zero, the up-down counter **48** initially being at the count of zero and the up-down counter **46** initially being at its uppermost count for a nominal operation, namely, the count of **32** in the example previously discussed. As soon as the clock pulses begin to be applied to the counters with the pulse train switch in the initial position, the fixed modulus counter begins to count these and its count increases as indicated by the straight line portion **272** of the analog curve depicting the increasing count of this counter. When this counter reaches its full count at point **274**, the first of its output pulses W is generated. It may be noted at this point that the pulses W are always synchronous with the variable frequency output C_p since they are derived from the same basic source. Thus other pulse trains synchronous with the output pulses C_p but relatively phase shifted are available from the output or from intermediate stages of the fixed counter. Where a variable frequency and phase control system such as described above is to be employed in an uninterruptible power system having a plurality of multiphase gated inverters, the availability of such a synchronous fixed frequency output pulse train such as the train of pulses of W, may be of great significance.

While the fixed modulus counter is counting its first full count, both of the reversible counters remain at their respective counts of zero and 32 as illustrated in FIG. **10**. Upon occurrence of the first pulse W the pulse train switch is operated to feed the pulses C_m to both of these counters which then proceed to count up and down respectively as indicated by the straight line portions **276** and **278** of the curves depicting contents of the reversible counters. It will be recalled that the direction control flip-flop of **226** is initially in set condition wherein it provides a high on line **242** and a low on line **244** to command counter **48** to count up and counter **46** to count down. As counter **46** counts down toward the count of "one," counter **48** counts up. When counter **46** reaches its count of "one," it provides an output signal from gate **184** (FIG. **5**) which appears on line **232** (FIG. **8**). This low signal is produced at the output of gate **184** upon attainment of the count of "one" by the counter only when counting down because of input **176** to gate **184**. The low on line **232** disables gate **230** whereby its output goes high to enable the reset input of the direction control flip-flop **226** and allows this circuit to be reset upon the fall of the next clock signal. Concomitantly the direction control flip-flop **226** is toggled, OR gate **236** provides a positive pulse C_p which is fed via line **217** to enable the setting of pulse train switch flip-flop **214** and also to reset the fixed counter **44** by application of the reset pulse thereto as illustrated in FIG. **4***b*. Pulse C_p is initiated via OR gate **236** (FIG. **8**) when the down counter enters the "one" state. When pulse C_p is high, the appropriate input gate of flip-flop **226** is also enabled. Thus, flip-flop **226** is toggled at the drop of the next clock pulse. The change of state of flip-flop **226** causes pulse C_p to go low via the action of the down input on line **176** of gate **184** (FIG. **5**). Thus pulse C_p is one clock pulse period wide.

Similarly, the pulse train switch flip-flop **214** (FIG. **7**) has its appropriate input gate enabled by pulse C_p and, accordingly, toggled simultaneously with the change of state of direction control flip-flop **226**. Thus the pulse C_p is coincident with the "one" count of the down counting counter. At the end of this pulse C_p (while $\overline{Q}$ of pulse train switch flip-flop **214** is still high, just as this $\overline{Q}$ is about to go low,) there is an additional toggle input to both up-down counters from the fall of the pulse C_m on line **188** via gates **224** (FIG. **7**) and **246**, **248** (FIG. **9**). Accordingly, the counters end their half cycle, not in counts of "one" and "thirty-two", but in counts of "zero" and "thirty-three" and there remain when the clock pulse input train is cut off by operation of the pulse train switch. One full cycle has occurred and the first of the output pulses C_p has been produced. The fixed modulus counter again begins its count while the two reversible counters remain at counts of "thirty-three" and "zero", respectively, and the next cycle has started. The system will continue to recycle in this manner, in steady state oscillatory operation, until it is disturbed. Each reversible counter operates intermittently in opposite half cycles, with a full count of counter **44** occurring between successive half cycles. Thus, one full cycle of the system includes (a) one full count of the fixed counter and (b) one half cycle (a full count in but one direction) of both of the reversible counters that are operating in mutually opposite phase. If deemed necessary or desirable for certain application the fixed interval between successive half cycles of reversible counter operation may be eliminated whereby each half cycle of one sense would immediately follow a half cycle of opposite sense for each counter. This operation is readily achieved by causing pulses C_m to be fed to the reversible counters at all times, as by severing the line **217** between gate **236** and the pulse train switch, or eliminating, or by passing this switch entirely.

Consider now the situation where a burst of commanded increase frequency pulses **268** is provided as a counting input during the counting operation of the reversible counters. As discussed in connection with the counter content control circuit of FIG. **9**, commanded increase frequency pulses are fed as inputs only to that one of the two counters that is counting down. Accordingly, counter **48** in this exemplary situation has begun its downward count indicated by the straight line portion **280** (FIG. **10**) and upon receipt of the additional pulses **268**, counts down more rapidly, or at an increased slope in this heuristic representation, as indicated by the increased slope potion **282**. Upon cessation of the added input pulses **268**, the counter resumes its normal rate of count as indicated at **284**, until it reaches the count of one whereupon it provides at its output the negative going signal. This is fed to the direction control circuit to terminate this half cycle of the operation of both reversible counters and again provides an output pulse C_p. It will be noted, however, that since the rate of down counting of the counter **48** was increased during this half cycle of operation, the total time required for the counter to count from its high count to the count of one is less in this instance than it would be if the counting rate had remained unchanged. Accordingly, if the interval from the beginning of the first cycle to the occurrence of the first pulse C_p be designated as T_1 and the following interval between pulses C_p be designated as T_2, it will be seen that the latter interval is less than the former, whereby at this point the second frequency will be greater than the first, presuming that no other changes are made in the normal counting operation of the several counters. This temporary change in down-counting rate of counter **48** is, in effect, "remembered" by the system to result in a changed steady-state operation. This memory action may be understood by considering the effect of the shortened interval T_2 upon the count attained by the counter **46** which was counting up during the half cycle of reversible counter operation in which the rate of counting of counter **48** was temporarily and momentarily increased. Since it is termination of the downward cycle of the down-counting counter that stops operation of the concurrent half cycles of both of the reversible counters and further, since the count of one is attained in a shorter time by the down-counting counter in this situation, the up-counting counter will have attained a lower value of count when this particular half cycle is terminated. Thus, for example, if seven counts are included in the burst of increased frequency pulses **268**, the down-counting counter will reach the count of one when the up-counting counter reaches the count of 25 rather than its nominal high count of 32 (although both receive a single additional input, remaining at counts of "zero" and "twenty-six" respectively). Now the fixed modulus counter is reset, the pulse train switch feeds pulses to the fixed counter and the reversible counters temporarily stop operation. If no other changes were made in the system, the counter **46** which had reached a count of only 26 would thereupon count down from the count of 26 and both counters would, accordingly, continue to count to and from the counts of 0 and 26, thereby providing a steady-state oscillatory operation having a decreased period.

A second burst of commanded increased frequency input pulses **270** is shown in the next half cycle of reversible counter operation to illustrate the fact that these pulses may act upon either of the two counters. Thus, with regard to the frequency increase command pulses **270**, counter **46** is counting down and temporarily, as indicated at **286**, will increase the rate of its count upon receipt of pulses **270** and thereby reach the count of one sooner than it would have in the absence of the commanded increased frequency pulses **270**. Accordingly, the next output pulse C_p occurs at a time interval T_3 following the end of interval T_2 and the frequency is again increased to decrease the period so that interval T_3 is still smaller than the preceding interval T_2. Again, absent any further commanded increase or decrease frequency input pulses, the system has attained a steady-state operation at this now increased frequency and will continue to so operate until additional commands are received.

Now consider the case of commanded decrease frequency input as indicated by the burst of pulses **266**. These decrease frequency pulses in the illustrated expository arrangement are provided only to the reversible counter that is in up-counting mode, namely, counter **48**. Given the additional counting input, the up-counting counter has an increased rate of count as

indicated by the portion **288** of increased slope whereby it will reach a higher magnitude of count by the time that the down-counting counter **46** reaches its count of one and recycles the system. Again assume that the commanded frequency input pulses are seven in number, and assume the system to have been counting at its nominal or midpoint of operation before receipt of this decreased frequency command, namely, that the counters were counting to and from the count of thirty-three. After receipt of a burst of seven commanded decrease frequency pulses, the up-counter **48** will have achieved a total count of 40, when its count is stopped and this half cycle terminated. The counter **48** will hold this count of forty during the ensuing counting of the fixed modulus counter **44**. Upon the next half cycle of operation of the reversible counters, counter **48** begins to count down, not from the count of 33, but from the count of forty. Accordingly, it takes longer for this counter to reach the count of one and the half cycle of this counter and that of the up-counting counter are accordingly increased in time. Increasing the time of the count of the up-counting counter **46** allows this counter also to attain the new count level of forty assuming no further frequency disturbing inputs occur. Both reversible counters assume a new steady-state level of counting to and from the count of **40** which provides an increase in the period and decrease in frequency in accordance with the commanded signal.

As previously indicated, the method of changing frequency by adding pulses to the counter that is counting down or counting up in order to increase or decrease the output frequency, is but one of several modes of operating upon this pair of reversible counters to control the frequency and/or phase of the output signals. It will be readily appreciated that, instead of adding pulses during the counting cycle of either of these counters, pulses of the normal counting input pulse train C_m, could be inhibited. Frequency of the system output in such a situation is increased by inhibiting pulses that are normally counted by that counter which is in the up-counting mode. Conversely, output frequency is decreased by inhibiting pulses that are normally counted by the down-counting counter. In the former instance, by inhibiting pulses to the up-counting counter, it attains a lower total value of its count when the down-counting counter terminates both half cycles. As will be understood from the previous description, when the total count attained by either of these counters has been changed, and assuming no further input disturbances, both counters then assume the changed count and count to and from such value.

As illustrated in FIG. **12**, the commanded frequency increase or decrease pulses, designated as pulse train f_c in FIG. **12** and shown as bursts **266**, **268**, **270** in FIG. **10**, must be out of phase with pulses C_m that are normally counted by the reversible counters. A variety of well known arrangements are available to achieve this phasing. Nevertheless, in a system such as that described in the aforementioned application for Frequency Comparator, the clock pulses C_m are generated by a divide by five counter from a higher frequency train of master clock pulses C_{m1}. With such a circuit, it is convenient to employ suitable gating to provide the commanded frequency change pulse train f_c at the frequency of the counting input train C_m, but out of phase therewith. Illustrated in FIG. **13** is an arrangement that provides frequency and phase control pulses to the counters in response to input commands. A master clock source **291** provides a high frequency pulse train that is fed to a divider **292** which provides the two like frequency out of phase pulse trains, C_m and f_c. C_m is fed to the several counters via starting circuit **40** and switch **42** as previously described and f_c is fed as the first input to a NAND gate **294**. The latter is enabled by the pulse train switch flip-flop **214** by receiving a high input on line **296** from the $\overline{Q}$ side of the flip-flop when the latter is set and is feeding the pulse train C_m to the up-down counters. The commanded frequency change pulses f_c are fed through gate **294** to a switch **298** which is operated to provide an output on either of two lines **300**, **302** by an increase/decrease frequency command. The latter selects the sense of the commanded change. The change frequency pulses f_c are provided on output line **300** for increase command and these are fed to a gate **304** which is enabled for a given number of pulses or for a predetermined time interval by a frequency change magnitude command signal to provide at its output **306**, one or a commanded group of increase frequency pulses. Similarly, when switch **298** is in the decrease frequency state, the pulses f_c appear on output line **302** and are fed to a gate **308** which is enabled for a selected period of time by a commanded frequency change magnitude to provide a selected number of decrease frequency command pulses.

PHASE CONTROL

For operation of the fixed modulus counter **44** to control phase of the output signal, the phase retard or phase advance signals are also provided in an out-of-phase relation with or following the fall of one of the clock pulses C_m. This phase relation is illustrated in FIG. **11**. Accordingly, the phase relation of the frequency change command pulses, f_c, with respect to the clock pulses C_m may be the same as the phase relation between the clock pulses C_m and the advance or retard pulses. Conveniently, the same pulses f_c may be fed to a phase advance gate **310** (FIG. **13**) and a phase retard gate **312** which are respectively enabled for one or more of these pulses by a suitable phase advance command or phase retard command. Outputs of gates **310**, **312** are fed to the direct set terminals of flip-flops **120**, **122**, respectively, of the fixed modulus counter shown in FIG. 4*a*, 4*b* and 4*c*.

The illustrated arrangement of independent circuits for controlling frequency and phase has a number of advantages. Nevertheless, it will be readily appreciated that the reversible counters themselves may be employed for phase control. Such an operation may be achieved, for example, by successively commanding opposite sense but equal magnitude frequency changes. In yet another mode of operation, in order to effect a phase change, that is, a temporary non-steady-state frequency change of the system output by operation solely upon the reversible counters, it is necessary only to either add or inhibit like numbers of input pulses to both of the reversible counters together. For example, if ten pulses are added to the down-counting counter and 10 pulses are added to the up-counting counter during the same half cycle of operation, the up-counting counter will achieve its nominal count, assuming it to have been previously in a nominal counting state, 10 counts earlier and, at the same time, the down-counting counter will terminate both half cycles at a time that is earlier than its normal time of termination by an equal amount. Thus, the up-counting counter sees no net change in its total count. The same would be true if like numbers of counting inputs are inhibited from both counters simultaneously, whereby there is no steady-state affect upon the operation but a temporary change, namely, a phase advance or phase retard is achieved. The phase advance, of course, occurs in the situation where both reversible counters have pulses added thereto to thereby momentarily increase the rate of count, whereas, the phase retard situation occurs upon concurrent inhibition of groups of pulses to both counters.

ALTERNATE MODES AND ARRANGEMENTS

Although control of the system in phase or frequency has been described as achieved during counting operation of the reversible counters, it will be readily appreciated that the frequency changing operation can be achieved by controlling the count of these counters while they are at rest, that is, during the time that the fixed modulus counter **44** is in operation. Thus, for example, with reference to FIG. **10**, the dotted line **314** indicates the situation that would occur if the counter **48**, at rest at its maximum count during the counting operation of the fixed modulus counter, were to have a group of pulses fed thereto in a down-counting mode. This counter, here assumed to be at rest at a count of 32, then would have its count

decreased to some smaller number, 25 for example, and then upon termination of the count of the fixed modulus counter and occurrence of its output signal W, the counter **48** would begin to count down from this smaller value. In such a situation the counter **48**, upon operation of pulse train switch **42** to feed clock pulses to the reversible counters, would start counting down from its smaller count whereby it would reach the count of one at the same time as such count would be reached by following the curves **280**, **282**, and **284**, assuming, of course, that the count had been decreased by the same number of pulses in the change frequency input pulse group **268**. Similarly, as indicated by the dotted curve **316** in FIG. **10**, the counter remaining at rest at its high or full count, may be fed with a group of frequency change pulses in the up-count mode, whereby upon occurrence of the output signal W, this counter would start counting down from a higher count. In such a situation, a longer time would be required for the counter to reach the count of one whereby the concurrent up-counting counter would be enabled to reach a similar higher count and the frequency of the recycling reversible counters has been decreased.

Similar operations may be carried out with regard to the counter remaining at the zero count while the reversible counters are at rest as indicated by the dotted curve **318** of counter **46** in FIG. **10**. In this mode of operation, during operation of the fixed modulus counter **44**, a selected number of counts is added to the counter that is ready to start counting in its up mode and these counts are added so that the counter will begin counting not from the count of zero, but from some higher count such as the count of eight. Accordingly, presuming that no change has been made in the count of the other reversible counter during this time, counter **46** will proceed to count as indicated by the dotted line **318** and will reach a higher count by the time that the down-counting counter reaches its count of one to terminate half cycles of both counters. Thereafter, as previously described, the other counter will attain the same higher count and both counters will follow a steady-state operation of counting to and from the higher count whereby a steady-state frequency decrease has been achieved. Similarly, concurrent changes in the counts of both counters while these are at rest, will achieve phase change which, in effect, is a frequency change only in the immediately ensuring half cycle of operation of both of the reversible counters.

As previously described in connection with FIGS. **1** and **13**, the frequency and phase control signals may be derived either open-loop, as incrementally commanded signals, or may be provided by a closed-loop system that continually compares output phase and frequency of the pulse train C_p with some reference phase and frequency. Closed-loop operation of the system to provide automatic frequency and phase synchronization with respect to a reference can be achieved in a variety of ways. For example, analog signals representing the output phase and frequency may be generated and compared with analog signals representing the reference phase and frequency to thereby generate analog phase and frequency error signals. Such analog error signals may be readily transmitted to operate the frequency and phase adjusting circuits **36** and **38** of FIG. **1** to provide either qualitative or both qualitative and quantitative operation. For a qualitative operation as previously described, it is only necessary to determine the sense of the error and to control the system in opposite direction. For quantitative control, where a tighter feedback loop is required, both magnitude and sense of the error signal are employed to achieve a phase or frequency adjustment of controlled magnitude and direction.

A preferred embodiment of the variable frequency and phase system has been shown employing a fixed counter followed by a pair of reversible counters that generate a digitally controlled variable interval. In other arrangements, the reversible counters may be positioned at different points in a string or series of fixed interval generators or fixed modulus counters. For example, a second fixed modulus counter, substantially identical to, though not necessarily of equal counting capacity to the counter **44**, may be employed to follow the pair of reversible counters with the pulse train switch **42** rearranged to switch the clock pulses C_m to the three interval generators in sequence; that is, to either of the two fixed modulus counter or to the pair of reversible counters in the order of first fixed counter, reversible counters, second fixed counter, and then back to the same sequence of first fixed counter, reversible counters, second fixed counter. Obviously, many modifications may be made in this overall arrangement of fixed and variable interval generators.

The pair of reversible counters with the illustrated content and direction control may be operated as a controllable oscillatory circuit without any fixed interval generator or pulse train switch. In such arrangement, the counting input C_m is continuously fed to both reversible counters with no pulse train switch interposed. Output pulses C_p need only provide one element of the system output pulse train and actuate the direction control circuit. Such an arrangement provides a readily variable digital divider or a digital oscillator that is readily synchronized or otherwise controlled in either phase or frequency or both.

Although, digital counters are illustrated, it will be readily appreciated that other types of counters may be employed. For example, the conventional stair-case counter comprising a capacitive device that integrates each input pulse and stores the sum as a voltage level may be employed. The output or counting level of such a counter, of course, depends upon the voltage level to which the storage device is allowed to charge.

Use of the described variable phase and frequency system in an uninterruptible or standby power supply that is normally synchronized with a source of line voltage has many advantages. If the line voltage should fail with the system having been synchronized to a frequency other than the nominal 360 Hz. signal, it is relatively simple to separately sense a drop out of the line voltage source and then cause the system to move back to its nominal 360 cycle frequency or 33 count operation of the reversible counters. One way to achieve such an operation would be to employ a memory or a reversible counting operation to keep track of the net total or sum of commanded frequency change pulses, both plus and minus, and then to employ this total to restore the counter maximum counts to their nominal value.

An additional advantage of a system of the type described herein that can be precisely synchronized to outside signals and which, nevertheless, provides a timing source of great stability and accuracy, resides in the fact that in many systems of computer operations there may be remote terminals along distances away from, or at least not on the same power line as the master processor that is driven by the power supply. In such a case, the remote computer terminals may be driven by separate utility lines that vary in frequency and phase with regard to the power supply of the master. Induced hum could then result because of the difference in neutral and ground potentials at any one time in the system. An example of such an operation occurs in telemetry systems which transmit small, highly sensitive signals over long distances. Most telemetry systems involve bridges of one sort or another. Designers go to great lengths to balance these bridges, both for exciting frequency and its quadratures. Too large a quadrature could swamp the output of error amplifiers. In addition, such systems must be carefully balanced to ground so that no component of the power supply frequency or voltage will be transmitted through the bridge as a signal. All of these efforts would be of no avail if there were two power supply frequencies. As more computers are tied together from remote locations and with remote terminals by means of telemetry systems, the need for synchronizing all of the power supply systems, both in frequency and phase, becomes greater. With such synchronization of all power supplies, hum cancellation is much easier to achieve. Additional advantages reside in the increased safety of the system since hum voltages can attain large values. Particularly from the standpoint of in-

verter circuits employed in a power supply, these voltages may be dangerous.

A still further advantage of the described arrangement derives from the fact that present electronic circuitry is often built with individually replaceable modules or integrated circuit cards or chips. Accordingly, with a variable frequency system involving two or more fixed, and/or variable interval generators collectively making up the total interval of the circuit output, there is readily available still further frequency control. It is no problem to change one or more entire circuit cards, substituting for the variable interval, a second shorter or longer fixed interval or any selected one of different fixed intervals so that the total output period may be made up of a first fixed interval and then a second fixed interval. For example, if at some time the total system output is desired to be changed to some predetermined fixed frequency, the second, variable, interval generator module or card is removed and replaced with a card having the desired fixed interval generator.

SUMMARY

There has been disclosed a timing system that is selectively variable and controllable in both frequency and phase and that specifically lends itself to digital mechanization. The generation of a basic timing interval made up of two parts, a longer fixed interval and a shorter variable interval, allows the synchronization of the timing system to some outside source and provides, by use of a relatively short variable portion of the period, a set of built-in limits beyond which the output frequency cannot be varied. A significant aspect of the system derives from the use of a novel arrangement of oscillatory counters each of which counts and then starts counting anew when a selected count is attained. This mode of operation may be employed as a selectively variable dividing circuit that is mechanized by a pair of recycling reversible counters operable in positive and negative half cycles and interconnected to operate in mutually opposite phase so that the attainment of a selected count by one of the counters in one of its half cycles achieves termination of a specific half cycle of both of the counters. Thus, by causing a variation of the total count contained in one of the counters the length of the cycle of both is readily controlled and a totally digital system is provided that may be controlled, both in frequency and phase.

The foregoing detailed description is to be clearly understood as given by way of illustration and example only, the spirit and scope of this invention being limited solely by the appended claims.

I claim:

1. A variable frequency and phase control system comprising means for generating a first interval,
- means responsive to termination of said first interval for generating a second interval,
- said means for generating a second interval comprising a pair of reversible counters connected to count in mutually opposite directions and means for causing both counters to reverse counting direction when either attains a predetermined count,
- means for providing an output signal at a preselected point of one of said intervals,
- means for selectively varying the duration of said second interval, and
- means responsive to termination of said second interval for initiating said first interval.

2. The system of claim 1 wherein the maximum duration of said second interval is not greater than the allowable tolerance of frequency variation of said system.

3. The system of claim 1 including
- means for momentarily varying the length of said first interval.

4. A counting circuit comprising
- first and second bi-directional counters connected to count in mutually opposite directions in response to counting inputs thereto, and
- means responsive to attainment of a selected count of each of said counters when counting in one of said opposite directions for simultaneously changing the counting direction of both counters.

5. The circuit of claim 4 including
- control means for changing the time required for one of said counters to attain said selected count.

6. The circuit of claim 4 wherein said selected count is a terminal count.

7. The circuit of claim 5 wherein said control means comprises means for changing the count attained by said one counter in one of said directions.

8. In combination
- first and second reversible counters, each operable in positive and negative half cycles and both connected to operate in mutually opposite phase,
- means responsive to termination of one of the half cycles of the first counter for terminating a concurrent half cycle of the second counter, said means comprising means for initiating the next half cycle of said second counter.

9. The structure of claim 8 wherein said last mentioned means comprises
- an interval generator,
- means for initiating operation of said interval generator upon said termination of said one half cycle, and means responsive to termination of the interval of said interval generator for initiating said next half cycle.

10. The structure of claim 9 including
- means responsive to termination of one half cycle of said second counter for terminating a concurrent half cycle of the first counter, said last mentioned means comprising
- means for initiating the next half cycle of said first counter.

11. The structure of claim 10 wherein both said means for initiating the next half cycles of said counters comprises
- an interval generator,
- means for initiating operation of said interval generator upon termination of either of said one half cycles of said first and second counters, and
- means responsive to termination of the interval of said interval generator for initiating said next half cycles of both said counters.

12. A digital signal generator controllable in both frequency and phase comprising
- a clock pulse generator,
- a fixed modulus counter;
- first and second reversible counters,
- a pulse train switch interposed between the clock pulse generator and the counters for selectively directing pulses from the generator to either said fixed modulus counter or to both said reversible counters,
- a direction control circuit for controlling the reversible counters to count in mutually opposite directions, first and second counter content control circuits interposed between the pulse train switch and the first and second reversible counters, respectively, each said counter content control comprising
  - means for feeding pulses from said pulse train switch to the counting input of the associated reversible counter, and
  - means responsive to the direction control circuit for controlling the counting input to the associated reversible counter;
- means responsive to attainment of a selected count by either of said reversible counters for resetting said fixed counter, for operating the pulse train switch to direct pulses from the pulse generator to the fixed modulus counter, and for actuating said direction control circuit to change the counting direction of both said reversible counters, and means responsive to attainment of a predetermined count by the fixed modulus counter for operating the pulse train switch to feed pulses to the reversible counters.

13. The system of claim 12 wherein said counter content control comprises

means for feeding additional pulses to the associated counter when it is counting in a selected direction in order to attain a predetermined change of the counting period of the reversible counters.

14. The system of claim 12 wherein said counter content control comprises

a source of commanded increase or decrease frequency pulses,

first and second coincidence gates,

means responsive to said direction control circuit for enabling said first and second gates when the associated counter is counting up and down, respectively,

means for feeding said commanded decrease frequency pulses to said first gate when it is enabled during the up-counting of the associated counter, and

means for feeding said commanded increase frequency pulses to the second gate when it is enabled during the down-counting of the associated counter.

15. The system of claim 12 including

means for providing a system output pulse whenever either of the reversible counters attains a selected count.

16. The system of claim 12 including

means for controlling frequency and phase of the system output pulses.

17. The system of claim 16 wherein said means for controlling phase and frequency comprises

a source of commanded frequency change pulses, and said counter content control circuit, the latter circuit further comprising

means for additionally feeding said commanded frequency change pulses to the associated reversible counter during its counting operation in one direction for commanded frequency increase and during its operation in the other direction for commanded frequency decrease.

18. The system of claim 16 wherein said phase control means comprises

means for operating said counter content control to achieve an increase of frequency followed by a decrease in frequency.

19. The system of claim 16 wherein said phase control means comprises

means for temporarily changing the count of the fixed modulus counter.

20. The method of operating a pair of reversible counters comprising the steps of

feeding pulses as counting inputs to both of the counters, controlling the counters to count up and down in mutually opposite phase,

changing the direction of counting of both counters when either counter attains a preselected count, whereby the counters cyclically reverse their counting directions.

21. The method of claim 20 including

means for generating an output signal each time that at least one of said counters attains a predetermined count.

22. The method of claim 20 including the step of

controlling the cyclical period of said pair of reversible counters, said last mentioned step comprising

the step of selectively and temporarily varying the count of one of said counters.

23. The method of claim 20 including the step of

controlling the phase of the cyclical operation of said reversible counters, said last mentioned step comprising

effecting a change in the count of one of the counters in a first sense, and

subsequently effecting a change in the count of said counter in an opposite sense.

24. The method of claim 20 including the step of

controlling the phase of the cyclical operation of the said counters, said last mentioned step comprising

changing the counts of both said counters by substantially equal amounts and in mutually opposite senses.

25. In combination

first and second oscillatory circuits connected to operate in mutually opposite phase, each operable through successive positive and negative half cycles,

means responsive to occurrence of a selected point in one of the half cycles of either circuit for terminating a concurrent half cycle of both circuits and initiating the following opposite sense half cycle of both circuits.

26. A timing generator comprising

first and second reversible counters connected to count in mutually opposite directions,

means responsive to attainment of a predetermined count by at least one of said reversible counters for changing the counting direction of both of said reversible counters, and

means for generating an output signal when one of said counters attains a predetermined count.

27. An oscillatory circuit comprising

a counter,

means for feeding input pulses to be counted by the counter, and

means responsive to attainment of a selected count for causing the counter to start counting anew, said last-mentioned means comprising

first and second cyclically reversible counter connected to count in mutually opposite directions in response to pulses from said means for feeding input pulses,

means for reversing the counting direction of both said reversible counters at a selected count of at least one of the reversible counters, and

means responsive to attainment of said count by said first-mentioned counter for causing both said reversible counter to start counting anew in respectively opposite directions.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,651,414 Dated March 21, 1972

Inventor(s) Robert S. Jamieson

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the specification,

Column 2, line 9, change "2aa-2d" to --2a-2d--.

In the claims,

Claim 12, line 4, change ";" to --,--.

Claim 12, line 21, change ";" to --,--.

Claim 27, line 8, change "counter" to --counters--.

Claim 27, line 16, change "counter" to --counters--.

Signed and sealed this 26th day of September 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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