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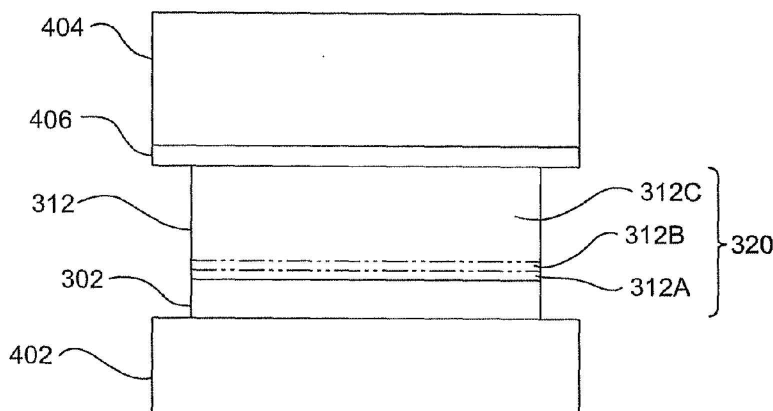
FIG. 7



(57) Abstract: Methods and apparatus for forming a semiconductor on glass-ceramic structure provide for: subjecting an implantation surface of a donor semiconductor wafer to an ion implantation process to create an exfoliation layer of the donor semiconductor wafer; bonding the implantation surface of the exfoliation layer to a precursor glass substrate using electrolysis; separating the exfoliation layer from the donor semiconductor wafer to thereby form an intermediate semiconductor on precursor glass structure; sandwiching the intermediate semiconductor on precursor glass structure between first and second support structures; applying pressure to one or both of the first and second support structures; and subjecting the intermediate semiconductor on precursor glass structure to heat-treatment step to crystallize the precursor glass resulting in the formation of a semiconductor on glass- ceramic structure.

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GLASS-CERAMIC-BASED SEMICONDUCTOR-ON-INSULATOR STRUCTURES AND METHOD FOR MAKING THE SAME

PRIORITY

[0001] This application claims priority to United States Patent Application number 12/324,576, filed November 26, 2008, titled "GLASS-CERAMIC-BASED SEMICONDUCTOR-ON-INSULATOR STRUCTURES AND METHOD FOR MAKING THE SAME".

BACKGROUND

[0002] The present invention relates generally to semiconductor structures, and more particularly to glass-ceramic containing semiconductor-on-insulator structures and methods for making glass-ceramic based semiconductor-on-insulator structures.

[0003] To date, the semiconductor material most commonly used in semiconductor-on-insulator structures has been silicon. Such structures have been referred to in the literature as silicon-on-insulator structures and the abbreviation "SOI" has been applied to such structures. The present invention relates to semiconductor-on-insulator structures in general, including silicon-on-insulator structures.

[0004] For ease of presentation, the following discussion will at times be in terms of silicon-on-insulator structures. The references to this particular type of semiconductor-on-insulator structure are made to facilitate the explanation of the invention and are not intended to, and should not be interpreted as, limiting the invention's scope in any way.

[0005] The SOI abbreviation is used herein to refer to semiconductor-on-insulator structures in general, including, but not limited to, silicon-on-insulator structures. Similarly, the SOG abbreviation is used to refer to semiconductor-on-glass structures in general, including, but not limited to, silicon-on-glass structures. The SOG nomenclature is also intended to include semiconductor-on-glass-ceramic structures, including, but not limited to, silicon-on-glass-ceramic structures. The abbreviation SOI encompasses SOGs.

[0006] Silicon-on-insulator technology is becoming increasingly important for high performance thin film transistors, solar cells, and displays, such as, active matrix displays. The silicon-on-insulator wafers consist of a thin layer of substantially single crystal silicon

(generally 0.1-0.3 microns in thickness but, in some cases, as thick as 5 microns) on an insulating material.

[0007] Various ways of obtaining such a wafer include epitaxial growth of Si on lattice matched substrates; bonding of a single crystal silicon wafer to another silicon wafer on which an oxide layer of SiO_2 has been grown, followed by polishing or etching of the top wafer down to, for example, a 0.1 to 0.3 micron layer of single crystal silicon; or ion-implantation methods in which either hydrogen or oxygen ions are implanted either to form a buried oxide layer in the silicon wafer topped by Si in the case of oxygen ion implantation or to separate (exfoliate) a thin Si layer to bond to another Si wafer with an oxide layer as in the case of hydrogen ion implantation. Of these three approaches, the approaches based on ion implantation have been found to be more practical commercially. In particular, the hydrogen ion implantation method has an advantage over the oxygen implantation process in that the implantation energies required are less than 50% of that of oxygen ion implants and the dosage required is two orders of magnitude lower.

[0008] Exfoliation by the hydrogen ion implantation method was initially taught in, for example, Bister et al., "Ranges of the 0.3-2 MeV H^+ and 0.7-2 MeV H_2^+ Ions in Si and Ge," Radiation Effects, 1982, 59:199-202, and has been further demonstrated by Michel Bruel. See Bruel, U.S. Patent No. 5,374,564; M. Bruel, Electronic Lett. 31, 1995 pp 1201-1202; and L. Dicioccio, Y. Letiec, F. Letertre, C. Jaussad and M. Bruel, Electronic Lett. 32, 1996, pp 1144-1145.

[0009] The method typically consists of the following steps. A thermal oxide layer is grown on a single crystal silicon wafer. Hydrogen ions are then implanted into this wafer to generate subsurface flaws. The implantation energy determines the depth at which the flaws are generated and the dosage determines flaw density. This wafer is then placed into contact with another silicon wafer (the support substrate) at room temperature to form a tentative bond. The wafers are then heat-treated to about 600 °C to cause growth of the subsurface flaws for use in separating a thin layer of silicon from the Si wafer. The resulting assembly is then heated to a temperature above 1,000 °C to fully bond the Si film with SiO_2 underlayer to the support substrate, i.e., the unimplanted Si wafer. This process thus forms a silicon-on-insulator structure with a thin film of silicon bonded to another silicon wafer with an oxide insulator layer in between.

[0010] Cost is an important consideration for commercial applications of SOI structures. To date, a major part of the cost of such structures has been the cost of the silicon wafer which supports the oxide layer, topped by the Si thin film, i.e., a major part of the cost has been the support substrate. In discussing support substrates, some of the above references have mentioned quartz glass, glass, and glass-ceramics. Other support substrate materials listed in these references include diamond, sapphire, silicon carbide, silicon nitride, ceramics, metals, and plastics.

[0011] Although glass and glass-ceramics had been disclosed in the prior art as a alternative to silicon as the base wafer, no practical techniques for forming SOI structures using glass or glass-ceramics as support substrates in had been developed.

[0012] U.S. Patent Nos. 7,176,528 and 7,192,844 disclose SOI structures that have one or more regions composed of a layer of a substantially single-crystal semiconductor (e.g., doped silicon) attached to a support substrate composed of an oxide glass or an oxide glass-ceramic. The oxide glass or oxide glass-ceramic is preferably transparent and preferably has a strain point of less than 1000°C, a resistivity at 250°C that is less than or equal to 10^{16} Ω-cm, and contains positive ions (e.g., alkali or alkaline-earth ions) which can move within the glass or glass-ceramic in response to an electric field at elevated temperatures (e.g., 300-1000°C).

[0013] Although these oxide glass or an oxide glass-ceramic based SOI structures were improvement over the aforementioned prior art SOI structures, the glasses utilized in this oxide glass oxide glass or an oxide glass-ceramic based SOI structures can not withstand the high temperature processing utilized in high performance display or electronic applications without a resulting deformation of the substrate; e.g. the growth of high temperature thermal gate oxides which are used to allow high performance TFTs to be fabricated on the silicon film.

[0014] US Patent Application No. 2006/0038228 co-assigned to the current assignee, addresses this issue. This reference discloses semiconductor-on-insulator structure that exhibit a first layer including a semiconductor material, attached to a second layer including a glass or glass-ceramic, with the strain point of the glass or glass-ceramic equal to or greater than about 800° C. These structures are capable of being used in these high performance display or electronic applications, yet are significantly lower cost to manufacture than the

prior art silica/quartz-based SOI structures, thus satisfying the demand in the high performance display or electronic fields for lower cost SOI structures and resultant devices.

[0015] Although these oxide glass or glass-ceramic based SOI structures were an improvement over the aforementioned prior art SOI structures, the glass-ceramic based semiconductor on insulator structures were difficult to produce and did not result in strongly bonded structures having a sufficiently large in situ barrier layer due, in part, to the lack of mobile ions in the glass ceramic which was cerammed/crystallized prior to the bonding of the glass-ceramic substrate to the silicon.

[0016] Efforts have been made to improve upon the prior art glass-ceramic based SOI structures, resulting SOI structures which are strongly bonded and exhibit a sufficiently large barrier layer. Details of such an approach may be found in U.S. Patent Application No. 12/238,784, the entire disclosure of which is hereby incorporated by reference. The process involves first bonding a semiconductor material to a glass precursor substrate using electrolysis, followed by ceramming the glass precursor substrate to nucleate and crystallize the glass. It has been found that the process may result in a semiconductor on glass-ceramic structure that includes significant warpage, possibly severe warpage (e.g., 1000 microns). The warping may occur due to a thermal expansion mismatch between the un-cerammed glass and the semiconductor as well as glass compaction during nucleation and crystallization. As a result of the warping, the cerammed SiOG-C structure may not be useful in further processes, such as epi-growth or fabrication of electronic circuits, etc.

[0017] The present invention addresses the shortcomings of prior work in the area of SOI fabrication and results in an SiOG-C structure with significantly less warpage.

SUMMARY

[0018] Methods and apparatus for forming a semiconductor on glass-ceramic structure provide for: subjecting an implantation surface of a donor semiconductor wafer to an ion implantation process to create an exfoliation layer of the donor semiconductor wafer; bonding the implantation surface of the exfoliation layer to a precursor glass substrate using electrolysis; separating the exfoliation layer from the donor semiconductor wafer to thereby form an intermediate semiconductor on precursor glass structure; sandwiching the intermediate semiconductor on precursor glass structure between first and second support structures; applying pressure to one or both of the first and second support structures; and

subjecting the intermediate semiconductor on precursor glass structure to heat-treatment step to crystallize the precursor glass resulting in the formation of a semiconductor on glass-ceramic structure.

[0019] The first support structure may be a semiconductor support wafer and the sandwiching step may include contacting the exfoliation layer with the semiconductor support wafer. The intermediate semiconductor on precursor glass structure may be oriented with the precursor glass substrate atop the exfoliation layer, and the second support structure may be formed from metal or ceramic material having a weight sufficient to provide the applied pressure when placed atop the precursor glass substrate. An intermediate material (such as a graphite material) may be interposed between the second support structure and the precursor glass substrate.

[0020] The applied pressure may be less than about 1 pound per square inch, between about 0.1 pound per square inch and about 1 pound per square inch, or about 0.8 pounds per square inch. In alternative embodiments advantageous results are obtained when the applied pressure is than about 0.1 pound per square inch, such as between about 0.03 – 0.1 pounds per square inch.

[0021] The bonding process may include: heating at least one of the glass substrate and the donor semiconductor wafer; bringing the precursor glass substrate into direct or indirect contact with the donor semiconductor wafer through the exfoliation layer; and applying a voltage potential across the precursor glass substrate and the donor semiconductor wafer to induce the bond. The temperature of the precursor glass substrate and the semiconductor wafer may be elevated to within about 150°C of the strain point of the glass substrate; and the temperatures of the precursor glass substrate and the semiconductor wafer may be elevated to different levels. The voltage potential across the precursor glass substrate and the semiconductor wafer may be between about 100 to 2000 volts.

[0022] The heat-treatment step may include subjecting the intermediate semiconductor on precursor glass structure to temperatures between about 800 – 1000°C to crystallize the precursor glass resulting in the formation of a semiconductor on glass-ceramic structure. The support step is carried out during the heat-treatment step such that warpage of the semiconductor on glass-ceramic structure may be no more than 200 microns, such as on the order of 10s of microns, such as about 70 microns.

[0023] The semiconductor-on-insulator structures and methods for making semiconductor-on-insulator structures of the present invention result in a number of advantages over prior art. The present invention satisfies the longstanding need in the art for lower cost substrates for use in high performance and electronic applications, when compared to fused silica or quartz based SOI structures. More particularly, the incorporation of the glass-ceramic allows the SOI wafer to be subject to high temperature processes such as thermal gate oxide without the deformation that would be expected with the prior art lower temperature strain point glasses. Additionally, the utilization of these high strain point glass or glass-ceramic as the substrate material for the SOI structures results in a minimized substrate compaction (i.e., dimensional change) which is typically experienced for lower strain point substrate materials during the TFT fabrication process. Finally, the resulting SOI structure exhibits significantly less warpage than other fabrication techniques.

[0024] Additional features and advantages of the invention will be set forth in the detailed description which follows, and in part will be readily apparent to those skilled in the art from the description or recognized by practicing the invention as described in the written description and claims hereof, as well as in the appended drawings.

[0025] It is to be understood that both the foregoing general description and the following detailed description are merely exemplary of the invention, and are intended to provide an overview or framework for understanding the nature and character of the invention as it is claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings are not necessarily to scale, and sizes of various elements may be distorted for clarity. The drawings illustrate one or more embodiment(s) of the invention, and together with the description serve to explain the principles and operation of the invention.

[0027] FIG. 1 is a schematic cross-sectional view of a semiconductor-on-glass-ceramic structure according to one or more embodiments of the present invention;

[0028] FIG. 2 is a schematic cross-sectional view of a semiconductor-on-glass-ceramic structure according to one or more further embodiments of the present invention;

[0029] FIGS. 3-6 are schematic cross-sectional views of steps of a method for making a semiconductor-on-insulator structure according to one or more embodiments of the present invention;

[0030] FIG. 7 is a schematic cross-sectional view of one or more steps of the method for making the semiconductor-on-insulator structure to achieve a glass-ceramic substrate according to one or more embodiments of the present invention;

[0031] FIG. 8 is a TOF-SIMs depth profile of a semiconductor-on-glass-ceramic structure of the type detailed in the description herein and made in accordance with one or more aspects of the embodiments of the invention described herein;

[0032] FIGS. 9A, 9B, 9C, 9D are topographic and line-graphs illustrating the warpage of a semiconductor-on-glass-ceramic structure of the type detailed in the description herein and made in accordance with one or more aspects of the embodiments of the invention described herein;

[0033] FIGS. 10A, 10B, 10C, 10D are topographic and line-graphs illustrating the warpage of a semiconductor-on-glass-ceramic structure of the type detailed in the description herein and made in accordance with one or more further aspects of the invention;

[0034] FIGS. 11A and 11B are line-graphs illustrating the surface texture of the precursor glass substrate following the ceramming process in accordance with one or more further aspects of the invention; and

[0035] FIGS. 12A, 12B, 12C, 12D, and 12E are topographic and line-graphs illustrating the warpage of a semiconductor-on-glass-ceramic structure of the type detailed in the description herein and made in accordance with one or more further aspects of the invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0036] With reference to the drawings, wherein like numerals indicate like elements, there is shown in FIG. 1 an SOG layered structure 100 in accordance with one or more embodiments of the present invention. The SOG structure 100 preferably includes a semiconductor component 102 comprised of a substantially single crystal semiconductor material layer 104 and a single-crystal semiconductor material with an enhanced oxygen content layer 106. The

SOG layered structure further includes a third layer 108 which comprises an oxide glass material, and a fourth layer 110 which comprises a glass-ceramic material.

[0037] Reference is now made to FIG. 2, which shows another embodiment of an SOG layered structure 200 of the present invention. The SOG structure 200 is comprised of a five-layer structure comprising a 2 layer semiconductor component 102, an oxide glass layer 108 and a two-layer oxide glass-ceramic substrate 110 which comprises positive ions. Specifically, the SOG layered structure 200 is comprised of the following layers: (1) a substantially single-crystal semiconductor material layer 104; (2) a semiconductor barrier layer 106 with an enhanced oxygen content; (3) an oxide glass material barrier layer 108; (4) an oxide glass-ceramic layer 204 with an enhanced positive ion concentration of modifier positive ions, including at least one alkaline earth modifier ion from the oxide glass material layer 108 with a reduced positive ion concentration; and, (5) an oxide glass-ceramic layer 206 comprised of glass ceramic having a bulk concentration.

[0038] The semiconductor on glass-ceramic structure is capable of high use temperature in excess of 1000°C, thus allowing applications in RF/high performance electronics, Photovoltaics, Digital Imaging, etc. which are not possible with prior art silicon on glass products.

[0039] The semiconductor-on-glass-ceramic structures of the present invention can be made with virtually any desirable semiconductor, glass and glass-ceramic layer thicknesses. For example, each of the layers desirably has a thickness less than about 1 mm. More desirably, the semiconductor layers desirably have a thickness less than about 1 mm. In certain desirable embodiments of the invention, the first semiconductor component has a thickness between about 10 nm and 500 nm. The glass and glass-ceramic layer each desirably has a thickness between about 0.1 mm and about 10 mm. More desirably, the glass-ceramic layer has a thickness between about 0.5 mm and about 1 mm. For some applications of semiconductor-on-glass-ceramic structures, glass-ceramic layers having a thickness greater than or equal to 1 mm are desirable, e.g., to avoid parasitic capacitive effects which arise when standard semiconductor-on-insulator structures having a silicon/SiO_2/silicon configuration are operated at high frequencies. In the past, such thicknesses have been difficult to achieve.

[0040] In general terms, the glass-ceramic layer 110 needs to be thick enough to support the semiconductor component 102 through the process steps of the invention, as well

as subsequent processing performed on the semiconductor-on-glass-ceramic structure. Although there is no theoretical upper limit on the thickness of the glass-ceramic substrate, a thickness beyond that needed for the support function or that desired for the ultimate semiconductor-on-glass-ceramic structure is generally not preferred since the greater the thickness of the precursor glass and so-formed glass-ceramic substrate, the lower the electric field strength within the substrate during later-described bonding step (B, specifically the voltage application of B3) of the method of the method described herein below and in U.S. Patent No. 7,192,844 for the same applied voltage difference.

[0041] The semiconductor material in the semiconductor layer/component 102 can be a silicon-based semiconductor material, or can be any other suitable type of semiconductor material, such as a III-V semiconductor, a II-IV semiconductor, a II-IV-V semiconductor, or a IV semiconductor. Examples of silicon-based semiconductor materials suitable for use as the semiconductor material of the first layer include silicon (e.g., undoped silicon, n-doped silicon, p-doped silicon); germanium-doped silicon (SiGe); and silicon carbide (SiC). Examples of other semiconductor materials which can be used in the first layer include Ge-, GaAs-, GaP-, and InP-based materials. The semiconductor layer material can have a wide range of CTEs depending on the material. For example, the semiconductor material of the first layer can have a CTE (at 25 °C) between about $20x10^{-7}$/°C and about $70x10^{-7}$/°C.

[0042] The semiconductor material layer is in the form of a substantially single-crystal material. The word "substantially" is used to take account of the fact that semiconductor materials normally contain at least some internal or surface defects either inherently or purposely added, such as lattice defects or a few grain boundaries. The word "substantially" also reflects the fact that certain dopants may distort or otherwise affect the crystal structure of the bulk semiconductor material.

[0043] The glass precursor and the so-formed glass barrier layer 108 and the glass-ceramic substrate 110 are formed from an oxide-based glass. Although not required, the embodiments described herein preferably include an oxide glass or glass-ceramic exhibiting a strain point of greater than 900°degrees C. As is conventional in the glass making art, the strain point is the temperature at which the glass or glass-ceramic has a viscosity of $10^{14.6}$ poise ($10^{13.6}$ Pa.s).

[0044] The oxide glass barrier layer and the glass-ceramic layer are desirably formed from a silica-based glass precursor. In one embodiment, SiO_2 is present in the precursor

glass and so-formed glass-ceramic at a concentration of at least about 50 wt. %. In a still further embodiment, SiO_2 is present in a concentration of at least about 55 wt%. Glass-ceramics suitable for use in the present invention include those which exhibit the crystalline phases mullite and spinel.

[0045] For certain applications, e.g., display applications, the glass-ceramic is desirably substantially transparent in the visible, near UV, and/or near IR wavelength ranges. For example, the glass-ceramic is desirably substantially transparent in the 350 nm to 2 um wavelength range.

[0046] The precursor glass (for forming the subsequent glass-ceramic layer and the oxide glass barrier layer) can be produced from conventional raw materials using a variety of techniques familiar to the skilled artisan, and can be attached to the semiconductor layer/component using the methods described herein below, and in U.S. Patent No. 7,192,844, entitled "GLASS-BASED SOI STRUCTURES", which is hereby incorporated herein by reference in its entirety.

[0047] In certain embodiments of the invention, the precursor glass desirably includes at least some positive ions which during the bonding step (Step B, and particularly the voltage application of Step B3) of the method described herein below and in U.S. Patent No. 7,192,844, move in the direction of the applied electric field, i.e., away from the interface between the bonded first (semiconductor) and second (precursor glass) layers and toward the back side of the second layer. Alkali ions, e.g., Li^+, Na^+, and/or K^+ ions, are suitable positive ions for this purpose because they generally have higher mobilities than other types of positive ions typically incorporated in glasses and glass-ceramics. Precursor glasses having no alkali ions are preferred for use in the present invention, though small amounts of alkali are acceptable for certain applications. For example, glasses having other mobile ions, such as alkaline-earth ions (e.g., Ca^{2+}, Mg^{2+}, Ba^{2+}, Sr^{2+}) or other positive ions such as Ag^+, Cu^+, Zn^{2+} and various transition metal ions are preferred in the second layer in the semiconductor-on-insulator structures of the present invention.

[0048] In embodiments of the invention in which the precursor glass contains alkali or alkaline-earth ions, the concentrations of alkali and alkaline-earth ions can vary over a wide range, representative concentrations being between 0.1 and 40 wt% on an oxide basis. Desirable alkali and alkaline-earth ion concentrations are 0.1-5 wt% on an oxide basis in the

case of alkali ions. Many nominally alkali-free glasses have tens to hundreds of ppm of alkali contaminant, which can move during step B3 of the method described herein below.

[0049] The precursor glass (for forming the subsequent glass-ceramic layer 110 and the oxide glass barrier layer 108) for use in the inventive SOI structures includes a family of transparent glasses within the following composition, as calculated in weight percent on an oxide basis: 50-65% SiO_2, 15-25% Al_2O_3, 6-15% ZnO, 0-6% MgO, 0-10% TiO_2 , 0-10% ZrO , 0-15% Cs_2O, 0-5% BaO, ZnO+MgO in combination being greater than or equal to about 8%, and TiO_2 +ZrO_2 in combination being greater than about 4%. Representative compositions for use in the present invention are detailed in Table I

[0050] The so-formed glass-ceramic material layers 110 contain spinel as the predominant crystal phase. By predominant crystal phase, it is meant that this crystal phase is at least about 75 volume percent, more preferably at least 85 percent, and most preferably at least 95 percent of the total crystalline phases present. The glass-ceramics of the present invention are at least about 20 weight percent crystalline phases dispersed within a glassy matrix.

[0051] Preferably, the glass oxide barrier layer 108 and the glass-ceramic substrate 110 exhibit coefficients of thermal expansion between about $22\text{-}42\times10^{-7}$ /° C, over the temperature range of 25-300° C, more preferably between about $30\text{-}42\times10^{-7}$ /° C., and most preferably between about $35\text{-}40\times10^{-7}$ /° C, providing a close thermal expansion match to silicon. By transparent it is meant that 1.1 mm thick sheets of the glass-ceramics of the present invention exhibit greater than 85 percent transmittance over the visible region (400 nm to 700 nm) of the spectrum. Preferably, for certain applications, it is also desirable that these sheets exhibit some transmittance in the near ultraviolet as well, for example, greater than 50 percent over the region 350-400 nm

[0052] Transparent glass-ceramic materials containing spinel as the predominant crystal phase are described in more detail in U.S. Patent No. 5,968,857 entitled "Glass-Ceramics", which is hereby incorporated herein by reference in its entirety.

Table I

Composition (wt %)	Example 1	Example 2	Example 3	Example 4	Example 5	Example 6	Example 7
SiO_2	60.3	58.3	57.0	55.0	57.0	57.3	59.3

Al_2O_3	19.0	20.2	18.0	21.0	21.8	18.5	19.1
ZnO	9.0	8.4	14.0	13.5	14.0	11.6	9.0
MgO	2.1	4.2	--	--	--	2.4	2.5
BaO	2.1	--	--	--	2.1	2.0	2.1
Cs_2O	--	4.0	4.0	--	--	--	
TiO_2	--	3.0	--	5.5	5.2	5.0	5.0
ZrO_2	7.5	5.0	7.0	--	--	3.0	3.0
As_2O_5	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Crystal Phase	spinel	spinel	spinel	spinel	spinel	spinel	spinel
Strain Point (°C)	>900	>900	>900	>900	>900	>900	>900
CTE($x10^{-7}$/°C)	37	38	37	37	37	38	37

[0053] As will be appreciated by the skilled artisan, the strength of the bond between the single crystal semiconductor material and the oxide containing material is a key property of a semiconductor-on-insulator structure. High bond strength and durability are very important to ensure that the semiconductor-on-insulator structure can withstand the processing associated with the manufacture of thin film transistors and other devices within or on the structure. The bond strength between the semiconductor component and the precursor substrate (and ultimately between the semiconductor and the oxide glass layer in final semiconductor-on-glass-ceramic) is desirably at least 8 J/m^2. More desirably, the bond strength between the bonded layers is at least 10 J/m^2. In certain especially desirable embodiments of the invention, the bond strength is at least 15 J/m^2. Bond energies can be determined using indentation measurements, which can be performed using a Nano Indenter II (MTS Systems Corporation, Eden Prairie, MN) equipped with a Berkovich diamond indenter. As the skilled artisan will appreciate, other equipment can be used to perform indentation measurements. Indentations are to be made covering a range of loads, and the region immediately surrounding the indentation is to be examined for evidence of delamination. Calculation of bond energy is made in accordance with D.B. Marshall and A.G. Evans, "Measurement of Adherence of Residually Stressed Films by Indentation. I. Mechanics of Interface Delamination", J. Appl. Phys, 56[10] 2632-2638 (1984), the relevant

portions of which are hereby incorporated herein by reference. Further details of the bond energy determination can be found in U.S. Patent Application Serial No. 10/779,582.

[0054] The methods described herein below and in U.S. Patent No. 7,176,528, the entire disclosure of which is hereby incorporated by reference, allow the skilled artisan to make semiconductor-on-glass-ceramic structures. With reference to FIG. 3, a donor semiconductor is subject to ion implantation, and thereafter a precursor glass substrate and the implanted donor semiconductor wafer are then subject to an electrolysis bonding process, followed by separation of a portion of the donor semiconductor wafer to form an intermediate structure comprising a precursor glass substrate having a thin semiconductor layer thereon. Portions of this electrolysis are discussed below, however, the basic process involves subjecting the precursor glass substrate 102 and donor semiconductor wafer 120 to temperature, voltage, and pressure for some period of time.

[0055] FIG. 3 illustrates process steps that may be carried out in order to produce an intermediate structure in connection with fabricating the semiconductor on glass-ceramic structure 100 and 200 of FIGS. 1 and 2, respectively. First step (Step A), involves creating an exfoliation layer 302 in the donor semiconductor wafer 304. For the purposes of discussion, the donor semiconductor wafer 304 is preferably a substantially single crystal Si wafer.

[0056] The exfoliation layer 302 is preferably a relatively thin layer of silicon that may be separated from the remaining portion of the Si semiconductor donor wafer 306 following the bonding and separation steps (Steps B and D which will be discussed later herein). Although the embodiments of the present invention are not limited to any particular method of forming the exfoliation layer, one suitable method includes the use of ion implantation to create a weakened region 308 below the surface 310 of the silicon wafer 304. By way of example, hydrogen ion implantation may be employed, although other ions or multiples thereof may be employed, such as boron + hydrogen, helium + hydrogen, or other ions known in the literature for exfoliation. Again, any other known or hereinafter developed technique suitable for forming the exfoliation layer 302 may be employed without departing from the spirit and scope of the present invention.

[0057] In one embodiment a single step hydrogen implantation alone is used and involves subjecting the Si wafer to an H ion implant dosage of between $1x10^{16}$-$1x10^{17}$ ions/cm^2. In another, low dosage embodiment, the Ge wafer is subject to multiple ion, low dosage,

implant steps. Particularly, a combination H and He low dosage implantation is utilized and involves first subjecting the Ge wafer to an H ion implant dosage ranging between $1x10^{15}$ to $5x10^{16}$ ions/cm^2 , followed by a Helium implant dosage, again at low dosage level ranging between $1x10^{15}$ to $5x10^{16}$ ions/cm^2.

[0058] No matter what technique is employed to create the exfoliation layer 302, the Si donor wafer 304 is preferably treated to reduce the (e.g., hydrogen) ion concentration on the surface 310. For example, the donor semiconductor wafer 304 is preferably washed and cleaned and the exfoliation layer surface 310 is preferably subject to mild oxidation. The mild oxidation treatments may include treatment in oxygen plasma, ozone treatments, treatment with hydrogen peroxide, hydrogen peroxide and ammonia, hydrogen peroxide and an acid or a combination of these processes. It is expected that during these treatments hydrogen terminated surface groups oxidize to hydroxyl groups, which in turn also makes the surface of the silicon wafer hydrophilic. The treatment is preferably carried out at room temperature for the oxygen plasma or ozonated water and at temperature between 25-150°C for the ammonia or acid treatments.

[0059] Regarding the precursor glass wafer 312, it is washed in a detergent followed by distilled water and thereafter further washed with nitric acid and again followed by distilled water.

[0060] It should be noted that these treatments are optimum. If hydrogen ion concentration is not reduced there is a repulsive force between the silicon and glass wafers which may be overcome during the bonding process via application of higher pressure.

[0061] Following ion implantation, the respective structures are preferably bonded together using an electrolysis bonding process (Step B). A preferred electrolysis bonding process is described in U.S. Patent No. 7,192,844, where portions of this process are discussed below. Initially, appropriate surface cleaning of the respective donor wafer surface 310 and precursor glass substrate surface 314 is preferably carried out. Thereafter, the donor wafer surface 310 and precursor glass substrate surface 314 are brought into direct or indirect contact (Step B1) to achieve the arrangement schematically illustrated in FIG. 4.

[0062] Referring now to FIG. 5, prior to or after the contact, the structure(s) comprising the donor Si semiconductor wafer 304, the exfoliation layer 302 and the precursor glass substrate 312 are heated (Step B2) under a differential temperature gradient; T_1 and T_2 respectively. Preferably the precursor glass substrate 312 is heated to a higher temperature (T_2) than the Si

donor semiconductor wafer 304 and exfoliation layer 302 (T_1). By way of example, the temperature difference between the precursor glass substrate 304 and the donor Si semiconductor wafer 304 is at least 1°C, although the difference may be as high as about 100 to about 150°C. This temperature differential is desirable for a glass having a coefficient of thermal expansion (CTE) matched to that of Silicon since it facilitates later separation of the exfoliation layer 302 from the remaining donor semiconductor wafer 306 due to thermal stresses.

[0063] Once the temperature differential between the precursor glass substrate 312 and the Si donor semiconductor wafer 304 is stabilized, mechanical pressure (P) is applied to the bonded assembly. In one embodiment, the pressure range is between about 1 to about 50 psi. Application of higher pressures, e.g., pressures above 100 psi, might cause breakage of the glass wafer.

[0064] The precursor glass substrate 312 and the Si semiconductor wafer 304 are ideally taken to a temperature within about +/- 150° C of the strain point of the precursor glass substrate 304.

[0065] Next, a voltage (V1/V2) is applied across the precursor glass/donor wafer intermediate assembly, with the Si semiconductor donor wafer 304 at the positive electrode (V1) and the glass substrate 312 the negative electrode (V2); Step B3. The application of the voltage potential causes alkaline earth ions (or alkali ions) in the glass substrate 312 to move away from the Si semiconductor/precursor glass interface 310/314 further into the glass substrate 312. More particularly, substantially all of the modifier positive ions of the glass substrate 312 migrate away from the higher voltage potential of the Si semiconductor donor wafer 304. This accomplishes two functions: (i) an alkaline earth (or alkali) ion free interface 310/314 is created; and (ii) the precursor glass substrate 312 becomes very reactive and bonds to the Si semiconductor layer 304 strongly with the application of heat at relatively low temperatures.

[0066] Referring now to FIG. 6, after the intermediate semiconductor on a (precursor) glass substrate structure is held under these conditions for some time (e.g., approximately 1 hr or less), the voltage is removed and the intermediate structure is allowed to cool to room temperature. The remaining Si semiconductor donor wafer 306 is separated from the exfoliation layer 302 which is left bonded to the precursor glass substrate 312 (Step C); this may include some peeling if they have not already become completely free. Separation may

occur as temperature is ramped up, at a dwell temperature, or as temperature is ramped down. The separation is preferably accomplished via fracture of the exfoliation layer 302 due to thermal stresses. Alternatively or in addition, mechanical stresses such as water jet cutting or chemical etching may be used to facilitate the separation.

[0067] It should be noted that the atmosphere during the bonding (heating and application of voltage) process may be either an inert atmosphere, such as nitrogen and/or argon or simply an ambient air atmosphere.

[0068] Following separation what is obtained is intermediate semiconductor on a (precursor) glass substrate 320; essentially a thin Si semiconductor/exfoliation layer 302 bonded to a glass substrate 312 as illustrated in FIG. 6. Again, it should be noted that the precursor glass substrate bonded to the Si semiconductor layer exhibits a reduced positive ion concentration layer 312A, an enhanced positive ion concentration layer 312B, adjacent the reduced positive ion concentration layer 312A, and a bulk glass layer 312C.

[0069] With reference to FIG. 7, the intermediate SOI with precursor glass substrate 320 is prepared for a ceramming process. In particular, the intermediate semiconductor on precursor glass structure 320 is sandwiched between first and second support structures 402, 404, and pressure is applied to one or both of the first and second support structures 402, 404 through the ceramming process (to be described later herein).

[0070] By way of example, the first support structure 402 may be a semiconductor support wafer (e.g., silicon, which is desirable when the exfoliation layer 302 is silicon). The exfoliation layer 302 is contacted with the first support structure 402. The first support structure 402 may be of a suitable thickness and flatness to provide support through the ceramming process. For example, the thickness may be between about 0.1 cm to 10 cm. The flatness may be between below about 100 microns, such as below about 50 microns.

[0071] In the illustrated example, the intermediate semiconductor on precursor glass structure 320 is oriented with the precursor glass substrate 312 atop the exfoliation layer 302. The second support structure 404 may be formed from metal or ceramic material having a weight sufficient to provide a desirable applied pressure when placed atop the precursor glass substrate 312. As an option, an intermediate material 406, such as a graphite material (GRAFOIL or equivalent) may be interposed between the second support structure 404 and the precursor glass substrate 312. The applied pressure may be less than 1 pound per square

inch, between about 0.1 pound per square inch and about 1 pound per square inch, such as about 0.8 pound per square inch.

[0072] Although the above-described ranges of pressure have produced satisfactory results, it has been found that in some circumstances, the application of pressure to the intermediate semiconductor on precursor glass structure 320 results in some surface texture irregularities on a surface of the precursor glass substrate 312 opposite to the exfoliation layer 302. For example, the texture of the second support structure 404 and/or the intermediate material 406 (GRAFOIL or equivalent) may be transferred to the surface of the precursor glass substrate 312 at some pressures. In this regard, alternative embodiments of the invention may include limiting the applied pressure to less than about 0.1 pounds per square inch, such as between about 0.03 to about 0.1 pound per square inch. The precise pressure limitation may be dependent on the temperature properties of the precursor glass substrate 312 (such as the liquidus temperature). Additionally, the surface texture of the second support structure 404 that is directly or indirectly (e.g., through the intermediate material 406) in contact with the precursor glass substrate 312 may be controlled. For example a surface texture of about 300 grit or higher may reduce the likelihood that undesirable texture features are imparted to the precursor glass substrate 312 from the second support structure 404, the intermediate material 406, or the combination thereof.

[0073] The intermediate semiconductor on precursor glass substrate 320 is then cerammed via a heat treatment step in an inert atmosphere such as argon; Step D (Not shown). The ceramming or heat-treatment step generally follows a heat treatment cycle where the structure 320 is held at a certain temperature to nucleate the crystals in the precursor glass 312 followed by a higher temperature hold for crystal growth. In a separate embodiment a heat treatment that does not involve nucleation hold temperature may be utilized; in this embodiment the ramp up schedule to the crystal growth hold temperature is sufficiently slow to achieve the necessary nucleation of the crystals: a rate no greater than 50°C/hr is capable of accomplishing this, nucleation hold-free, crystal growth.

[0074] In one or more embodiments, the cerramming or heat-treatment schedule for a spinel glass-ceramic-based semiconductor-on-glass ceramic structure, includes a nucleation hold at 800C for 2 hours followed by crystal growth hold at 1000°C for 2-4 hours.

[0075] As a result of the heat-treatment a portion of the precursor glass substrate 312 remains glass and a portion is converted to a glass-ceramic structure. This is further illustrated in

FIGS. 6-7. Specifically, the portion which remains an oxide glass is that portion of the glass closest to the semiconductor 302, the aforementioned reduced positive ion concentration layer 312A. This is due to the fact that there is a lack of spinel forming cations Zn, Mg in this portion of the precursor glass 312 due to the fact that all the positive modifier ions have moved away from the interface as a result of the bonding process. At some depth into the precursor glass (specifically that portion of the precursor glass material with an enhanced positive ion concentration 312B) there are sufficient ions to enable crystallization of that glass portion so as to form glass-ceramic layer 312B with an enhanced positive ion concentration. It follows that the remaining precursor glass portion (the bulk glass portion 312C) also possesses sufficient spinel forming cations to achieve crystallization. The resultant glass-ceramic structure is thus a two layer glass-ceramic portion comprised of a layer having an enhanced positive ion concentration 312B, which is adjacent the remaining oxide glass layer 312A, and a bulk glass-ceramic layer 312C.

[0076] Notably, the resultant semiconductor on glass and glass-ceramic 320 exhibits significantly less warpage than previously achieved. Indeed, by providing the proper thickness and flatness of the support structures 402, 404 as well as the appropriate pressure through the ceramming process, the warpage of the semiconductor on glass-ceramic structure 320 may be controlled to be no more than about 200 microns, more particularly, on the order of 10s of microns, such as about 70 microns, in some cases less that 45 microns (e.g., for a 100 mm diameter semiconductor layer), or in other cases less that 65 microns (e.g., for a 200 mm diameter semiconductor layer). These warpage levels are compared to about 1000 microns using prior fabrication techniques.

[0077] The crystallized glass ceramic with silicon film on top has advantages over the glass based compositions in that the glass ceramic based wafers are capable of sustaining significantly higher temperatures during device fabrication or other processing. Furthermore, the high temperatures capability to allow sepitaxial growth of silicon or other semiconductors on the semiconductor-on-glass-ceramic wafer.

EXAMPLE 1

[0078] The present invention is further described by the following non-limiting example. A 100mm diameter, 100 microns thick silicon wafer was implanted with hydrogen ions at dosage of $8X10^{16}$ ions/cm2 and implantation energy of 100KeV using commercially

available, room temperature ion implantation techniques. The implanted wafer was then treated in oxygen plasma to oxidize the surface groups. A 100mm in diameter precursor glass wafer was produced and comprised a composition in weight percent of: 60.3% SiO_2, 19% Al_2O_3, 2.1 % MgO, 2.1% BaO, 1.0% As_2O_5, 7.5% ZrO_2 and 9.0% ZnO. The precursor glass wafer was then ultrasonically washed for 15 minutes in detergent utilizing a Fischer Scientific Contrad 70 apparatus. Thereafter the precursor glass wafer was placed in a distilled water rinse, subjected to an ultrasonic bath for 15 minutes, soaked in 10% nitric acid for a period of 1 hour, and finally rinsed again in distilled water.

[0079] Both the silicon and precursor glass wafers were finally cleaned in spin washer dryer utilizing distilled water and thereafter were allowed to dry in a clean room. The two wafers were brought into contact to create a room temperature pre-bond and then placed in a Suss Microtech bonder. The precursor glass wafer was placed on the "negative" electrode and the silicon wafer was placed on the "positive" electrode.

[0080] The two wafers were then differentially heated in vacuum atmosphere (10^{-3} millibars); the silicon wafer to a temperature of 545°C and the precursor glass wafer to a temperature and 595°C. Thereafter the wafers were subject to a potential of 1750 Volts which was applied across the wafer surfaces. The wafers were held under these conditions for a period of 20 minutes. Following this sustained application of voltage, the voltage was brought to zero and the wafers were cooled to room temperature.

[0081] Following cooling it was observed that the wafers could be separated easily, resulting in a thin layer of silicon bonded to the precursor glass wafer. Specifically, it was observed that an excellent quality sample with a strongly adhered thin silicon film (500 nm) on glass wafer surface was obtained via this process.

[0082] The intermediate silicon on precursor glass structure was then sandwiched such that the silicon exfoliation layer of the intermediate silicon on precursor glass structure contacted a silicon support wafer of about 600 micron thickness and a ceramic (fused silica) support structure contacted the precursor glass (as in FIG. 7). The ceramic support structure applied a 0.8 psi pressure to the structure.

[0083] The intermediate silicon on precursor glass structure was then subjected to heat treatment in an argon atmosphere at 800°C for a period of 2 hours followed by further treatment at 1000°C for 2 hours to crystallize the glass wafer portion of the silicon on glass so as to produce a silicon on glass-ceramic structure. It should be noted that the silicon film

layer of so-produced silicon on glass-ceramic structure remained intact and did not delaminate or crack.

[0084] The silicon on glass-ceramic structure so-produced by the techniques above was subjected to a ToF-SIMS analysis as follows. Two ion beams were employed using the dual beam strategy--one for intermittent sputtering and another for analyzing the newly created surface. Analysis was performed using a TRIFT II instrument manufactured by Physical Electronics, Inc., Eden Prairie, Minn. A low energy Cs beam was used to sputter in synchronization with a pulsed Ga beam for analysis. A small piece of the sample was cleaved to fit the ToF-SIMS sample holder (~1 cm^2). A 5 kV $^{133}Cs^+$ beam was used for sputtering in conjunction with 15 kV, 600 pA $^{69}Ga^+$ beam for analysis. The Cs beam was rastered over 500 $\mu m \times 500$ μm area of the sample; the Ga beam analyzed a 50 $\mu m \times 50$ μm window at the center of the Cs-sputtered region.

[0085] The results of this ToF-SIMS analysis are shown in FIG. 8. The following can be observed in an examination of FIG. 8: (1)) an oxide glass layer beginning at a depth of 0.15 nm (designated as AA) and ending at a depth of about 0.175 nm (designated as BB); (2) a first glass-ceramic layer, beginning at a depth of 0.175 (designated as BB) and ending at a depth of 0.3 nm (designated CC), having an enhanced positive ion concentration of modifier positive ions, including at least one alkaline earth modifier ion from the first glass-ceramic layer; and (2) a second glass-ceramic layer, beginning at about a depth of 0.3 nm, exhibiting the bulk glass composition.

[0086] Measurements of the warpage of the silicon on glass-ceramic structure were also made using a suitable measurement tool as would be understood by a skilled artisan. FIGS. 9A and 9B illustrate top view and perspective views, respectively, of the topology of the silicon on glass-ceramic structure. FIG. 9C is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 9C-9C in FIG. 9A. FIG. 9D is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 9D-9D in FIG. 9A. Each of these line graphs show that the warpage is no more than about 70 microns.

EXAMPLE 2

[0087] The testing carried out in Example 1 was repeated in a further test with some changes. In particular, a precursor silicon wafer of 100 mm diameter and 525 microns thick was used

to prepare the intermediate silicon on precursor glass structure. The intermediate silicon on precursor glass structure was then sandwiched such that the silicon exfoliation layer of the intermediate silicon on precursor glass structure contacted a silicon support wafer of about 600 micron thickness and a ceramic (fused silica) support structure contacted the precursor glass (as in FIG. 7). The ceramic support structure applied a pressure of about 0.032 psi to the structure. The intermediate silicon on precursor glass structure was then subjected to heat treatment in an argon atmosphere at 800°C for a period of 2 hours followed by further treatment at 1000°C for 2 hours to crystallize the glass wafer portion of the silicon on glass so as to produce a silicon on glass-ceramic structure.

[0088] Measurements of the warpage of the silicon on glass-ceramic structure were made using a suitable measurement tool as would be understood by a skilled artisan. FIGS. 10A and 10B illustrate top views of flatness and micro-waviness, respectively, of the silicon on glass-ceramic structure. FIG. 10C is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 10C-10C in FIG. 10A. FIG. 10D is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 10D-10D in FIG. 10A. Each of these line graphs show that the warpage is no more than about 31 microns. FIGS. 11A and 11B are graphs showing the measured surface texture, which indicate substantially no surface texture resulting from the second support structure 404, the intermediate material 406, or the combination thereof.

EXAMPLE 3

[0089] The testing carried out in Examples 1 and 1 was repeated in a further test with some additional changes. In particular, a precursor silicon wafer of 200 mm diameter and 525 microns thick was implanted with hydrogen ions at a dosage of $4.2X10^{16}$ ions/cm2 and implantation energy of 100KeV using commercially available, room temperature ion implantation techniques. The precursor silicon wafer was used to prepare the intermediate silicon on precursor glass structure. The intermediate silicon on precursor glass structure was then sandwiched such that the silicon exfoliation layer of the intermediate silicon on precursor glass structure contacted a silicon support wafer of about 600 micron thickness and a ceramic (fused silica) support structure contacted the precursor glass (as in FIG. 7). The ceramic support structure applied a pressure of about 0.039 psi to the structure. The intermediate silicon on precursor glass structure was then subjected to heat treatment in an

argon atmosphere at 800°C for a period of 2 hours followed by further treatment at 1000°C for 2 hours to crystallize the glass wafer portion of the silicon on glass so as to produce a silicon on glass-ceramic structure.

[0090] Measurements of the warpage of the silicon on glass-ceramic structure were made using a suitable measurement tool as would be understood by a skilled artisan. FIGS. 12A, 12B, and 12C illustrate top views of the flatness, micro-waviness, bow/warp, respectively, of the silicon on glass-ceramic structure. FIG. 12D is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 12D-12D in FIG. 12A. FIG. 12E is a line graph of the flatness of the silicon on glass-ceramic structure from the point of view illustrated as 12E-12E in FIG. 12A. Each of these line graphs show that the warpage is no more than about 56 microns. No visible surface texture was found resulting from the second support structure 404, the intermediate material 406, or the combination thereof.

[0091] It will be apparent to those skilled in the art that various modifications and variations can be made to the present invention without departing from the spirit and scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

CLAIMS

1. A method of forming a semiconductor on glass-ceramic structure, comprising:

subjecting an implantation surface of a donor semiconductor wafer to an ion implantation process to create an exfoliation layer of the donor semiconductor wafer;

bonding the implantation surface of the exfoliation layer to a precursor glass substrate using electrolysis;

separating the exfoliation layer from the donor semiconductor wafer to thereby form an intermediate semiconductor on precursor glass structure;

sandwiching the intermediate semiconductor on precursor glass structure between first and second support structures;

applying pressure to one or both of the first and second support structures; and

subjecting the intermediate semiconductor on precursor glass structure to heat-treatment step to crystallize the precursor glass resulting in the formation of a semiconductor on glass-ceramic structure.

2. The method of claim 1, wherein:

the first support structure is a semiconductor support wafer; and

the sandwiching step includes contacting the exfoliation layer with the semiconductor support wafer.

3. The method of claim 1, wherein:

the intermediate semiconductor on precursor glass structure is oriented with the precursor glass substrate atop the exfoliation layer;

the second support structure is formed from metal or ceramic material having a weight sufficient to provide the applied pressure when placed atop the precursor glass substrate.

4. The method of claim 3, further comprising interposing an intermediate material between the second support structure and the precursor glass substrate.

5. The method of claim 4, wherein the intermediate material includes a graphite material.

6. The method of claim 1, wherein the applied pressure is one of: less than about 1 pound per square inch, between about 0.1 pound per square inch and about 1 pound per square inch, and about 0.8 pounds per square inch.

7. The method of claim 1, wherein the applied pressure is one of: less than about 0.1 pound per square inch, and between about 0.03 - 0.1 pound per square.

8. The method of claim 1, wherein a surface finish of the first or second support structure that is in direct or indirect contact with the precursor glass substrate is about 300 grit or higher.

9. The method of claim 1, wherein the step of bonding includes:

heating at least one of the glass substrate and the donor semiconductor wafer;

bringing the precursor glass substrate into direct or indirect contact with the donor semiconductor wafer through the exfoliation layer; and

applying a voltage potential across the precursor glass substrate and the donor semiconductor wafer to induce the bond.

10. The method of claim 9, wherein at least one of:

the temperature of the precursor glass substrate and the semiconductor wafer are elevated to within about 150°C of the strain point of the glass substrate; and

the temperatures of the precursor glass substrate and the semiconductor wafer are elevated to different levels.

11. The method of claim 9, wherein the voltage potential across the precursor glass substrate and the semiconductor wafer is between about 100 to 2000 volts.

12. The method of claim 1, wherein the heat-treatment step includes subjecting the intermediate semiconductor on precursor glass structure to temperatures between about 800 – 1000°C to crystallize the precursor glass resulting in the formation of a semiconductor on glass-ceramic structure.

13. The method of claim 12, wherein the support step is carried out during the heat-treatment step such that warpage of the semiconductor on glass-ceramic structure is no more than 200 microns.

14. The method of claim 13, wherein the support step is carried out during the heat-treatment step such that warpage of the semiconductor on glass-ceramic structure is on the order of 10s of microns.

15. The method of claim 14, wherein the support step is carried out during the heat-treatment step such that warpage of the semiconductor on glass-ceramic structure is about 70 microns.

16. A semiconductor on glass-ceramic structure comprising:

a semiconductor material component comprising a substantially single-crystal semiconductor material layer and a single-crystal semiconductor material with an enhanced oxygen content layer;

an oxide glass material layer; and

a glass-ceramic layer,

wherein warpage of the semiconductor on glass-ceramic structure is no more than about 200 microns.

17. The semiconductor on glass-ceramic structure of claim 16, wherein the warpage of the semiconductor on glass-ceramic structure is on the order of 10s of microns.

18. The semiconductor on glass-ceramic structure of claim 16, wherein the warpage of the semiconductor on glass-ceramic structure is about 70 microns.

19. The semiconductor on glass-ceramic structure of claim 16 wherein the glass ceramic further comprises a first layer having an enhanced positive ion concentration of modifier positive ions, including at least one alkaline earth modifier ion from the first glass-ceramic layer; and a second layer comprising bulk glass-ceramic.

20. The semiconductor on glass-ceramic structure of claim 16, wherein the oxide glass and the glass-ceramic is free of alkali ions.

FIG. 1

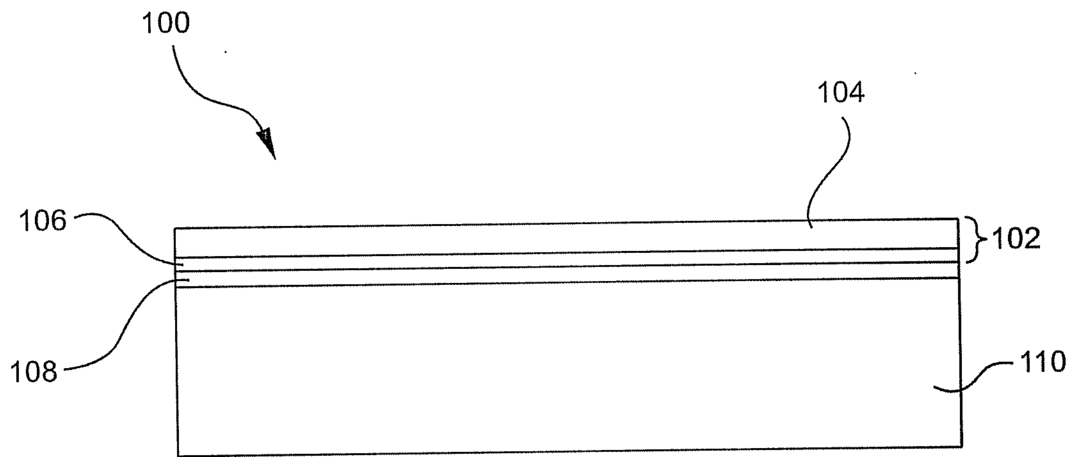


FIG. 2

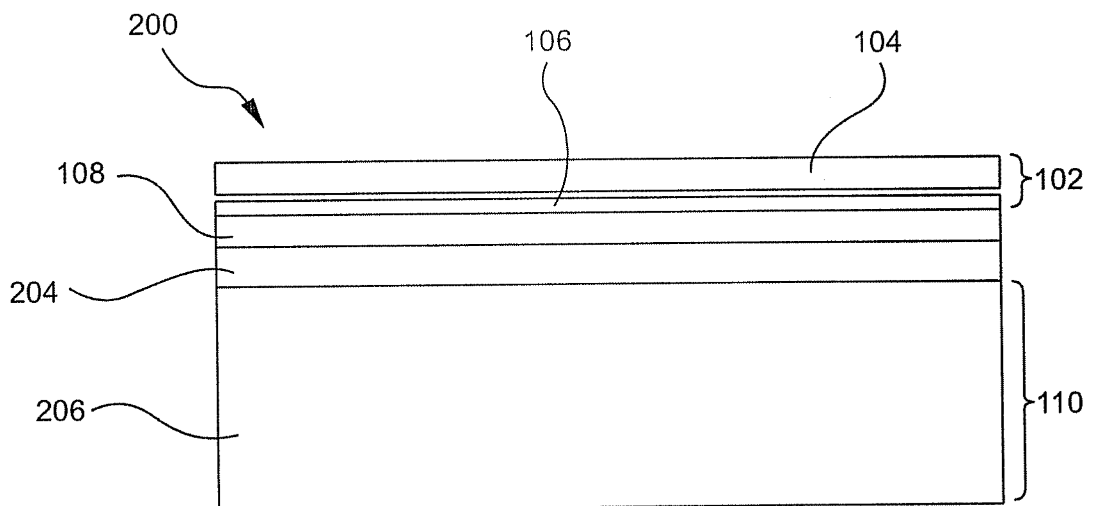


FIG. 3

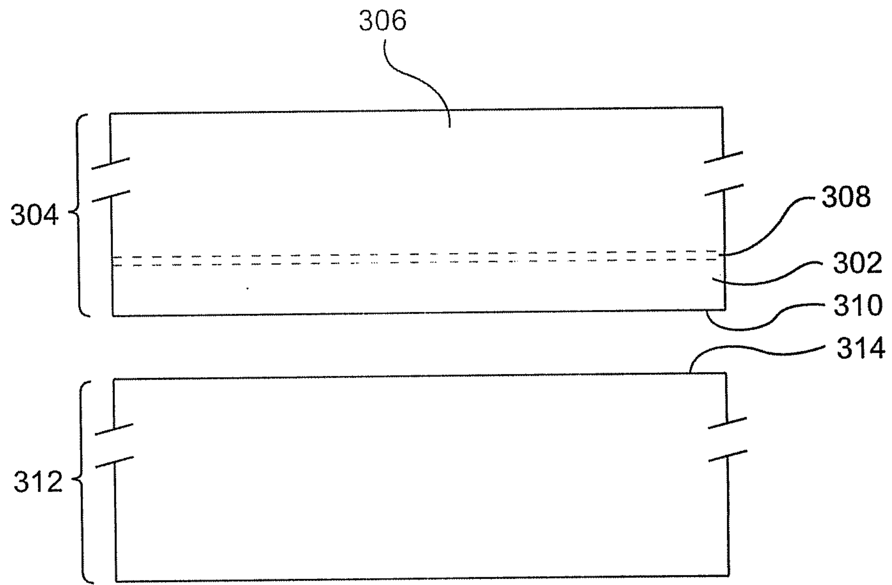


FIG. 4

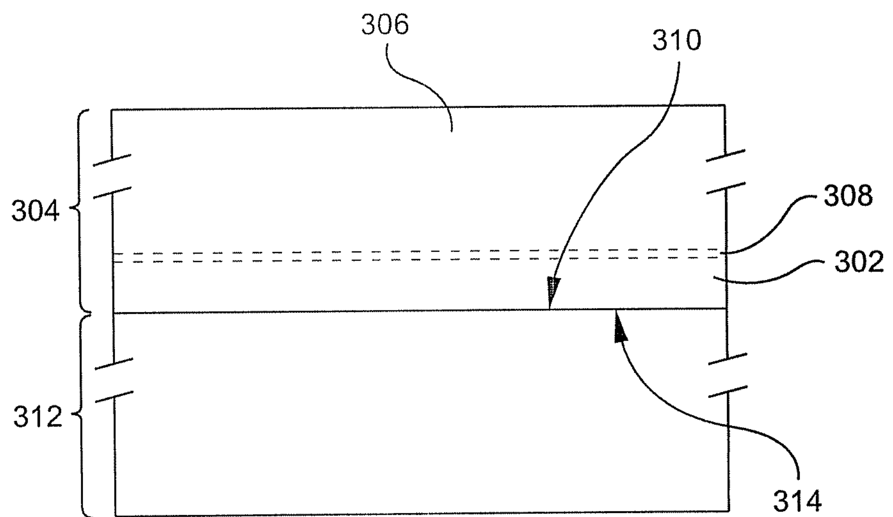


FIG. 5

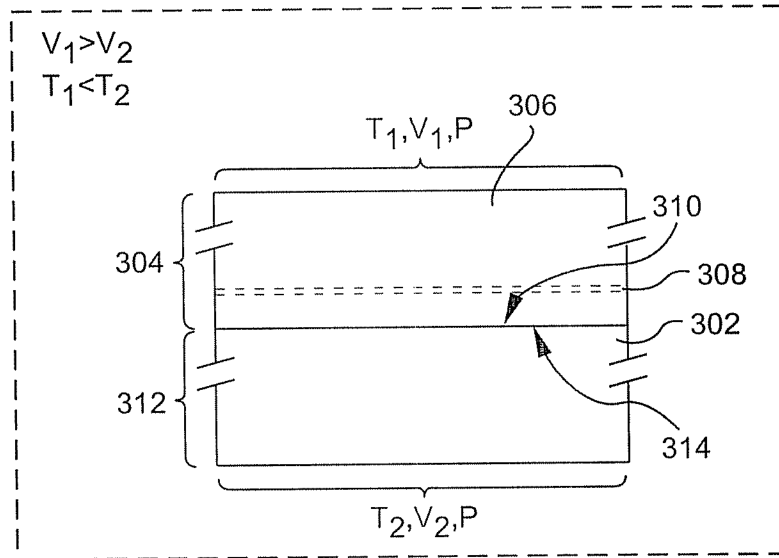


FIG. 6

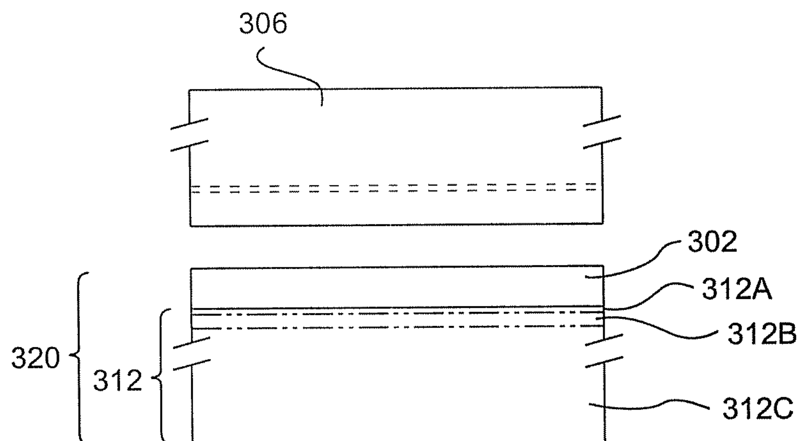


FIG. 7

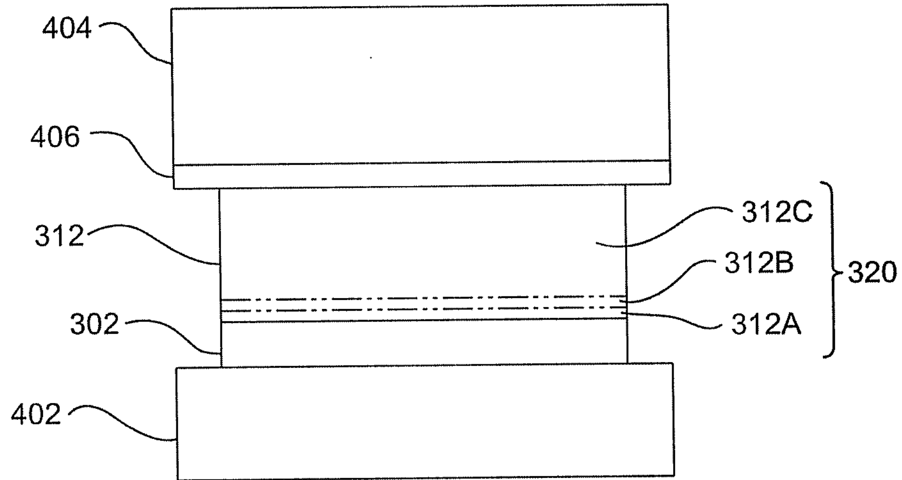


FIG. 8

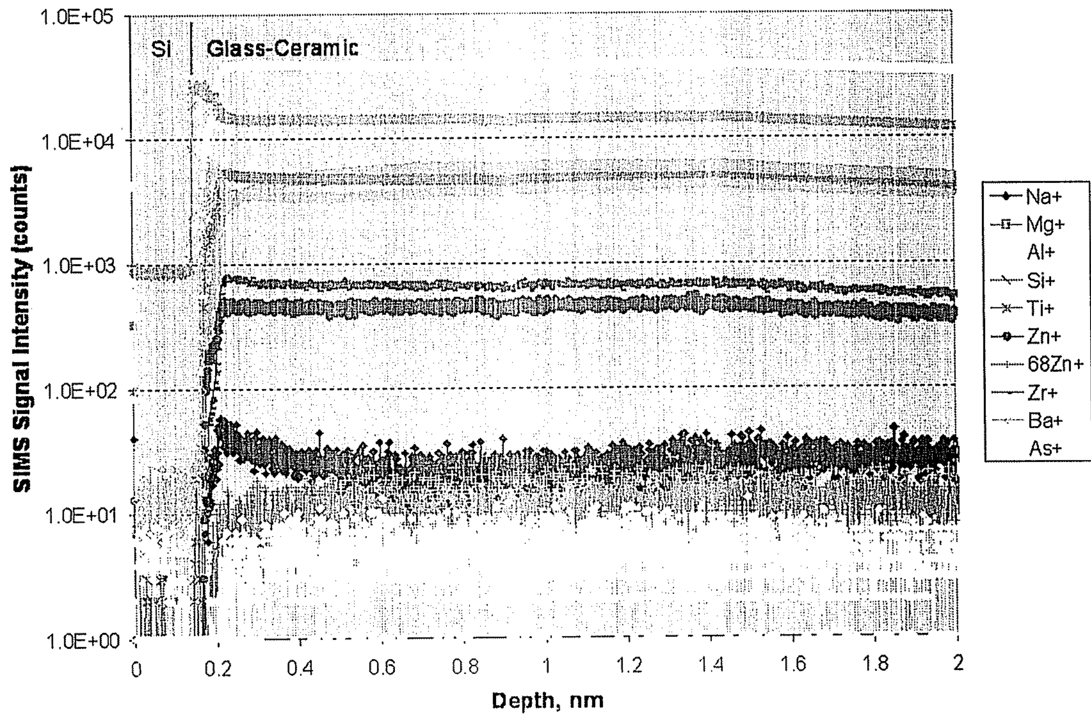


FIG. 9A

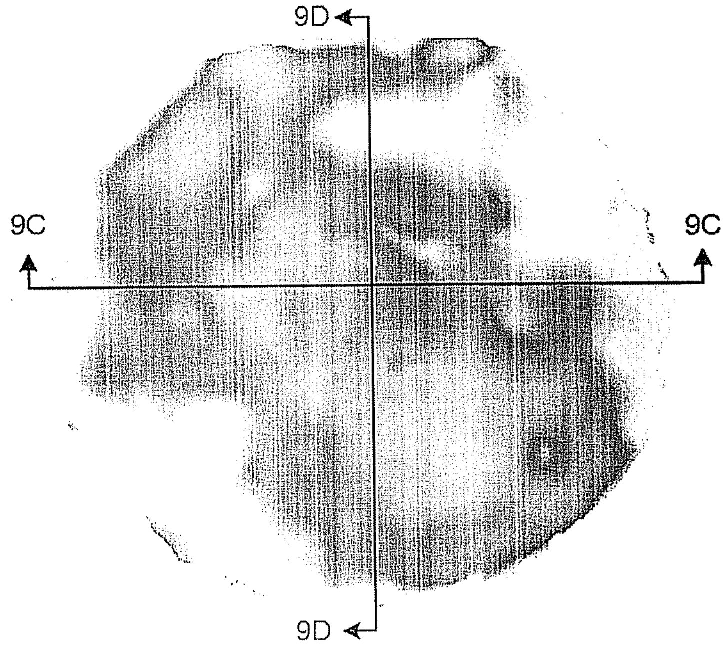


FIG. 9B

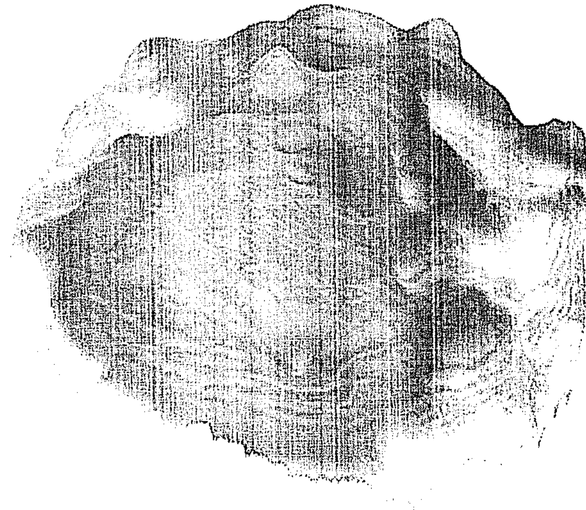


FIG. 9C

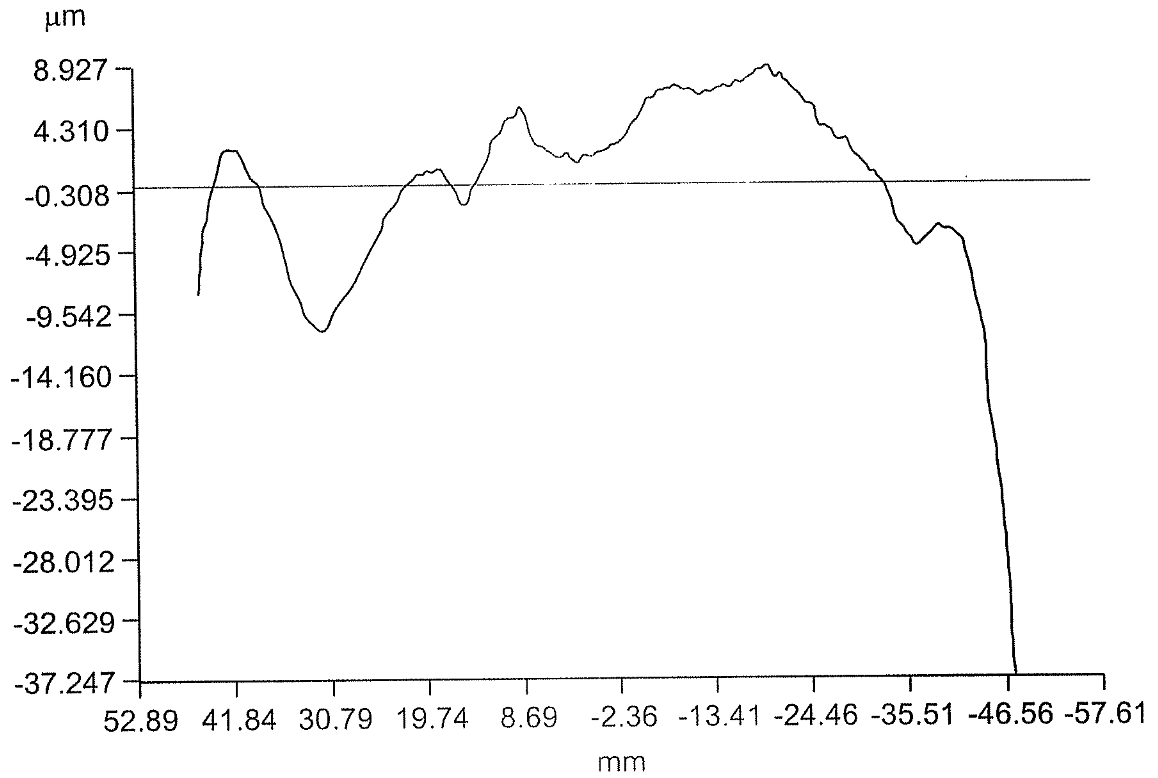


FIG. 9D

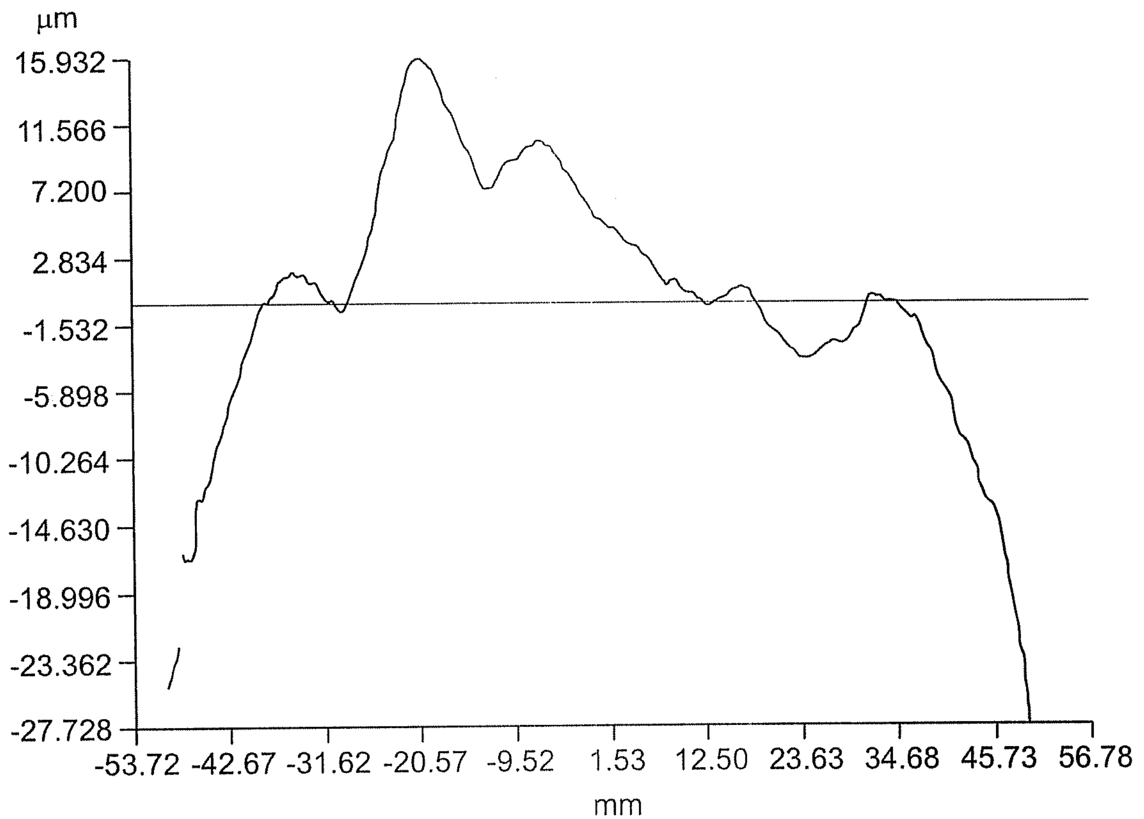


FIG. 10A

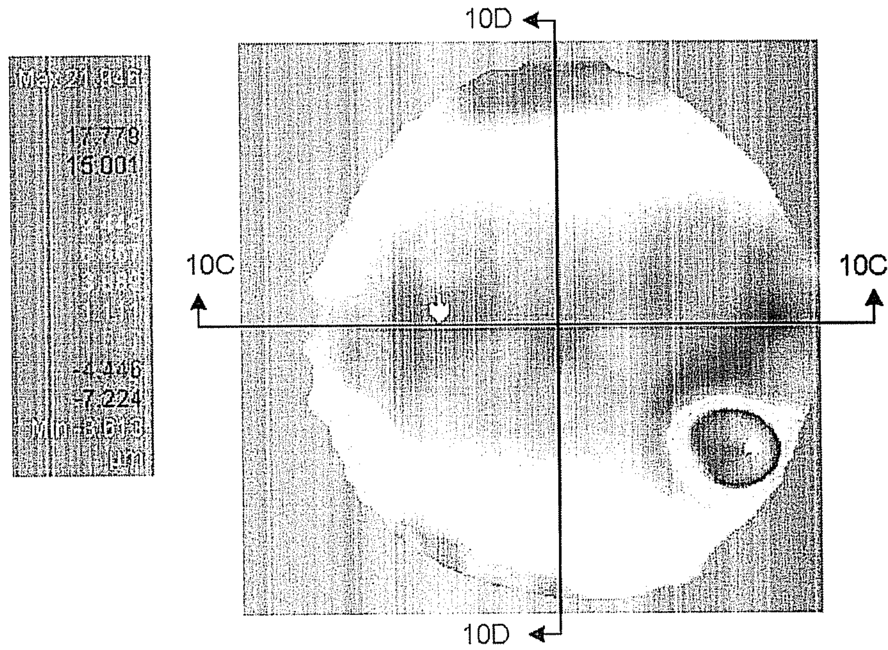


FIG. 10B

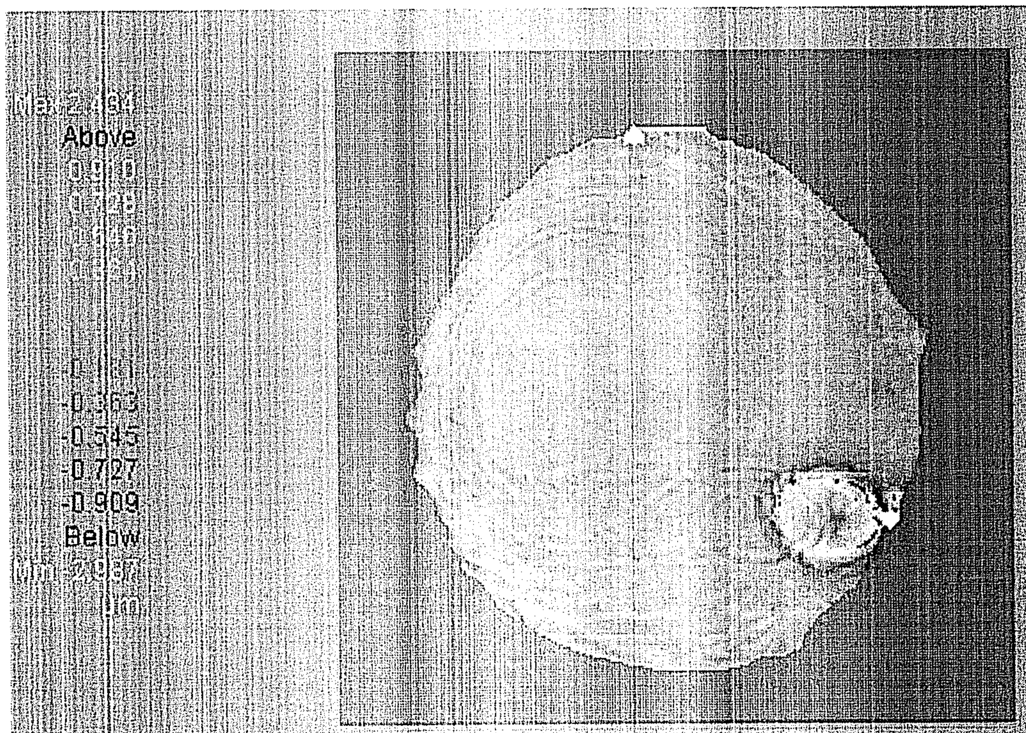


FIG. 10C

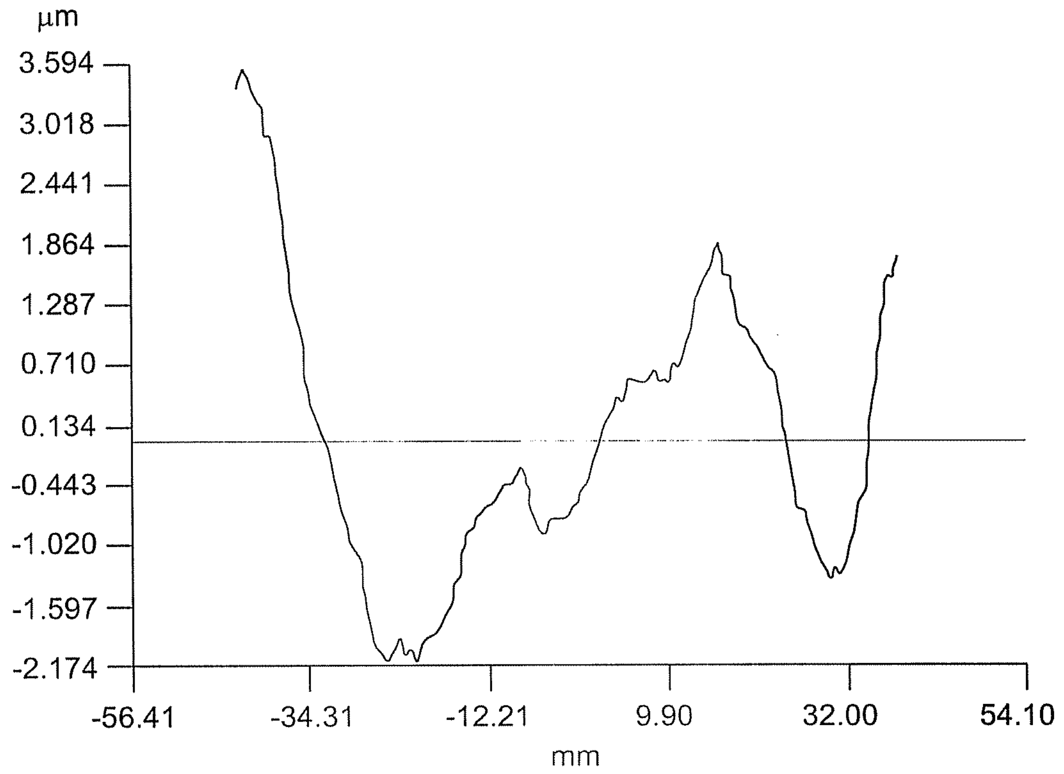


FIG. 10D

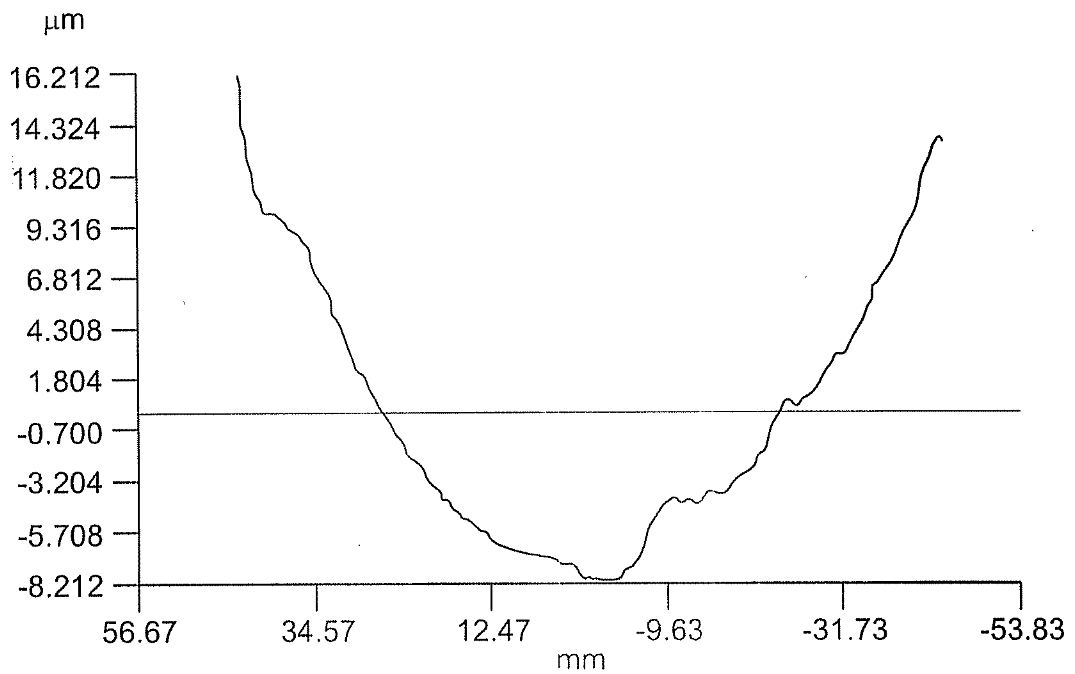


FIG. 11A

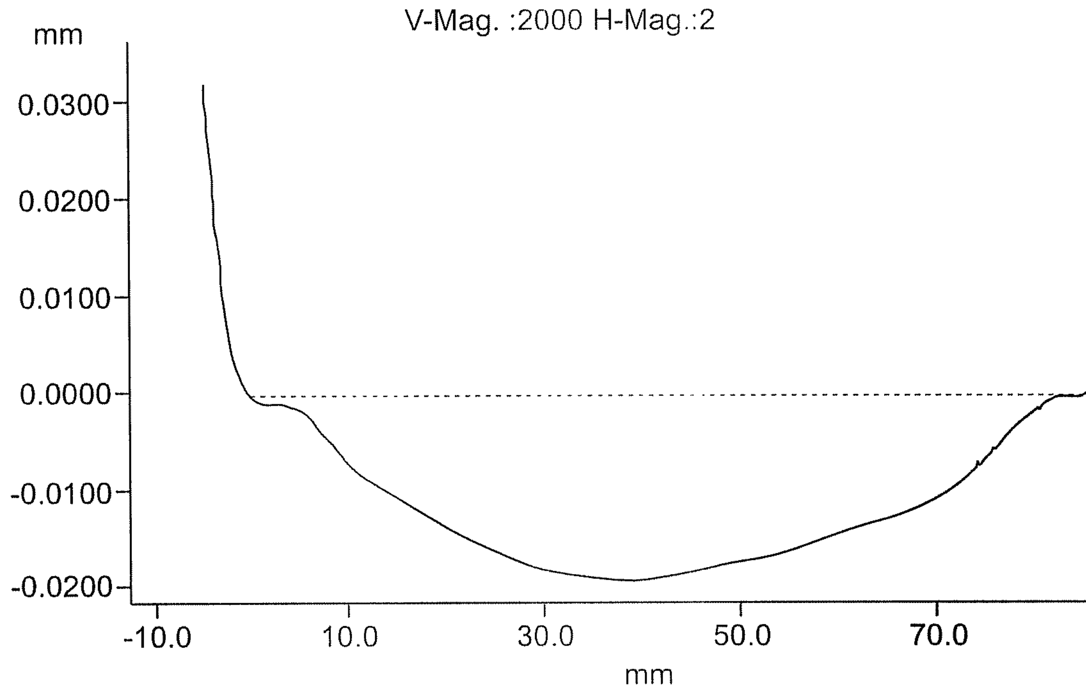


FIG. 11B

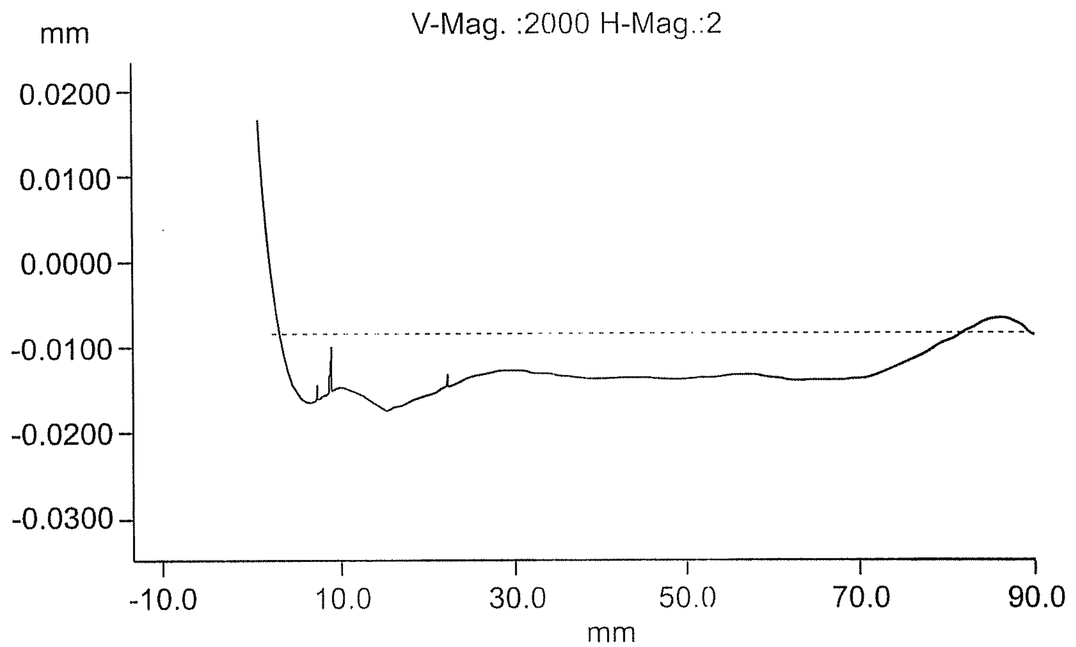


FIG. 12A

17.600
-17.837
-22.899
12E
12D
12D
12E

FIG. 12B

-1.689
-2.145
-2.607

FIG. 12C

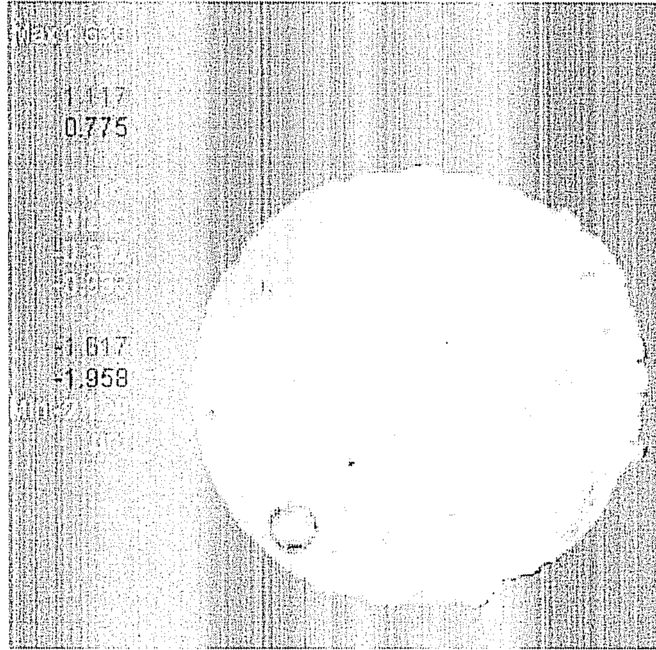


FIG. 12D

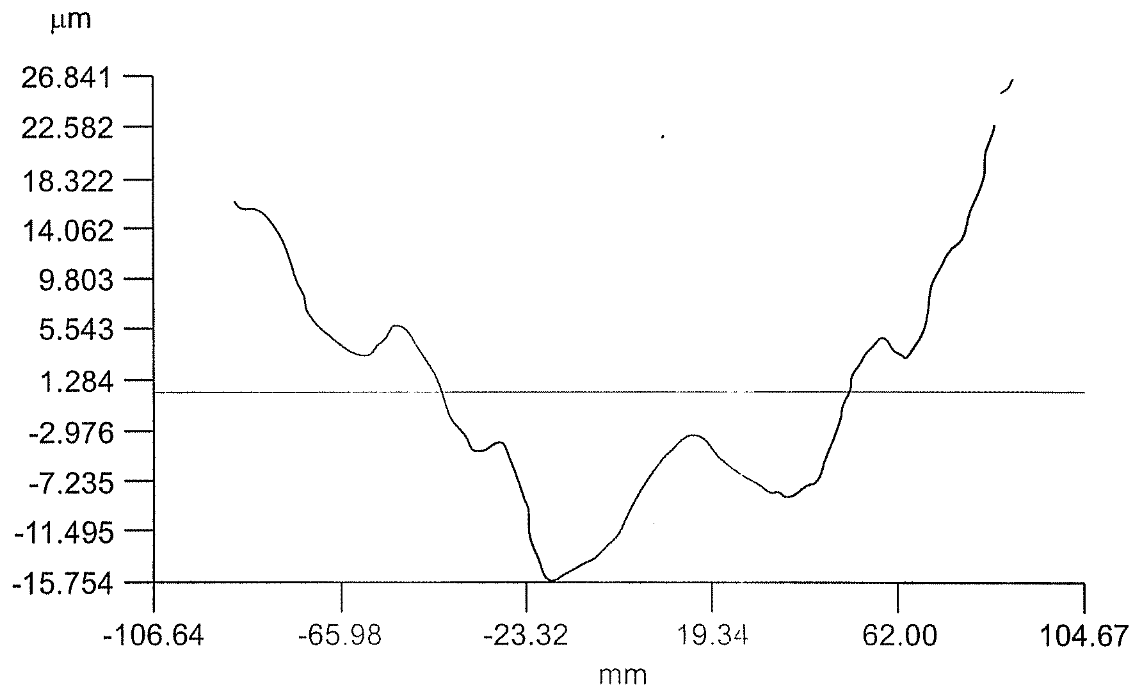
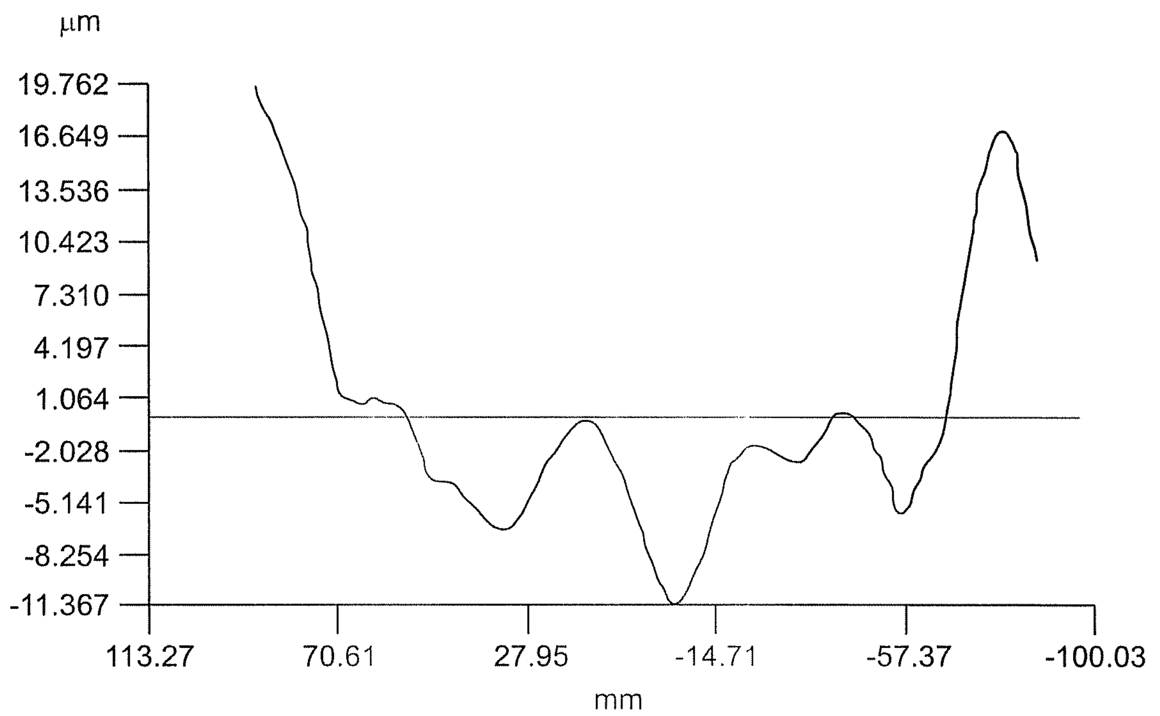


FIG. 12E



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/065632

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/76

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2008/121262 A2 (CORNING INC [US]; GADKAREE KISHOR P [US]; PINCKNEY LINDA R [US]) 9 October 2008 (2008-10-09) cited in the application page 4, paragraph 16 - page 17, paragraph 76; claims 1-20; figures 1-6	1-20
A	US 7 176 528 B2 (COUILLARD JAMES G [US] ET AL) 13 February 2007 (2007-02-13) cited in the application column 3, line 1 - column 29, line 67; figures 1-2	1-20
A	US 2006/038228 A1 (AITKEN BRUCE G [US] ET AL AITKEN BRUCE GARDINER [US] ET AL) 23 February 2006 (2006-02-23) page 2, paragraph 17 - page 12, paragraph 116; figures 1-8	1-20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
4 March 2010	16/03/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lyons, Christopher

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/065632

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/268618 A1 (YAMAZAKI SHUNPEI [JP]) 30 October 2008 (2008-10-30) page 1, paragraph 8 - page 10, paragraph 132	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

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