



(51) International Patent Classification:

H01L 29/74 (2006.01) *H01L 25/07* (2006.01)
H01L 29/744 (2006.01) *H03K 17/73* (2006.01)

(21) International Application Number:

PCT/US2010/025053

(22) International Filing Date:

23 February 2010 (23.02.2010)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

12/437,929 8 May 2009 (08.05.2009) US

(71) Applicant (for all designated States except US): **CREE, INC.** [US/US]; 4600 Silicon Drive, Durham, North Carolina 27703 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ZHANG, Qingchun** [CN/US]; 108 Hickorywood Boulevard, Cary, North Carolina 27519 (US). **RICHMOND, James, Theodore** [US/US]; 1516 Poplar Lane, Hillsborough, North Carolina 27278 (US). **CALLANAN, Robert, J.** [US/US]; 5629 Bennettwood Court, Raleigh, North Carolina 27612 (US).

(74) Agent: **MYERS BIGEL SIBLEY & SAJOVEC, P.A.**; P.O. Box 37428, Raleigh, North Carolina 27627 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: WIDE BANDGAP BIPOLAR TURN-OFF THYRISTOR HAVING NON-NEGATIVE TEMPERATURE COEFFICIENT AND RELATED CONTROL CIRCUITS

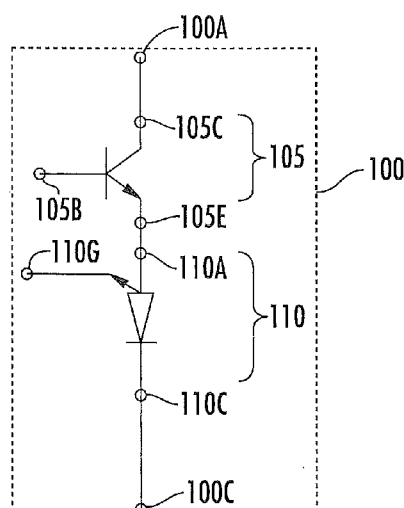


FIG. 1

(57) Abstract: An electronic device includes a wide bandgap thyristor having an anode, a cathode, and a gate terminal, and a wide bandgap bipolar transistor having a base, a collector, and an emitter terminal. The emitter terminal of the bipolar transistor is directly coupled to the anode terminal of the thyristor such that the bipolar transistor and the thyristor are connected in series. The bipolar transistor and the thyristor define a wide bandgap bipolar power switching device that is configured to switch between a nonconducting state and a conducting state that allows current flow between a first main terminal corresponding to the collector terminal of the bipolar transistor and a second main terminal corresponding to the cathode terminal of the thyristor responsive to application of a first control signal to the base terminal of the bipolar transistor and responsive to application of a second control signal to the gate terminal of the thyristor. Related control circuits are also discussed.

WIDE BANDGAP BIPOLAR TURN-OFF THYRISTOR HAVING NON-NEGATIVE TEMPERATURE COEFFICIENT AND RELATED CONTROL CIRCUITS

STATEMENT OF GOVERNMENT INTEREST

[001] The present invention was developed with Government support under Army Research Laboratory Contract No. W911NF-04-2-0022. The Government has certain rights in this invention.

FIELD

[002] This invention relates to power semiconductor devices, and more particularly, to devices and circuits including power switching devices.

BACKGROUND

[003] Power devices are widely used to carry large currents and support high voltages. Modern power devices are generally fabricated from monocrystalline silicon semiconductor material. One type of power device is the thyristor. A thyristor is a bistable power semiconductor device that can be switched from a nonconducting "off" state to a conducting "on" state, or vice versa. Power semiconductor devices, such as thyristors, high-power bipolar junction transistors ("HPBJT"), or power metal oxide semiconductor field effect transistors ("MOSFET"), are semiconductor devices capable of controlling or passing large amounts of current and blocking high voltages.

[004] Thyristors are generally known and conventionally have three terminals: an anode, a cathode, and a gate. A thyristor may be activated to conduct current between its anode and cathode terminals when a current pulse is received at its gate terminal. More particularly, a thyristor may be turned on by applying a short current pulse across the gate and the cathode. Once the thyristor turns on, the gate may lose its control to turn off the device. The turn off may be achieved by applying a reverse voltage across the anode and the cathode. A specially designed gate turn-off thyristor ("GTO"), however, is typically turned off by a reverse gate pulse. The GTO

thyristors generally start conduction by some trigger input and then behave as diodes thereafter.

[005] A thyristor is a highly rugged device in terms of transient currents, di/dt and dv/dt capability. The forward voltage (V_F) drop in conventional silicon thyristors is about 1.5 V to 2 V, and for some higher power devices, about 3 V. Therefore, the thyristor can control or pass large amounts of current and effectively block high voltages (*i.e.*, a voltage switch).

[006] Two parameters of a thyristor are the built-in potential (which is a characteristic of the bandgap of the semiconductor material used to manufacture the thyristor) and the specific on-resistance (*i.e.*, the electrical resistance across the anode and cathode of the device in the linear region when the device is turned on). The specific on-resistance for a thyristor is typically as small as possible so as to provide a large current per unit area for a given voltage applied to the thyristor. The lower the specific on-resistance, the lower the forward voltage (V_F) drop is for a given current rating. The minimum V_F for a given semiconductor material is its built-in potential (voltage).

[007] Some conventional thyristors may be manufactured in silicon (Si) or gallium arsenide (GaAs), such as a silicon controlled rectifier ("SCR"). Thyristors formed in Si or GaAs, however, may have certain performance limitations resulting from the Si or GaAs material itself, such as the minority carrier lifetime and the thickness of the drift region. The largest contributory factor to specific on-resistance is the resistance of the thick low-doped drift region of the thyristor. In a majority carrier device, such as a MOSFET, the specific on-resistance is determined by the doping concentration and the thickness of the lightly doped drift layer. In a minority carrier (or bipolar) device, carriers, both electrons and holes, are injected into this drift layer, and substantially reduces the specific on-resistance. This effect is referred to as conductivity modulation. As the rated voltage of a thyristor increases, typically the thickness of the drift region increases and the doping of the drift region decreases. For effective conductivity modulation, a very long minority carrier lifetime is required. At the same time, the amount carriers stored in the drift layer increases because the volume of the drift layer is increased. Therefore, the time required to remove excess

carriers in the drift layer, which determines the switching times and frequencies, may increase dramatically for devices with higher blocking voltage ratings.

[008] Development efforts in power devices have included the use of silicon carbide (SiC) devices for power devices. Silicon carbide has a wide bandgap, a lower dielectric constant, a high breakdown field strength, a high thermal conductivity, and a high saturation electron drift velocity relative to silicon. These characteristics may allow silicon carbide power devices to operate at higher temperatures, higher power levels and with lower specific on-resistance and higher switching frequency than conventional silicon-based power devices. A theoretical analysis of the superiority of silicon carbide devices over silicon devices is found in a publication by Bhatnagar *et al.* entitled "*Comparison of 6H-SiC, 3C-SiC and Si for Power Devices*", IEEE Transactions on Electron Devices, Vol. 40, 1993, pp. 645-655.

SUMMARY

[009] According to some embodiments of the present invention, an electronic device includes a wide bandgap thyristor having an anode, a cathode, and a gate terminal, and a wide bandgap bipolar transistor having a base, a collector, and an emitter terminal. The emitter terminal of the bipolar transistor is coupled to the anode terminal of the thyristor. The bipolar transistor and the thyristor define a hybrid or monolithic wide bandgap bipolar power switching device. The wide bandgap bipolar power switching device is configured to switch between a nonconducting state and a conducting state that allows current flow between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor responsive to application of a first control signal to the base terminal of the bipolar transistor and responsive to application of a second control signal to the gate terminal of the thyristor.

[010] In some embodiments, the electronic device may further include a control circuit configured to generate the first and second control signals, supply the first control signal to the gate terminal of the thyristor, and supply the second control signal to the base terminal of the bipolar transistor to switch the bipolar power switching device to the conducting state such that a load current flows between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor.

The control circuit may be further configured to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor such that the load current is commutated to the gate terminal of the thyristor to switch the bipolar power switching device to the nonconducting state.

[011] In some embodiments, the control circuit may include a first voltage source configured to generate the first control signal configured to switch the bipolar transistor to a conductive state, a second voltage source configured to generate the second control signal configured to switch the thyristor to a conductive state, a first switching element configured to couple the first voltage source to the base terminal of the bipolar transistor to supply the first control signal thereto, a second switching element configured to couple the second voltage source to the gate terminal of the thyristor to supply the second control signal thereto, and a third switching element configured to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor.

[012] In some embodiments, the control circuit may include a first switching element coupled to the gate terminal of the thyristor, an inverting driver device configured to provide the first control signal to the base terminal of the bipolar transistor and configured to switch the first switching element to provide the second control signal to the gate terminal of the thyristor, a second switching element coupled between the gate terminal of the thyristor and the collector terminal of the bipolar transistor, and a noninverting driver device configured to switch the second switching element to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor.

[013] In some embodiments, the first switching element may be a wide bandgap metal-oxide-semiconductor (MOS) transistor having a source/drain terminal coupled to the gate terminal of the thyristor and a gate terminal coupled to an output of the inverting driver device. The second switching element may be a wide bandgap commutating bipolar transistor having a collector terminal coupled to the collector terminal of the bipolar transistor, an emitter terminal coupled to the gate terminal of the thyristor, and a base terminal coupled to an output of the noninverting driver device.

[014] In some embodiments, the control circuit may further include an optically triggered driver device configured to provide an output signal responsive to light applied thereto. The inverting driver device and the noninverting driver device may be coupled to an output of the optically triggered driver device. The inverting driver device may be configured to provide the first control signal to the base terminal of the bipolar transistor and may be configured to switch the MOS transistor to a conducting state to provide the second control signal to the gate terminal of the thyristor when light is applied to the optically triggered driver device. The noninverting driver device may be configured to switch the commutating bipolar transistor to a conducting state to couple the collector terminal of the first bipolar transistor to the gate terminal of the thyristor when light is not applied to the optically triggered driver device.

[015] In some embodiments, the control circuit may further include a bypass stage coupled between the gate terminal of the thyristor and the collector terminal of the bipolar transistor. The bypass stage may be configured to conduct current therebetween to switch the bipolar power switching device to the nonconducting state when the current between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor exceeds a predetermined level.

[016] In some embodiments, the bypass stage may include a zener diode that is configured to conduct when the voltage drop between the collector of the bipolar transistor and the gate of the thyristor exceeds a breakdown voltage of the zener diode. In some embodiments, the bypass stage may include a plurality of power diodes connected in series between the gate terminal of the thyristor and the collector terminal of the bipolar transistor.

[017] In some embodiments, the bypass stage may further include a commutating bipolar transistor having a collector terminal coupled to the collector terminal of the bipolar transistor, an emitter terminal coupled to the gate terminal of the thyristor, and a base terminal coupled to the zener diode. The commutating bipolar transistor may be configured to be switched to a conducting state responsive to conduction of the zener diode to provide the load current to the gate terminal of the thyristor and switch the bipolar power switching device to the nonconducting state.

[018] In some embodiments, the bipolar transistor and the thyristor may be included in a common package. An on-resistance between the anode and cathode terminals of the thyristor may decrease as operating temperature of the thyristor increases. An on-resistance between the collector and emitter terminals of the bipolar transistor may increase as operating temperature of the bipolar transistor increases.

[019] In some embodiments, the increase in the on- resistance of the bipolar transistor may be greater than the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase. As such, an electrical resistance of the bipolar power switching device in the conducting state may increase as operating temperature of the bipolar power switching device increases.

[020] In some embodiments, the increase in the on- resistance of the bipolar transistor may be substantially similar to the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase. As such, an electrical resistance of the bipolar power switching device in the conducting state may not substantially change as operating temperature of the bipolar power switching device increases.

[021] In some embodiments, the bipolar power switching device may be configured to provide current saturation capability when the bipolar transistor is operated in the active region.

[022] In some embodiments, the bipolar transistor may be a silicon carbide bipolar junction transistor (BJT), and the thyristor may be a silicon carbide gate turn-off thyristor (GTO).

[023] According to further embodiments of the present invention, a packaged bipolar power switching device includes a wide bandgap bipolar transistor having a base, a collector, and an emitter terminal, and a wide bandgap thyristor having an anode, a cathode, and a gate terminal. The anode terminal of the thyristor is coupled to the emitter terminal of the bipolar transistor. The collector terminal corresponds to a first main terminal of the bipolar power switching device, and the cathode terminal corresponds to a second main terminal of the bipolar power switching device. The bipolar power transistor is configured to switch between a nonconducting state and a conducting state that allows current flow between the first and second main terminals.

The bipolar power transistor has a non-negative temperature coefficient, where an electrical resistance between the first and second main terminals does not decrease as operating temperature of the bipolar power switching device increases.

[024] In some embodiments, an on-resistance between the anode and cathode terminals of the thyristor may decrease as an operating temperature of the thyristor increases. An on-resistance between the collector and emitter terminals of the bipolar transistor may increase as an operating temperature of the bipolar transistor increases.

[025] In some embodiments, the increase in the on- resistance of the bipolar transistor may be greater than the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase to provide a positive temperature coefficient where an electrical resistance between the first and second main terminals of the bipolar power switching device in the conducting state increases as operating temperature of the bipolar power switching device increases.

[026] In some embodiments, the increase in the on- resistance of the bipolar transistor is substantially similar to the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase to provide a near-zero temperature coefficient where an electrical resistance between the first and second main terminals of the bipolar power switching device in the conducting state does not substantially change as operating temperature of the bipolar power switching device increases.

[027] According to still further embodiments of the present invention, a packaged bipolar turn-off thyristor device includes a wide bandgap gate turn-off thyristor (GTO) having an anode, a cathode, and a gate terminal, and a wide bandgap bipolar junction transistor (BJT) having a base, a collector, and an emitter terminal. The emitter terminal of the BJT is directly coupled to the anode terminal of the GTO. The bipolar power switching device is configured to switch between a nonconducting state and a conducting state that allows current flow between the collector of the BJT and the cathode of the GTO responsive to application of a first control signal to the base terminal of the BJT and responsive to application of a second control signal to the gate terminal of the GTO.

[028] In some embodiments, an on-resistance between the anode and cathode terminals of the GTO may decrease as operating temperature of the GTO increases, and an on-resistance between the collector and emitter terminals of the BJT may increase as operating temperature of the BJT increases.

[029] In some embodiments, the GTO may include a substrate of a first conductivity type having the cathode terminal thereon, a drift layer of a second conductivity type opposite to the first conductivity type on the substrate opposite the cathode terminal, a base layer of the first conductivity type on the drift layer and having the gate terminal thereon, and a first layer of the second conductivity type on the base layer and having the anode terminal thereon. The BJT may include a layer of the first conductivity type directly on the first layer of the second conductivity type and having the emitter terminal thereon, and a second layer of the second conductivity type on the layer of the first conductivity type. The second layer may include a highly doped first region of the first conductivity type therein having the collector terminal thereon, and a highly doped second region of the second conductivity type therein having the base terminal thereon.

[030] In some embodiments, the first conductivity type may be n-type, and the second conductivity type may be p-type. The substrate and the layers thereon may be silicon carbide.

BRIEF DESCRIPTION OF THE DRAWINGS

[031] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate certain embodiment(s) of the invention. In the drawings:

[032] **Figures 1-4** are schematic circuit diagrams illustrating devices and/or circuits according to some embodiments of the invention;

[033] **Figures 5 and 6** are graphs illustrating current-voltage (I-V) characteristics of devices according to some embodiments of the invention; and

[034] **Figure 7** is a cross sectional illustration of the device of **Figure 1**.

DETAILED DESCRIPTION OF EMBODIMENTS

[035] The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. It will be understood that when an element or layer is referred to as being "on", "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Like numbers refer to like elements throughout.

[036] It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section may be termed a first region, layer or section without departing from the scope of the present invention.

[037] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompass both an orientation of "lower" and "upper," depending of the

particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[038] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "includes" and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[039] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of this disclosure and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[040] Referring now to the drawings, **Figures 1** through **4** are schematic circuit diagrams illustrating various embodiments of the present invention. Transistors and thyristors according to embodiments of the present invention may be formed of silicon carbide having a polytype of 3C, 2H, 4H, 6H, and 15R, or from any of the various Group III-nitride materials useful for fabricating electronic devices. In the illustrated embodiments, the n⁺ and n⁻ regions, as well as the p⁺ and p⁻ regions, are designated "+" and "-" to symbolize different doping concentration levels respectively of the same conductivity type material in a manner well understood to those of ordinary skill in this art. As used herein, the "+" and "-" designations do not necessarily imply that a material is degenerate on one hand or semi-insulating on the other. The p-type silicon carbide may be doped, for example, with aluminum or boron and the n-type silicon carbide maybe doped, for example, with nitrogen or

phosphorous. P-type nitrides may be doped, for example, with magnesium, while n-type nitrides may be doped, for example, with silicon.

[041] As is known to those skilled in the art, a thyristor is a four-layer latching switching device having an anode and a cathode for current flow and a gate for switching the device from a blocking state to a conducting state, and vice versa. A control signal applied to the gate causes the device to "latch" into an "on" or conductive state, in which current can flow freely between the anode and cathode of the device. The device remains in the conductive state even after the control signal is removed. A second control signal, opposite in polarity to the first control signal, switches the device back into the "off" or blocking state. A specially designed gate turn-off thyristor ("GTO"), however, is typically turned off by a reverse gate pulse. The GTO thyristors generally start conduction by some trigger input and then behave as diodes thereafter. While certain wide bandgap thyristor designs are discussed in more detail below, the design of wide bandgap thyristors is generally known in the art. For example, U.S. Patent No. 5,539,217 describes the design and manufacture of silicon carbide (SiC) thyristors. Such silicon carbide thyristors may exhibit improved power handling capabilities over similar silicon thyristors.

[042] Some embodiments of the present invention may arise from realization that conventional thyristors may be difficult to implement in parallel due to differences in inherent on-resistances, especially as operating temperatures increase. In particular, some conventional SiC thyristors may have a negative temperature coefficient (NTC), where the on-resistance (and thus, the forward voltage drop V_F) across the device may decrease as operating temperature increases. Such a negative temperature coefficient for the forward voltage drop may increase the conducting current, due to the increase in the junction temperature. This may lead to current concentration on one or more thyristors connected in parallel, which may result in thermal run-away.

[043] Embodiments of present invention provide a bipolar power switching device including a wide bandgap thyristor and a wide bandgap bipolar transistor connected in series. Such wide bandgap devices include an active semiconductor layer of a wide bandgap material, such as silicon carbide (SiC), gallium nitride (GaN),

and/or other Group-III nitride material. In particular, embodiments of the present invention provide a SiC thyristor having at least a SiC bipolar junction transistor (BJT) connected in series with the thyristor anode terminal. Such configuration, also referred to herein as a Bipolar Turn-Off thyristor ("BTO"), may provide enhanced operating characteristics as compared to conventional SiC thyristors.

[044] In particular, bipolar power switching devices according to embodiments of the present invention can provide a near-zero temperature coefficient (e.g., such that the on-resistance across the device does not substantially change as operating temperature increases) or even a positive temperature coefficient (PTC) (e.g., such that the on-resistance across the device increases as operating temperature increases) for the forward voltage drop V_F by connecting a wide bandgap BJT in series with a wide bandgap thyristor. For example, a SiC BJT, which has a positive temperature coefficient for the forward voltage drop, can be specifically chosen to reduce the negative temperature coefficient of an SiC thyristor, and may provide a near-zero or even slightly positive temperature coefficient across the main terminals of the BTO. More particularly, the SiC BJT may act like a resistor when it is operated in saturation region, and may provide a positive temperature coefficient for the forward voltage drop. Accordingly, bipolar power switching devices according to embodiments of the present invention can be more easily paralleled, as the forward voltage drop may increase with increasing temperature to promote more even current distribution in parallel connected devices.

[045] In addition, bipolar power switching devices according to some embodiments of the present invention may provide current saturation capability when the SiC BJT operates in the active region. The current saturation capability can protect such devices from inrush current during turning-on, and/or current overshooting in the case of short-circuit failure. Bipolar power switching devices according to some embodiments of the present invention may also provide a negative temperature coefficient for the saturation current.

[046] Bipolar power switching devices according to some embodiments of the present invention can also switch at relatively high speed. For example, a BTO according to some embodiments of the present invention can be turned off faster than

conventional SiC thyristors, as the SiC BJT may be used to turn off the anode current of the SiC thyristor at a relatively high rate. Also, a bypass stage including a zener diode and/or several power diodes connected in series may be used to divert anode current to the thyristor gate terminal to turn off the thyristor. Bipolar power switching devices according to some embodiments of the present invention can also operate at relatively high temperatures, due to the absence of a gate dielectric film.

[047] **Figure 1** is a schematic diagram illustrating a bipolar power switching device or "BTO" **100** according to some embodiments of the present invention. Referring now to **Figure 1**, the BTO **100** includes a wide bandgap bipolar transistor (illustrated in **Figure 1** as a SiC BJT emitter follower **105**) connected in series with a wide bandgap thyristor (illustrated in **Figure 1** as a SiC GTO **110**) to provide a pseudo cascode pair. In particular, the SiC GTO **110** includes a gate terminal **110g**, a cathode terminal **110c**, and an anode terminal **110a**. The SiC BJT **105** includes a base terminal **105b**, a collector terminal **105c**, and an emitter terminal **105e**. The emitter terminal **105e** of the SiC BJT **105** is directly coupled to the anode terminal **110a** of the SiC GTO **110**. The collector **105c** of the SiC BJT **105** is coupled to and/or provides the anode terminal (also referred to herein as a first main terminal) **100a** for the BTO, and the cathode **110c** of the SiC GTO **110** is coupled to and/or provides the cathode terminal (also referred to herein as a second main terminal) **100c** for the BTO **100**. The base terminal **105b** and the gate terminal **110g** provide control terminals for the BTO **100**. The BJT **105** and the GTO **110** may be provided in a common package, and may be selected based on their particular temperature coefficients and/or other characteristics to provide a packaged BTO **100** having a non-negative temperature coefficient and/or other desired characteristics. Although described herein with reference to silicon carbide devices, it will be understood that the BJT **105** and/or the GTO **110** may be fabricated from other wide bandgap semiconductor materials, for example, as described in any of the patents described herein. Also, while **Figure 1** illustrates an npn-type BJT **105** and a p-type thyristor **110**, it will be understood that a pnp-type BJT and an n-type thyristor may also be used in some embodiments.

[048] Application of respective control signals to the base **105b** and the gate **110g** terminals switches the BTO **100** from a nonconducting state (where current does not flow between the anode **100a** and cathode **100b**) to a conducting state (which allows current flow between the anode **100a** and cathode **100c**). More particularly, application of a control signal to the gate **110g** causes the SiC GTO **110** to "latch" into a conductive or "on" state, which allows current flow between the anode **110a** and cathode **110c**. Likewise, application of a control signal to the base **105b** causes the SiC BJT **105** to turn on, conducting current between the collector **105c** and emitter **105e** terminals. In particular, the control signal applied to the base **105b** is sufficient to operate the BJT **105** in the saturation region, e.g., where changes in the base current I_B have little effect on the collector current I_C . As similar current levels may be provided to the base **105b** and the gate **110g** to activate the BJT **105** and the GTO **110** to a conducting state, respectively, a control circuit may be used to generate and supply the control signals to both the base **105b** of the BJT **105** and the gate **110g** of the GTO **110**.

[049] **Figure 2** is a schematic diagram illustrating an example circuit for driving the BTO **100** of **Figure 1** in accordance with some embodiments. Referring now to **Figure 2**, the control circuit **200** includes a voltage source **210**, a buffer amplifier or driver **205** coupled to the base **105b** of the BJT **105**, and a bypass stage (illustrated in **Figure 2** as a zener diode **215**) coupled between the collector **105c** of the BJT **105** and the gate **110g** of the GTO **110**. The collector **105c** of the BJT **105** (e.g., the anode terminal **100a** of the BTO **100**) is coupled to ground **230**, while the cathode **110c** of the GTO (e.g., the cathode terminal **100c** of the BTO **100**) is coupled to the negative connection of supply voltage V_{CC} **220**. The bypass stage is configured to conduct when the voltage drop between the gate **110g** of the GTO **110** and the collector **105c** of the BJT **105** exceeds the breakdown voltage of the zener diode **215** to provide a fault current limiting feature. Although illustrated with reference to zener diode **215** in **Figure 2**, other elements (for example, one or more power diodes connected in series) may be used to implement the bypass stage in some embodiments.

[050] **Figure 3** illustrates an example circuit **300** for driving the BTO **100** in greater detail in accordance with some embodiments. The control circuit **300** for controlling the BTO **100** includes two anode-referenced voltage sources **V1 310** and **V2 320**, four switches **301 –304**, and a bypass stage, implemented in **Figure 3** by a voltage clamp diode (or zener diode) **D1 315**. **V1 310** provides the control signal to the base **105c** to drive the SiC BJT **105**. **V2 320** provides the control signal to the gate **110g** to drive the SiC GTO **110**. The clamp diode **D1 315** has a breakdown voltage V_z that is greater than the voltage provided by **V2 320**.

[051] To turn on the BTO **100** to a conducting state, switches **301** and **303** are closed and switches **302** and **304** are open. Closing switch **301** connects the base **105b** to the positive connection of **V1 310**. Being an emitter follower (also referred to as a "common collector"), the base **105b** of the SiC BJT **105** should be pulled above the collector potential to place the SiC BJT **105** in saturation. **V1 310** is used to provide this voltage, and has a voltage rating that is greater than the base-to-emitter voltage drop V_{BE} of the SiC BJT **105**. For example, in some embodiments, **V1 310** may be configured to provide a voltage of about 3V to about 3.5 V. **V1 310** is also configured to regulate the base current I_B that is applied to the SiC BJT **105**. Closing switch **303** connects the gate **110g** of the SiC GTO **110** to the negative connection of **V2 320**, which causes the SiC GTO **110** to transition from a blocking or nonconducting state to a conducting state. The voltage rating of **V2 320** is also set to a value somewhat higher than the forward voltage of the anode-to-gate junction of the SiC GTO **110**. For example, in some embodiments, **V2 320** may be configured to provide a voltage of about 3V to about 3.5 V. **V2 320** is also configured to regulate the gate current I_G that is applied to the SiC GTO **110**. As such, when the BJT **105** and the GTO **110** are both switched to a conducting state, a load current may flow between the anode **100a** and cathode **100c** terminals of the BTO **100**.

[052] To turn off the BTO **100** to a blocking or nonconducting state, switches **301** and **303** are opened and switches **302** and **304** are closed. The opening of switch **301** and the closing of switch **302** tie the base **105b** of the SiC BJT **105** to the negative terminal of **V2 320**, thereby turning off the SiC BJT **105**. The opening of switch **303** and the closing of switch **304** tie the gate **110g** of the SiC GTO **110** to the

anode **100a** of the BTO **100**. As a result, the load current is commutated from the BTO anode **100a** to the GTO gate **110g**. This causes the anode-to-gate junction of the SiC GTO **110** to be reverse biased, resulting in rapid turn-off of the SiC GTO **110**.

[053] Still referring to **Figure 3**, the control circuit **300** including the BTO **100** according to some embodiments of the present invention provides a fault current limiting feature. In particular, the SiC BJT **105** remains in hard saturation so long as its collector current I_C is below the product of the base current I_B and the current gain β of the SiC BJT **105**. Once this criterion is no longer met, the SiC BJT **105** enters its active region and limits the current to the product of the base current I_B and current gain β . This causes the collector-to-emitter voltage V_{CE} of the SiC BJT **105** to rapidly increase, and as a result, the SiC GTO gate-to-SiC BJT collector voltage also increases at a corresponding rate. The voltage drop between the gate **110g** and the collector **105c** rises until it exceeds the breakdown voltage V_Z of the clamp diode D1 **315**, at which point the clamp diode D1 **315** begins to conduct. The clamp or breakdown voltage V_Z is greater than the voltage provided by V2 **320**, which prevents clamp diode D1 **315** from conducting in normal operation. The combination of the increase in the collector-to-emitter voltage V_{CE} of the SiC BJT **105** and the clamping of the SiC BJT collector **105c** to the SiC GTO gate **110g** by clamp diode D1 **315** causes the anode-to-gate junction of the SiC GTO **110** to be reverse biased. This forces the load current to commute from the BTO anode **100a** to the GTO gate **110g**, which rapidly turns off the SiC GTO **110**, thereby interrupting the fault current.

[054] Another example control circuit **400** according to some embodiments of the present invention is illustrated in **Figure 4**. As shown in **Figure 4**, the control circuit **400** uses a BJT Q2 **425** as the commutation element for the SiC GTO **110**. Referring now to **Figure 4**, when the BTO **100** is in the conducting state, a load current flows from the anode terminal **100a** of the BTO **100**, through SiC BJT Q1 **105** and the SiC GTO **110**, and to the cathode terminal **100c** of the BTO **100**. The remainder of the circuit **400** is used to control the SiC GTO **110** and the SiC BJT Q1 **105**. In particular, the control circuit **400** includes an optically triggered driver **401** (including a light emitting diode or other light source **401a** and an inverting driver **401b**) to provide an isolated turn on/turn off signal, an inverting driver INV **402** and a

non-inverting driver BUF 403, a low-voltage n-type metal-oxide semiconductor (NMOS) transistor 404 and a resistor R1 405 to provide turn-on gate current for the SiC GTO 110, and a bypass stage (including BJT Q2 425 and zener diode D1 415), which is used to clamp the SiC GTO gate 110g during commutation and fault conditions. The BTO 100 includes the cascode SiC BJT Q1 105 and the SiC GTO 110. The cathode terminal 100c of the BTO 100 is coupled to the negative terminal of supply voltage Vcc 220. Two floating DC voltage sources, V1' 410 and V2' 420, which are referenced to the grounded anode terminal 100a of the BTO 100, are used to supply power.

[055] Operation of the example control circuit 400 of **Figure 4**, as described in detail below, is based on the following implementation. In particular, the reference point or ground 230 for the drive voltages is the anode terminal 100a of the BTO 100. The outputs of the inverting driver INV 402 and the non-inverting driver BUF 403 provide both positive and negative potentials referenced to the anode terminal 100a of the BTO 100. The voltage swing is from +V1' (high) and -V2' (low), where the voltages provided by V1' 410 and V2' 420 may be similar to those provided by the voltage sources V1 310 and V2 320, respectively, of **Figure 3**. The magnitude of the voltage provided by voltage source V1' 410 and the current sourcing capability of the inverting driver INV 402 and non-inverting driver BUF 403 are sufficient to pull the emitters of SiC BJT Q1 105 and BJT Q2 425 to anode potential under many (if not all) collector current conditions. The magnitude of the voltage provided by voltage source V2' 420 and the current capability of the NMOS transistor 404 are sufficient to turn on the SiC GTO 110 (when SiC BJT Q1 105 is conducting) under many (if not all) load current conditions. Adequate current limiting is provided on the outputs of the inverting driver INV 402, the non-inverting driver BUF 403, and the NMOS transistor 404 to allow safe operation under many (if not all) operating conditions.

[056] Still referring to **Figure 4**, the blocking or nonconducting state of the BTO 100 is described as follows. When the SiC GTO 110 is in the blocking or nonconducting state and light is not provided by the light source 401a to trigger the optically triggered driver 401, the output of inverting driver INV 402 is at a voltage -V2', and the output of non-inverting driver BUF 403 is at a voltage +V1'. As a

result, SiC BJT Q1 105 and NMOS transistor 404 are in the "off" or blocking state, and BJT Q2 425 is in "on" or conducting state. This effectively ties the SiC GTO gate 110g to the BTO anode 100a, providing a robust blocking state with relatively high immunity to changes in voltage over time (dV/dt).

[057] The transition from the blocking state to the conducting state of the BTO 100 is as follows. When light is provided by the light source 401a to trigger the optically triggered driver 401 to provide the turn on signal, the output of inverting driver INV 402 swings to +V1', and the output of non-inverting driver BUF 403 swings to -V2'. As a result, BJT Q2 425 is turned off, and SiC BJT Q1 105 and NMOS transistor 404 are turned on. With SiC BJT Q1 105 in the conducting state, the anode 110a of SiC GTO 110 is strongly connected to the anode terminal 100a of the BTO 100. This causes current to flow from DC voltage source V2' 420 through NMOS transistor 404, to resistor R1 405, into the gate 110g of the SiC GTO 110, through the anode 110a of the SiC GTO 110, and back to DC voltage source V2' 420. This action forward biases the gate 110g of the SiC GTO 110, with the gate current I_G limited by the resistance of resistor R1 405. This puts the BTO 100 in the conducting state, and a load current flows between the anode terminal 100a and the cathode terminal 100c. During this time, NMOS transistor 404 may be biased in such a way to limit its drain current to a level appropriate to drive the SiC GTO gate 110g.

[058] Operation of the BTO 100 in the conducting state is as follows. The load current flows into the anode terminal 100a of the BTO 100, into the collector 105c and out of the emitter 105e of SiC BJT Q1 105, into the anode 110a and out of the cathode 110c of the SiC GTO 110, and out of the cathode terminal 100c of the BTO 100. The SiC BJT Q1 105 and the SiC GTO 110 are connected in series to decrease the anode-to-cathode voltage drop of the SiC GTO 110. In particular, the SiC BJT 105 has a positive temperature coefficient, where the collector-to-emitter voltage drop V_{CE} increases with increases in operating temperature. As such, SiC BJT Q1 105 in each packaged BTO 100 according to some embodiments of the present invention may be specifically selected based on its positive temperature coefficient for the forward voltage drop and based on the negative temperature coefficient of the SiC GTO 110 to reduce and/or effectively negate the negative

temperature coefficient of the SiC GTO 110, and may even provide a positive temperature coefficient for the BTO 100 in some embodiments. The negative temperature coefficient of the SiC GTO 110 may make static current sharing difficult in parallel arrays of conventional SiC GTOs. Accordingly, by employing the SiC BJT Q1 105 in series with the SiC GTO 110, the BTO 100 may have a non-negative (e.g., near-zero or even positive) temperature coefficient, which may promote more even current distribution and ease in paralleling BTOs according to some embodiments of the present invention.

[059] The transition from the conducting state to the blocking state of the BTO 100 is as follows. When the light is not provided by the light source 401a to trigger the optically triggered driver 401, the output of inverting driver INV 402 driver swings to $-V_2'$, and the output of non-inverting driver BUF 403 swings to $+V_1'$. As a result, SiC BJT Q1 105 and NMOS transistor 404 are turned off, and BJT Q2 425 is turned on. With the SiC BJT Q1 105 in a nonconducting state, the anode 110a of the SiC GTO 110 is disconnected from the anode terminal 100a of the BTO 100. With BJT Q2 425 in a conducting state and NMOS transistor 404 in a nonconducting state, the gate 110g of the SiC GTO 110 is disconnected from the voltage source V_2' 420 and is connected to the anode terminal 100a of the BTO 100. Accordingly, the load current is commutated from the anode terminal 100a into the gate 110g of the SiC GTO 110, causing the SiC GTO 110 to be rapidly turned off.

[060] Embodiments of the present invention as illustrated in **Figure 4** may also provide an over current feature that turns off the SiC GTO 110 in the event that the load current exceeds a predetermined value. More particularly, the collector current I_C provided by SiC BJT Q1 105 may be determined by the product of its base current I_B and its current gain β . When this value is exceeded, SiC BJT Q1 105 enters its linear region and begins to behave as a constant current source. As a result, the collector-to-emitter voltage V_{CE} of SiC BJT Q1 105 may rapidly increase, which results in an increase in the voltage between the BTO anode terminal 100a and the SiC GTO gate 110g. When the anode-to-gate voltage drop exceeds the breakdown voltage of zener diode D1 415, the diode D1 415 will conduct, causing BJT Q2 425 to clamp the gate voltage to a predetermined level. As the fault current increases, the

collector-to-emitter voltage V_{CE} across SiC BJT Q1 105 will further increase, thereby reverse biasing the anode-to-gate junction of the SiC GTO 110 and causing the SiC GTO 110 to turn off, interrupting the load current. The voltage at which BJT Q2 425 clamps the gate 110g of the SiC GTO 110 may be selected to prevent damage to the control circuit 400.

[061] As discussed above with reference to **Figure 4**, SiC BJT Q1 105 may be selected to support continuous full load current in the conducting state, and to support voltage V_2' when in the blocking state. During conduction, the collector-to-emitter voltage drop V_{CE} across SiC BJT Q1 105 should remain low enough to forward bias the anode-to-gate junction of the SiC GTO 110. BJT Q2 425 may also be selected to support full load current in the conducting state (e.g., during the commutation of the SiC GTO 110), and to support voltage V_2' when in the blocking state. During conduction, the collector-to-emitter voltage drop V_{CE} across BJT Q2 425 should be less than V_2' , to reduce and/or prevent possible damage to NMOS transistor 404.

[062] **Figures 5 and 6** are graphs illustrating current-voltage (I-V) characteristics of a BTO according to some embodiments of the present invention. In particular, **Figures 5 and 6** illustrate forward I-V characteristics of an SiC BTO according to some embodiments of the present invention that includes a 10 kV SiC GTO and a 1600 V SiC BJT. As shown in **Figure 5**, such a configuration provides a positive temperature coefficient, as the on-resistance of the BTO increases with temperature. In particular, the on-resistance of the BTO increases (illustrated by the increased voltage drop across the BTO) as the operating temperature increases, as shown by lines 505 (room temperature), 510 (about 100°C), 515 (about 150°C), and 520 (about 200°C). **Figure 6** illustrates that a SiC BTO according to some embodiments of the present invention provides current saturation capability as operating temperature increases, as shown by line 605 (room temperature) and line 610 (about 200°C).

[063] **Figure 7** is a cross-sectional view illustrating a SiC BTO 100 according to some embodiments of the present invention that includes a bipolar transistor 105 and a thyristor 110 on a common substrate. In some embodiments, the

bipolar transistor **105** and the thyristor **110** described in detail above may be fabricated and/or subsequently provided on an n-type 4H silicon carbide layer **52**. SiC bipolar transistors are described, for example, in U.S. Patent No. 4,945,394, while SiC thyristors are described, for example, in U.S. Patent No. 5,539,217, the disclosures of which are incorporated by reference herein in their entireties.

[064] As shown in **Figure 7**, a BTO **100** according to some embodiments includes an n-type layer **52**. A contact **100c/110c** is provided on the n-type layer **52**, and provides the cathode terminal for both the BTO **100** and the GTO **110**. A p-type drift layer **54** is provided on the n-type layer **52**, an n-type base layer **56** is provided on the p-type drift layer **54**. A gate contact **110g** for the GTO **110** is provided on a highly doped n⁺ region **57** of the n-type base layer **56**. A p-type layer **58** is provided on the n-type base layer **56**, and an n-type layer **60** is provided on the p-type layer **58**. Contacts **105e** and **110a** are provided on the n-type layer **60** and the p-type layer **58** as an emitter terminal for the BJT **105** and an anode terminal for the GTO **110**, respectively. A p-type layer **62** is provided on the n-type layer **60**. The p-type layer **62** includes a highly doped p⁺ region **63**, and a highly-doped n⁺ region **64**. A base contact **105b** for the BJT **105** is provided on the highly-doped p⁺ region **63**, and a contact **100a/105c** is provided on the highly-doped n⁺ region **64** as an anode terminal for the BTO **100** and a collector terminal for the BJT **105**.

[065] Accordingly, the n-type region **64**, the p-type layer **62**, and the n-type layer **60** define the SiC BJT **105**. The contact **105b** on the p⁺ region **63** provides the base terminal of the BJT **105**, the contact **100a/105c** on the n⁺ region **64** provides the collector terminal of the BJT **105** (and the anode terminal of the BTO **100**), and the contact **105e** on the n-type layer **60** provides the emitter terminal of the BJT. Also, the p-type layer **58**, the n-type base layer **56**, the p-type drift layer **54**, and the n-type layer **52** define the SiC GTO **110**. The contact **110g** on the n-type base layer **56** provides the gate terminal of the GTO **110**, the contact **110a** on the p-type layer **58** provides the anode terminal of the GTO **110**, and the contact **100c/110c** on the n-type layer **52** provides the cathode terminal of the GTO **110** (and the cathode terminal of the BTO **100**). The n-type layer **60**, which provides the BJT emitter, is directly on the

p-type layer **58**, which provides the GTO anode, such that the BJT **105** and the GTO **110** are connected in series.

[066] Embodiments of the present invention as described above with reference to **Figures 1-7** can be achieved by monolithic integration or a hybrid combination of the bipolar transistor **105** and the thyristor **110**. As used herein, a "hybrid" bipolar power switching device may refer to a cascode configuration and/or other combination of a discrete bipolar transistor **105** and a discrete thyristor **110**. A "monolithic" bipolar power switching device may refer to a device where both the bipolar transistor **105** and the thyristor **110** are fabricated in the same semiconductor chip and/or substrate. A packaged bipolar power switching device according to some embodiments of the present invention may include both monolithic and hybrid combinations of the bipolar transistor **105** and the thyristor **110**.

[067] While the above embodiments are described with reference to particular figures, it is to be understood that some embodiments of the present invention may include additional and/or intervening layers, structures, or elements, and/or particular layers, structures, or elements may be deleted. More generally, the foregoing is illustrative of the present invention and is not to be construed as limiting thereof. Although a few exemplary embodiments of this invention have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention as defined in the claims. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims. The invention is defined by the following claims, with equivalents of the claims to be included therein.

That Which Is Claimed:

1. An electronic device, comprising:
 - a wide bandgap thyristor having an anode, a cathode, and a gate terminal; and
 - a wide bandgap bipolar transistor having a base, a collector, and an emitter terminal, the emitter terminal of the bipolar transistor being coupled to the anode terminal of the thyristor,wherein the bipolar transistor and the thyristor define a wide bandgap bipolar power switching device that is configured to switch between a nonconducting state and a conducting state such that current flows between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor responsive to application of a first control signal to the base terminal of the bipolar transistor and responsive to application of a second control signal to the gate terminal of the thyristor.
2. The electronic device of Claim 1, further comprising:
 - a control circuit configured to generate the first and second control signals, supply the first control signal to the gate terminal of the thyristor, and supply the second control signal to the base terminal of the bipolar transistor to switch the bipolar power switching device to the conducting state such that a load current flows between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor,wherein the control circuit is further configured to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor such that the load current is commutated to the gate terminal of the thyristor to switch the bipolar power switching device to the nonconducting state.
3. The electronic device of Claim 2, wherein the control circuit comprises:
 - a first voltage source configured to generate the first control signal configured to switch the bipolar transistor to a conductive state;

a second voltage source configured to generate the second control signal configured to switch the thyristor to a conductive state;

a first switching element configured to couple the first voltage source to the base terminal of the bipolar transistor to supply the first control signal thereto;

a second switching element configured to couple the second voltage source to the gate terminal of the thyristor to supply the second control signal thereto; and

a third switching element configured to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor.

4. The electronic device of Claim 2, wherein the control circuit comprises:

a first switching element coupled to the gate terminal of the thyristor;

an inverting driver device configured to provide the first control signal to the base terminal of the bipolar transistor and configured to switch the first switching element to provide the second control signal to the gate terminal of the thyristor;

a second switching element coupled between the gate terminal of the thyristor and the collector terminal of the bipolar transistor; and

a noninverting driver device configured to switch the second switching element to couple the gate terminal of the thyristor to the collector terminal of the bipolar transistor.

5. The electronic device of Claim 4, wherein:

the first switching element comprises a wide bandgap metal-oxide-semiconductor (MOS) transistor having a source/drain terminal coupled to the gate terminal of the thyristor and a gate terminal coupled to an output of the inverting driver device; and

the second switching element comprises a wide bandgap commutating bipolar transistor having a collector terminal coupled to the collector terminal of the bipolar transistor, an emitter terminal coupled to the gate terminal of the thyristor, and a base terminal coupled to an output of the noninverting driver device.

6. The electronic device of Claim 5, wherein the control circuit further comprises:

an optically triggered driver device configured to provide an output signal responsive to light applied thereto,

wherein the inverting driver device and the noninverting driver device are coupled to an output of the optically triggered driver device,

wherein the inverting driver device is configured to provide the first control signal to the base terminal of the bipolar transistor and configured to switch the MOS transistor to a conducting state to provide the second control signal to the gate terminal of the thyristor when light is applied to the optically triggered driver device,

and wherein the noninverting driver device is configured to switch the commutating bipolar transistor to a conducting state to couple the collector terminal of the first bipolar transistor to the gate terminal of the thyristor when light is not applied to the optically triggered driver device.

7. The electronic device of Claim 2, wherein the control circuit further comprises:

a bypass stage coupled between the gate terminal of the thyristor and the collector terminal of the bipolar transistor and configured to conduct current therebetween to switch the bipolar power switching device to the nonconducting state when the current between the collector terminal of the bipolar transistor and the cathode terminal of the thyristor exceeds a predetermined level.

8. The electronic device of Claim 7, wherein the bypass stage comprises a zener diode that is configured to conduct when the voltage drop between the collector of the bipolar transistor and the gate of the thyristor exceeds a breakdown voltage of the zener diode.

9. The electronic device of Claim 8, wherein the bypass stage further comprises a commutating bipolar transistor having a collector terminal coupled to the

collector terminal of the bipolar transistor, an emitter terminal coupled to the gate terminal of the thyristor, and a base terminal coupled to the zener diode,

wherein the commutating bipolar transistor is configured to be switched to a conducting state responsive to conduction of the zener diode to provide the load current to the gate terminal of the thyristor and switch the bipolar power switching device to the nonconducting state.

10 The electronic device of Claim 7, wherein the bypass stage comprises a plurality of power diodes connected in series between the gate terminal of the thyristor and the collector terminal of the bipolar transistor.

11. The electronic device of Claim 1, wherein the bipolar transistor and the thyristor are included in a common package, wherein an on-resistance between the anode and cathode terminals of the thyristor decreases as operating temperature of the thyristor increases, and wherein an on-resistance between the collector and emitter terminals of the bipolar transistor increases as operating temperature of the bipolar transistor increases.

12. The electronic device of Claim 11, wherein the increase in the on-resistance of the bipolar transistor is greater than the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase such that an electrical resistance of the bipolar power switching device in the conducting state increases as operating temperature of the bipolar power switching device increases.

13. The electronic device of Claim 11, wherein the increase in the on-resistance of the bipolar transistor is substantially similar to the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase such that an electrical resistance of the bipolar power switching device in the conducting state does not substantially change as operating temperature of the bipolar power switching device increases.

14. The electronic device of Claim 1, wherein the bipolar power switching device is configured to provide current saturation capability when the bipolar transistor is operated in the active region.

15. The electronic device of Claim 1, wherein the bipolar transistor comprises a silicon carbide bipolar junction transistor (BJT), and wherein the thyristor comprises a silicon carbide gate turn-off thyristor (GTO).

16. A packaged bipolar power switching device, comprising:
a wide bandgap bipolar transistor having a base, a collector, and an emitter terminal, the collector terminal corresponding to a first main terminal of the bipolar power switching device; and

a wide bandgap thyristor having an anode, a cathode, and a gate terminal, the anode terminal of the thyristor being coupled to the emitter terminal of the bipolar transistor, and the cathode terminal corresponding to a second main terminal of the bipolar power switching device,

wherein the bipolar power transistor is configured to switch between a nonconducting state and a conducting state such that current flows between the first and second main terminals, and wherein the bipolar power transistor has a non-negative temperature coefficient across the first and second main terminals in the conducting state.

17. The device of Claim 16, wherein an on-resistance between the anode and cathode terminals of the thyristor decreases as operating temperature of the thyristor increases, and wherein an on-resistance between the collector and emitter terminals of the bipolar transistor increases as operating temperature of the bipolar transistor increases.

18. The device of Claim 17, wherein the increase in the on-resistance of the bipolar transistor is greater than the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase such that the bipolar power

switching device has a positive temperature coefficient across the first and second main terminals in the conducting state.

19. The device of Claim 17, wherein the increase in the on-resistance of the bipolar transistor is substantially similar to the decrease in the electrical resistance of the thyristor as the respective operating temperatures increase such that the bipolar power switching device has a near-zero temperature coefficient across the first and second main terminals in the conducting state.

20. The device of Claim 1, wherein the bipolar transistor comprises a silicon carbide bipolar junction transistor (BJT), and wherein the thyristor comprises a silicon carbide gate turn-off thyristor (GTO).

21. A packaged bipolar turn-off thyristor device, comprising:
a wide bandgap gate turn-off thyristor (GTO) having an anode, a cathode, and a gate terminal; and

a wide bandgap bipolar junction transistor (BJT) having a base, a collector, and an emitter terminal, the emitter terminal of the BJT being directly coupled to the anode terminal of the GTO,

wherein the bipolar power switching device is configured to switch between a nonconducting state and a conducting state that allows current flow between the collector of the BJT and the cathode of the GTO responsive to application of a first control signal to the base terminal of the BJT and responsive to application of a second control signal to the gate terminal of the GTO.

22. The device of Claim 21, wherein an on-resistance between the anode and cathode terminals of the GTO decreases as operating temperature of the GTO increases, and wherein an on-resistance between the collector and emitter terminals of the BJT increases as operating temperature of the BJT increases.

23. The device of Claim 21, wherein the GTO comprises:

a substrate of a first conductivity type having the cathode terminal thereon;
a drift layer of a second conductivity type opposite to the first conductivity type on the substrate opposite the cathode terminal;
a base layer of the first conductivity type on the drift layer and having the gate terminal thereon; and
a first layer of the second conductivity type on the base layer and having the anode terminal thereon,
and wherein the BJT comprises:
a layer of the first conductivity type directly on the first layer of the second conductivity type and having the emitter terminal thereon; and
a second layer of the second conductivity type on the layer of the first conductivity type, the second layer including a highly doped first region of the first conductivity type therein having the collector terminal thereon, and a highly doped second region of the second conductivity type therein having the base terminal thereon.

24. The device of Claim 23, wherein the first conductivity type comprises n-type, and wherein the second conductivity type comprises p-type.

25. The device of Claim 23, wherein the substrate and the layers thereon comprise silicon carbide.

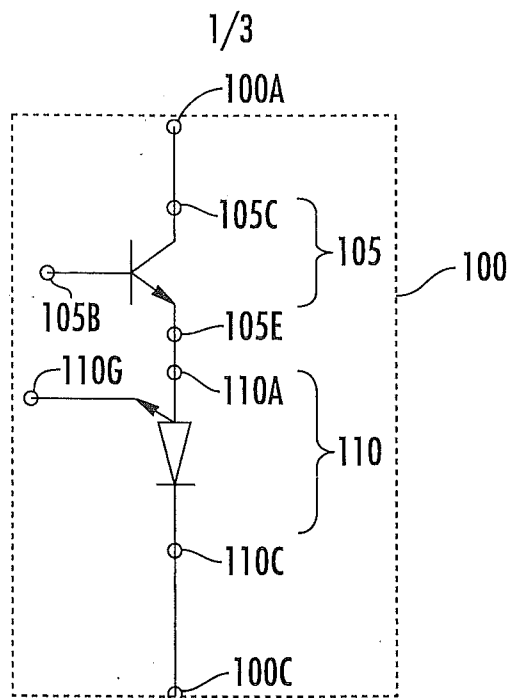


FIG. 1

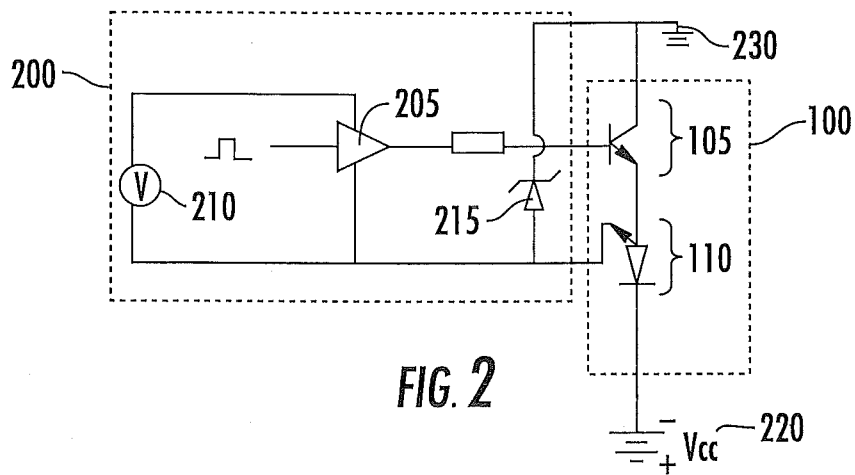


FIG. 2

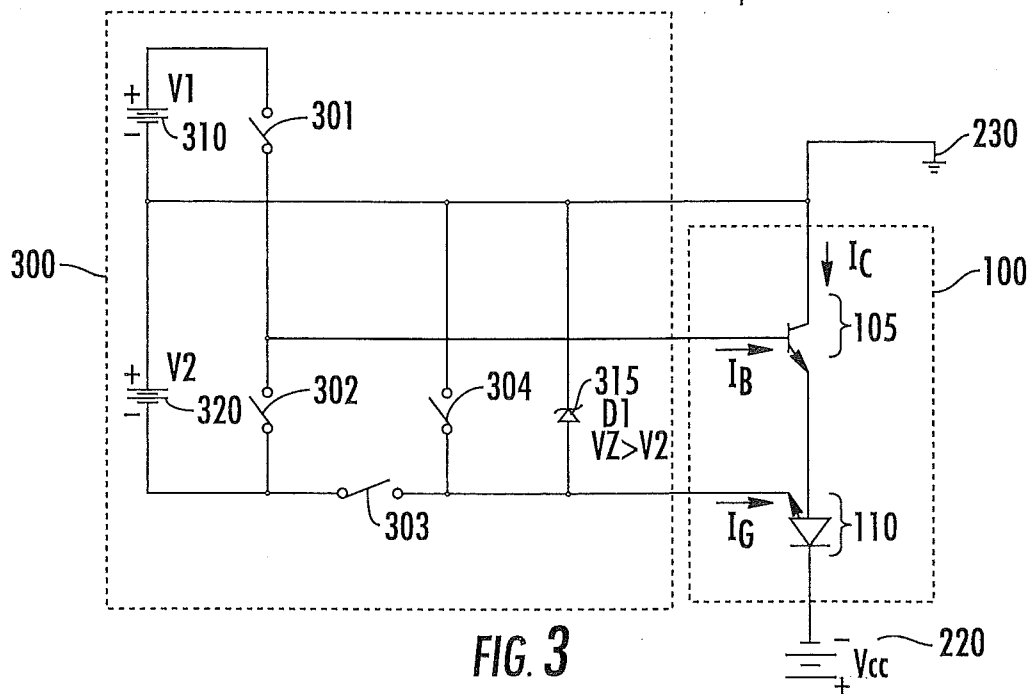


FIG. 3

2/3

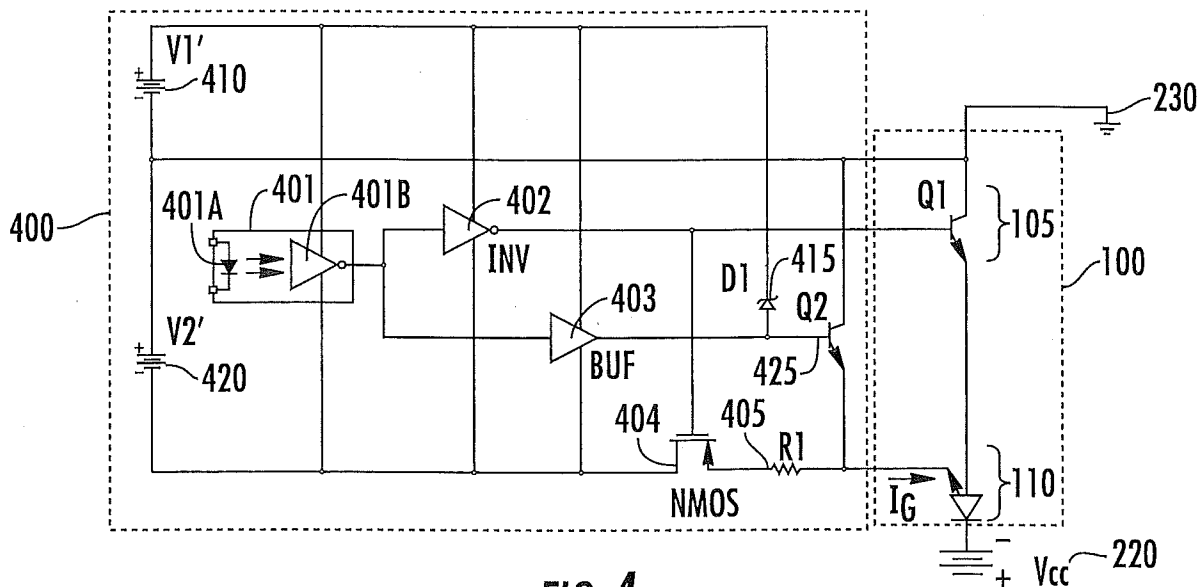


FIG. 4

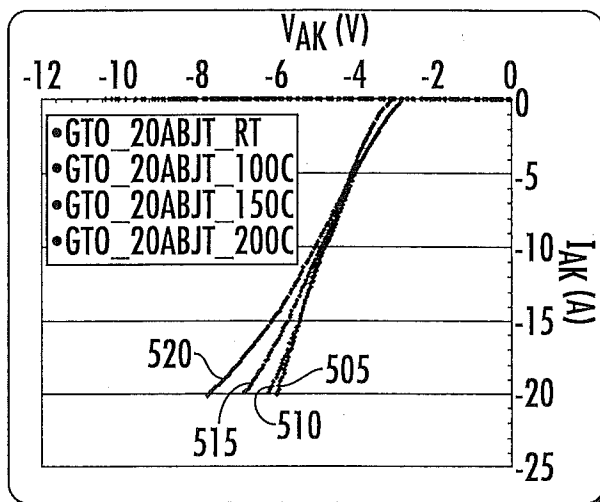


FIG. 5

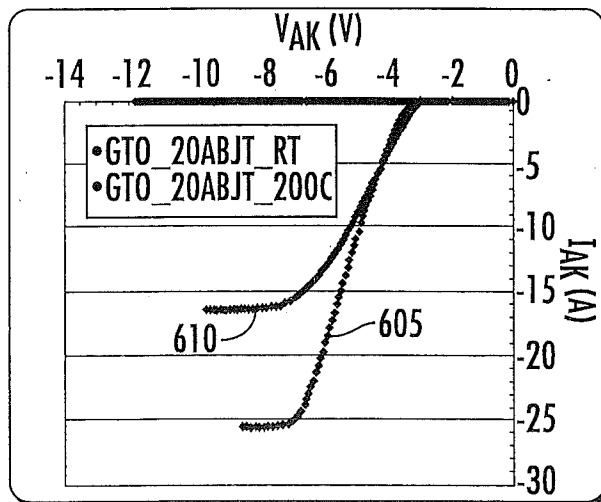


FIG. 6

3/3

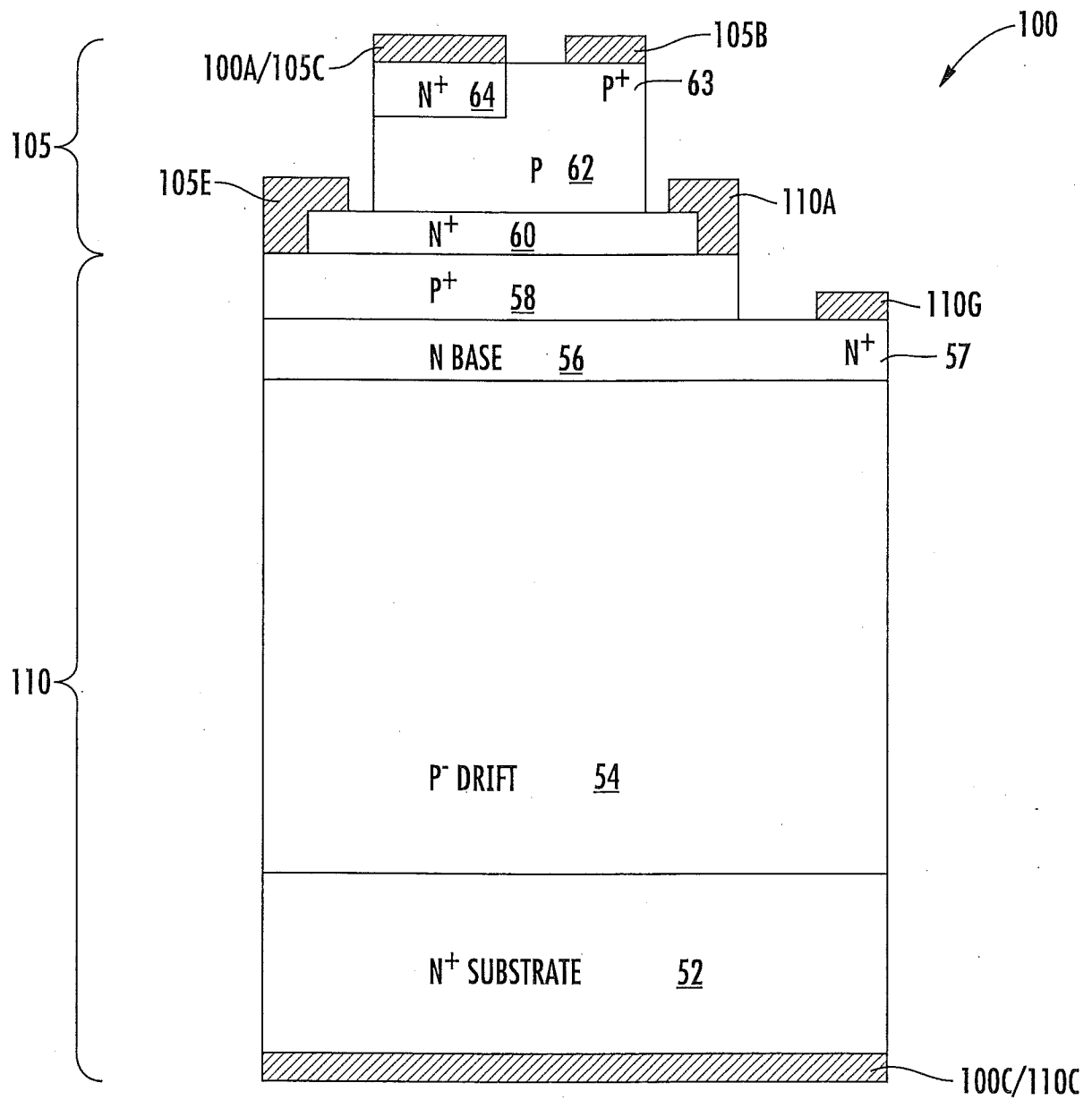


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/025053

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/74 H01L29/744 H01L25/07 H03K17/73

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 439 189 A (PETRY RICHARD E) 15 April 1969 (1969-04-15) the whole document	1-15, 21-25
A	US 6 239 463 B1 (WILLIAMS RICHARD K [US] ET AL) 29 May 2001 (2001-05-29) the whole document	1-15, 21-25
X	US 4 581 542 A (STEIGERWALD ROBERT L [US]) 8 April 1986 (1986-04-08) the whole document	1-15, 21-25
A	WO 98/08259 A1 (ABB RESEARCH LTD [CH]; BAKOWSKI MIETEK [SE]; BLEICHNER HARRY [SE]; GUS) 26 February 1998 (1998-02-26) the whole document	1-15, 21-25
	----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

19 April 2010

Date of mailing of the international search report

02/07/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Kusztelan, Leonard

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/025053

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 160 920 A (COURIER DE MERE HENRI) 10 July 1979 (1979-07-10) the whole document -----	1-15
A	US 5 155 289 A (BOWLES EDWARD E [US]) 13 October 1992 (1992-10-13) the whole document -----	1-15
A	US 2004/183079 A1 (KANEKO SAICHIROU [JP] ET AL) 23 September 2004 (2004-09-23) the whole document -----	1-15, 21-25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/025053

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-15, 21-25

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15, 21-25

Control means for a cascode switch comprising series connected high band gap hybrid bipolar and thyristor/GTO devices

2. claims: 16-20

A packaged cascode switch comprising series connected high band gap hybrid bipolar and thyristor/GTO devices, the bipolar device having a non-negative temperature coefficient in the conducting state

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2010/025053

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 3439189	A	15-04-1969	NONE	
US 6239463	B1	29-05-2001	NONE	
US 4581542	A	08-04-1986	NONE	
WO 9808259	A1	26-02-1998	EP 0958610 A1 US 5831287 A	24-11-1999 03-11-1998
US 4160920	A	10-07-1979	DE 2731383 A1 FR 2347780 A1 JP 53014543 A	26-01-1978 04-11-1977 09-02-1978
US 5155289	A	13-10-1992	NONE	
US 2004183079	A1	23-09-2004	JP 2004247545 A US 2006208261 A1	02-09-2004 21-09-2006