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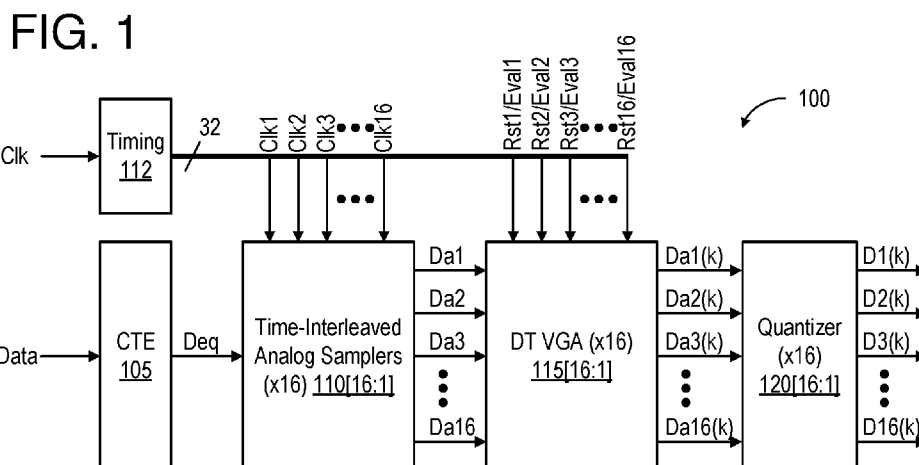
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(54) Title: SERIAL-LINK RECEIVER USING TIME-INTERLEAVED DISCRETE TIME GAIN



(57) **Abstract:** A serial receiver combines continuous-time equalization, analog interleaving, and discrete-time gain for rapid, efficient data reception and quantization of a serial, continuous -time signal. A continuous-time equalizer equalizes a received signal. A number N of time-interleaved analog samplers sample the equalized continuous-time signal to provide N streams of analog samples transitioning at rate reduced by 1/N relative to the received signal. A set of N discrete-time variable-gain amplifiers amplify respective streams of analog samples. A quantizer then quantizes the amplified streams of analog samples to produce a digital signal.

SERIAL-LINK RECEIVER USING TIME-INTERLEAVED DISCRETE TIME GAIN

BACKGROUND

[0001] Wired communication refers to the transmission of data over a wire-based communication technology. Receiving such data, particularly at high data rates, requires sensitive, linear analog amplifiers. An amplifier is linear if its output is a linear function of its input, which means in part that signal components of different frequencies receive the same level of amplification. Linearity is difficult to obtain in practice and is a main factor limiting the speed performance of analog receivers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The detailed description is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0003] Figure 1 depicts a serial receiver 100 that uses a combination of time-interleaving and discrete-time gain for rapid, efficient data reception and quantization of a serial, continuous-time signal Data on a like-identified single-ended or differential input node.

[0004] Figure 2A details an embodiment of discrete-time variable-gain amplifier 115(1), one of sixteen such amplifiers 115[16:1] introduced in Figure 1.

[0005] Figure 2B is a timing diagram 225 illustrating the operation of discrete-time variable-gain amplifier 115(1) of Figure 2A.

DETAILED DESCRIPTION

[0006] Figure 1 depicts a serial receiver 100 that uses a combination of continuous-time equalization, analog interleaving, and discrete-time gain for rapid, efficient data reception and quantization of a serial, continuous-time input signal Data on a like-identified single-ended or differential input node. Signal Data is conveyed at a relatively high symbol rate, 56GBd (56 billion symbols per second) as of this writing. A continuous-time equalizer 105 equalizes signal

Data to provide an equalized continuous-time signal Deq that operates at the same symbol rate. In this context, a “continuous-time” signal is one that is continuous in time, and a “continuous-time” equalizer is one that is also continuous in time, e.g. it does not use any clocking and operates over a range of frequencies. Suitable continuous-time equalizers are well known to those of skill in the art so a detailed discussion is omitted.

[0007] A set of sixteen time-interleaved analog samplers 110[16:1] samples equalized continuous-time signal Deq using sixteen differently phased clock signals $Clk1$ through $Clk16$ to obtain sixteen respective series of analog samples $Da1$ through $Da16$. Timing circuitry 112 derives clock signals $Clk1$ through $Clk16$ from a reference clock signal Clk synchronized to signal $Data$. Each analog sample expressed in series $Da1$ through $Da16$ is a voltage level corresponding to one symbol time of equalized continuous-time signal Deq . Time interleaving samplers 110[16:1] reduces the sample rate by a factor of sixteen, and thus relaxes time constraints on downstream circuitry and increases overall gain bandwidth. In this embodiment in which signal $Data$ is conveyed at 56GBd, for example, analog sample streams $Da1$ through $Da16$ are each conveyed at about 3.5GBd. The number of time-interleaved analog samplers can be generalized to N , which may be more or fewer than sixteen in other embodiments. Analog samplers, such as so-called “track-and-hold amplifiers,” are well known to those of skill in the art.

[0008] Each of the sixteen time-interleaved analog samplers 110[16:1] feeds a corresponding one of sixteen discrete-time variable-gain amplifiers 115[16:1]. Amplification through discrete-time variable-gain amplifiers 115[16:1] is linear relative to continuous-time variable-gain amplifiers and contributes to the overall linearity of receiver 100. Considering equalized, continuous-time signal $Da1$, for example, one of discrete-time variable-gain amplifiers 115[16:1] provides linear amplification of that series of analog symbols to produce an amplified series of analog samples $Da1(k)$. Timing circuitry 112 controls the timing of discrete-time variable-gain amplifiers 115[16:1] by issuing sixteen sets of reset and evaluation signals $Rst\#/Eval\#$, examples of which are detailed below in connection with Figures 2A and 2B. The remaining fifteen amplifiers 115[16:1] similarly amplify signals $Da2$ - $Da16$ to produce amplified series of analog samples $Da2(k)$ through $Da16(k)$. In general, a signal $x_n(k)$ represents a sample from the n th instance of $n=16:0$ constituent amplifier 115[16:1] at a discrete time k . The voltage gain provided by discrete-time variable-gain amplifiers 115[16:1] in the discrete-time domain reduces

the need for continuous-time amplification at earlier stages. Reduced continuous-time amplification allows CTE 105 and analog samplers 110[16:1] to operate at lower voltage levels, and thus in more linear amplification ranges. Finally, a set of sixteen conventional quantizers 120[16:1] coupled to the outputs of discrete-time variable-gain amplifiers 115[16:1] quantizes analog, discrete-time signals $Da1(k)$ through $Da16(k)$ to produce sixteen series of digital signals $D1(k)$ - $D16(k)$ that collectively convey the digital values represented by the original received continuous-time signal Data.

[0009] Figure 2A details an embodiment of discrete-time variable-gain amplifier 115(1), one of sixteen such amplifiers 115[16:1] introduced in Figure 1. Amplifier 115(1) is a differential amplifier with a gain stage that employs a pair of NMOS transistors M1 and M2 with control terminals (gates) connected to complementary input nodes to receive differential analog signal $Da1$. The sources (current-handling terminals) of transistors M1 and M2 are coupled to a lower power-supply terminal V_{ss} via respective current sources 200 and to one another via a variable resistance 205. The drains (also current-handling terminals) of transistors M1 and M2 are selectively coupled to complementary output nodes $Da1(k)$ via ganged switching elements 210, both controlled by evaluation signal $Eval1$, which can be of transistors (not shown). Output nodes $Da1(k)$ are also coupled to upper power-supply terminal V_{dd} via a pair of capacitors 215 and ganged switching elements 220 that selectively discharge capacitors 215 responsive to reset signal $Rst1$.

[0010] Figure 2B is a timing diagram 225 illustrating the operation of discrete-time variable-gain amplifier 115(1) of Figure 2A. The trace for signal $Da1$ represents the analog voltage difference between the gates of transistors M1 and M2, which voltage difference can be positive or negative depending upon the value expressed by the symbol under consideration. The trace for signal $Da1(k)$ represents the positive or negative voltage difference between differential output nodes $Da1(k)$.

[0011] Signals $Rst1$ and $Eval1$, both digital, are low from time $T0$ to $T1$ to open switching elements 210 and 210. Output nodes $Da1(k)$ thus float at voltages that are a function of a prior symbol. Reset signal $Rst1$ is asserted at time $T1$ to close switching elements 220 to discharge capacitors 215. Both nodes $Da1(k)$ are thus set to the high supply voltage V_{dd} and their differential value to zero. An evaluation stage begins at time $T2$ when reset signal $Rst1$ returns low and evaluation signal $Eval1$ is asserted. Switching elements 220 open and switching

elements 210 close. The relative voltages across capacitors 220 thus change as a function of the currents through transistors M1 and M2, and thus the differential voltage across the gates of transistors M1 and M2. The voltage across each capacitor 215, and thus across output nodes Da1(k), changes linearly responsive to the constant currents pulled by current sources 200. Beginning evaluation with output nodes Da1(k) at supply voltage Vdd maximizes signal headroom and amplitude to further contribute to linearity. Source degeneration established by resistor 205 also contributes by reducing the impact of the input transconductances of transistors M1 and M2 on the gain of amplifier 115(1). Resistance 205 can be tuned to establish a desired level of source degeneration and to match and calibrate amplifier 115(1) with respect to the other variable-gain amplifiers 115[16:2].

[0012] The evaluation stage ends at time T3 when evaluation signal Eval1 is deserted, leaving a measure of symbol magnitude stored as a voltage across nodes Da1(k). Quantizer 120(1) quantizes the analog value of signal Da1(k) between times T3 and T4 to produce a digital value D1(k) (Figure 1). Reset signal Rst1 is once again asserted in anticipation of the next symbol. Each of the reset and read stages takes about 25% of one symbol time in this example, leaving 50% for evaluation.

[0013] Input signal Data is a PAM-4 signal (for pulse-amplitude modulation, 4-level) in the example of Figure 1. That is, signal Data is modulated using four pulse amplitudes to represent symbols, each symbol conveying two binary bits (i.e., 00, 01, 10, and 11). Quantizer 120[16:1] quantizes each analog level—each symbol—of sixteen 3.5GBd series Da[16:1](k) into two bits for a total data rate of 112Gb/s ($3.5\text{GBd} * 16 * 2\text{bits} = 112\text{Gb/s}$). Binary or other modulation schemes can be used in other embodiments.

[0014] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding. In some instances, the terminology and symbols may imply specific details that are not required. The term "coupled," for example, is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Furthermore, while the subject matter has been described in connection with specific embodiments, other embodiments are also envisioned. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description. Only those claims specifically reciting "means for" or "step for" should be construed in the manner required under the sixth paragraph of 35 U.S.C. §112.

CLAIMS

What is claimed is:

1. A receiver comprising:

a continuous-time equalizer to equalize a continuous-time signal conveyed at a symbol rate, thereby providing an equalized continuous-time signal at the symbol rate;

analog samplers each coupled to an output of the continuous-time equalizer, the analog samplers to sample the equalized continuous-time signal, thereby providing multiple series of analog samples, each of the multiple series of analog samples conveyed at a sample rate lower than the symbol rate; and

for each of the analog samplers:

a discrete-time variable-gain amplifier coupled to an output of the analog sampler to amplify the respective series of analog samples, thereby providing an amplified series of analog samples; and

a quantizer coupled to an output of the discrete-time variable-gain amplifier to quantize the respective amplified series of analog samples.

2. The receiver of claim 1, each of the discrete-time variable-gain amplifiers including:

a transistor having:

a control terminal coupled to the output of the analog sampler;

a first current-handling terminal; and

a second current-handling terminal; and

a first switching element to selectively connect the first current-handling terminal to the quantizer.

3. The receiver of claim 2, each of the discrete-time variable-gain amplifiers further including a capacitor connected between the switching element and a power-supply terminal.

4. The receiver of claim 3, each of the discrete-time variable-gain amplifiers further including a second switching element connected in parallel with the capacitor, the second switching element to selectively discharge the capacitor.

5. The receiver of claim 4, further comprising timing circuitry coupled to the discrete-time variable-gain amplifier, the timing circuitry to control the first switching element to charge the capacitor responsive to each of the analog samples.
6. The receiver of claim 5, the timing circuitry to control the second switching element to discharge the capacitor between the analog samples.
7. The receiver of claim 6, the second switching element to discharge the capacitor to zero volts.
8. The receiver of claim 2, each of the discrete-time variable-gain amplifiers further including a current source coupled between the second current-handling terminal and a power-supply terminal.
9. The receiver of claim 8, further comprising a second current source coupled between the second current-handling terminal and the power-supply terminal, the receiver further comprising an impedance disposed between the second current source and the second current-handling terminal.
10. The receiver of claim 9, wherein the second impedance is programmable.
11. A method for quantizing a continuous-time signal conveyed at a symbol rate, the method comprising:
 - equalizing a continuous-time signal, conveyed at a symbol rate, to provide an equalized continuous-time signal at the symbol rate;
 - periodically sampling the equalized continuous-time signal responsive to phase-offset clock signals, thereby providing multiple series of analog samples;
 - amplifying each of the multiple series of analog samples to produces multiple amplified series of analog samples; and
 - quantizing each of the multiple amplified series of analog samples.
12. The method of claim 11, wherein the periodically sampling comprises charging a capacitor responsive to the equalized continuous-time signal.

13. The method of claim 12, further comprising discharging the capacitor between the series of analog samples.

14. The method of claim 13, wherein the discharging of the capacitor sets a voltage across the capacitor to zero.

15. The method of claim 12, wherein the charging of the capacitor comprises drawing a constant current through the capacitor.

16. The method of claim 11, wherein the equalized continuous-time signal comprises complementary signal halves.

17. The method of claim 11, wherein quantizing each of the multiple amplified series of analog samples comprises quantizing each analog symbol in each of the multiple amplified series of analog symbols.

18. The method of claim 17, wherein the quantizing produces two binary bits for each of the analog symbols in each of the multiple amplified series of analog symbols.

19. A receiver comprising:

a continuous-time equalizer to equalize a continuous-time signal conveyed at a symbol rate, thereby providing an equalized continuous-time signal at the symbol rate;

differential analog samplers each coupled to an output of the continuous-time equalizer, the differential analog samplers to sample the equalized continuous-time signal, thereby providing multiple series of analog samples, each of the multiple series of analog samples conveyed at a sample rate lower than the symbol rate; and

for each of the analog samplers, a discrete-time variable-gain amplifier coupled to an output of the analog sampler to amplify the respective series of analog samples, thereby providing an amplified series of analog samples.

20. The receiver of claim 19, further comprising a quantizer coupled to an output of the discrete-time variable-gain amplifier to quantize the respective amplified series of analog samples.

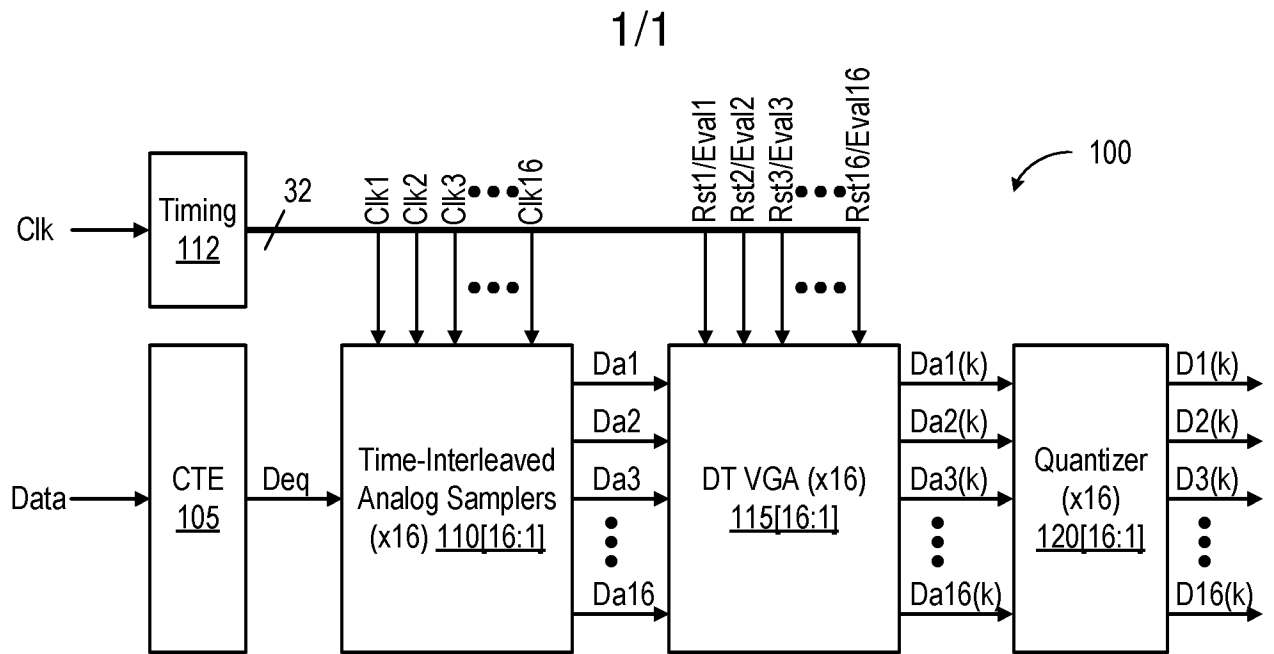


FIG. 1

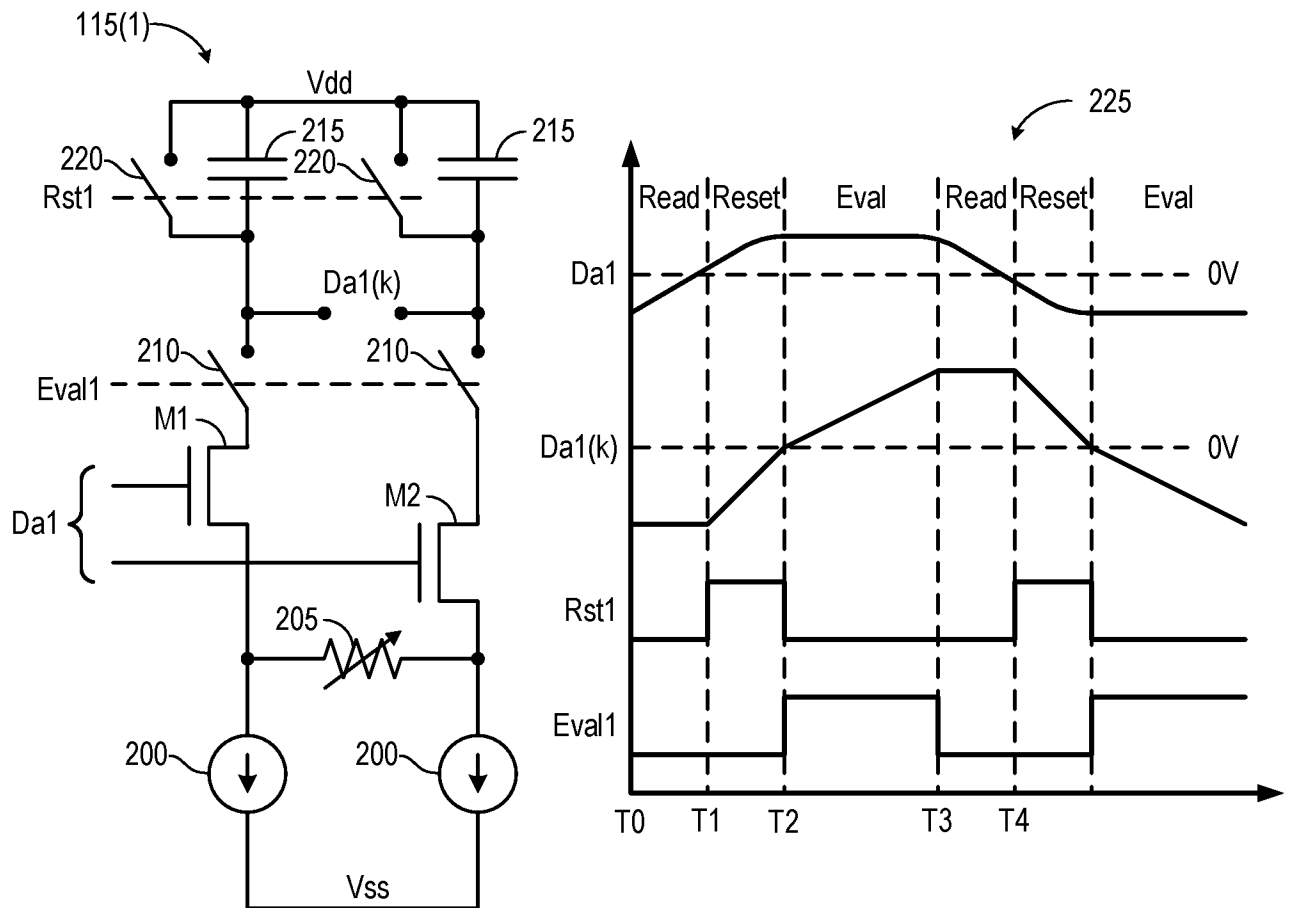


FIG. 2A

FIG. 2B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 19/23913

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H04L 25/03; H03M 1/50; H03M 1/08 (2019.01)

CPC - H04L 25/03; H03M 1/121; H03M 1/50; H03M 1/185; H03M 1/08; H03M 1/06; H03M 3/466

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2017/0295039 A1 (Fujitsu Limited) 12 October 2017 (12.10.2017); entire document, especially, abstract, FIG.1, para [0025], [0026], [0028], [0033], [0034], [0036], [0037].	1-20
Y	WO 2017/066251 A1 (Rambus Inc) 20 April 2017 (20.04.2017); entire document, especially, abstract, FIG.22, para [0138], [0145], [0146]	1-20
Y	US 2015/0326198 A1 (Linear Technology Corporation) 12 November 2015 (12.11.2015); entire document, especially, abstract, FIG. 3A-4, para [0034], [0037], [0039], [0056], claim 1	2-10
Y	US 2003/0174023 A1 (Miyasita) 18 September 2003 (18.09.2003); entire document, especially, abstract, FIG.18, 61, 62, para [0040], [0043], [0090] - [0096], [0247]	3-7, 12-15
Y	US 2006/0132191 A1 (Palmer) 22 June 2006 (22.06.2006); entire document, especially, abstract, FIG.3, 4, para [0018], [0022]	16
Y	US 2012/0076181 A1 (Aziz et al.) 29 March 2012 (29.03.2012); entire document, especially, abstract, para [0024]	18
Y	US 7,889,006 B1 (Jones) 15 February 2011 (15.02.2011); entire document, especially, abstract, FIG. 4, col.9, 7-31,	8-10
A	US 2011/0228823 A1 (Lutz et al.) 22 September 2011 (22.09.2011); entire document,	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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