

[54] **DISPLAY DEVICE WITH MEANS FOR DRAWING VECTORS**

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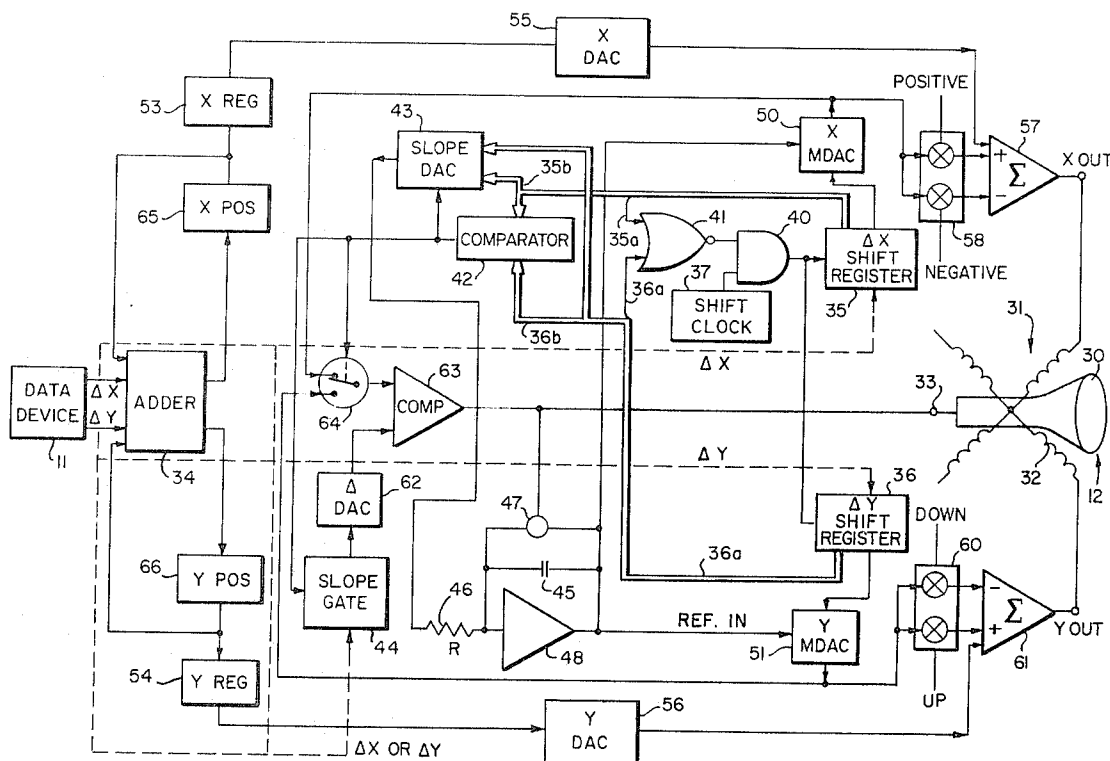
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[57]

ABSTRACT

A system for displaying (straight lines) of variable length and angle on a cathode ray tube with the beam deflection rate being substantially constant regardless of line length or angle. Each line is defined by its starting point and deflection components ΔX and ΔY along axes in a rectangular coordinate system. Two binary numbers identify the deflection components. Both numbers are shifted to the left in respective ΔX and ΔY registers until a "one" in one of the numbers reaches the leftmost stage in its register. This number corresponds to a deflection component along the "major" axis, i.e., the axis with the larger deflection. X and Y multiplying digital-to-analog converters receive a common ramp voltage and the respective shifted numbers. The larger number, after being shifted, controls the ramp voltage slope so an output signal from the multiplying digital-to-analog converter associated with the major axis has a constant slope when any length line is drawn. Hence, all lines are drawn with the same constant velocity component along the major axis.

5 Claims, 3 Drawing Figures



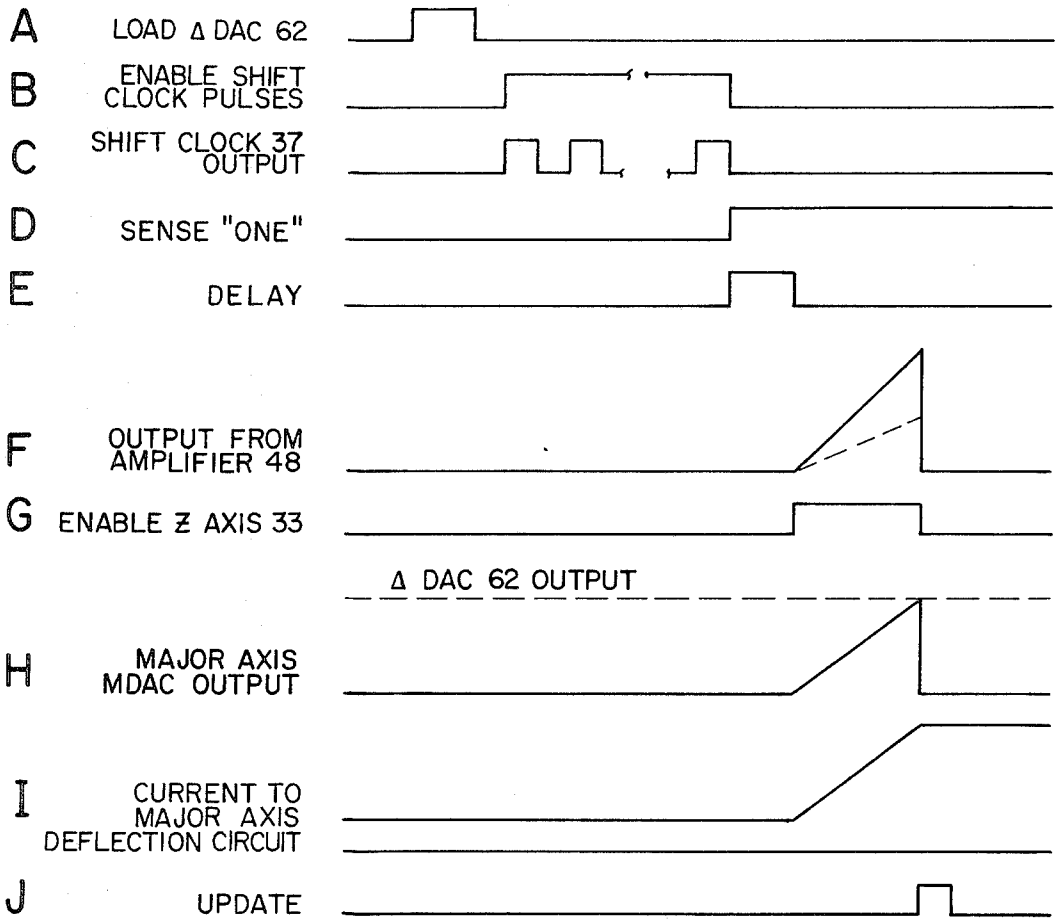
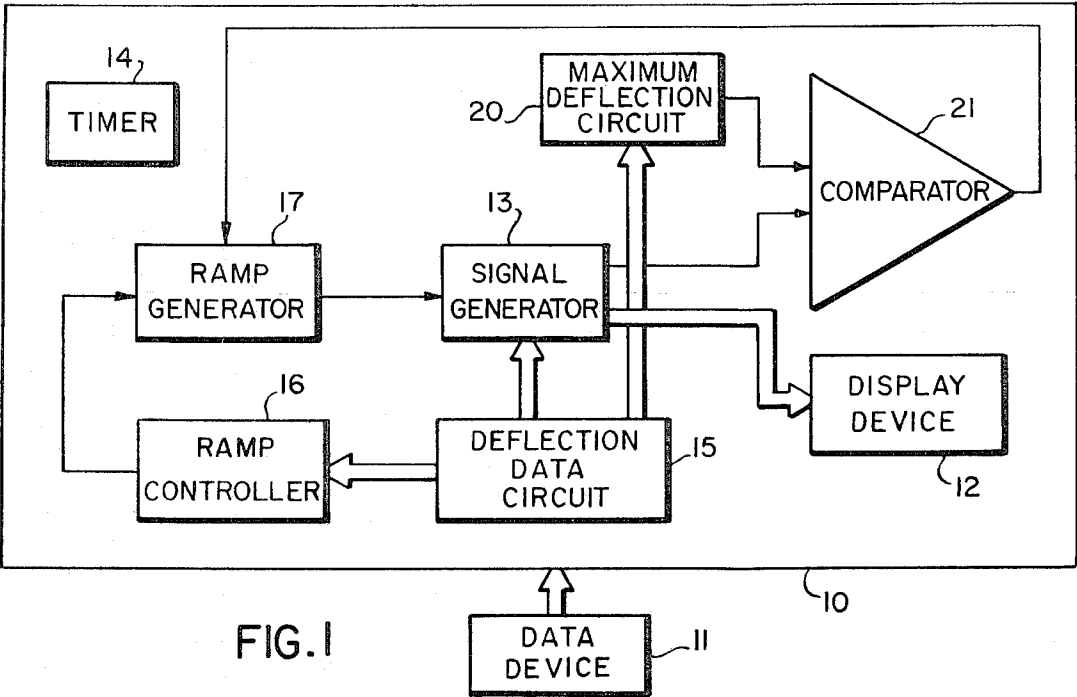
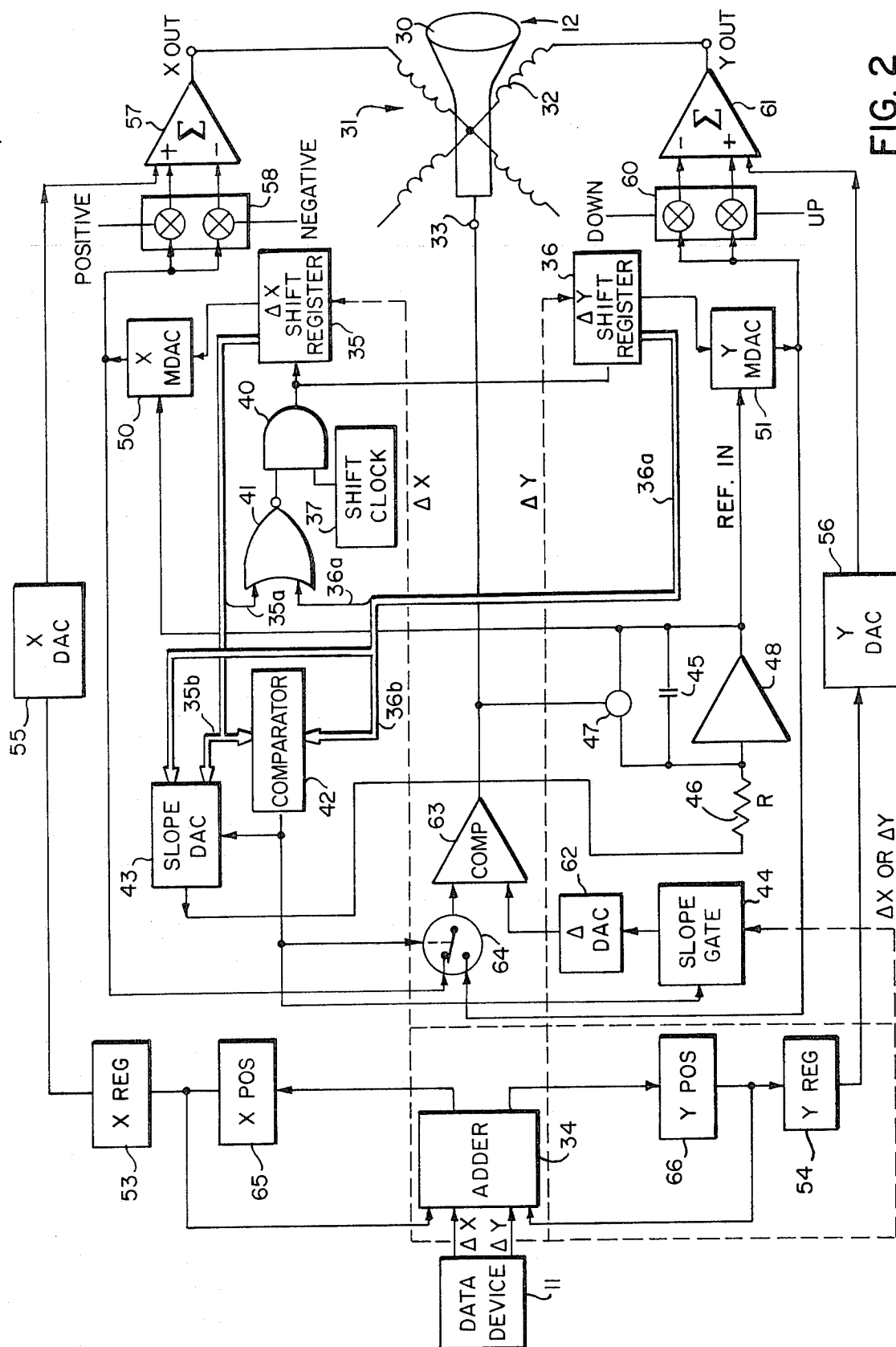


FIG. 3



DISPLAY DEVICE WITH MEANS FOR DRAWING VECTORS

BACKGROUND OF THE INVENTION

This invention generally relates to display devices and more specifically to devices for displaying straight lines on cathode ray tube screens or the like in response to digital data inputs.

There are two basic types of display devices for drawing straight lines on a plane which both use a Cartesian coordinate system to identify points in the plane. In "point-to-point" systems, the coordinates of the end points of each line are given and the line is drawn from one point to the other. In a second type, called the "vector" system, a starting point and required deflection along X and Y axes define the line.

There are two types of vector display systems. In a "constant time" system, the time to draw any line is constant regardless of line length. However, the velocity of the "writing element" (e.g., electron beam in a cathode ray tube device or ink pen in a X-Y plotter device) is proportional to line length. As the intensity of a line, in turn, may vary inversely with the velocity of the writing element, a long line may be noticeably dimmer than a short line.

A "constant velocity" display should overcome the intensity problem. However, prior "constant velocity" systems do not compensate for a wide range of line lengths. For example, in one specific display, binary numbers representing deflections along X and Y axes are compared and a composite group of digital signals are generated. In response, a weighting circuit then sets an analog signal to one of three values depending upon the relative magnitudes of the range of the absolute magnitude deflections along the axes. As a result, there are a number of different velocities that may occur. This type of system does reduce line brightness variations. However, the wide range of line length variations and angles still produce noticeable intensity variations.

Therefore, it is an object of this invention to provide a constant velocity display which more nearly approximates a true constant velocity system.

Another object of this invention is to provide a display which draws a vector on a cathode-ray tube display without noticeable intensity variations.

SUMMARY

In accordance with my invention, a display system stores deflection data for the X and Y axes as separate binary numbers. The system shifts both numbers to the left until a "one" appears in one of the most significant bit position. If the larger deflection is associated with the X axis, then the X axis is the "major axis" for the display. The shifted binary number associated with the major axis sets the slope of a ramp voltage. This ramp voltage energizes two digital-analog converter circuits in parallel. Each shifted binary number is a second input to one converter circuit. Each converter circuit produces an output which is a function of the product of ramp voltage and the shifted binary number. Changes in the ramp voltage slope and values shifted to the converter circuit associated with the major axis are offsetting, so that the output signal from that circuit always has the same slope and the line is drawn with a

constant velocity component in the major axis, notwithstanding its length.

As shown below, the shifting operation assures that the maximum velocity variation along the major axis cannot exceed a 2:1 ratio. In turn, this permits the use of a conventional ramp generator, which produces a narrow range of ramp slopes for the other converter inputs, to decrease the trace velocity. The resulting velocity range speed is approximately 1.4:1, so there are no noticeable brightness changes for lines of different lengths.

This invention is pointed out with particularity in the appended claims. A more thorough understanding of the above and further objects and advantages of this invention may be attained by referring to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a display system in accordance with my invention;

FIG. 2 is a detailed schematic diagram of one embodiment of a display system using my invention; and

FIG. 3 is a chart which indicates a typical sequence of events in a display system shown in FIGS. 1 and 2.

DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

As will become apparent, this invention may be applied to display systems with retentive or non-retentive display surfaces. Examples of the former include X-Y plotters and cathode ray tubes with retentive screens. Conventional cathode ray tubes are in the second category, and they must be "refreshed" by continuously re-tracing any given display on the screen at a rate which provides a persistent display. Although the following description merely discusses the operation for drawing one line one time, the invention is applicable to both retentive and non-retentive displays and to systems which draw curves using a series of straight-line segments.

Now referring to FIG. 1, a display system 10 incorporating my invention receives four items of data from a data device 11. Two items are binary numbers representing the X and Y coordinates of one end of a line to be traced. The other two items constitute the deflections along the X and Y axes required to trace the line.

Within the display system 10, a cathode ray tube display device 12 receives signals from a signal generator 13. Two of these signals are analog signals (hereinafter an "X signal" and a "Y signal") which respectively energize X and Y deflection circuits of the display device 12. The other is a blanking or "Z" signal. The "Z" signal enables or disables a beam in a cathode ray tube display or raises or lowers the marking element in a X-Y plotter from the paper. Other signals for the display device 12 are not necessary to an understanding of this invention.

Still referring to FIG. 1, a timer 14 controls operation within the display system 10. A deflection data circuit 15 stores binary numbers associated with deflections along the X and Y axes and contains circuitry for determining which of the two deflection binary numbers is larger and for shifting both simultaneously to the left. The larger number is associated with a "major" axis

and shifting largely normalizes the representation of the component of the line along this axis. Subsequently, the shifted or normalized binary numbers are gated into the signal generator 13. In addition, the shifted binary number which defines the major axis sets the output of a ramp controller 16. This ramp controller, in turn, sets the slope of a ramp signal from a ramp generator 17.

The signal generator 13, in essence, multiplies the ramp signal and each normalized binary number to produce X and Y deflection signals. As a result, the slope of the signal associated with the major axis is always the same and not dependent on line length along the major axis. The component of velocity along the major axis is therefore always the same for all lines which are traced. Moreover, the slope of the minor axis signal is proportional to the minor axis deflection required for the tracing of a straight line.

The system controls the termination of the line by storing the absolute magnitude of the major axis deflection in a maximum deflection circuit 20. This circuit generates a constant analog signal which is one input to a comparator circuit 21. The other input to this circuit 21 is the major axis output from the signal generator 13. When these two signals are equal, the comparator 21 disables the ramp generator 17 and thus terminates tracing of the line.

Finally, the display device 12 receives the X and Y signals from the signal generator 13.

As will be apparent, this system is not a true constant because the velocity (V_1) along a line is an increasing function of the velocity (V_2) along the major axis and the angle (ϕ) between the line and the major axis, the relationship being given by definition of $V_1 = V_2 / \cos \phi$. However, the angle ϕ with respect to the major axis cannot exceed 45° . The velocity range is, therefore, from V_2 to $1.41 V_2$. When the velocity is limited within this range of variation, there are usually no noticeable brightness changes.

FIG. 2 shows how this invention may be applied to a cathode ray tube (CRT) system. A cathode ray tube 30 has circuits associated with X and Y deflection coils 31 and 32, respectively. A terminal 33 represents the circuitry associated with the blanking or "Z" axis control. In the following remarks, we do not discuss any time delays in an electromagnetic display system. If such delays are present, then certain timing variations must be made, but these are within the knowledge of one ordinarily skilled in the art. Such delays might not even exist in other displays.

When the data device 11 transmits the ΔX and ΔY deflection data as binary numbers, that data is received in an adder 34 and ΔX and ΔY shift registers 35 and 36 under the control of pulses from the timer 14. Then the timer 14 (FIG. 1) generates a pulse (GRAPH A in FIG. 3) to transfer the larger deflection component through a slope gate 44 to a ΔDAC register 62 (FIG. 2) for purposes discussed later. As shown in GRAPH B (FIG. 2), the timer 14 then generates an enabling signal so a shift clock 37 begins pulsing AND circuit 40 (GRAPH C in FIG. 3). Each pulse defines a time period for an iteration during which contents in the ΔX and ΔY shift registers 35 and 36 shift simultaneously one place to the left.

For purposes of this discussion, a conductor 35a connects to the most significant bit (leftmost) position in the ΔX shift register 35, while a bus 35b connects to

the remaining positions. Normally, the conductor 35a is part of the bus 35b. Similarly, a conductor 36a and a bus 36b connect to a corresponding position in the ΔY shift register 36. When a "ONE" appears in either of the two most significant bit positions, the signal level in conductor 35a or 36a jumps as shown in GRAPH D so a NOR circuit 41 disables the gate 40 (GRAPH B). This disconnects the shift clock 37 and terminates the iterative shifting operation.

The appearance of a "ONE" in a most significant bit position also causes the timer 14 (FIG. 1) to begin a time delay shown in GRAPH E of FIG. 3 to allow the data to settle before it is used. This delay may be omitted in some circuits. The contents of the registers 35 and 36 at this point may be termed "normalized deflections."

During the interval preceding the delay, several events occurred. Specifically, comparator 42 determined which shift register contained the larger deflection number and then moved it into the ΔDAC 62. It also controlled the transfer of the larger binary number, after it is shifted, to a digital-to-analog converter 43 (hereinafter slope DAC 43).

The slope DAC 43 generates an analog output voltage which varies inversely as the magnitude of the binary number applied at its input. That is, if all "ONES" are applied to the slope DAC 43, the output signal is at a minimum value, while all "ZEROES" will generate a maximum output signal. As will be apparent, however, with one exception in which both deflections are zero, the most significant bit into the slope DAC 43 is always a "ONE." Therefore, the output of the slope DAC ranges from a minimum to some intermediate value (usually twice the minimum) as shown in GRAPH F.

During any operation, the binary number is constant so the analog output voltage is constant. The voltage is integrated by an integrator circuit comprising a feedback capacitor 45, input resistor 46, control switch 47 and amplifier 48. The integrator circuit thus generates a linear ramp signal where slope is proportional to the output signal from the slope DAC 43. Specifically, when the slope DAC 43 generates its minimum output voltage, the ramp has a base slope with respect to time (the dashed line in GRAPH F). As the binary number which controls the slope DAC 43 decreases, the analog output voltage increases and so the ramp slope also increases. If there is a 2:1 ratio in the DAC output voltage range, the integrator circuit generates a ramp voltage which has a slope between the base slope or twice the base slope.

The ramp signal serves as the analog or reference input for a multiplying digital-to-analog converter 50 associated with the X axis, (hereinafter X MDAC 50) and another MDAC associated with the Y axis (hereinafter Y MDAC 51). A multiplying digital-to-analog converter is a digitally adjustable variable gain follower with an output equal to an analog input signal multiplied by the value of a digital input. In this particular application, the digital inputs are the normalized deflections in the respective registers 35 and 36; the analog input is the ramp signal.

Accordingly, the output of each MDAC is a ramp voltage whose slope is the product of the digital input to MDAC and the slope of the ramp output of the integrator amplifier 48. Moreover, the MDAC digital inputs are proportional to the X and Y deflections (ΔX and ΔY), since the shifting operation in the registers 35

and 36 merely multiplies the contents of these registers by the same factor. The slopes of the MDAC 50 and 51 outputs are, therefore, related to each other by the ratio $\Delta X/\Delta Y$. These outputs are the X and Y deflection voltages and their slopes thus govern the X and Y velocity components of the electron beam in cathode ray tube 30. The velocity components are therefore also in proportion by the ratio $\Delta X/\Delta Y$.

The normalized major axis deflection may be as little as 1,000-- and as great as 1111---, approximately a 2:1 range. With a constant slope, of the ramp voltage applied to the MDAC's 50 and 51, this would result in a 2:1 range in the major axis component of the trace velocity. The ramp slope control by the slope DAC 43, as described above, provides an offsetting 2:1 range of ramp slopes and the major axis trace velocity is therefore constant, i.e., independent of line length. The minor axis velocity may vary from zero to a value equal to the major axis velocity and consequently the overall velocity may vary over a range of 1.41:1. This is well within the requirement for an apparently constant trace intensity.

The outputs of the XDAC 55 and X MDAC 50 are summed by a summing circuit 57 which generates the analog signal for the X deflection circuitry 31. In order to control whether a line is drawn from right-to-left or left-to-right the X MDAC 50 may energize either a positive (+) or (-) summing circuit input. A switch 58 responds to a POSITIVE signal to cause the summing circuit 57 to add the two analog signals; when a NEGATIVE signal appears, the summing circuit 57 actually subtracts the signals. In the first case, the line moves to the right; in the second case, it moves to the left. A similar switching circuit 60 couples the output of the Y MDAC 51 to a summing circuit 61 that also receives the output of the YDAC 56 to energize the Y axis deflection circuitry 32. A POSITIVE signal causes the beam to move upwardly during the tracing; a NEGATIVE signal causes it to move downward.

The slope gate 44 enables the digital-to-analog converter 62 (a Δ DAC) to receive the major axis deflection from the data device 11 before the shifting operation. The resulting analog signal is one input of a comparator 63; it represents the limits of deflection along the major axis. The other input to the comparator 63 comes from a switch 64 controlled by the comparator 42, which couples the output of the major axis MDAC (MDAC 50 or 51) to the comparator 63. As the output from the major axis MDAC represents the instantaneous deflection along the major axis, the comparator 63 indicates when the beam reaches the end of its major axis deflection and this, in turn, coincides with completion of the line then being drawn.

When the timer 14 (FIG. 1) completes the delay interval (GRAPH E in FIG. 3), the switch 47 opens and the integrator amplifier 48 begins to generate the ramp (GRAPH F) with slopes in the range shown between the solid and dashed lines. A signal from the comparator 63 at the Z axis terminal 33 turns on the cathode ray tube beam as shown in GRAPH G.

Graph H shows the major axis MDAC output. It has a constant slope, notwithstanding the slope of the signal from the amplifier 48 (GRAPH F). As shown in GRAPH I, the current to the major axis deflection circuit depends on the starting position held in the XDAC 55 or the YDAC 56. The appropriate summing amplifier 57 or 61 generates this signal for the deflection

coil, but no display occurs because the voltage on terminal 33 inhibits the beam. As soon as the switch 47 opens, simultaneously with the voltage to the terminal 33 enabling the beam, the major axis MDAC output begins to increase linearly from zero.

This action continues and the beam traces a straight line. When the major axis MDAC 50 or 51 generates an output signal (GRAPH H) which reaches a value corresponding to the output from the Δ DAC 62 (and represented by the dashed line in GRAPH H), the timer terminates all operations. Specifically, the timer turns off the beam, deactivates the comparator 63 and closes the switch 47.

The timer 14 (FIG. 1) also generates an update pulse (GRAPH J) which couples the outputs of X and Y position registers 65 and 66, respectively, to the X register 53 and Y register 54. Hence, the X and Y registers 53 and 54 contain data which has been updated digitally and therefore is not subject to any signal shifts which might occur over an extended period if the position were stored in an analog fashion such as by charging a capacitor. This updated data may represent the beginning point of the next line to be drawn and, as shown in GRAPH I, the current to the deflection circuits 31 and 32 assumes the new level. Then the system is ready to trace the next line.

As will be apparent, there are many modifications which can be made to the circuit previously described. For example, different methods for comparing the binary numbers to determine the major axis or controlling the deflection along the X and Y axes may be substituted for those specifically described circuits with the attainment of some, if not all, of the advantages of this invention. Thus, the foregoing description indicates that the entire value of the larger shifted binary number is used to control the slope DAC 43. In fact, I find that reasonable accuracy can be attained by using only the three or four of the most significant digit positions from the ΔX or ΔY shift registers 35 and 36.

Therefore, it is the object of the appended claims to cover all such variations and modifications as come within the true spirit and scope of this invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. In a display device for drawing a line based on rectangular coordinates by deflecting a displayed point from a starting position, the improvement of means for controlling the point deflection along the line comprising:

- A. means for generating signals indicating the starting position of the line,
- B. means for storing a digital representation of the deflection component from said starting position along each of perpendicular axes,
- C. a variable slope ramp generator,
- D. comparator means for determining the larger digital representation,
- E. iteratively operable means connected to said storage means for normalizing both digital representations by detecting the location of the most significant digit of the larger digital representation,
- F. means connected to said normalizing means and ramp generator for controlling the slope of said ramp generator in response to the larger normalized representation,

- G. means for combining each of the normalized digital representations with the ramp generator output to generate deflection signals, and
- H. means responsive to said deflection signals for deflecting said point whereby the velocity component along the axis with the larger deflection component is substantially uniform.
2. A display device as recited in claim 1 wherein:
- A. said ramp generator comprises an integrator circuit responsive to a dc input voltage for generating a linear output signal having a slope dependent upon the magnitude of the dc input voltage, and
- B. said slope control means comprises a digital-to-analog converter and means for applying larger normalized representation to said digital-to-analog converter, the analog output signal said converter energizing said integrator.
3. A display as recited in claim 1 wherein said normalizing means comprises first and second shift registers for receiving digital deflection data for first and second axes, respectively, and means for shifting the data in each register toward a most significant bit position and means responsive to a "ONE" in the most significant bit position for inhibiting said shifting means.
4. A display device as recited in claim 3 wherein said combining means comprises first and second multiplying digital-to-analog converters associated with the first and second perpendicular axes respectively, each said multiplying digital analog converters having a first input for receiving digital data and a second input for being energized by said ramp generator, and means responsive to a completion of a shifting operator for transferring the normalized contents of said shift registers to the respective multiplying digital-to-analog converters and thereafter enabling said ramp generator, each of said multiplying digital-to-analog converters generating an analog output signal.
5. In a display device including a cathode ray tube, means for generating an electron beam to illuminate a point on a cathode ray tube defined in rectangular coordinates using X and Y axes, X axis and Y axis deflection circuits for positioning the beam, and a blanking circuit for turning the beam on and off, the improvement of means for controlling the deflection of the beam for drawing a line in response to digital data defining the coordinates of a starting position of the line and the deflections of the line from the starting position along the X and Y axes, the circuit comprising:
- A. means for generating first and second analog sig-

- nals, respectively, for indicating the initial position of the beam,
- B. first and second means for respectively storing the deflections along the X and Y axes as binary deflection numbers,
- C. comparator means connected to said storage means for determining the larger deflection number,
- D. iteratively operable means for simultaneously shifting the X-Y deflection numbers to detect the location of the larger deflection number and normalize the deflection numbers with respect to the larger deflection binary number,
- E. a digital-to-analog converter responsive to the normalized contents of said first or second shift means containing the larger binary number, said converter generating an analog signal,
- F. gated ramp means including input means connected to the output of said digital-to-analog converter so said ramp means generates a linear signal with a slope which varies between a normal value and twice normal value,
- G. first and second multiplying digital-to-analog converters with each having an input connected to the output of said gated ramp means, said first and second multiplying digital-to-analog converters each having digital input means for receiving the normalized outputs from said first and second shift means, respectively, each of said converters generating an analog signal which represents the product of the ramp signal and its respective digital input signal,
- H. first and second means for summing the X and Y analog signals representing starting positions and the respective outputs from said first and second multiplying digital-to-analog converters,
- I. timing means for gating said ramp means on to initiate deflection of the beam and to enable the blanking circuit to turn the beam on,
- J. reference means for generating an analog signal representation of the larger digital deflection number, and
- K. means for comparing the output signal of the multiplying digital-to-analog converter associated with the larger deflection number and the output signal of said reference means for resetting said gated ramp means and turning off the beam in response to correspondence of the two signals.

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