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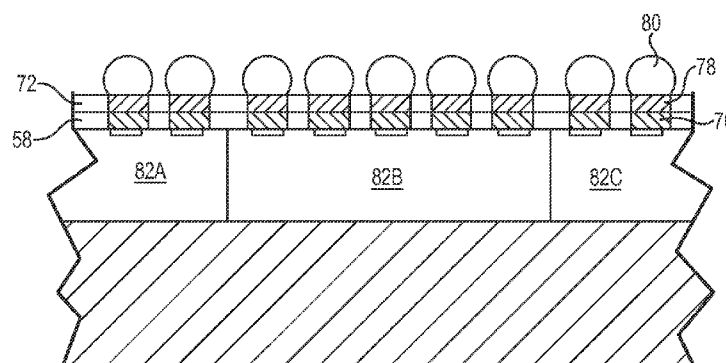


Fig. 6

(57) Abstract: A wafer-level package for semiconductor devices and a method for making the package. At least one dielectric layer is selectively printed on at least a portion of the semiconductor devices creating first recesses aligned with a plurality of electrical terminals on the semiconductor devices. A conductive material is printed in the first recesses to form contact members on the semiconductor devices. At least one dielectric layer is selectively printed to create a plurality of second recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the second recesses to create a circuit geometry. The circuit geometry includes a plurality of exposed terminals adapted to electrically couple to another circuit member. The wafer is diced to provide a plurality of discrete packaged semiconductor devices.

COMPLIANT PRINTED CIRCUIT WAFER LEVEL SEMICONDUCTOR PACKAGE

Technical Field

[0001] The present application is directed to leveraging the capabilities of additive printing processes to provide a wafer level semiconductor package that results in a high performance packaged IC devices after wafer dicing.

Background of the Invention

[0002] Traditional semiconductors and IC devices are typically packaged in a variety of ways to provide redistribution from the terminals on the die to a spacing that is conducive to cost effective printed circuit board ("PCB") fabrication techniques. In many cases, the size and distance between die terminals is so small that the device cannot be connected to the final PCB without some sort of fan out or routing. The packages also serve to protect the fragile silicon or provide additional functions such as thermal management or near device decoupling. In many cases, the size and distance between die terminals is so small that the IC device cannot be connected to the final PCB without some sort of re-routing interface.

[0003] Most IC devices are produced with terminals in either a peripheral pattern that runs along the edges of the IC device or an area array pattern that spans across the surface of the IC device. A main method for attachment when the terminals are in an area array pattern is to connect the terminals with solder. Basically, the package has an array of terminals that correspond to the IC device terminals. Solder is applied the terminals on the IC device and/or the package and reflowed to create the mechanical and electrical connection in a process commonly called flip chip attachment. In a flip chip attachment the IC device is flipped over to mate the terminals on the die to the terminals on the IC package substrate.

[0004] The IC devices in these types of packages are often under filled with an epoxy of some type to provide support and strength to the solder joints. The epoxy protects the solder joints during use from thermal expansion, miss-match and/or shock. In both cases, the connection of the IC device to the package is generally not reworkable once packaged and if there is a missing or broken connection it is difficult to repair.

[0005] Once the IC devices are packaged, they are usually tested in a variety of ways to determine the reliability and performance of the IC devices in the package as they would be used in the final application. In many cases, the functional performance of the IC device is not known prior to placing it into the package and if the packaged IC device fails testing the cost of the package and processing is lost.

[0006] A packaging method that has increased in popularity in recent years is called Wafer Level Packaging, where the packaging materials are applied to the IC devices directly while they are still in the wafer format prior to dicing. This method has shown to be effective for relatively small pin count devices and has some advantages over handling individual IC devices and packaging them in an offline operation. Wafer Level packages tend to have routing and termination that is within the footprint of the die and not fanned out due to the fact that the fan out would be cut when the wafer is diced.

[0007] Area array packaging has been utilized for many years, and provides a method for interconnecting IC devices with larger terminal counts than peripheral lead packaging. In general, the area array packaging is more expensive due to the larger pin counts and more sophisticated substrates required. The main limitations for area array packaging are the terminal pitch, thermal management, cost, ability to rework faulty IC devices and reliability of the solder joints.

Brief Summary of the Invention

[0008] The present disclosure is directed to providing a wafer level semiconductor package. The present semiconductor package preferably permits the IC devices to be tested prior to, or after, dicing.

[0009] The present wafer level semiconductor package resembles a traditional package in construction, but utilizes additive printing processes rather than conventional subtractive processes. The unique nature of the additive printing processes allows for a direct writing of circuitry and dielectrics, with the added benefit of stress decoupling at the terminal joints as well as embedded function not seen in traditional wafer-level packaging.

[0010] The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and flex circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the

features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0011] One embodiment is directed to a wafer including a plurality of semiconductor devices. At least one dielectric layer is selectively printed on at least a portion of the wafer to create a plurality of first recesses aligned with a plurality of electrical terminals on the semiconductor devices. A conductive material is printed in the first recesses to form contact members on the semiconductor devices. At least one dielectric layer is selectively printed to create a plurality of second recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the second recesses to create a circuit geometry. The circuit geometry includes a plurality of exposed terminals adapted to electrically couple to another circuit member. The wafer is then diced to provide a plurality of discrete packaged semiconductor devices.

[0012] Conductive plating is preferably added to one or more of the contact members and the circuit geometry. The conductive material can be sintered conductive particles or a conductive ink. In one embodiment, a compliant material is located between the exposed terminals and the semiconductor device. In another embodiment, at least one electrical device is printed on a dielectric layer and electrically coupled to at least a portion of the circuit geometry. In one embodiment, the exposed terminals extend above the package.

[0013] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to the second recesses. The use of additive printing processes permit conductive material, non-conductive material, and semi-conductive material to be located on a single layer.

[0014] In one embodiment, pre-formed conductive trace materials are located in the second recesses. The second recesses are then plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0015] In another embodiment, a conductive foil is pressed into at least a portion of the second recesses. The conductive foil is sheared along edges of the second recesses. The excess conductive foil not located in the second recesses is removed

and the second recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0016] In another embodiment, at least one external dielectric layer extends beyond the discrete packaged semiconductor devices. External routing is printed on the external dielectric layer and electrically coupled to a portion of the circuit geometry.

[0017] The discrete packaged semiconductor devices can include a plurality of semiconductor devices. The circuit geometry may include at least one of an inter-die circuit path or an intra-die circuit paths. The plurality of semiconductor devices are optionally arranged in a stacked configuration.

[0018] The present disclosure is also directed to an electrical assembly including a circuit member with a plurality of contact pads electrically coupled to the exposed terminals on the wafer-level semiconductor package. This coupling can be done before dicing of the wafer or on the discrete packaged semiconductor devices. The circuit member can be selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

[0019] This present discrete packaged semiconductor devices provide internal and/or external compliance to enhance the mechanical performance. The present discrete packaged semiconductor devices can be produced digitally, without tooling or costly artwork. The wafer-level semiconductor package can be produced as a "Green" product, with dramatic reductions in environmental issues related to the production of conventional semiconductor packages.

[0020] The present disclosure is also directed to a method of making a wafer-level semiconductor package. The method includes the step of printing at least one dielectric layer selectively on at least a portion of a wafer having a plurality of the semiconductor devices to create first recesses aligned with electrical terminals on the semiconductor devices. A conductive material is printed in a plurality of the first recesses to form contact members on the semiconductor devices. At least one dielectric layer is selectively printed on at least a portion of the wafer to create a plurality of second recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the second recesses to form a circuit geometry. The circuit geometry includes a plurality of exposed terminals

electrically coupled to the semiconductor devices. The wafer is then diced into a plurality of discrete packaged semiconductor devices.

[0021] The present disclosure is also directed to several additive processes that combine the mechanical or structural properties of a polymer material, while adding metal materials in an unconventional fashion, to create electrical paths that are refined to provide electrical performance improvements. By adding or arranging metallic particles, conductive inks, plating, or portions of traditional alloys, the compliant printed semiconductor package reduces parasitic electrical effects and impedance mismatch, potentially increasing the current carrying capacity.

[0022] The printing process permits the fabrication of functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0023] The wafer-level semiconductor package can be configured with conductive traces that reduce or redistribute the terminal pitch, without the addition of an interposer or daughter substrate. Grounding schemes, shielding, electrical devices, and power planes can be added to the semiconductor package, reducing the number of connections to the PCB and relieving routing constraints while increasing performance.

Brief Description of the Several Views of the Drawing

[0024] Figure 1 is a cross-sectional view of a method of making a wafer level semiconductor package in accordance with an embodiment of the present disclosure.

[0025] Figure 2 illustrates a method of printing dielectric material on the semiconductor package of Figure 1.

[0026] Figure 3 illustrates a method of printing contact members on the semiconductor package of Figure 1.

[0027] Figures 4 and 5 illustrate a method of printing circuit geometry on the semiconductor package of Figure 1.

[0028] Figure 6 illustrates a wafer level semiconductor package before dicing in accordance with an embodiment of the present disclosure.

[0029] Figure 7 illustrates the semiconductor package of Figure 6 after dicing.

[0030] Figure 8 illustrates a plurality of discrete packaged semiconductor devices after dicing in accordance with an embodiment of the present disclosure.

[0031] Figure 9 illustrates an alternate packaged semiconductor with printed compliant circuit geometry in accordance with an embodiment of the present disclosure.

[0032] Figure 10 illustrates the packaged semiconductor of Figure 9 electrically coupled to another circuit member in accordance with an embodiment of the present disclosure.

[0033] Figure 11 illustrates an alternate packaged semiconductor with printed electrical devices in accordance with an embodiment of the present disclosure.

[0034] Figure 12 illustrates the packaged semiconductor of Figure 11 electrically coupled to another circuit member in accordance with an embodiment of the present disclosure.

[0035] Figure 13 illustrates a stacked multichip packaged semiconductor in accordance with an embodiment of the present disclosure.

[0036] Figure 14 illustrates a layered multichip packaged semiconductor in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0037] Figure 1 is a side sectional view of semiconductor wafer 50 containing a plurality of IC devices 52A, 52B, 52C (collectively "52") located on substrate 54. The IC terminals 56 are facing up. The substrate 54 may be a temporary work surface or may be a portion of the final semiconductor package. The substrate 54 can be constructed from a variety of rigid or flexible polymeric materials, such as for example, UV stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert and resistant to fire. Other suitable plastics include phenolics, polyester (PET), polyimide (PI), polyethylene naphthalate (PEN), Polyetherimide (PEI), along with various fluoropolymers (FEP) and copolymers, and Ryton® available from Phillips Petroleum Company. For some applications, the substrate 54 can be a polyimide film due to their advantageous electrical, mechanical, chemical, and thermal properties.

[0038] Figure 2 illustrates printed layer 58 printed to top surface 60 of the wafer 50 at locations 62 between IC terminal 56. The printed layer 58 at locations 62 creates one or more recesses 64 corresponding to each of the IC terminals 56 that are used in subsequent steps of the process.

[0039] As illustrated in Figure 3, the recesses 64 for the IC terminals 56 are metalized to create contact members 70. Metalizing can be performed by printing conductive particles followed by a sintering step, by printing conductive inks, or a variety of other techniques. The metalizing material is preferably of copper or similar metallic materials such as phosphor bronze or beryllium-copper. The resulting contact members 70 are optionally plated to improve conductive properties. The plating is preferably a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple layers thereof.

[0040] As illustrated in Figure 4, dielectric layer 72 is printed on surface 74 with recesses or trenches 76 corresponding to a desired circuit geometry. Alternatively, the dielectric layer 72 is placed on surface 74. The recesses 76 can be defined by printing, embossing, imprinting, chemical etching with a printed mask, or a variety of other techniques. As illustrated in Figure 5, the recesses 76 are metalized as discussed above to create circuit geometry 78.

[0041] The printed dielectric layers 58, 72 may be constructed of any of a number of dielectric materials that provide electrostatic dissipation or to reduce cross-talk between the traces of the circuit geometry 78. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0042] In one embodiment, the circuit geometry 78 is formed by depositing a conductive material in a first state in the recesses 76, and then processed to create a second more permanent state. For example, the metallic powder is printed according to the circuit geometry and subsequently sintered, or the curable conductive material flows into the circuit geometry and is subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. "Curable" refers to an uncured material having the potential to be cured, such as for example by the application of a suitable energy source.

[0043] The recesses 64, 76 in the layers 58, 72 permit control of the location, cross section, material content, and aspect ratio of the contact members 70 and the conductive traces in the circuit geometry 78. Maintaining the conductive traces with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses 64, 76 to control the aspect ratio of the conductive traces results in a more rectangular or square cross-section of the conductive traces in the circuit geometry 78, with the corresponding improvement in signal integrity.

[0044] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 64, 76. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 64, 76. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 64, 76 not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 64, 76.

[0045] In another embodiment, a thin conductive foil is pressed into the recesses 64, 76, and the edges of the recesses 64, 76 act to cut or shear the conductive foil. The process locates a portion of the conductive foil in the trenches 64, 76, but leaves the negative pattern of the conductive foil not wanted outside and above the trenches 64, 76 for easy removal. Again, the foil in the trenches 64, 76 is preferably post plated to add material to increase the thickness of the conductive traces in the circuit geometry 78 and to fill any voids left between the conductive foil and the recesses 64, 76.

[0046] In the embodiment of Figure 6, solder balls 80 are deposited on the contact members 70 and/or the circuit geometry 78 to create packaged semiconductors 82A, 82B, 82C (collectively "82"). The packaged semiconductor devices 82 can be tested while still part of the wafer 50. As illustrated in Figure 7, the packaged semiconductor devices 82 are then singulated or cut from the wafer 50 at locations 84 using traditional methods and removed from the substrate 52.

[0047] Figure 8 illustrates an alternate embodiment in which metalized terminals 90 are printed on the circuit geometry 78 to create posts or pillars as an alternative to the solder balls 80 or bumps. The shape of the metalized terminals 90 can be altered to promote electrical coupling to another circuit member.

[0048] Figure 9 illustrates an alternate packaged semiconductor device 100 with modified terminals 102, 104 in accordance with an embodiment of the present disclosure. Resilient material 106 is preferably printed during the creation of layers 108 and the circuit geometry 109. In the preferred embodiment, dielectric material is printed to leave a recess into which the resilient material 106 is deposited. The resilient material 106 permit the terminals 102, 104 to move in all six degrees of freedom (X-Y-Z-Pitch-Roll-Yaw) to facilitate electrical coupling with another circuit member 116 (see Figure 10). In one embodiment, solder ball 110 is located on terminal 102. In another embodiment, conductive material 112 is printed on the terminal so it extends above surface 114 of the packaged semiconductor device 100.

[0049] The circuit geometry 109 re-routes the terminal 102, 104 relative to the terminals 122 on the IC device 118. The size and pitch of exposed terminals 102, 104 are printed to electrically couple the IC device 118 to another circuit member 116, such as a printed circuit board or a socket. The packaged semiconductor device 100 permits fine contact-to-contact spacing (pitch) on the order of less than 1.0 mm pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter.

[0050] The resilient material 106 increases the compliance of the terminals 102, 104 to permit electrical coupling by compression, without the need to solder the packaged semiconductor device 100. As illustrated in Figure 10, the packaged semiconductor device 100 permits IC device 118 to be tested prior to final packaging by pressing against pads 120 on a circuit member 116 and powered without the need for a socket, such as printed circuit board (PCB), or by insertion into a LGA or BGA socket. The present packaged semiconductor device 100 also permits the performance of the IC device 118 to be evaluated before being incorporated into a multi-chip module, permitting an individual die to be replaced if necessary. Alternatively, the packaged semiconductor device 100 can be soldered to a circuit member, such as a PCB, to provide a more reliable stress-decoupled solder joint. As used herein, the term "circuit members" refers to, for example, a packaged integrated circuit device, an unpackaged integrated circuit device, a printed circuit

board, a flexible circuit, a bare-die device, an organic or inorganic substrate, a rigid circuit, or any other device capable of carrying electrical current.

[0051] Figure 11 illustrates an alternate packaged semiconductor device 140 formed on wafer 142, with printed electrical devices 144 in accordance with an embodiment of the present disclosure. The electrical devices 144 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0052] Figure 12 illustrates the packaged semiconductor device 140 after the wafer 142 is singulated. The circuit geometry 148 includes external contact pads 152 that can electrically couple with contact pads 154 on circuit member 156.

[0053] The electrical devices 144 are preferably printed during construction of the dielectric layers 146 and the circuit geometry 148. The electrical devices 144 can be ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. For example, the electrical devices 144 can be formed using printing technology, adding intelligence to the packaged semiconductor device 140. Features that are typically located on the IC device 150 can be incorporated into the packaged semiconductor device 140 in accordance with an embodiment of the present disclosure.

[0054] The availability of printable silicon inks provides the ability to print electrical devices 144, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio

applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[0055] The electrical devices 202 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference.

[0056] Printing processes are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0057] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0058] In one embodiment, a plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[0059] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0060] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0061] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0062] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinylidenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicyclobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0063] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108

(December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[0064] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a substrate, or a combination thereof.

[0065] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakis(methyl)animine. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[0066] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0067] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0068] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0069] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll

coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[0070] Figure 13 illustrates a packaged semiconductor 170 with stacked IC devices 172, 174 in accordance with an embodiment of the present disclosure. Through silicon vias 176 permit contact pads 178 on IC device 172 to electrically couple with circuit geometry 180 and/or IC device 174. The circuit geometry 180 permits the IC devices 172, 174 to be routed discretely to circuit member 182, inter-die or die-to-die. The through silicon vias 176 eliminate edge wiring and permit a shorter vertical stack. The through silicon vias 176 can be formed using the printing processes discussed herein or other methods. In the illustrated embodiment, the packaged semiconductor 170 is located on base wafer 184.

[0071] Figure 14 illustrates an alternate packaged semiconductor 200 in accordance with an embodiment of the present disclosure. RF shielding 202 is optionally printed in recess 204 of substrate 206. In one embodiment, substrate 206 is optimized for thermal management. In another embodiment, IC device 208 is retained to substrate 206 by overmolding or encapsulation 210.

[0072] Dielectric layers 212 and circuit geometry 214 are preferably printed as discussed above. In the embodiment of Figure 14, the circuit geometry 214 is configured to add additional IC device 216 in a double sided configuration. Alternatively, the packaged semiconductor 200 can be mated with another circuit member 218 to create a complex system in package or multichip module.

[0073] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the disclosure. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the present disclosure.

[0074] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0075] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0076] Other embodiments of the disclosure are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the disclosure, but as merely providing illustrations of some of the presently preferred embodiments of this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the disclosure. Thus, it is intended that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[0077] Thus the scope of this disclosure should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present disclosure fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present disclosure is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred

embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present disclosure, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A wafer-level semiconductor package comprising:
a wafer including a plurality of semiconductor devices;
at least one dielectric layer selectively printed on at least a portion of the semiconductor devices creating first recesses aligned with a plurality of electrical terminals on the semiconductor devices;
a conductive material printed in the first recesses forming contact members on the semiconductor devices;
at least one dielectric layer selectively printed to create a plurality of second recesses corresponding to a target circuit geometry; and
a conductive material printed in at least a portion of the second recesses comprising circuit geometry, the circuit geometry comprising a plurality of exposed terminals adapted to electrically couple to another circuit member; and
a plurality of discrete packaged semiconductor devices cut from the wafer.
2. The package of claim 1 comprising a conductive plating layer on one or more of the contact members or the circuit geometry.
3. The package of claim 1 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.
4. The package of claim 1 comprising a compliant material located between the exposed terminals and the semiconductor device.
5. The package of claim 1 comprising at least one printed electrical device on a dielectric layer and electrically coupled to at least a portion of the circuit geometry.
6. The package of claim 1 wherein the exposed terminals extend above the package.
7. The package of claim 1 comprising a plurality of vias electrically coupling adjacent layers of the circuit geometry.

8. The package of claim 1 comprising:
at least one external dielectric layer extending beyond the package; and
external routing on the external dielectric layer electrically coupled to a portion of the circuit geometry.

9. The package of claim 1 wherein a discrete packaged semiconductor devices comprises a plurality of semiconductor devices and the circuit geometry comprises at least one of an inter-die circuit path or an intra-die circuit paths.

10. The package of claim 1 wherein a discrete packaged semiconductor devices comprises:
at least two vertically stacked semiconductor devices; and
a plurality of through silicon vias electrically coupling at least two of the stacked semiconductor devices.

11. The package of claim 1 wherein a discrete packaged semiconductor devices comprises a plurality of semiconductor devices electrically coupled by the circuit geometry.

12. The package of claim 1 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

13. The package of claim 1 wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer.

14. An electrical assembly comprising:
a discrete packaged semiconductor devices of claim 1; and
a circuit member with a plurality of contact pads electrically coupled to the exposed terminals.

15. The electrical interconnect assembly of claim 14 wherein the circuit member is selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

16. A method of making a wafer-level semiconductor package, the method comprising the step of:

printing at least one dielectric layer selectively on at least a portion of a wafer containing a plurality of the semiconductor devices to create first recesses aligned with electrical terminals on the semiconductor devices;

printing a conductive material in a plurality of the first recesses to form contact members on the semiconductor devices;

printing at least one dielectric layer selectively on at least a portion of the wafer to create a plurality of second recesses corresponding to a target circuit geometry;

printing a conductive material in at least a portion of the second recesses to form a circuit geometry, the circuit geometry comprising a plurality of exposed terminals electrically coupled to the semiconductor devices; and

dicing the wafer into a plurality of discrete packaged semiconductor devices.

17. The method of claim 16 comprising plating with a conductive material one or more of the contact members and the circuit geometry.

18. The method of claim 16 wherein printing the conductive material comprises one or more of printing a conductive material in the recesses and sintering the conductive material or printing a conductive ink in the recesses.

19. The method of claim 16 comprising printing a compliant material in a location between the semiconductor devices and at least one of the exposed terminals.

20. The method of claim 16 comprising:
printing at least one electrical device on a dielectric layer; and
electrically coupling the electrical device to at least a portion of the circuit geometry.

21. The method of claim 16 comprising printing at least one via in a dielectric layer to electrically couple adjacent layers of the circuit geometry.

22. The method of claim 16 comprising printing one or more contact members on the exposed terminals that extend above the dielectric layer.

23. The method of claim 16 comprising the steps of:
locating a plurality of semiconductor devices on the discrete packaged semiconductor device; and
printing the circuit geometry to include at least one of an inter-die circuit path or an intra-die circuit paths.

24. The method of claim 16 comprising the steps of:
vertically stacking at least two semiconductor devices in the discrete packaged semiconductor devices; and
electrically coupling at least two of the stacked semiconductor devices with through silicon vias.

25. The method of claim 16 comprising electrically coupling a second semiconductor device to the exposed terminals on the discrete packaged semiconductor devices.

26. The method of claim 16 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

27. The method of claim 16 comprising printing a conductive material, a non-conductive material, and a semi-conductive material is printed on a single layer.

28. The method of claim 16 comprising the steps of:
locating pre-formed conductive trace materials in the second recesses; and
plating the second recesses to form conductive traces with substantially rectangular cross-sectional shapes.

29. The method of claim 16 comprising the steps of:
pressing a conductive foil into at least a portion of the second recesses;
shearing the conductive foil along edges of the second recesses;
removing excess conductive foil not located in the second recesses; and

plating the second recesses to form conductive traces with substantially rectangular cross-sectional shapes.

30. A method of making an electrical assembly comprising the steps of:
making the discrete packaged semiconductor device according to the method of claim 16; and
electrically coupling a circuit member with a plurality of the exposed terminals on the discrete packaged semiconductor devices.

31. The method of claim 30 wherein the circuit member is selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

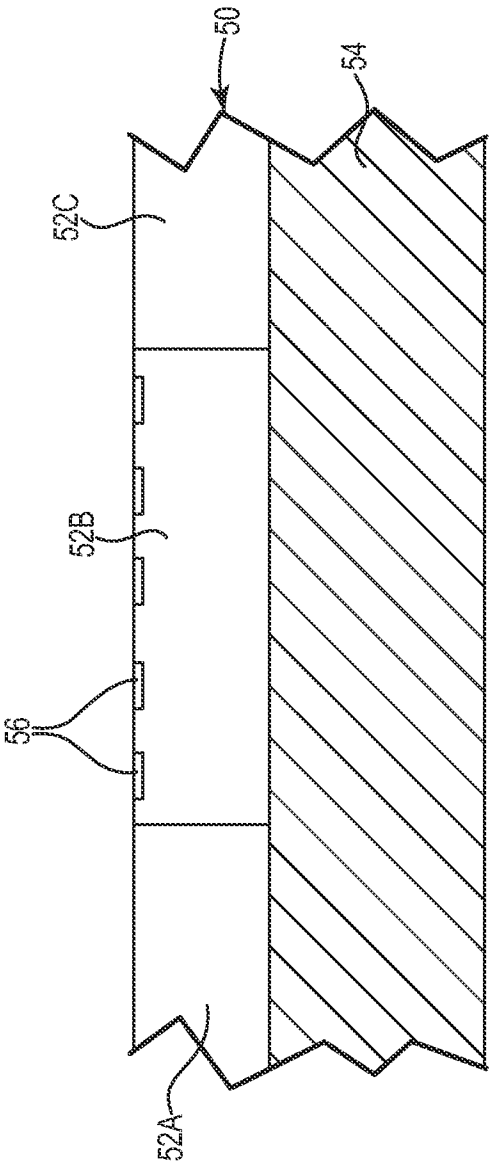


Fig. 1

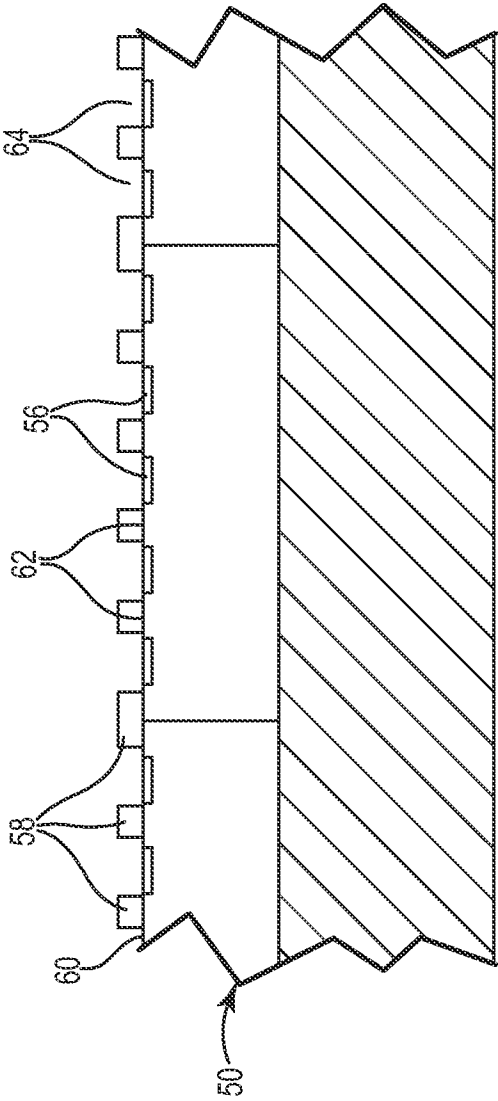


Fig. 2

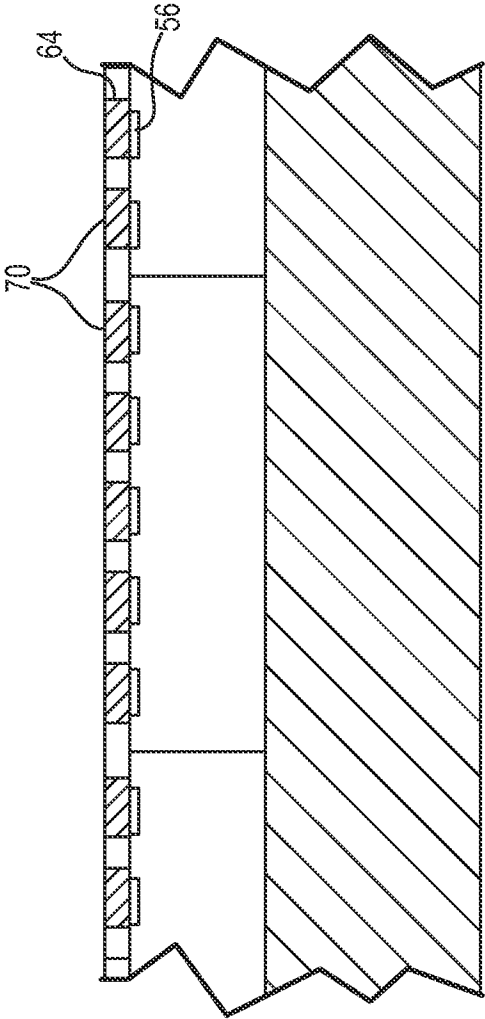


Fig. 3

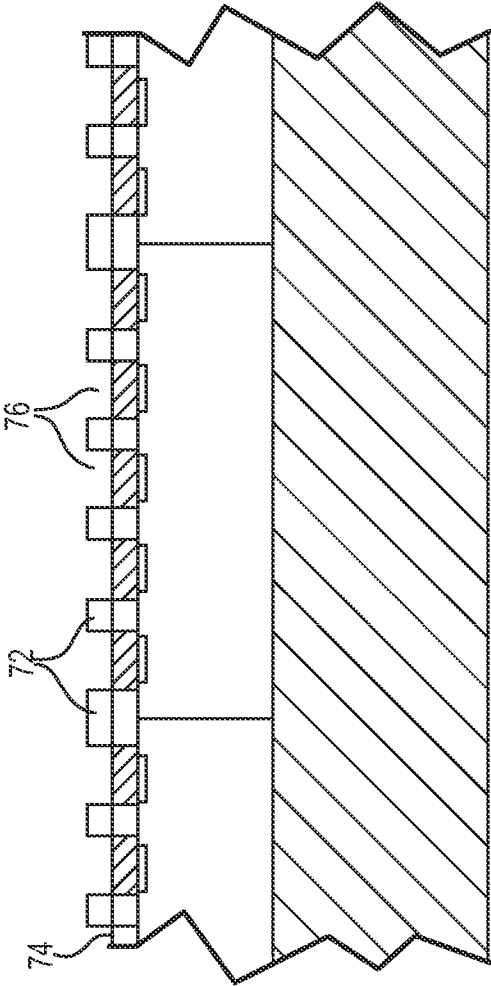


Fig. 4

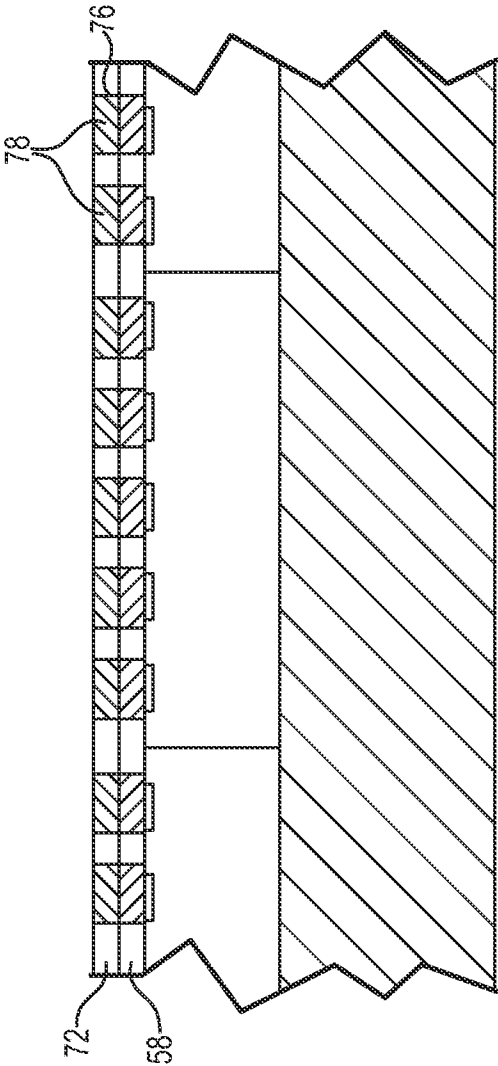


Fig. 5

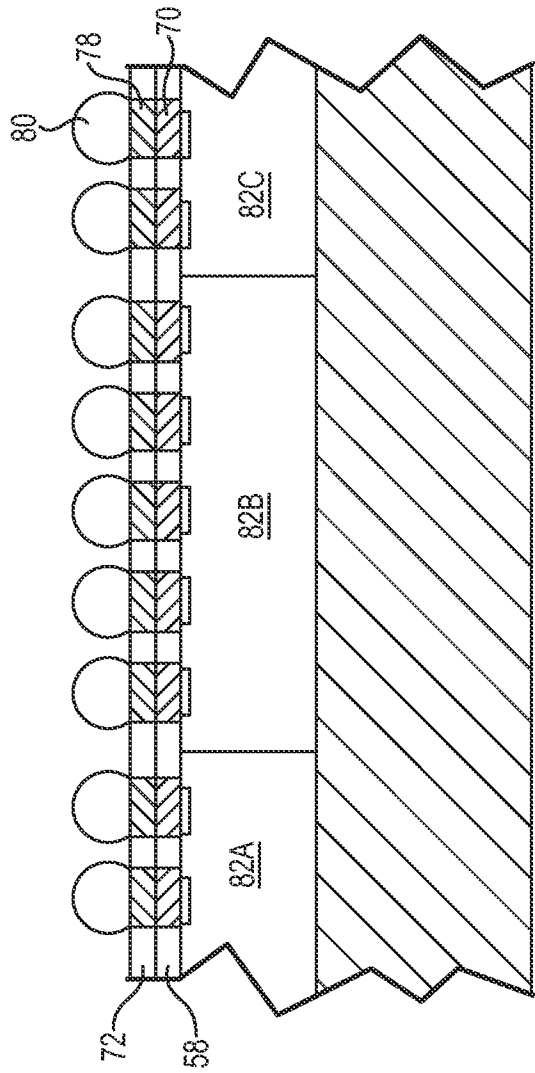


Fig. 6

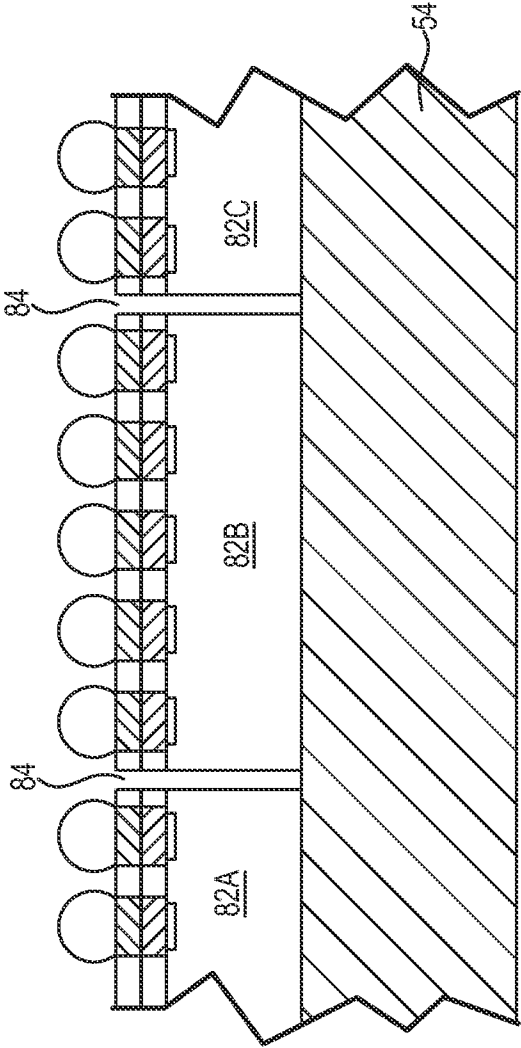


Fig. 7

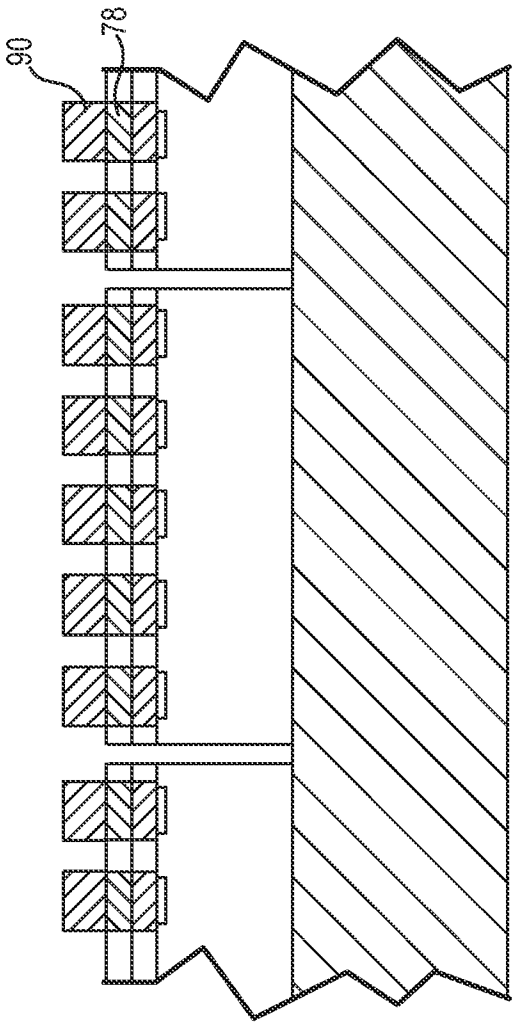


Fig. 8

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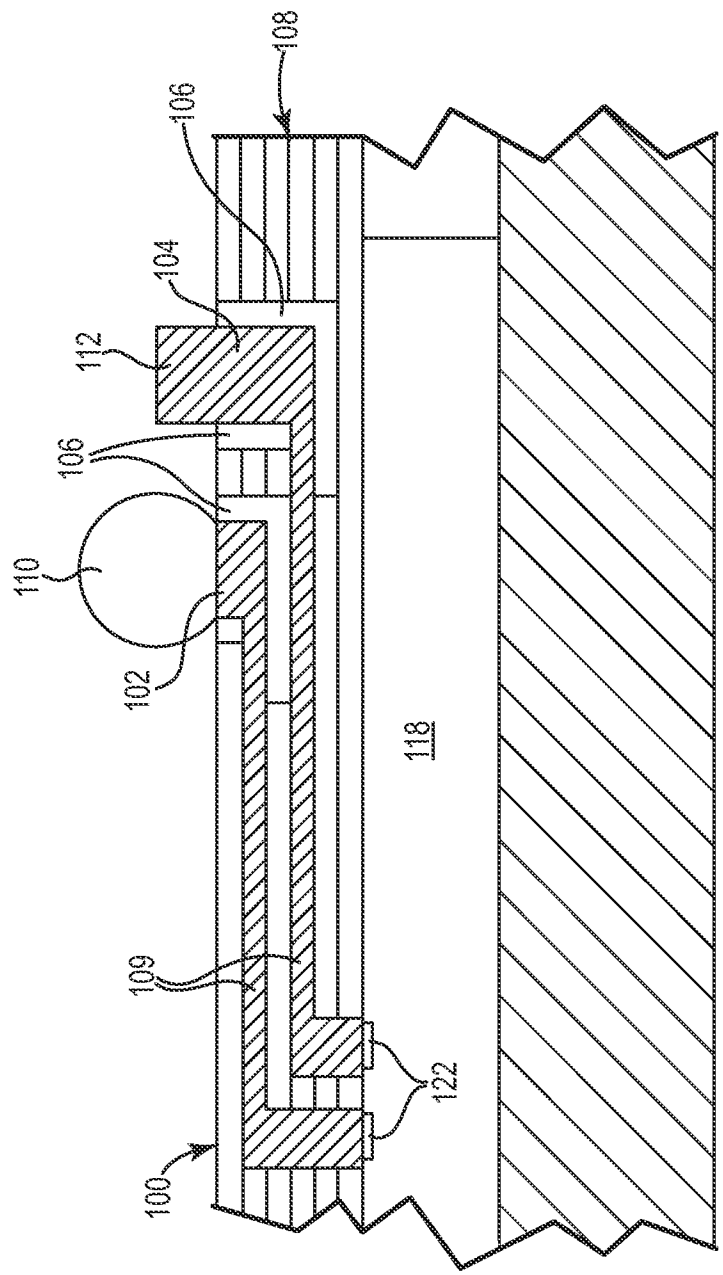


Fig. 9

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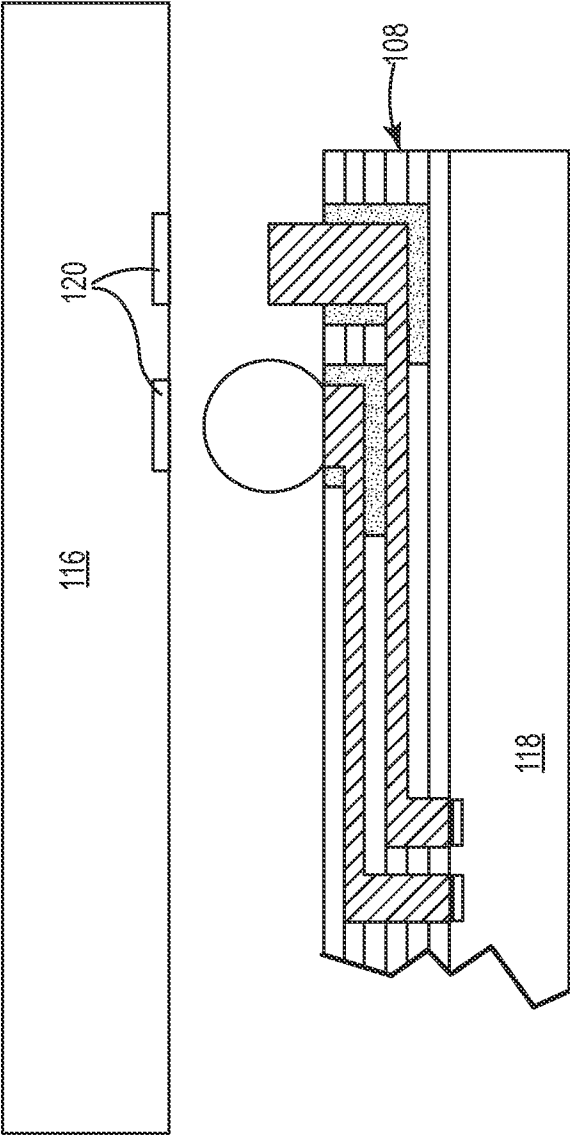


Fig. 10

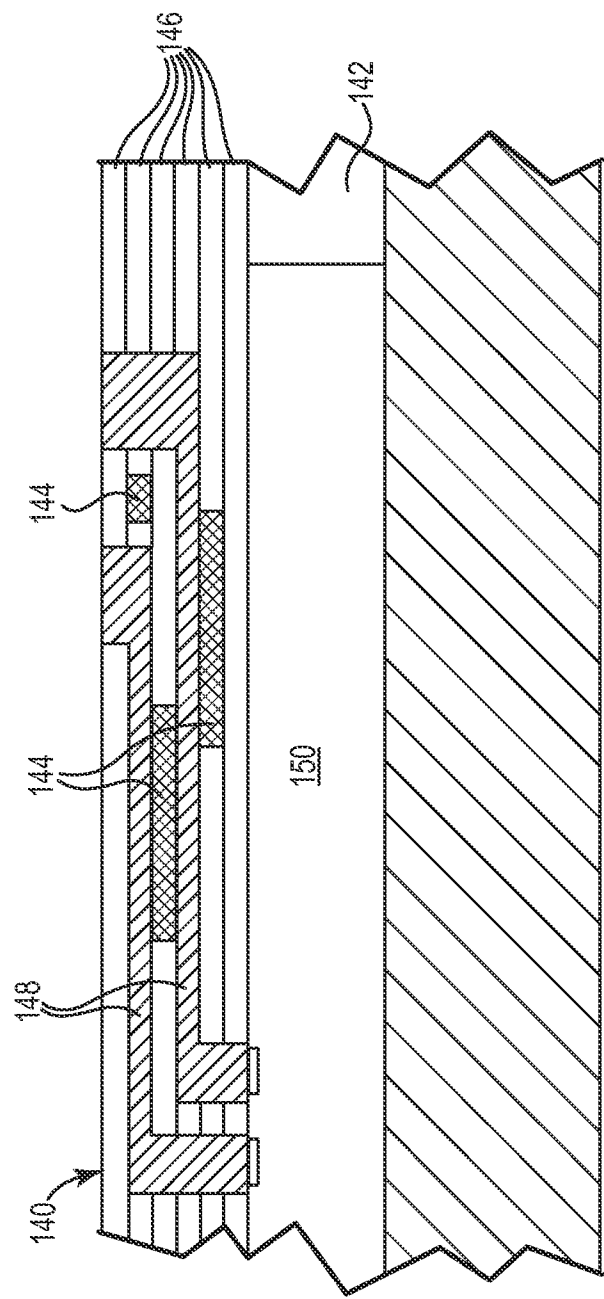


Fig. 11

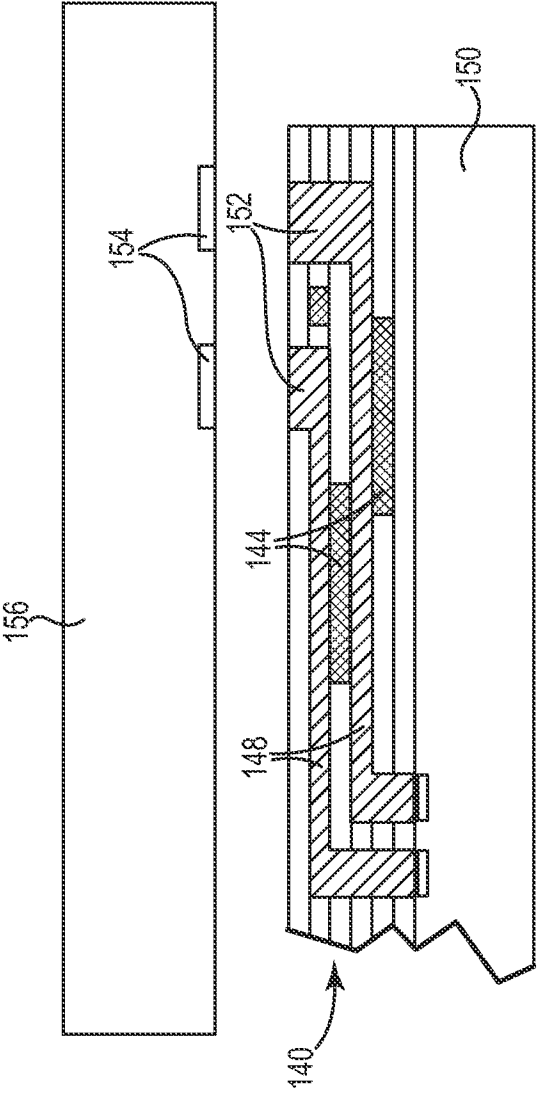


Fig. 12

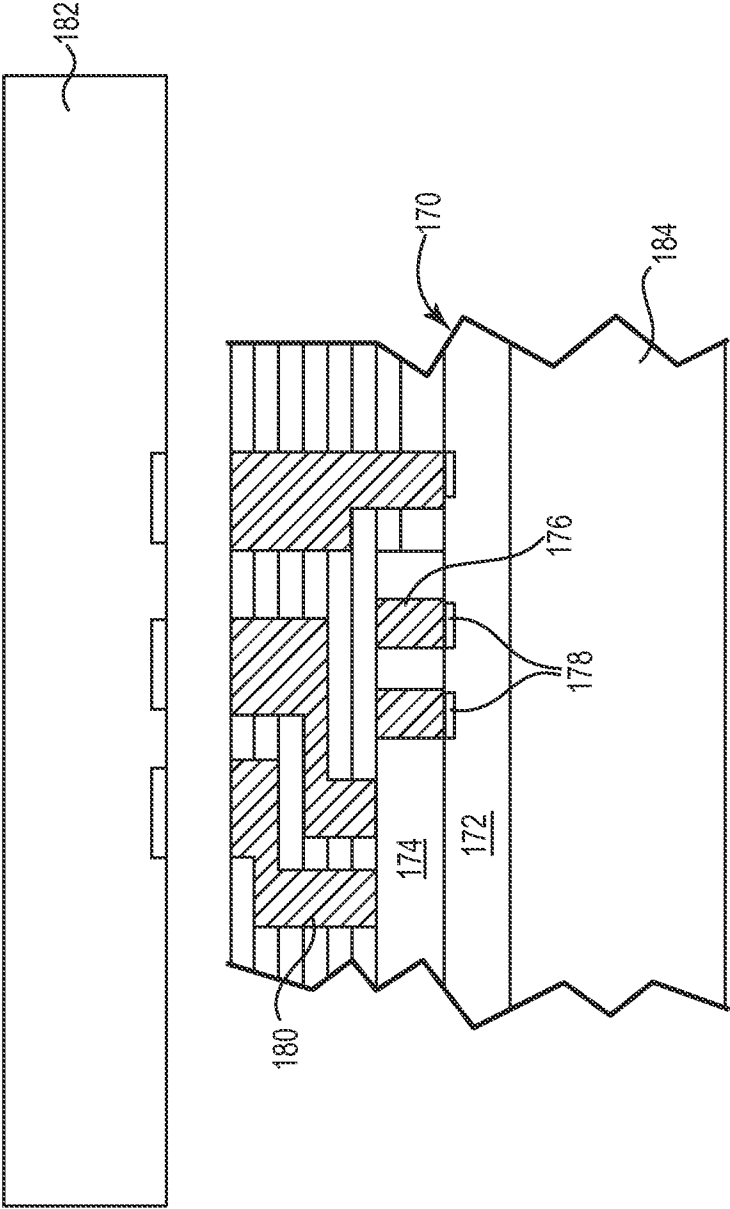


Fig. 13

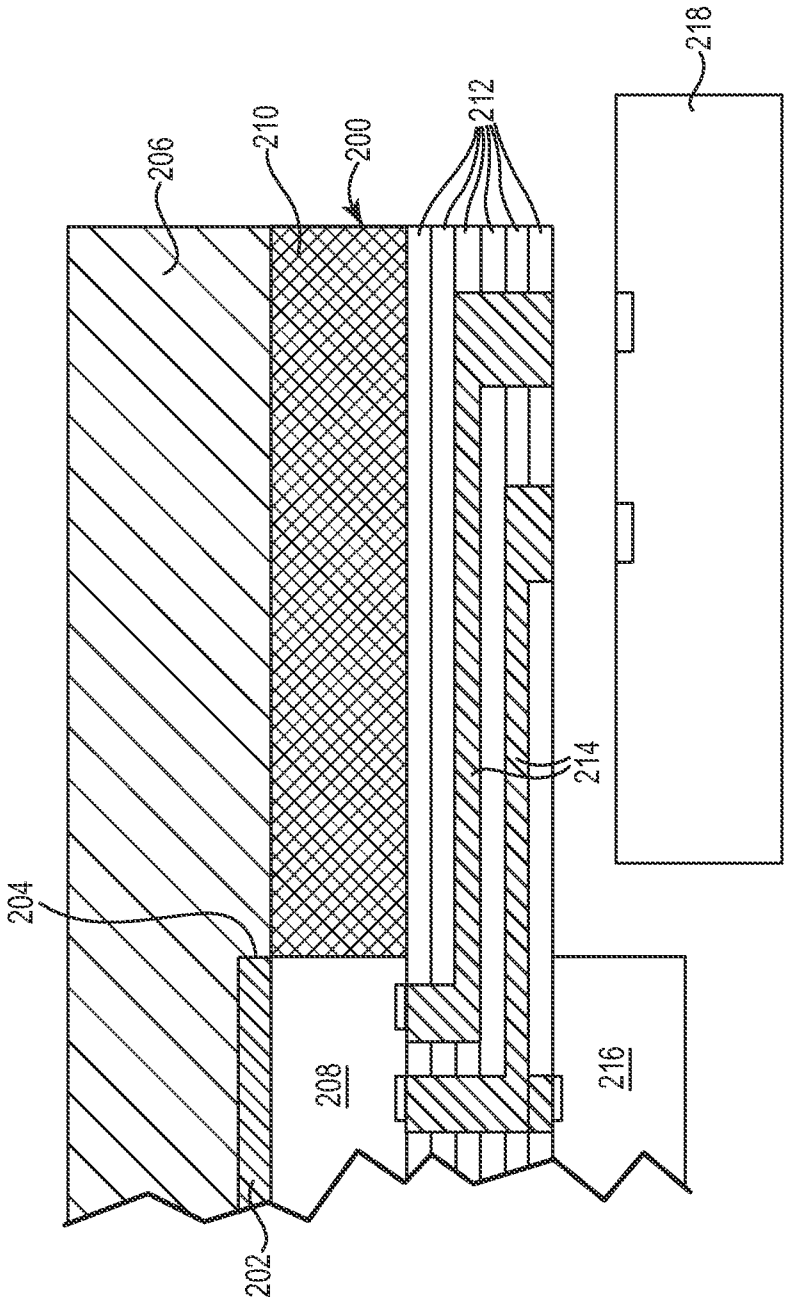


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2010/036288

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 23/04 (2010.01)

USPC - 257/698

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 23/04, 23/12 (2010.01)

USPC - 257/698, 730, E23.023, E23.151

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 91/14015 A1 (WILBOURN et al) 19 September 1991 (19.09.1991) entire document	1-3, 5-8, 11-18, 20-22, 25-27, and 30-31
Y		4, 9-10, 19, 23-24 and 28-29
Y	US 7,321,168 B2 (SU TAO) 22 January 2008 (22.01.2008) entire document	4 and 19
Y	WO 2006/124597 A2 (FOSTER et al) 23 November 2006 (23.11.2006) entire document	9, 10, 23, 24, and 28-29
A	US 2008/0220584 A1 (KIM et al) 11 September 2008 (11.09.2008) entire document	1-31
A	US 2004/0217473 A1 (YU-NUNG SHEN) 04 November 2004 (04.11.2004) entire document	1-31
A	US 2009/0127698 A1 (RATHBURN) 21 May 2009 (21.05.2009) entire document	1-31
A	US 2008/0143358 A1 (BREINLINGER) 19 June 2008 (19.06.2008) entire document	1-31
A	US 5,913,109 A (DISTEFANO et al) 15 June 1999 (15.06.1999) entire document	1-31

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 July 2010

Date of mailing of the international search report

04 AUG 2010

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