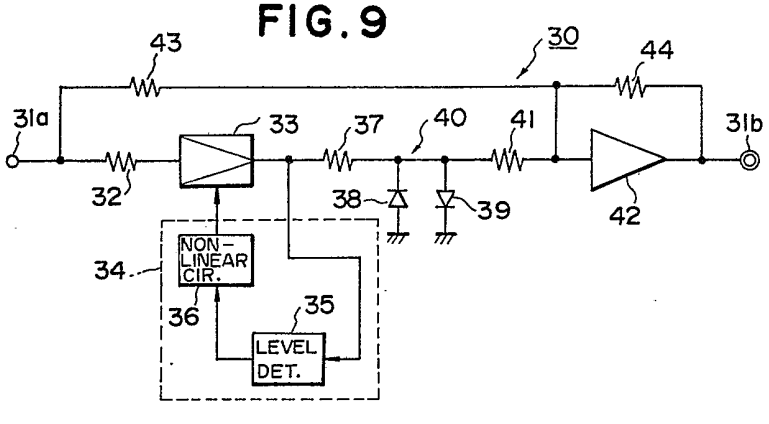
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H04B 1/64
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GB 1432763
GB 1404332
GB 1404331
GB 1257287
GB 1120541
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H3G
H4R
(71) Applicant
Sony Corporation, 7-35 Kitashinagawa-6, Shinagawa-ku, Tokyo, Japan
(72) Inventor
Kenzo Akagir
(74) Agent
D. Young & Co.

(54) **Information Signal Processing; Companding**

(57) A compression circuit for an audio signal includes a first transmission path 40 for compressing an audio signal supplied thereto and having a variable gain amplifier 33 and a control circuit 34 which supplies a control signal to the variable gain amplifier 33 for varying the gain thereof, a second transmission path 30 for transmitting the audio signal with substantially unity gain through a resistor 43 thereof, and an adder amplifier 42 for adding the audio signal from the first transmission path and the audio signal from the second transmission path whereby the compressed audio signal is effectively transmitted when the level of the audio signal is below a predetermined value and the audio signal with substantially unity gain is transmitted when the level of the audio signal is above the predetermined value. A complementary output gain control circuit substantially recreates the original audio signal when the above signal is reproduced.

FIG. 9



GB 2 052 220 A

FIG.1

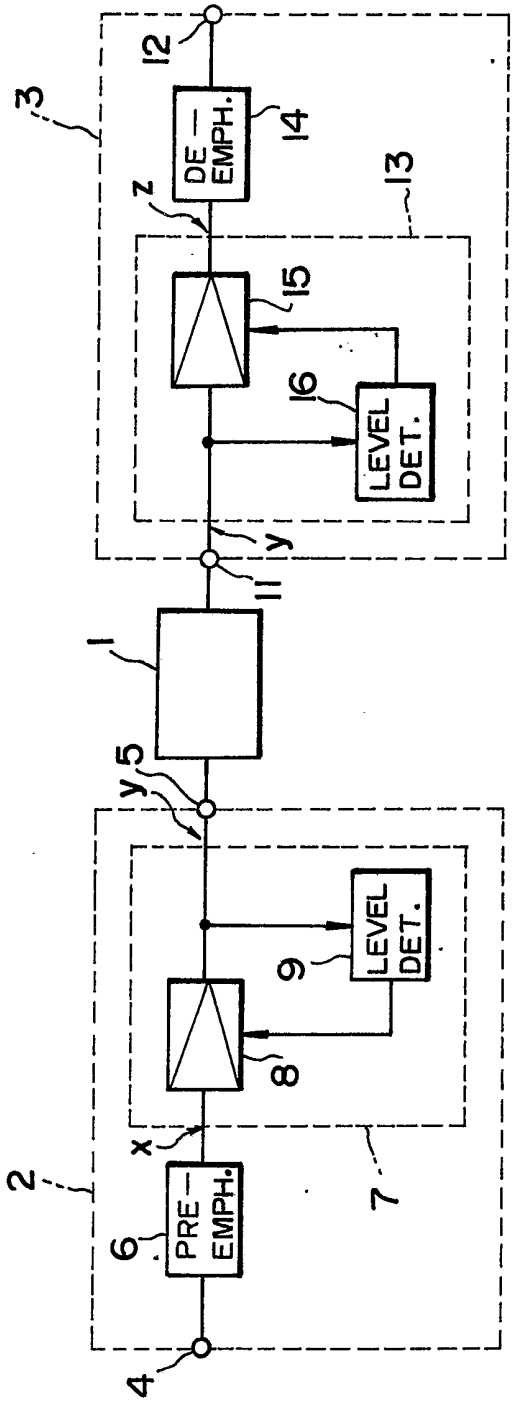

12
3
DE-EMPH.
14
13
z
15
16
LEVEL DET.
y
11
1
5
y
LEVEL DET.
9
8
x
2
7
PRE-EMPH.
6
4

FIG.2

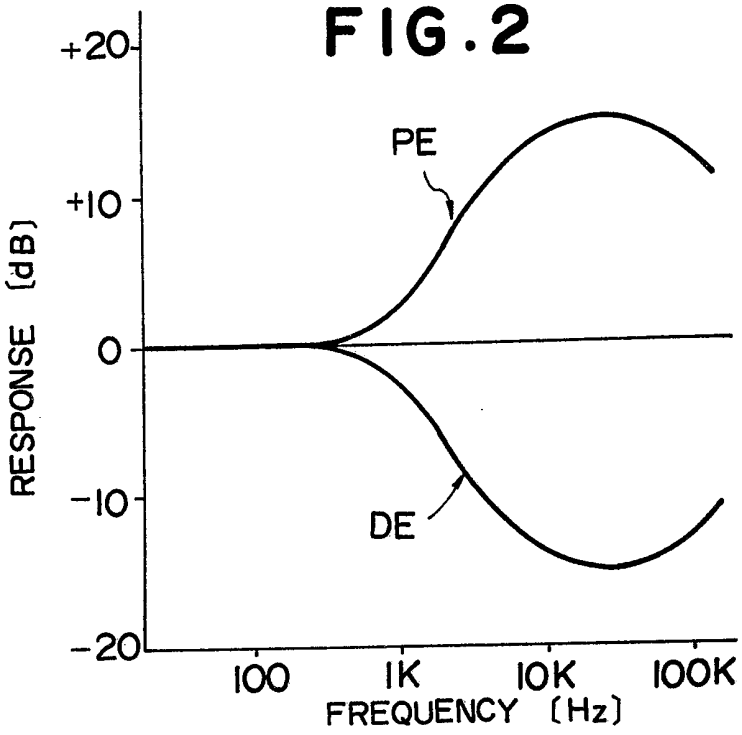

+20
+10
0
-10
-20
RESPONSE (dB)
PE
DE
100
1K
10K
100K
FREQUENCY (Hz)

FIG.3

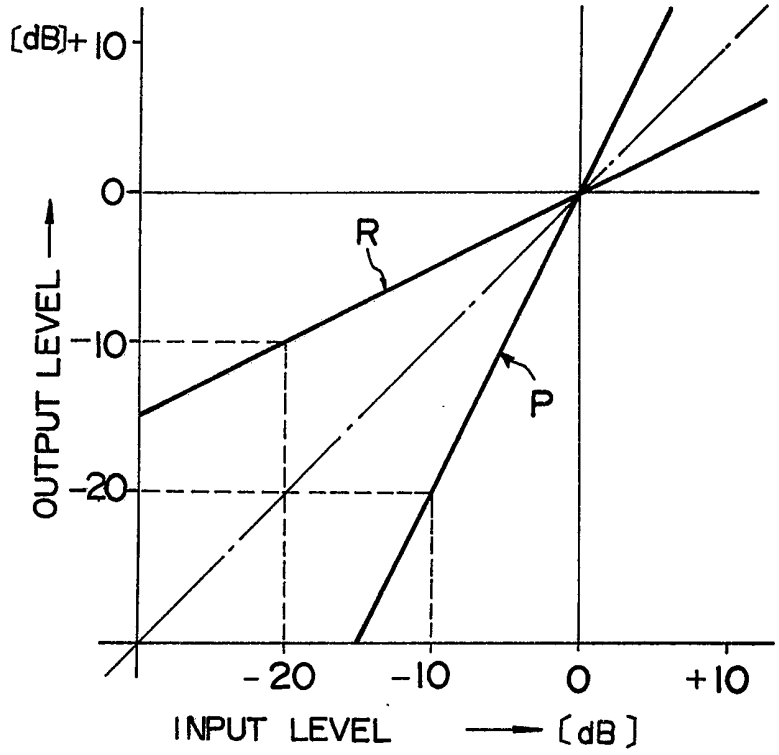

(dB)+10
0
-10
-20
OUTPUT LEVEL
R
P
-20
-10
0
+10
INPUT LEVEL (dB)

FIG.4

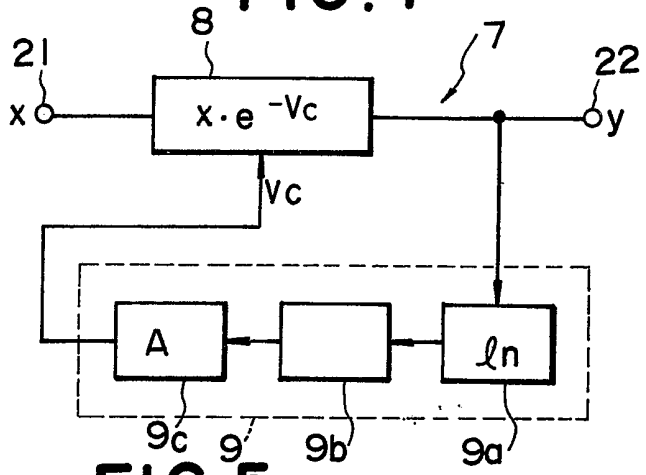


FIG.5

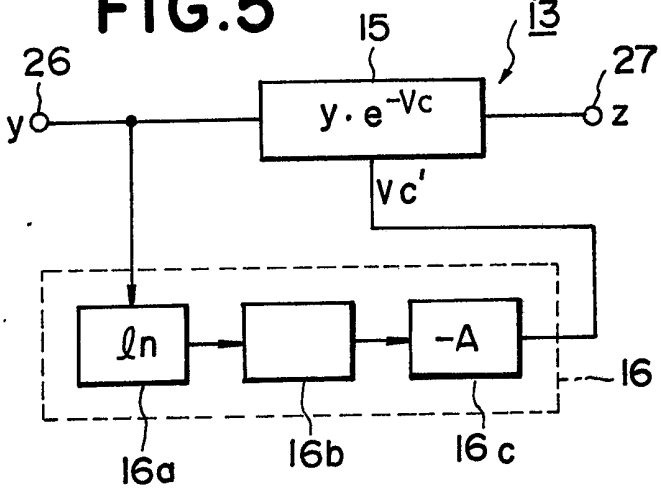


FIG.6

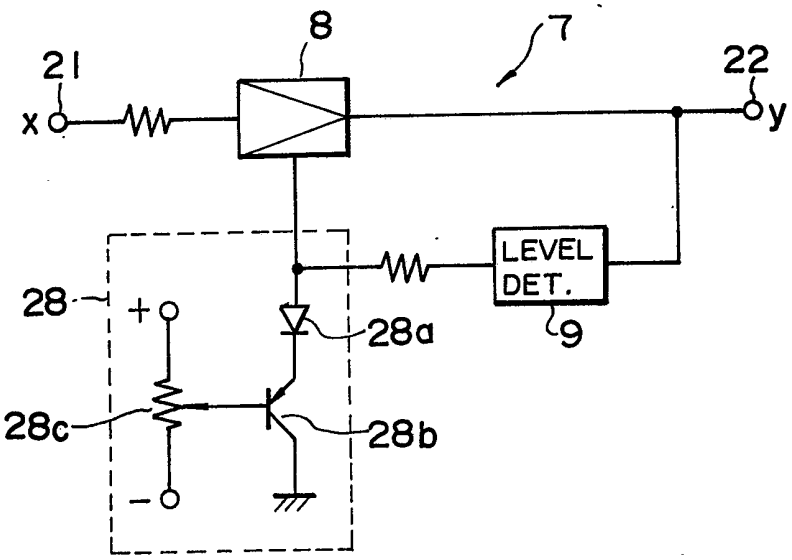


FIG.7

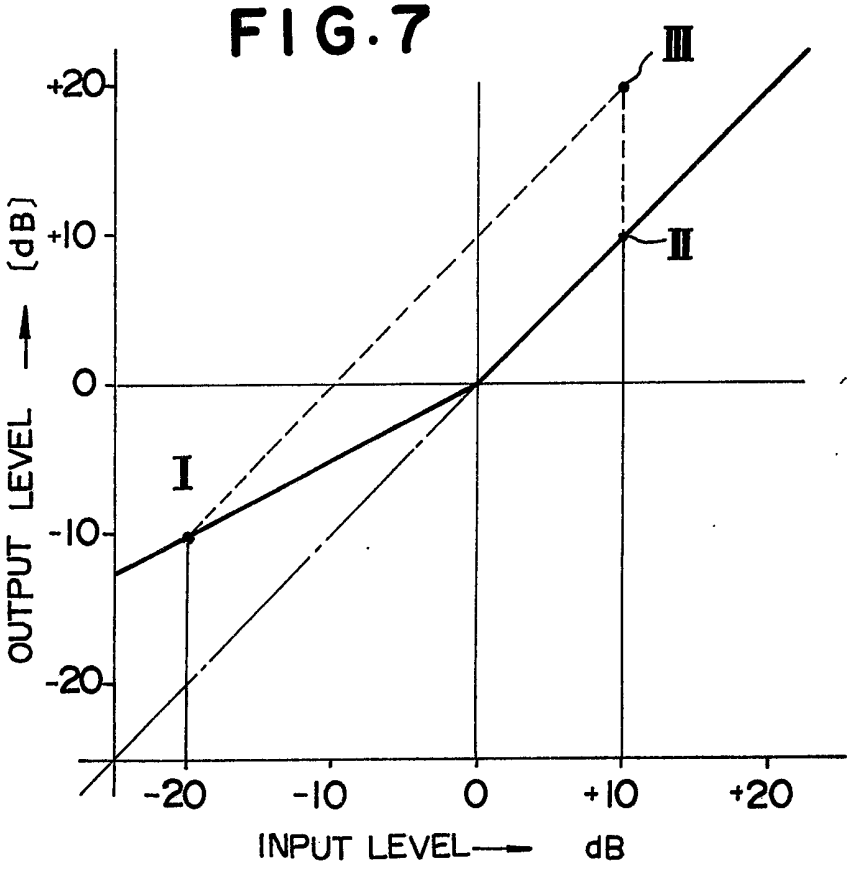

+20
+10
0
-10
-20
OUTPUT LEVEL ⟶ (dB)
I
II
III
-20
-10
0
+10
+20
INPUT LEVEL⟶ dB

FIG.8

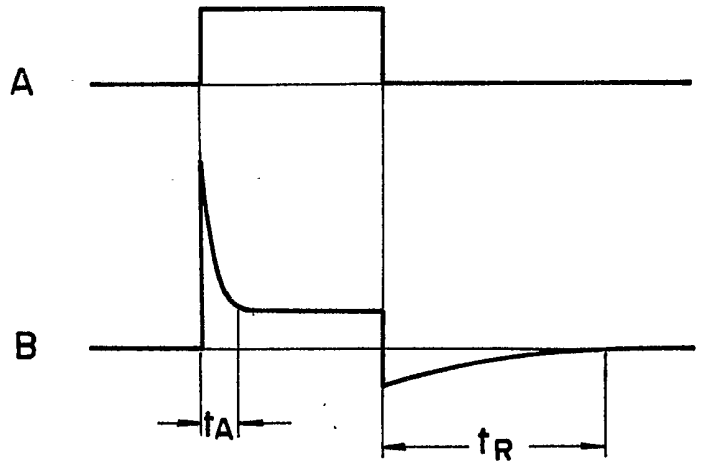

A
B
t_A
t_R

FIG. 9

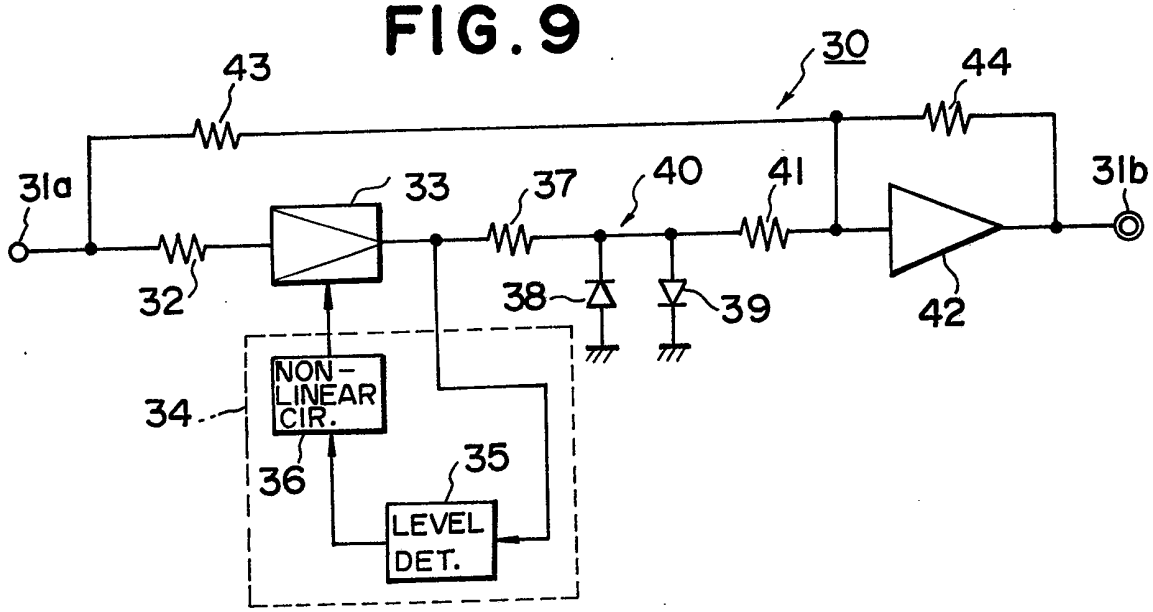


FIG. 10

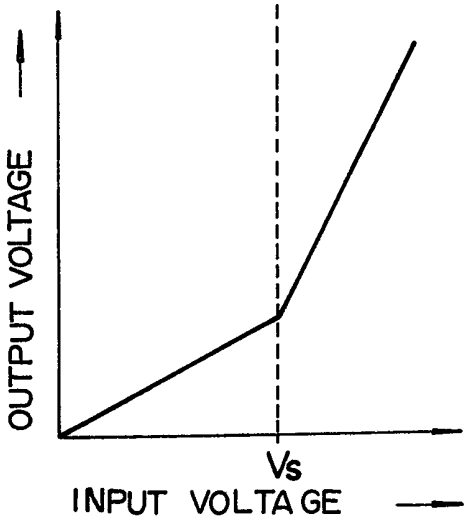


FIG. 11

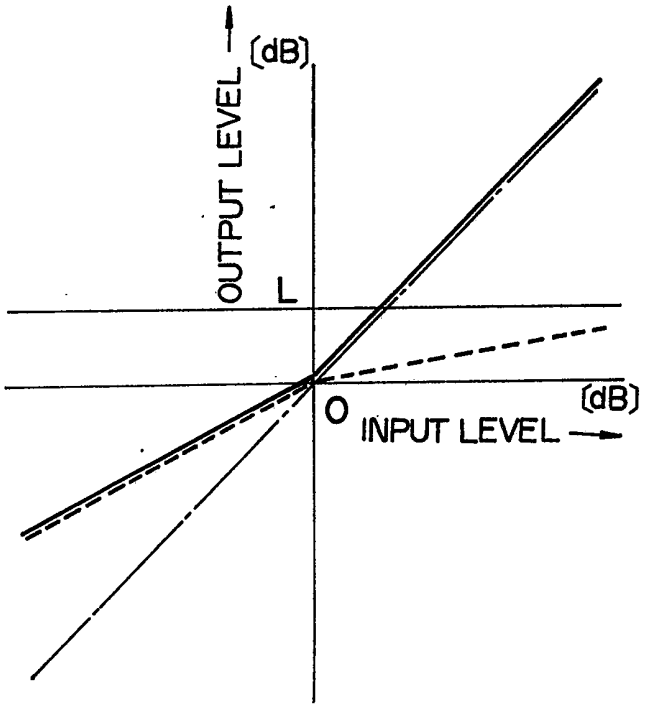


FIG. 12

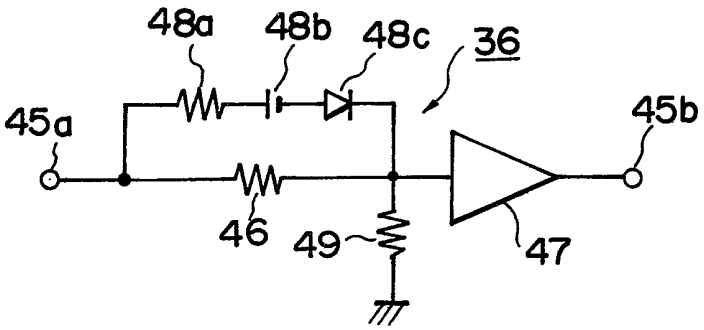


FIG. 13

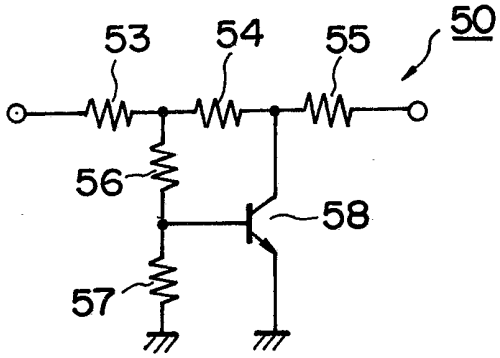


FIG. 14

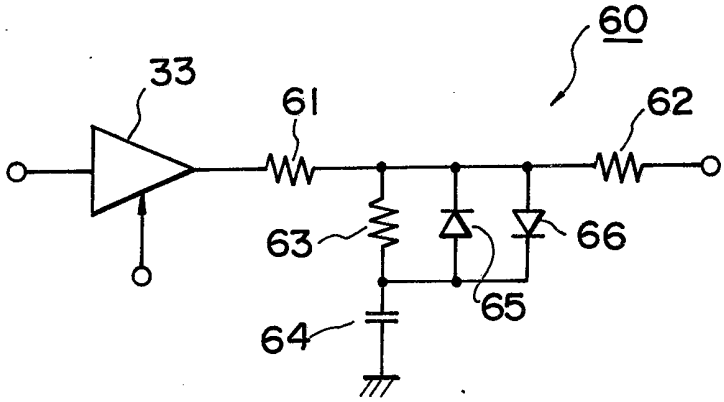


FIG.15

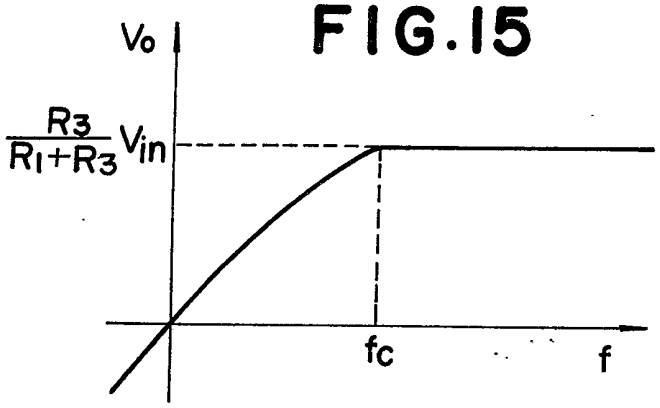


FIG.16

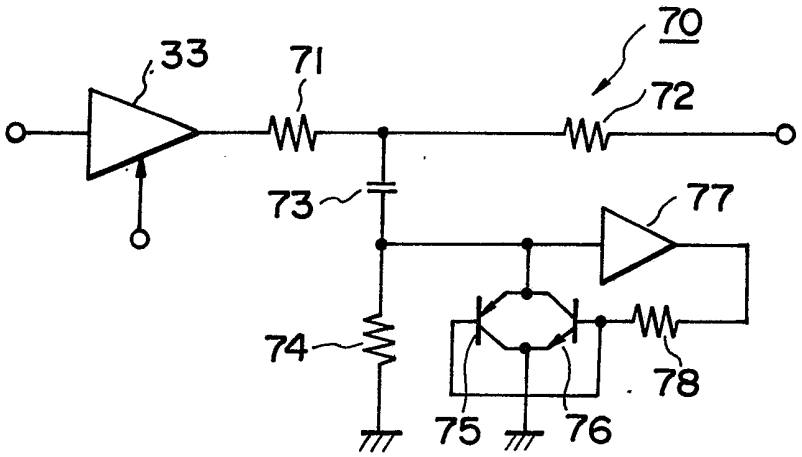


FIG.17

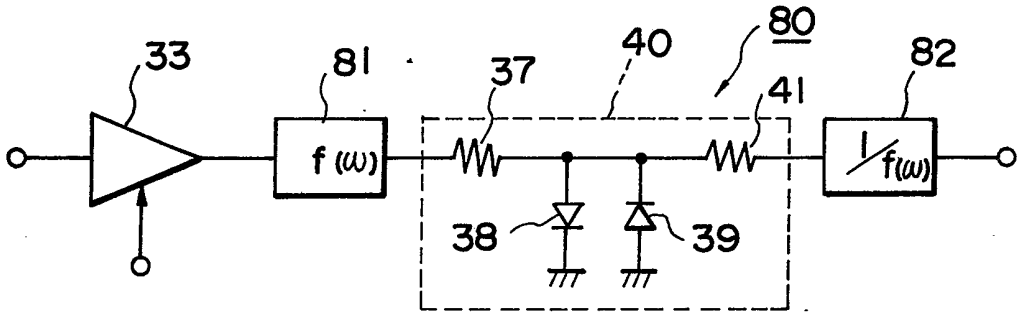


FIG.18

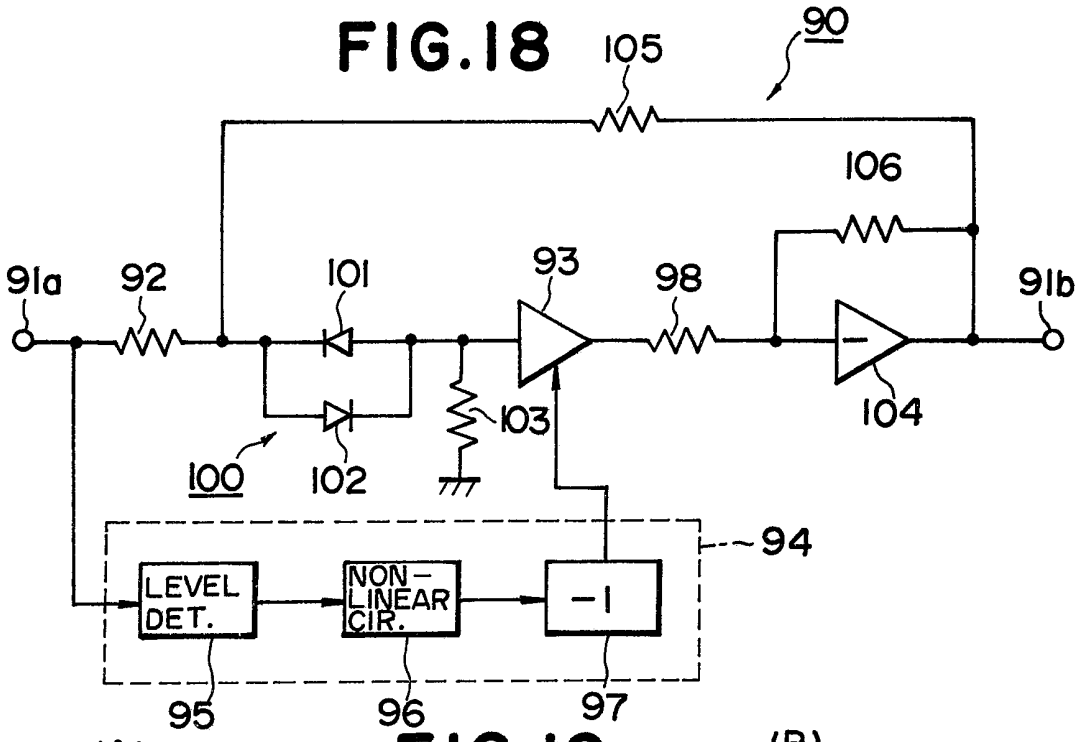


FIG.19

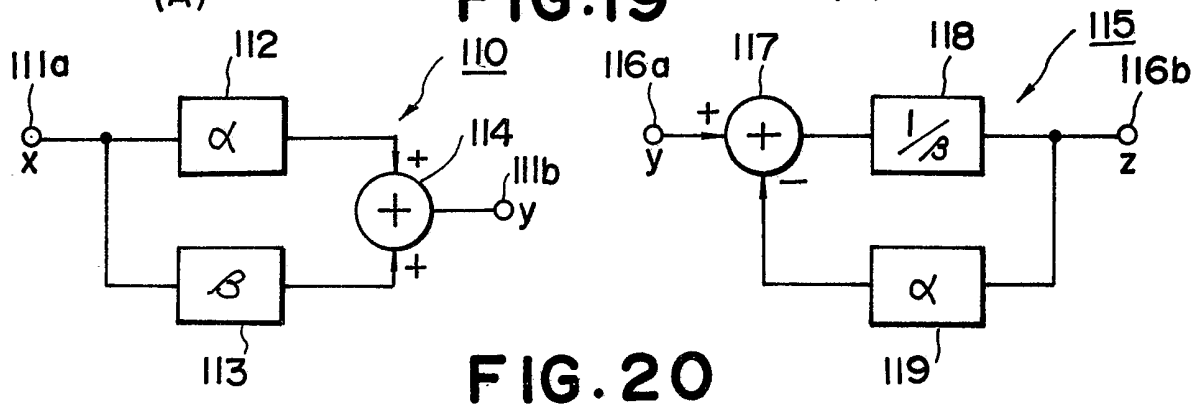
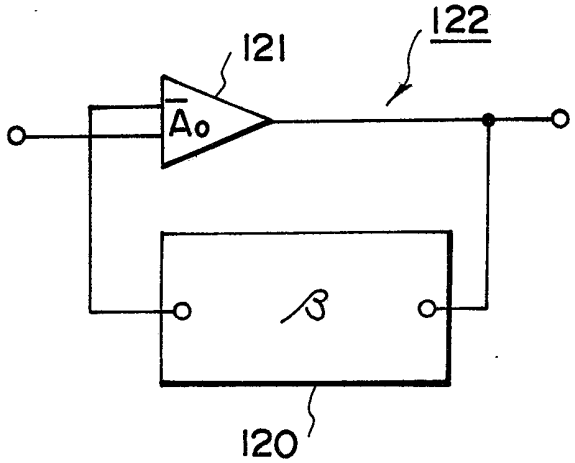


FIG.20



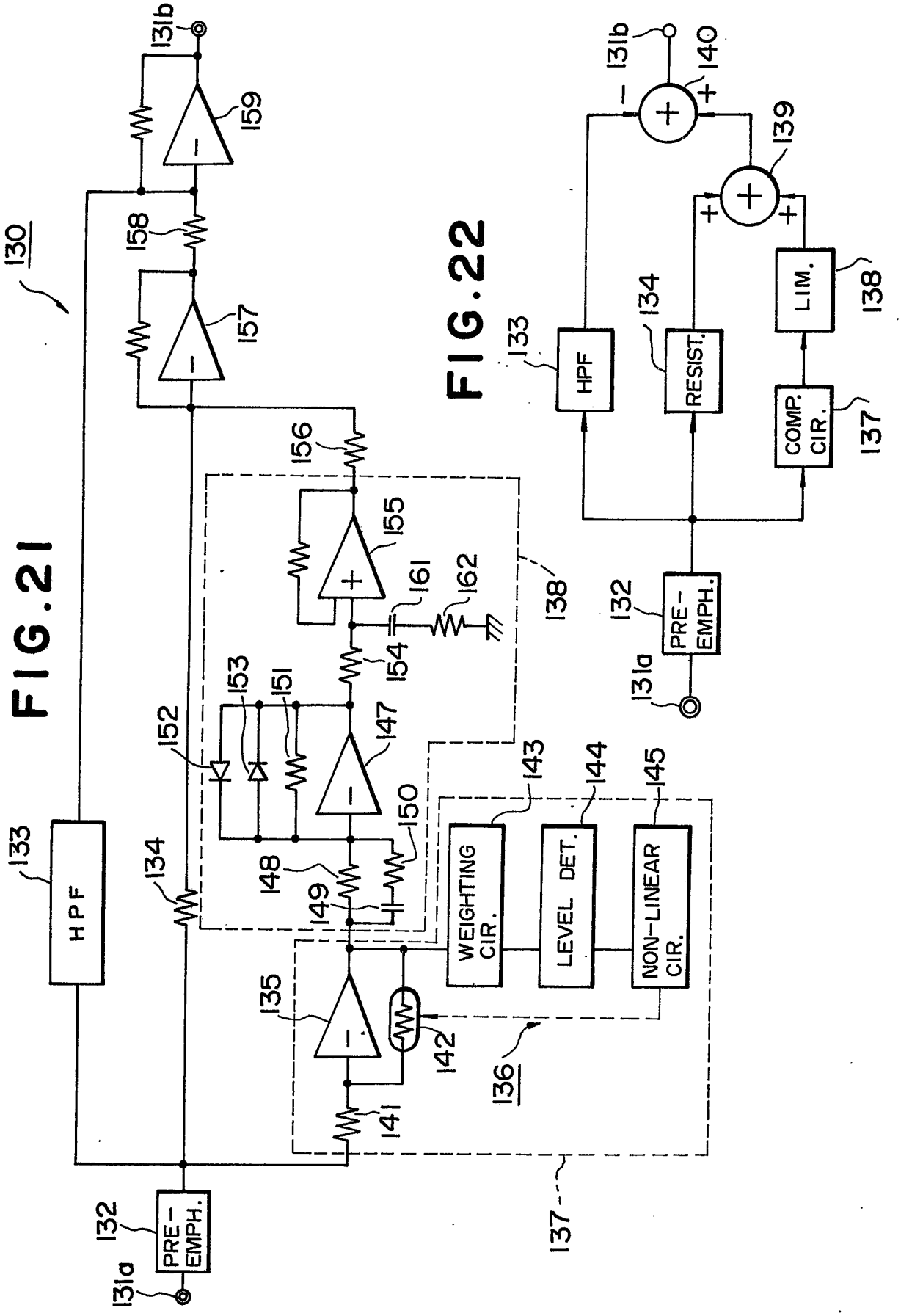

130
131b
159
158
157
156
155
161
162
154
153
151
152
147
150
148
149
134
133
HPF
135
142
141
136
137
143
144
145
WEIGHTING CIR.
LEVEL DET.
NON-LINEAR CIR.
138
132
PRE-EMPH.
131a

FIG. 21

131b
140
139
133
HPF
134
RESIST.
LIM.
138
COMP. CIR.
137
132
PRE-EMPH.
131a

FIG. 22

FIG. 23

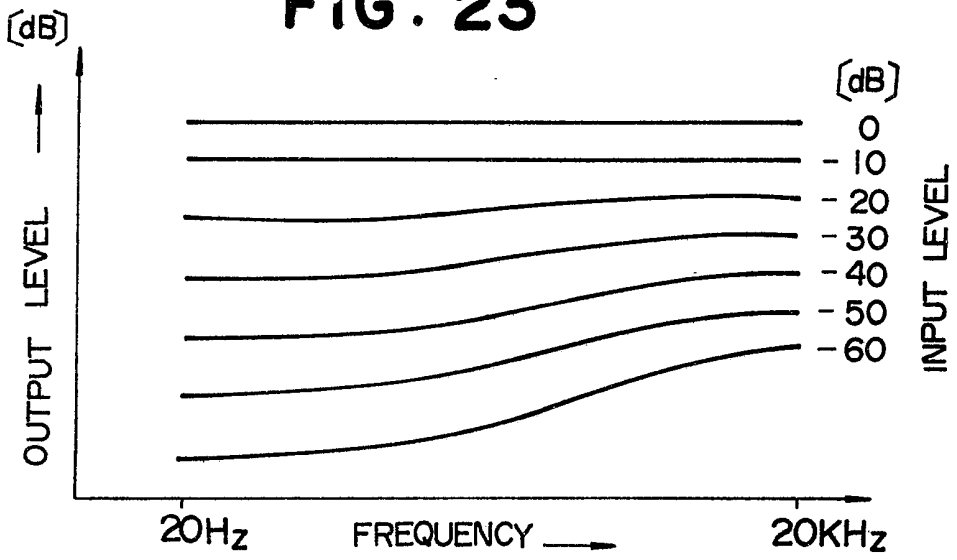

(dB)
OUTPUT LEVEL
(dB)
0
-10
-20
-30
-40
-50
-60
INPUT LEVEL
20Hz
FREQUENCY
20KHz

FIG. 24

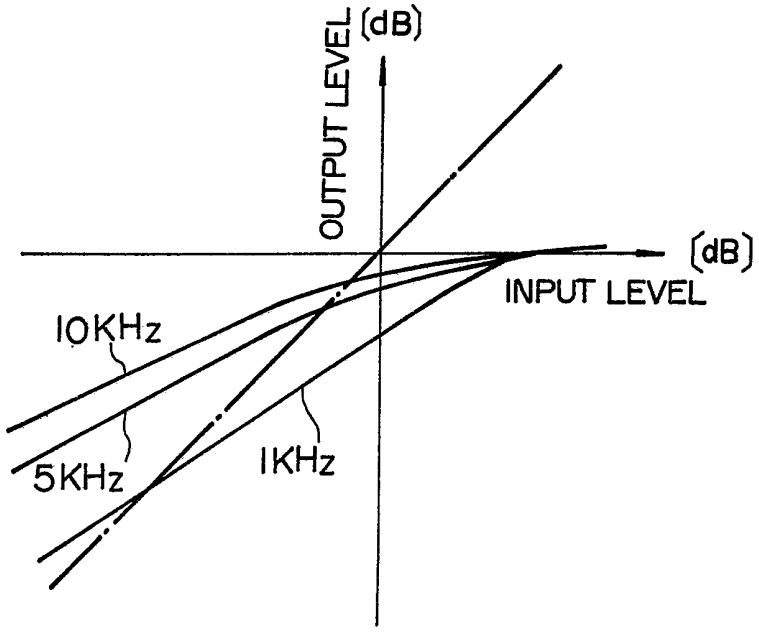

OUTPUT LEVEL
(dB)
(dB)
INPUT LEVEL
10KHz
5KHz
1KHz

FIG.25

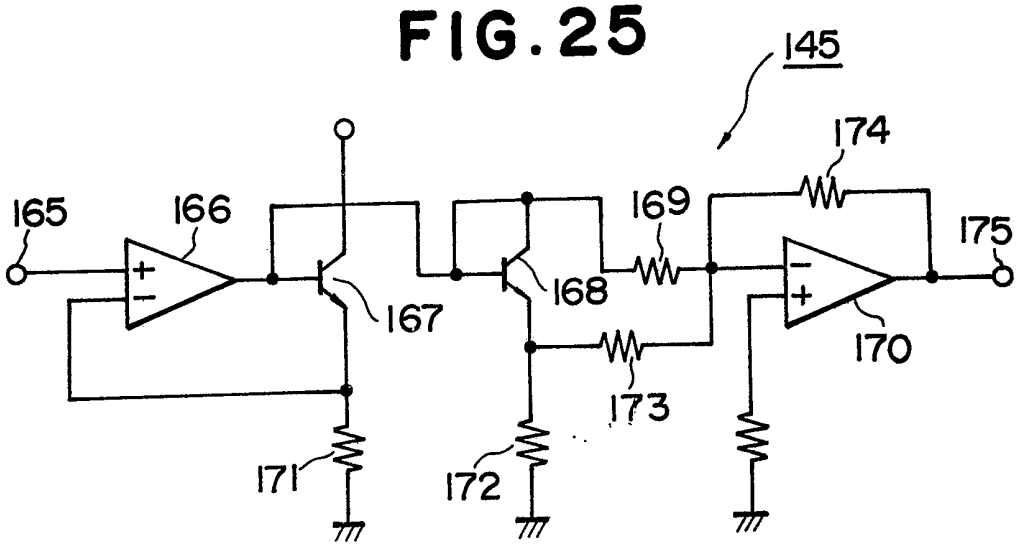


FIG.26

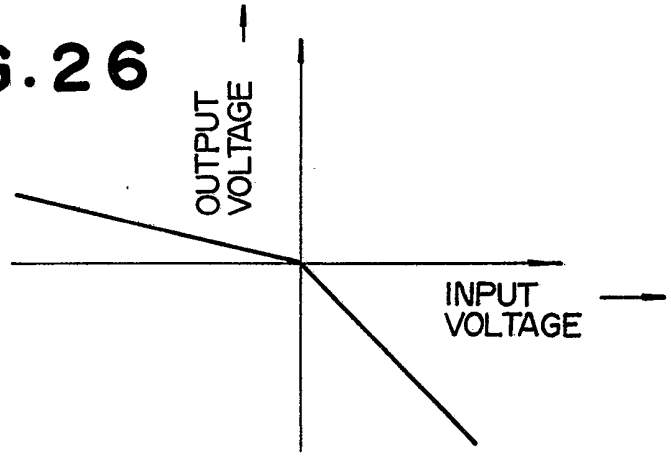
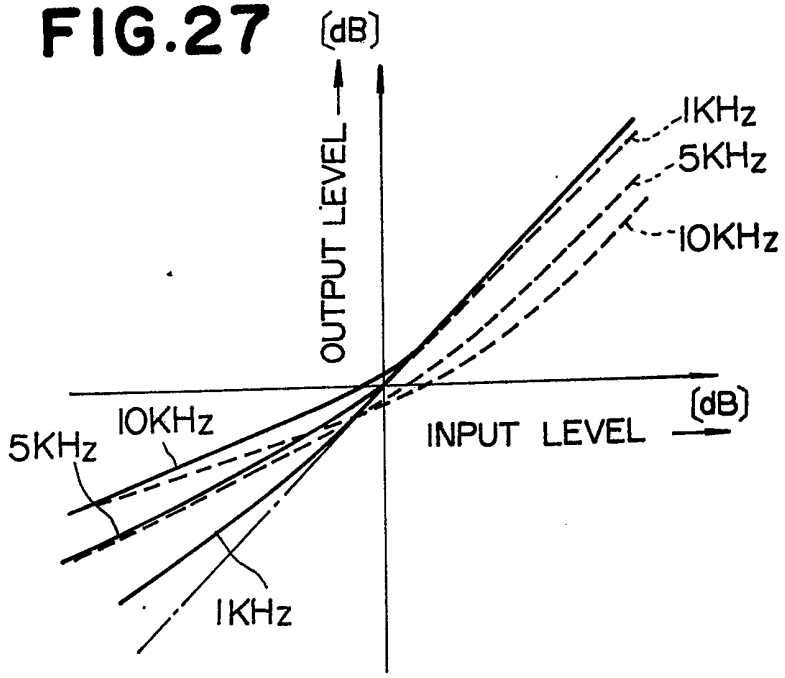


FIG.27



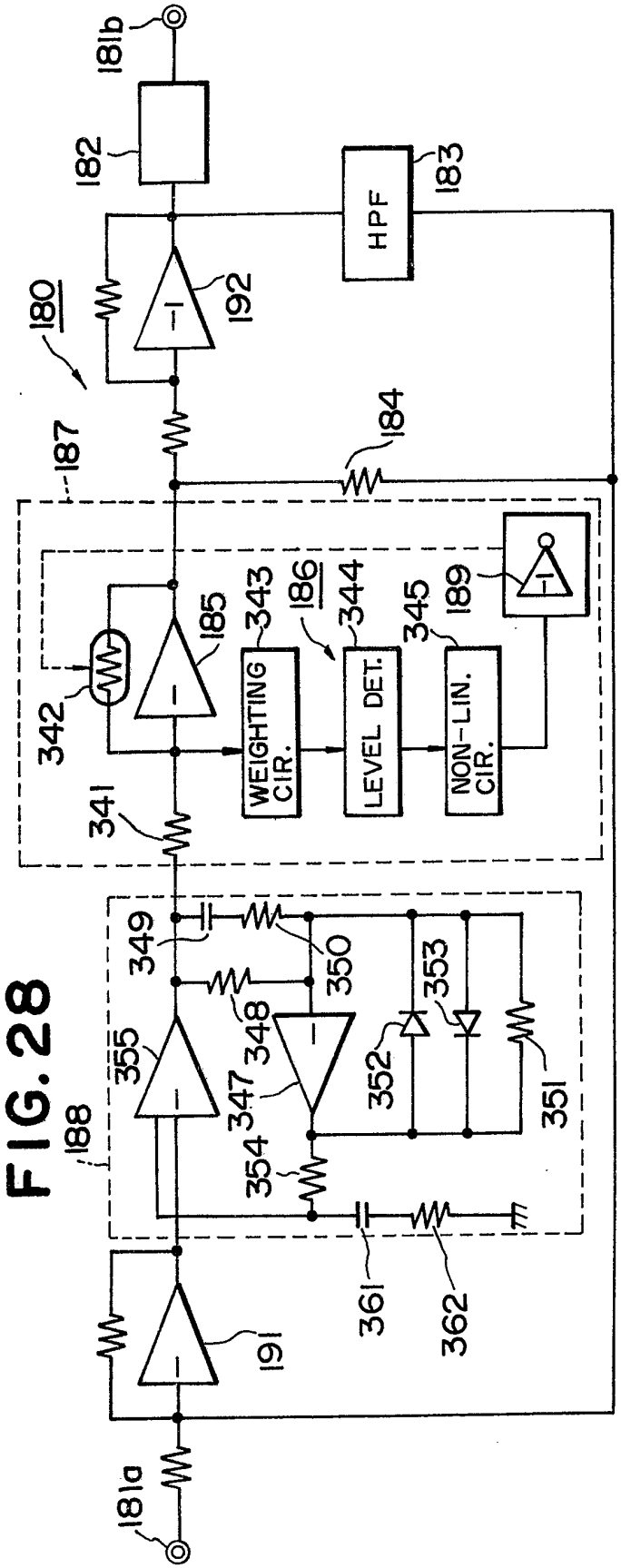

181b
182
HPF
183
180
192
187
184
342
185
343
186
344
345
189
WEIGHTING CIR.
LEVEL DET.
NON-LIN. CIR.
341
349
350
353
348
355
347
352
351
354
188
361
362
191
181a

FIG. 28

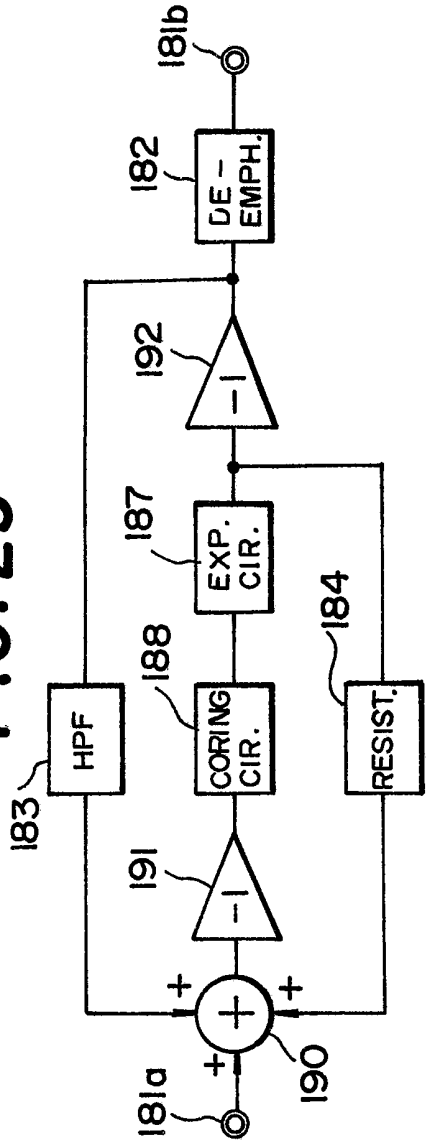

181b
182
DE-EMPH.
192
187
EXP. CIR.
184
188
CORING CIR.
RESIST.
183
HPF
191
190
181a

FIG. 29

FIG.30

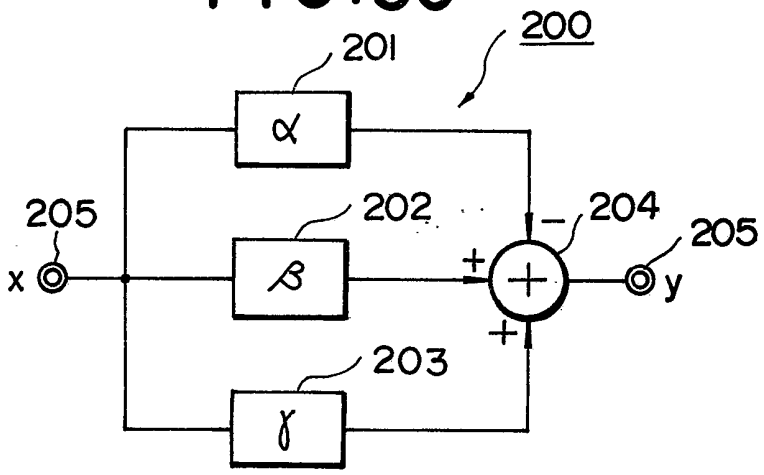
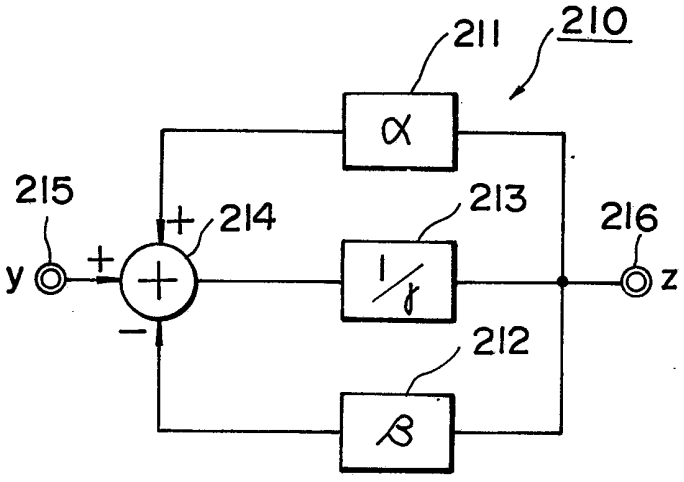

200
201
α
205
x
202
β
204
205
+
−
y
+
203
γ

FIG.31


211
210
α
215
y
+
214
+
−
213
1/γ
216
z
212
β

SPECIFICATION

Information Signal Recording and Reproducing

This invention relates to information signal recording and reproducing and, more particularly, is concerned with gain control circuits for reducing the noise accompanying a reproduced information signal.

Noise reduction systems for reducing noise and distortion which accompany a reproduced information signal in, for example, an audio tape recorder, are well-known. Such systems are designed to increase the dynamic range of the signal that can be recorded and reproduced from a recording medium such as a magnetic tape. Such systems generally incorporate an encoding process which compresses the level of the information signal and amplifies the high frequency components thereof prior to recording the signal on the recording medium. A decoding process is provided during the reproducing operation which is complementary to the compression and amplification which occur during the recording operation. In other words, the decoding process results in an expansion of the level of the reproduced information signal and an attenuation of the high frequency components thereof.

In one known noise reduction system, during the recording operation, the information signal is first transmitted through a pre-emphasis circuit which is provided with a large gain for pre-emphasizing the high frequency components of the signal supplied thereto. The pre-emphasized signal from the pre-emphasis circuit is then supplied to a compression circuit which compresses the pre-emphasized signal when the level of the information signal is less than a predetermined value and which transmits the signal with substantially unity gain for signal levels greater than the predetermined value. For example, the compression circuit may include a variable gain amplifier, such as a voltage controlled amplifier, which acts on the output from the pre-emphasis circuit. A control voltage for varying the gain of the variable gain amplifier is derived from a level detecting circuit and a limiter circuit in response to the output from the variable gain amplifier. When the level of the information signal is less than the predetermined value, the limiter circuit is inoperative so that the control signal from the level detecting circuit results in the variable gain amplifier imparting a compression characteristic to the information signal and when the level of the information signal is greater than the predetermined value, the limiter circuit grounds the control signal so that the variable gain amplifier transmits the information signal with substantially unity gain. Complementary de-emphasis and expanion circuitry are provided during the reproducing operation.

However, there are certain disadvantages with this noise reduction system. For example in addition to the variable gain amplifier requiring adjustment, the limiter circuit must also be precisely adjusted for correct operation and such adjustment is often difficult. In addition, the system exhibits a poor transient characteristic for changes in the level of the information signal. In particular, the compression circuit fails to respond adequately when the level of the information signal is abruptly increased, resulting in overshoots being created in the information signal. This occurs because the gain of the variable gain amplifier cannot instantaneously change with changes in the signal level, with the result that the large gain normally applied to low level signals is applied to the high level signals for a short time when the level of the information signal abruptly rises from a low to a high level. This results in a so-called "noise breathin" phenomenon. This is particularly noticeable when the level of the information signal changes from a level below the aforementioned predetermined value to a level above the predetermined value whereby the gain of the variable gain amplifier cannot change instantaneously from its compression gain characteristic to its substantially unity gain characteristic. Such overshoots in the level of the information signal result in a distorted waveform being recorded and reproduced from the recording medium due to magnetic saturation of the recording tape.

According to the present invention there is provided in apparatus for recording an information signal on a recording medium by a recording device, gain control means comprising:

means for defining a first transmission path for compressing said information signal;

means defining a second transmission path for transmitting said information signal with substantially unity gain; and

means for supplying the information signal to said recording device by way of said first path when the level of said information signal is below a predetermined value and for supplying said information signal to said recording device by way of said second path with substantially unity gain when the level of said information signal is above said predetermined value.

According to the present invention there is also provided in apparatus for reproducing an information signal from an encoded information signal which has been recorded on a recording medium with the information signal effectively compressed for levels thereof below a predetermined value and with the information signal effectively transmitted with substantially unity gain for levels thereof above said predetermined value; gain control means for reproducing said information signal from said encoded information signal, the gain control means comprising:

means defining a first transmission path for expanding said encoded information signal into an expanded signal; and

means defining a second transmission path for negatively feeding back said expanded signal to

said first transmission path with substantially unity gain.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a gain control circuit for a prior art noise reduction system;

Figure 2 is a graphical diagram illustrating the pre-emphasis and de-emphasis frequency characteristic for the gain control circuit of Figure 1;

Figure 3 is a graphical diagram illustrating the compression and expansion characteristics of the gain control circuit of Figure 1;

Figure 4 is a block diagram of a known compression circuit that may be used in the gain control circuit of Figure 1;

Figure 5 is a block diagram of known expansion circuit that may be used in the gain control circuit of Figure 1;

Figure 6 is a block circuit diagram of another known compression circuit that may be used in the gain control circuit of Figure 1;

Figure 7 is a graphical diagram illustrating the input-output level characteristic for the compression circuit of Figure 6;

Figure 8A is a waveform diagram illustrating changes in the signal level of an input information signal;

Figure 8B is a waveform diagram illustrating changes in the level of the signal of Figure 8A when transmitted through the recording circuits of Figures 1 and 6;

Figure 9 is a block circuit diagram of a compression circuit of a gain control circuit for an embodiment of the invention;

Figure 10 is a graphical diagram illustrating the input-output level characteristics of a non-linear circuit of the compression circuit of Figure 9;

Figure 11 is a graphical diagram illustrating the input-output level characteristic of the compression circuit of Figure 9;

Figure 12 is a circuit diagram of a non-linear circuit that can be used in the compression circuit of Figure 9;

Figure 13 is a circuit diagram of a limiter circuit that can be used in the compression circuit of Figure 9;

Figure 14 is a circuit diagram of another limiter circuit having a frequency dependency and which can be used in the compression circuit of Figure 9;

Figure 15 is a graphical diagram illustrating the frequency characteristic of the limiter circuit of Figure 14;

Figure 16 is a circuit diagram of yet another limiter circuit having a frequency dependency and which can be used in the compression circuit of Figure 9;

Figure 17 is a block circuit diagram of a further limiter circuit having a frequency dependency and which can be used in the compression circuit of Figure 9;

Figure 18 is a block circuit diagram of an expansion circuit of a gain control circuit for an embodiment of the invention and having a characteristic complementary to that of the compression circuit of Figure 9;

Figure 19A is a block diagram to which reference will be made in explaining the operation of the compression circuit of Figure 9;

Figure 19B is a block diagram to which reference will be made in explaining the operation of the expansion circuit of Figure 18;

Figure 20 is a block diagram to which reference will be made in explaining another mode of operating the expansion circuit of Figure 18 by using many of the same components of the compression circuit of Figure 9;

Figure 21 is a block circuit diagram of another input gain control circuit for an embodiment of the invention;

Figure 22 is a block diagram to which reference will be made in explaining the operation of the circuit of Figure 21;

Figure 23 is a graphical diagram illustrating the variable pre-emphasis frequency characteristic of the gain control circuit of Figure 21;

Figure 24 is a graphical diagram illustrating the input-output characterstic of the compression circuit of the gain control circuit of Figure 21;

Figure 25 is a circuit diagram of a non-linear circuit included in the compression circuit of Figure 21;

Figure 26 is a graphical diagram illustrating the input-output characteristic of the non-linear circuit of Figure 25;

Figure 27 is a graphical diagram illustrating the input-output level characteristic of the gain control circuit of Figure 21;

Figure 28 is a block circuit diagram of another output gain control circuit for an embodiment of the invention and having a characteristic complementary to the input gain control circuit of Figure 21;

Figure 29 is a block diagram to which reference will be made in explaining the operation of the output gain control circuit of Figure 28;

Figure 30 is a block diagram to which reference will be made in explaining the operation of the input gain control circuit of Figure 21; and

Figure 31 is a block diagram to which reference will be made in explaining the complementary output characteristic of the gain control circuit of Figure 28.

Referring initially to Figure 1, it will be seen that, in a gain control circuit for a prior art information signal recording and reproducing apparatus, an information signal is supplied to an input terminal 4 of an input gain control or encoder circuit 2 for removing certain high frequency components of the signal, such as noise or the like. The encoder circuit 2 includes a pre-emphasis circuit 6 supplied with the information signal from the input terminal 4 and having a large gain for pre-emphasizing the high frequency components of the information signal, as illustrated by a curve PE of Figure 2. The output from the pre-emphasis circuit 6 is supplied to a compression circuit 7 of the encoder circuit 2 and,

more particularly, to a variable gain amplifier 8, such as a voltage controlled amplifier, of the compression circuit 7. Although the pre-emphasis circuit 6 is shown in Figure 1 to be positioned before the compression circuit 7, this order may be reversed without changing the effect on the signal. The compression circuit 7 further includes a level detecting circuit 9 which detects the level of the output from the variable gain amplifier 8 and produces a *dc* control voltage in response thereto which is supplied to the variable gain amplifier 8 for varying the gain thereof. The input-output level characteristic for the compression circuit 7 is shown by a curve R in Figure 3 where it is seen that an input information signal *x* supplied thereto is compressed in a substantially linear manner on a logarithmic graph.

Referring now to Figure 4, there is shown a known compression circuit 7 which is used in the prior art gain control circuit of Figure 1. As shown therein, the variable gain amplifier 8 produces an output signal *y* which can be represented as follows:

$$y=x.e^{-V_c} \quad (1)$$

where V_c is the control voltage supplied to the variable gain amplifier 8 from the level detecting circuit 9. The detecting circuit 9 includes a natural logarithmically converting circuit 9*a* which is supplied with the output from the variable gain amplifier 8 and, in turn, supplies a natural logarithmically converted signal to a smoothing circuit 9*b*. The signal from the smoothing circuit 9*b* is amplified by an amplifier 9*c* having a gain A and which is also included in the level detecting circuit 9. The amplifier 9*c* thereby supplies the control voltage V_c which can be represented as follows, to the variable gain amplifier 8:

$$V_c=A \,.\, \ln y=\ln y \quad (2)$$

Equations (1) and (2) can be combined to form a simplified expression for the output signal *y* as follows:

$$y = x \cdot e^{-V_c} = x \cdot e^{-\ln y^A}$$

$$= x \cdot y^{-A}$$

$$y^{1+A} = x$$

$$y = x^{\frac{1}{1+A}} \quad \cdots (3)$$

If the input signal *x* and the output signal *y* are transformed into their decibel or logarithmic equivalents, the output signal *y* can be represented as follows:

$$\log y=\frac{1}{1+A}\log x \quad (4)$$

It should, therefore, be appreciated that the input signal *x* and the output signal *y* are in logarithmic-linear relation, as illustrated by the curve R in Figure 3 with the output signal *y* being compressed in relation to the input signal *x* and with the compression ratio being dependent on the gain A of the amplifier 9*c*. For example, if A=1 and log y=1/2 log x, then, as shown in Figure 3, when the input signal *x* has a level of −20 dB, the output signal *y* is compressed to a level of −10 dB. The compressed signal from the compression circuit 7 is then fed to a recording and reproducing device 1 through an output terminal 5 of the encoder circuit 2. The device 1 may be of conventional design, such as an audio signal tape recording and reproducing apparatus, and is effective to record on a magnetic tape or other recording medium the encoded signal received at the output terminal 5.

Referring back to Figure 1, it is seen that, in the known information signal recording and reproducing apparatus there illustrated, a reproducing section includes an output gain control or decoder circuit 3 having an input terminal 11 supplied with the encoded signal reproduced from the recording medium. The decoder circuit 3 transforms the reproduced encoded signal into the original information signal supplied to the input terminal 4 of the encoder circuit 2 and acts on the signal supplied thereto in a manner substantially complementary to the encoder circuit 2. The decoder circuit 3 includes an expansion circuit 13 for expanding the reproduced information signal in a manner substantially complementary to the amount of compression from the compression circuit 7. Thus, as shown in Figure 3 by a curve P, the input-output level characteristic of the expansion circuit 13 is a mirror image of the curve R of the compression circuit 7. For example, when the level of the information signal supplied to the compression circuit 7 is −20 dB, the compression circuit 7 produces an output signal having a level of −10 dB. When this output signal having a level of −10 dB is applied to the expansion circuit 13, the information signal is returned to its original level of −20 dB, as shown by the dotted lines in Figure 3. The output of the expansion circuit 13 is supplied to a de-emphasis circuit 14 also included in the decoder circuit 3 for attenuating the high frequency components of the reproduced encoded signal in a manner substantially complementary to the amount of pre-emphasis from the pre-emphasis circuit 6, as shown by the curve DE in Figure 2. It should be realised, however, that the positional arrangement of the expansion circuit 13 and the de-emphasis circuit 14 may be reversed with no change in the effect on the reproduced encoded signal. The resulting reproduced signal is supplied to an output terminal 12 of the decoder circuit 3.

As shown in Figure 1, the expansion circuit 13 includes a variable gain amplifier 15 supplied with the reproduced encoded signal from the input terminal 11 and which is similar to the variable

gain amplifier 8 of the compression circuit 7. A level detecting circuit 16 is also supplied with the encoded signal and produces a control voltage in response thereto which is supplied to the variable gain amplifier 15 so as to regulate the gain thereof.

Referring now to Figure 5, there is shown an expansion circuit 13 commonly used with the decoder circuit 3 of Figure 1. As shown therein, the variable gain amplifier 15 is supplied at an input terminal 26 thereof with the encoded information signal y and produces an output signal z at an output terminal 27 in response thereto which can be represented as follows:

$$z=y \cdot e^{-V_c'} \quad (5)$$

wherein V_c' is the control voltage supplied to the variable gain amplifier 15 by the level detecting circuit 16. The level detecting circuit 16 includes a natural logarithmically converting circuit 16*a* supplied with the encoded information signal y and which, in turn, produces an output which is supplied through a smoothing circuit 16*b* to an amplifier 16*c* having a gain of —A. The amplifier 16*c* produces the control voltage V_c' which is represented as follows:

$$V_c'=-A \cdot \ln y \quad (6)$$

Equations (5) and (6) can be combined to form a simplified expression for the output signal z as follows:

$$z=y \cdot e^{A \cdot \ln y}=y \cdot e^{\ln y^A}=y \cdot y^A$$
$$z=y^{1+A} \quad (7)$$

Equation (7) can be transformed into its logarithmic or decibel equivalent and rewritten as follows:

$$\log z=(1+A)\log y \quad (8)$$

Upon comparing equations (4) and (8), it should be appreciated that the slopes of the logarithmic input-output characteristics thereof are in reciprocal relation. For example when A=1, the slope of the logarithmic input-output curve for the compression circuit 7 is 1/2 while the slope of the logarithmic input-output curve of the expansion circuit 13 is 2.

It should further be appreciated that the decoder circuit 3 reproduces exactly, at an output terminal 12 thereof, the original information signal supplied to the input terminal 4 of the encoder circuit 2. More particularly, if equation (3) is substituted into equation (7), it is seen that:

$$z=\left\{x^{\frac{1}{1+A}}\right\}^{(1+A)}=x \quad \cdots (9)$$

However, the above encoder circuit 2 needlessly compresses both the high and low signal levels of the information signal, as shown by the curve R in Figure 3. In other words, high signal levels result in a sufficiently high signal-to-noise ratio so that there is no need to compress such signals. In comparison, when the signal level is of a relatively low value, the gain of the variable gain amplifier 8 is of a relatively high value so that background noise is greatly amplified, resulting in a low signal-to-noise ratio. This results in a hissing sound in the reproduced signal which is particularly noticeable as the level of the signal varies. Accordingly, it is only necessary to compress low levels of the information signal to attenuate the background noise in relation to the low level signal while providing no compression to signal levels of a relatively high level.

Referring now to Figure 6, there is shown a previously proposed improved compression circuit 7 in which elements corresponding to those described above with reference to the compression circuit of Figure 4 are identified by the same reference numerals. As shown therein, the pre-emphasized information signal from the pre-emphasis circuit 6 (Figure 1) is supplied to the variable gain amplifier 8 from an input terminal 21. As previously discussed in regard to Figure 4, the variable gain amplifier 8 produces a compressed output signal y at an output terminal 22 thereof which is also supplied to a level detecting circuit 9. The level detecting circuit 9 produces the control voltage which is supplied to the variable gain amplifier 8 for varying the gain thereof. The control voltage from the level detecting circuit 9 is supplied to the variable gain amplifier 8 through a limiter circuit 28 which has no effect on the control voltage when the level thereof is below a predetermined value but which grounds the control voltage when the level thereof is greater than the predetermined value. In particular, the limiter circuit 28 includes a PNP transistor 28*b* having its collector connected to ground and its emitter connected through a diode 28*a* to the output of the level detecting circuit 9 and to the control voltage input of the variable gain amplifier 8. The base of the transistor 28*b* is connected to the movable tap of the variable resistor 28*c* which is, in turn, connected to a voltage source. Thus, as the level of the output signal y from the variable gain amplifier 8 increases so that the control voltage from the level detecting circuit 9 becomes greater than a predetermined value, the diode 28*a* is turned ON so as to render the transistor 28*b* conductive. As a result, the output from the level detecting circuit 9 is grounded through the diode 28*a* and the collector-emitter path of the transistor 28*b* so that a control voltage at ground potential is supplied to the variable gain amplifier 8. Since the input-output characteristic of the variable gain amplifier 8 is represented by equation (1), it should be appreciated that, at such time when the control voltage supplied to the variable gain amplifier 8 is at ground potential, the variable gain amplifier 8 has a unity gain. In other words, the information signal is not compressed when the level thereof exceeds the predetermined

value. However, when the level of the information signal is below the predetermined value, the diode 28*a* is turned OFF so that the variable gain amplifier 8 provides a compression effect to the low level information signals in response to the control voltage supplied thereto from the level detecting circuit 9. The input-output characteristic for the compression circuit 7 of Figure 6 is shown by the solid line in Figure 7. Of course, when the compression circuit of Figure 6 is used in the input gain control circuit, an expansion circuit is provided on the output side of recording and reproducing device 1 which has an input-output expansion characteristic which is complementary to the characteristic of the compression circuit 7 shown in Figure 7.

However, the above compression circuit 7 of Figure 6 still poses various problems. For example, in addition to the need to adjust the variable gain amplifier 8 correctly to respond to the control voltage supplied thereto, adjustment of the limit level of the limiter circuit 28 and, more particularly, of the variable resistor 28*c*, is also required. However, because of these two phases of adjustment, it is often difficult to obtain exact adjustment levels. This means that the level of the output signal *y* may not always correctly correspond to the level of the input signal *x* as shown in Figure 7.

In addition, the compression and expansion circuits of Figures 4 to 6 exhibit a poor transient characteristic for changes in signal level. In particular, these circuits fail adequately to respond when the signal level is abruptly increased from a first low level to a second higher level. For example, when the level of an input signal is abruptly increased, as shown in Figure 8A, the output signal *y*, as shown in Figure 8B, is produced at the output terminal 22 of each of the compression circuits 7 of Figures 4 and 6. Thus, when the input signal level is increased, as shown by the positive-going edge in Figure 8A, the resulting output signal has a corresponding overshoot portion which is substantially greater than the desired level of the output signal. The time within which this overshoot falls back to its desired level is termed the attack time t_A. However, it becomes difficult to choose a correct attack time t_A since an attack time which is too long will distort the sound which is eventually reproduced and an attack time t_A that is too short will result in a clicking noise in the reproduced sound. An optimum attack time t_A is therefore set in the range of 100 microseconds to 10 microseconds. In like manner, when the input signal level falls from a high value to a low value as shown by the negative-going edge of the signal in Figure 8A, a negative overshoot occurs and the time within which the level of the signal returns from the overshoot level to its desired level is termed the recovery time t_R. As shown in Figure 8B, the recovery time t_R is optimally set for a comparatively long time which is generally greater than 100 microseconds. It should be appreciated that the attack time t_A and the recovery time t_R result from the charging and discharging of a capacitor in the circuit. However, the setting of these response times t_A and t_R becomes difficult.

Further, overshoots as a result of increasing signal levels within the relatively short attack time t_A may, for example, have a level which is 10 dB greater than the desired signal level. Such increase in signal level is, of course, undesirable and results in the occurrence of a distorted sound when reproduced from a magnetic tape. This distortion results because the magnetic tape is only designed to record, without distortion, signals up to certain level. Above this level, the magnetic tape becomes saturated so that recording of signals above this level results in distortion of the reproduced sound.

Referring now to Figure 7, it is seen that if an input signal level changes from −20 dB to+10 dB, the output signal level changes from a point I on the solid line curve of Figure 7 to a point II thereon. However, because the gain of the variable gain amplifier 8 cannot instantaneously follow the above-described rapid signal level increase, the output signal level is first raised from the point I to a point III, as represented by the broken line in Figure 7. This results in the high level input signal being acted on for a short interval with a large gain from the variable gain amplifier 8. Thereafter, the output signal level is slowly lowered from the point III to the point II within the attack time t_A as the gain of the variable gain amplifier 8 slowly decreases. It should therefore be appreciated that the utilization of a single signal path for signals above the aforementioned limit level and for signals below the aforementioned limit level may have a deleterious effect on the reproduced sound, as previously discussed.

Referring now to Figure 9, there is shown a compression circuit 30 for a gain control circuit of an embodiment of the invention. In this embodiment, the information signal is supplied to a pre-emphasis circuit 6 (Figure 1) for pre-emphasizing the high frequency components of the signal. The pre-emphasized signal is then supplied to an input terminal 31*a* of a compression circuit 30 (Figure 9) where signal levels lower than the predetermined value are compressed and signal levels greater than the predetermined value are passed therethrough with substantially unity gain. In particular, the compression circuit 30 includes a first transmission path including a variable gain amplifier 33, such as a voltage controlled amplifier, having its input connected to the input terminal 31*a* through a resistor 32. A control circuit 34 supplies a control voltage to the variable gain amplifier 33 for varying the gain thereof and includes a level detecting circuit 35 supplied with the output signal from the variable gain amplifier 33 and a non-linear circuit 36 which produces the control voltage in response to the detected output signal from the level detecting circuit 35. The non-linear circuit 36 has

an input-output characteristic which, as shown in Figure 10, has a first linear slope when the detected output signal from the level detecting circuit 35 is less than a predetermined voltage V_S and a second linear slope which is greater than the first linear slope when the level of the detected output signal is greater than the predetermined voltage V_S. In other words, the input-output characteristic of the non-linear circuit 36 is of a "bent-linear" nature.

Therefore, if the input-output level characteristic of the variable gain amplifier 33 is plotted, a "bent-linear" curve will also be exhibited, as shown by the broken line in Figure 11. In this regard, the 0 dB reference level at which the broken line curve of Figure 11 is bent, corresponds to the predetermined voltage V_S of the detected output signal from the level detecting circuit 35. As a result, the gradient of the input-output level curve of the variable gain amplifier 33 for input levels less than 0 dB is 2. In other words, for such low levels of the input signal, a compression ratio of 2:1 is produced. However, for input levels greater than 0 dB, the gradient of the input-output level curve is less than the aforementioned gradient so that a compression ratio of *n*:1 is produced where *n* is greater than 2.

The output from the variable gain amplifier 33 is transmitted through a resistor 37 to a diode limiter circuit 40 comprised of two diodes 28 and 39, each being connected between the output of the resistor 37 and ground and arranged in opposing relation to the other. In other words, as shown in Figure 9, the cathode of the diode 38 and the anode of the diode 39 are connected to the output of the resistor 37 and the anode of the diode 38 and the cathode of the diode 39 are connected to ground. It should therefore be appreciated that for output levels of the variable gain amplifier 33 greater than the positive limiting level L (Figure 110 of the limiter circuit 40, the diode 39 is turned ON so as to connect this output to ground. In like manner, it should be realised that the diode 38 acts to produce a negative limiter level for the output of the variable gain amplifier 33. The output of the variable gain amplifier 33 is thereby supplied through the limiter circuit 40 and another resistor 41 to an input of an adder amplifier 42. The adder amplifier 42 is preferably an operational amplifier and the output from the variable gain amplifier 33 is supplied to the inverting input of the adder amplifier 42.

A second transmission path is connected in parallel with the first transmission path between the input terminal 31*a* and the inverting input of the adder amplifier 42 and comprises a single resistor 43 which provides a flat pass characteristic having a constant gain. In particular, and as shown in Figure 11 by the dot-dash line therein, the input-output characteristic of the second transmission path has a gradient of one so as to transmit the information signal with substantially unity gain. Thus, the compressed information signal from the first transmission path of the variable gain amplifier 33 and the information signal with substantially unity gain from the second transmission path through the resistor 43 are both supplied to an input, preferably the inverting input, of the adder amplifier 42.

As can readily be seen from the broken line and dot-dash line characteristics of Figure 11, when the level of the input information signal is less than the 0 dB reference level, the compressed information signal from the variable gain amplifier 33 of the first transmission path is much greater than the transmitted information signal from the second transmission path so that the compressed signal from the variable gain amplifier 33 is effectively produced at the output of the adder amplifier 42. In comparison, when the level of the input information signal is greater than the 0 dB reference level, the transmitted information signal through the second transmission path of the resistor 43 is much greater than the compressed signal through the variable gain amplifier 33 so that the transmitted signal from the second transmission path of the resistor 43 is effectively produced at the output of the adder amplifier 42. In other words, the output from the second transmission path of the resistor 43 can effectively be ignored when the level of the information signal is less than the 0 dB reference level, and the compressed signal from the variable gain amplifier 33 can effectively be ignored when the level of the information signal is greater than the 0 dB reference level. Accordingly, the adder amplifier 42 adds the effective signals at such time to produce an effective composite input-output characteristic shown by the solid line in Figure 11. It should be realised that this characteristic is substantially identical to the prior art characteristic shown in Figure 7. Moreover, a feedback resistor 44 is connected between the output of the adder amplifer 42 and the inverting input thereof for stabilizing the gain of the adder amplifer 42.

It should be appreciated that the use of the first and second transmission paths substantially eliminates the problems inherent in the prior art apparatus previously discussed. For example, with the prior art compression circuit shown in Figure 6, since the gain of the variable gain amplifier 8 cannot change instantaneously with changes in the signal level, when a signal level having a low value is abruptly increased to a higher value, the high gain of the variable gain amplifier 8 acting on the low level signal also acts on the abruptly increased higher level signal for a short time. This results, as previously discussed, in overshoots being formed in the signal which produce a deleterious effect on the sound reproduced from such a signal recorded on a magnetic tape. However, the gain control circuit shown in Figure 9 substantially eliminates such adverse effects. Thus, when the level of the input signal changes from a low value, for example, below 0 dB, to a higher value above the 0 dB reference level, the

variable gain amplifier 33 produces an output signal having overshoots. However, since the limiter circuit 40 is positioned outside of the control circuit 34, the overshoots are effectively suppressed. In other words, when large overshoots from the variable gain amplifier 33 are supplied to the limiter circuit 40, the diode 39 turns ON so as to ground such overshoots. However, since the output level is now greater than 0 dB, the adder amplifier 42 is effectively supplied with the information signal through the second transmission path of the resistor 43. As a result, any distortion in the signals is substantially eliminated.

Referring now to Figure 12, there is shown one circuit arrangement that may be used for non-linear circuit 36 in the gain control circuit of an embodiment of the invention. As shown therein, the detected output signal from the level detecting circuit 35 is supplied through an input terminal 45*a* and a resistor 46 to an amplifier 47. A series circuit comprising a resistor 48*a*, a voltage source 48*b* for producing a voltage substantially equal to the predetermined voltage V_s (Figure 10) and having its positive terminal connected to the resistor 48*a*, and a diode 48*c* having its anode connected to the negative terminal of the voltage source 48*b*, is connected in parallel with the resistor 46 between the input terminal 45*a* and the input of the amplifier 47. Moreover, the input of the amplifier 47 is connected to ground through a resistor 49, and the output of the amplifier 47 is connected to a terminal 45*b* which is, in turn, connected to the control input of the variable gain amplifier 33. Thus, when the level of the information signal supplied to the input terminal 45*a* is less than the predetermined voltage V_s, the diode 48*c* is rendered inoperative so that a first voltage divider comprising resistors 46 and 49 supplies a voltage divided signal to the amplifier 47. However, when the level of the information signal supplied to the input terminal 45*a* is greater than the predetermined voltage V_s, the diode 48*c* is turned ON. This results in the resistors 46 and 48*a*, which are in parallel, forming an equivalent resistance which forms a voltage divider circuit with the resistor 49. Accordingly, the voltage-dividing ratio acting on the signal supplied to the amplifier 47 changes so that the bent-linear input-output characteristic shown in Figure 10 is obtained.

Although the limiter circuit used in the embodiment of Figure 9 is a diode limiter circuit 40, it should be appreciated that any equivalent limiter circuit may be substituted therefor. For example, as shown in Figure 13, a transistor limiter circuit 50 may be used. In this circuit, three resistors 53, 54 and 55 are connected in series between an input terminal and output terminal of the limiter circuit 50 and two resistors 56 and 57 are connected in series between a junction point of the resistors 53 and 54 and ground. An NPN transistor 58 has its base connected to ground through the resistor 57, its emitter connected directly to ground and its collector connected to a junction point between the resistors 54 and 55. Thus, when the level of the information signal supplied from the variable gain amplifier 33 of Figure 9 to the input terminal of the limiter circuit 50 is less than the predetermined voltage V_s, the voltage supplied to the base of the transistor 58 is insufficient to turn the transistor 58 ON. Accordingly, at such time, the compressed information signal from the variable gain amplifier 33 is supplied through the resistors 53, 54 and 55 to the inverting input of adder amplifier 42. However, when the level of the compressed information signal is greater than the predetermined voltage V_s, the transistor 58 is turned ON so that the compressed information signal is grounded through the collector-emitter path of the transistor 58.

The limiter circuits 40 and 50 have a relatively flat frequency characteristic, that is, a characteristic which is dependent only upon the level of the signal supplied thereto and not on the frequency of the signal. However, conventional magnetic tape used in audio signal recording and reproducing apparatus has a frequency characteristic whereby the maximum signal level which can be reproduced from the magnetic tape decreases at higher frequencies as a result of the saturation characteristic thereof. Since the limiter circuits 40 and 50 have a flat frequency characteristic, that is, are not frequency dependent, the limiting levels thereof are set to conform with the maximum output level which can be reproduced from the magnetic tape for high frequency signals. The signal levels of low and mid-frequency signals are thereby limited to a greater extent than necessary. In the case where a compromise is sought between the excessive limitation in the low and mid-frequency ranges and the decreased limiting level for the high frequency range, the low and mid-frequency signals will still have their signal levels limited to an extent greater than necessary while signal levels in the high frequency range will not be sufficiently limited so that some saturation in this latter range will occur. Accordingly, it is desirable to have a limiter circuit which is frequency dependent in a complementary manner to the frequency characteristic of the magnetic tape utilized.

Referring now to Figure 14, there is shown a limited circuit 60 which can be substituted for limiter circuit 40 of Figure 9 and which has a frequency characteristic corresponding to the saturation characteristic of the magnetic tape. As shown therein, resistors 61 and 62 are connected in series between the output of the variable gain amplifier 33 and the output of the limiter circuit 60 which, in turn is connected to the inverting input of the adder amplifier 42. A series circuit of a resistor 63 and a capacitor 64 is connected between a junction point of the resistors 61 and 62 and ground. Two diodes 54 and 66 are each connected in parallel with resistor 63 and are arranged in opposing relation. In particular, the

cathode of the diode 65 and the anode of the diode 66 are connected to the junction point between the resistors 61 and 62 and the anode of the diode 65 and the cathode of the diode 66 are connected in common to the junction point between the resistor 63 and the capacitor 64. Given that the resistance values of the resistors 61 and 63 are R_1 and R_3, respectively, and the capacitance of the capacitor 64 is C, a voltage V_o applied across the resistor 63 and, of course, across each of the diodes 65 and 66, can be expressed as follows:

$$V_o = \frac{R_3}{R_1 + R_3 + \frac{1}{j\omega C}} \cdot V_{in}$$

$$= \frac{j\omega C R_3}{1 + j\omega C (R_1 + R_3)} \cdot V_{in} \quad \cdots (10)$$

where V_{in} is the voltage supplied to the limiter circuit 60 from the variable gain amplifier 33. It should, therefore, be appreciated that, at high frequencies, the capacitor 64 is effectively shorted in the circuit so that the diodes 65 and 66 operate in a subsantially identical manner to the limiter circuit 40 of Figure 9. In other words and as shown in Figure 15, a substantially flat frequency response is generated for high frequency signals above the frequency f_c, with the maximum value of the output signal from the limiter circuit 60 being equal to:

$$\frac{R_3}{R_1+R_1} \cdot V_{in}$$

This latter value is, of course, equal to the cut-in voltage of either of the diodes 65 and 66 depending on the polarity of the input voltage V_{in}. In comparison, at low frequencies, the capacitor 64 retains a charge whereby the junction point between the resistor 63 and the capacitor 64 is raised to a voltage greater than ground potential. This means that a higher level of input voltage V_{in} is required to turn ON the diode 66 so that the maximum output level from the limiter circuit 60 which can be recorded on the magnetic tape is greater for low frequency signals. In a practical form of the arrangement of Figure 14, the frequency characteristic of the voltage developed across the resistor 63, and consequently, across the diodes 65 and 66, provides a substantially flat characteristic for high frequencies, whereas, at low frequencies below cut-off frequency f_c where:

$$f_c = \frac{1}{2\pi C(R_1+R_3)} \quad (11)$$

the voltage V_o developed across the resistor 63 falls at a rate of 6 dB/octave. It should be realized, however, that a predetermined limiting level may be provided for the low frequency signals which is different than that for the high frequency signals by merely connecting a resistor in parallel with the capacitor 64.

Referring now to Figure 16, there is shown another of a frequency dependent limiter circuit 70 which can be substituted for the limiter circuit 40 (Figure 9) and which has a frequency characteristic substantially identical to the limiter circuit 60 of Figure 14. As shown therein, resistors 71 and 72 are connected in series between the output of the variable gain amplifier 33 and the output of the limiter circuit 70. A capacitor 73 and a resistor 74 are connected in series between the junction of the resistors 71 and 72 and ground, and a pair of transistors 75 and 76 each have their collector-emitter paths connected in parallel with the resistor 74. In particular, the transistor 75 is a PNP transistor and the transistor 76 is an NPN transistor whereby the emitter of the transistor 75 and the collector of the transistor 76 are commonly connected to a junction point between the capacitor 73 and the resistor 74 and the collector of the transistor 75 and the emitter of the transistor 76 are connected in common to ground. Moreover, an amplifier 77 has its input connected to the junction point between the capacitor 73 and the resistor 74 and its output connected through a resistor 78 to the commonly connected bases of the transistors 75 and 76. It should be appreciated that this circuit operates in a substantially identical manner to the limiter circuit 60 of Figure 14. In particular, at high frequencies, capacitor 73 is effectively shorted so that the signal from the variable gain amplifier 33 is supplied across the resistor 74 for turning ON one of the transistor 75 and 76, depending on the polarity of the signal across the resistor 74. When either of the transistors 75 or 76 is turned ON, the output signal from the variable gain amplifier 33 is grounded through the collector-emitter path thereof. However, at low frequencies, the level of the signal from the variable gain amplifier 33 must be higher in order to supply the same operating voltage across the resistor 74, due to the charging of the capacitor 73. Accordingly, the maximum level of the input signal which is recorded on the magnetic tape is higher for low and mid-frequency signals than for high frequency signals.

A further frequency dependent limiter circuit 80 is shown in Figure 17. The limiter circuit 80 comprises a sub-limiter circuit 40 identical to the limiter circuit of Figure 9 and which has a substantially flat frequency characteristic. A first filter circuit 81 is interposed between the variable gain amplifier 33 and the input of the sub-limiter circuit 40 and has a frequency characteristic $f(\omega)$, and a second filter circuit 82 is supplied with the output from the sub-limiter circuit 40 and has a frequency characteristic $1/f(\omega)$ which is the reciprocal or inverse of the frequency characteristic of the filter circuit 81. In this manner, the filter circuits 81 and 82 are designed to have a desired frequency characteristic which,

in conjunction with the limiter circuit 40 of Figure 17, provides an effective frequency dependent limiter circuit 80.

Referring now to Figure 18, there is shown an expansion circuit 90 for a gain control of an embodiment of the invention and which can be used in place of the expansion circuit 13 of Figure 1 and which has an input-output characteristic complementary to that of the compression circuit 30 of Figure 9. In other words, the expansion circuit 90 provides an expansion characteristic to the reproduced encoded signal which is the reverse of the characteristic imparted by compression circuit 30 of Figure 9 so as to return the encoded signal to its original form.

In particular, a reproduced encoded signal which is recorded on a recording medium, such as a magnetic tape, is fed by transducers or the like to an input terminal 91*a* of the expansion circuit 90. This signal is further transmitted through a resistor 92 to an output terminal 91*b* of the expanion circuit 90 through first and second transmission paths. The first transmission path includes a variable gain amplifier 93 supplied at its input terminal wih the encoded signal from the input terminal 91*a* through the resistor 92 and a diode coring limiter circuit 100. This latter circuit comprises a pair of diodes 101 and 102 which are connected in a parallel combination in opposing relation between the resistor 92 and the variable gain amplifier 93. A resistor 103 is connected between the input of the variable gain amplifier 93 and ground. Thus, the diode limiter circuit 100 limits the level of the reproduced encoded signal supplied thereto at two independent levels and provides a characteristic opposite to that of the limiter circuit 40 of Figure 9. For example, if the diodes 101 and 102 are of identical construction and have a cut-in voltage level of 0.7 volts, the reproduced encoded signal from the terminal 91*a* is supplied to the variable gain amplifier 93 only when the level of this signal is above 0.7 volts (through the diode 102) or less than −0.7 volts (through the diode 101).

The first transmission path further includes a control circuit 94 for supplying a control voltage to the variable gain amplifier 93 for varying the gain thereof. The control circuit 94 includes a level detecting circuit 95 supplied with the reproduced encoded signal from the input terminal 91*a* and which, in turn, supplies a detected output signal to a non-linear circuit 96 also of the control circuit 94. An amplifier 97 having a gain of minus one, that is, an inverter, is supplied with the output from the non-linear circuit 96 and produces the control voltage which is supplied to the variable gain amplifier 93. It should be appreciated that the control circuit 94, along with the variable gain amplifier 93, acts on the reproduced encoded signal in a manner substantially complementary to the corresponding variable gain amplifier 33 and the control circuit 34 of Figure 9. The output from the variable gain amplifier 93 is supplied to an inverting amplifier 104 through a resistor 98.

The second transmission path comprises a negative feedback resistor 105 supplies with the expanded inverted signal from the inverting amplifier 104 and which transmits the signal with a substantially flat pass characteristic, that is, with substantially unity gain, to the input of the first transmission path and more particularly, to the the limiter circuit 100 thereof. More particularly, the resistor 105 is connected between the output side of the resistor 92 and the output of the inverting amplifier 104. Thus, the encoded signal supplied through the first transmission path is inverted by the amplifier 104 and this inverted signal is fed back to the first transmission path so as to reproduce the original information signal that had previously been supplied to the compression circuit 30 of Figure 9. A feedback resistor 106 is also connected between the input and output terminals of the inverting amplifier 104 for adjusting the gain thereof. Moreover, the output gain control or decoder circuit includes a de-emphasis circuit, such as the circuit 14 shown in Figure 1, which is connected to either the input or output terminal 91*a* or 91*b* of the expansion circuit 90 for providing a characteristic complementary to the pre-emphasis circuit in the input gain control or encoder circuit. In other words, the de-emphasis circuit attenuates the high frequency components of the encoded signal.

Referring now to Figures 19 and 20, the principle of operation of the gain control circuit will now be discussed in relation to Figures 19A and 19B. Referring first to Figure 19A which illustrates an encoder circuit 110 of an embodiment of the invention and which is representative, for example, of the compression circuit 30 of Figure 9, an input information signal x is supplied to an input terminal 111*a* of the encoder circuit 110. The information signal x is then supplied through a first transmission path 113 which acts on the signal with a transmission function β and through a second transmission path 112 which acts on the signal with a transmission function α. The signals transmitted through the two tranmission paths 112 and 113 are added in an adding circuit 114 and this added signal is supplied as an output signal y to an output terminal 111*b* of the encoder circuit 110. It should be realised, of course, that in relation to the circuit of Figure 9, the first transmission path 113 includes the variable gain amplifier 33 and the control circuit 34 which compresses the input information signal, and the second transmission path 112 comprises the resistor 43 which transmits the information signal with substantially unity gain. Thus, output signal y from the adding circuit 114 can be represented as follows:

$$y=(\alpha+\beta)x \qquad (12)$$

A decoder circuit 115 of an embodiment of the invention is shown in Figure 19B. In particular, the encoded signal y from the output terminal 111*b* of the encoder circuit 110 is supplied to an input

terminal 116*a* of the decoder circuit 115. This signal is then supplied to a positive input terminal of an adding circuit 117 which, in turn, transmits the signal to an output terminal 116*b* of the decoder circuit 115 through a first transmission path 118 having a transmission function $1/\beta$ which is the reciprocal of the function of the first transmission path 113 of the encoder circuit 110. This results in an output signal *z* being supplied to the output terminal 116*b* of the decoder circuit 115 and also to a negative input terminal of the adding circuit 117 through a second transmission path 119 having a transmission function α. Accordingly, an output signal *z* is produced at output terminal 116*b* which can be represented as follows:

$$z=1/\beta(y-\alpha z) \qquad (13)$$

Equation (12) may be substituted in equation (13), as follows:

$$z=\frac{1}{\beta}[(\alpha+\beta)x-\alpha z]$$

$$\beta z=(\alpha+\beta)x-\alpha z$$

$$(\alpha+\beta)z=(\alpha+\beta)x$$

$$z=x \qquad \ldots(14)$$

In other words, the information signal which had previously been subjected to compression in the encoder circuit 110 is returned to its original form by the decoder circuit 115 which provides a complementary expansion to the encoded signal. It should be noted, however, that in order to obtain complementary characteristics between the compression circuit 30 (the encoder circuit 110) and the expansion circuit 90 (the decoder circuit 115), the resistance of the resistor 43 (Figure 9) should be equivalent to the resistance of the resistor 105 (Figure 18) and the gain characteristic of the variable gain amplifier 33 (Figure 9) should be equal and opposite to that of the variable gain amplifier 93 (Figure 18).

The inverse or reciprocal tranmission function $1/\beta$ of the transmission path 118 (Figure 19B) can be obtained by utilizing the circuitry of the encoder circuit 110 (Figure 19A). For example, a negative feedback circuit 122 (Figure 20) may include an operational amplifier 121 having the encoded signal *y* supplied to its non-inverting input. The output from the operational amplifier 121 is supplied to the inverting input thereof in a negative feedback loop through a transmission path 120 having a transmission function β, where the transmission path 120 is equivalent to the transmission path 113 of Figure 19A. If the gain of the operational amplifier 121 is α, the transmission function G of the negative feedback circuit 122 can be represented as follows:

$$G=\frac{\alpha}{1+\alpha\beta} \qquad (15)$$

If the values of α and β are chosen as that $\alpha\beta$ is much greater than one, then the transmission function G can be represented as follows:

$$G=\frac{1}{\beta} \qquad (16)$$

In this manner, the reciprocal or inverse transfer function $1/\beta$ for the transmission path 118 of Figure 19B is obtained by utilizing circuitry similar to that of the encoder circuit 110.

It should therefore be appreciated that the gain control circuit of an embodiment of the invention provides distinct advantages over the prior art gain control circuit. For example, by providing two transmission paths and a 0 dB reference level at which the effect of the two transmission paths on the compression and expansion characteristics of the compression circuit 30 and the expansion circuit 90 changes, respectively, it is only necessary to adjust the variable gain amplifiers 33 and 93, respectively, without the necessity of further adjusting the variable resistor 28*c* (Figure 6) as required by the prior art. Further, by providing the limiter circuits 40, 50, 60, 70 or 80 at the output of the variable gain amplifier 33 and the limiter circuit 100 at the input of the variable gain amplifier 93, any overshoots in the compressed signal are effectively suppressed so as substantially to eliminate any adverse effects from saturation of a magnetic tape. It should be appreciated that compression and expansion of the level of an information signal are thus peformed in a desired manner while saturation of a magnetic tape is prevented and any spectral components in the low frequency range of the information signal, which would normally be generated as a result of such saturation, are substantially eliminated or reduced.

Referring now to Figure 21, there is shown another input gain control or encoder circuit 130 of an embodiment of the present invention. In this embodiment, an information signal is supplied through an input terminal 131*a* and a pre-emphasis circuit 132 of the encoder circuit 130 comprised of three transmission paths. The pre-emphasis circuit 132 pre-emphasizes the high frequency components of the information signal supplied thereto in much the same manner as the pre-emphasis circuit 6 of Figure 1.

The encoder circuit 130 includes a first transmission path comprising a compression circuit 137 having a variable gain amplifier 135, such as an operation amplifier, and a control circuit 136 for varying the gain of the variable gain amplifier 135. The variable gain amplifier 135 is supplied with the pre-emphasized signal from the pre-emphasis circuit 132 through a resistor 141, for example, as its inverting input. The control circuit 136 includes a weighting

circuit 143 supplied with the output from the variable gain amplifier 135 and which weights the signal supplied thereto in accordance with the frequency of the signal. For example, the weighting circuit 143 may comprise a high pass filter which weights the high frequency spectrum of the signal. The output of the weighting circuit 143 is supplied to a level detecting circuit 144 which detects the level of the signal from the weighting circuit 143 and which may, for example, comprise a full wave rectifier for rectifying or smoothing the signal. A non-linear circuit 145 is supplied with the output from the level detecting circuit 144 for non-linearly converting the level detected output signal and producing a control voltage for varying the gain of the variable gain amplifier 135. More particularly, a negative feedback resistor 142, such as a CdS photoconductive cell, is connected between the output and inverting inputs of the variable gain amplifier 135, and a light emitting element (not shown), such as a light emitting diode, emits light in accordance with the control voltage from the non-linear circuit 145 for irradiating the negative feedback resistor 142. In this manner, depending on the level of the control signal from the non-linear circuit 145, the resistance value of the negative feedback resistor 142 is varied so as to vary the gain of the variable gain amplifier 135.

The output from the variable gain amplifier 135 is supplied to a limiter circuit 138 which limits the level of the output from the variable gain amplifier 135. In the limiter circuit 138, a resistor 148 is connected in parallel with a series combination of a capacitor 149 and a resistor 150 and this parallel combination is connected between the output of the variable gain amplifier 135 and the inverting input of an operational amplifier 147. A resistor 151, a first diode 152 and a second diode 153 are each connected in parallel with each other and are connected between the input and output terminals of the operational amplifier 147 with the diodes 152 and 153 being arranged in opposing relation. It should be appreciated that the diodes 152 and 153 perform the same function as the diodes 38 and 39 of Figure 9, and the resistor 151 is a negative feedback resistor for stabilizing the gain of the amplifier 147. The limiter circuit 138 further includes an operational amplifier 155 supplied with the output from the amplifier 147 at its non-inverting input through a resistor 154. The non-inverting input of the operational amplifier 155 is further connected to ground through a capacitor 161 and resistor 162 and a negative feedback resistor is connected between the output of the operational amplifier 155 and the inverting input thereof for stabilizing the gain of the operational amplifier 155. It should be appreciated that the output from the limiter circuit 138 is substantially identical to the output from the limiter circuit 40 of Figure 9. In other words, the output signal from the limiter circuit 138 which has been compressed in the compression circuit 137 is limited in level by the limiter circuit 138. The output from the limiter circuit 138 is supplied through a resistor 156 to the inverting input of an operation amplifier 157.

The second transmission path comprises a resistor 134 supplied with the output from the pre-emphasis circuit 132 and providing a signal having a substantially flat pass characteristic, that is, the information signal with substantially unity gain, which is also supplied to the inverting input of the operational amplifier 157. Thus, the second transmission path comprising the resistor 134 operates in a substantially identical manner to the second transmission path of Figure 9 comprising the resistor 43. The first and second transmission paths are connected in parallel with each other and the respective signals therefrom are added at the input of the operational amplifier 157 in much the same manner as previously described for the adder amplifier 42 of Figure 9. The operational amplifier 157 further has a resistor connected between the output and inverting input thereof for stabilizing the gain of the operational amplifier 157. The added signal is inverted by the operational amplifier 157 and supplied to the inverting input of an operational amplifier 159 through a resistor 158.

The third transmission path comprises a high pass filter 133 supplied with the output from the pre-emphasis circuit 132. The high pass filter 133 tranmits the high frequency components of the pre-emphasized signal to the inverting input of the operational amplifier 159. It should therefore be appreciated that, since the added signal from the first and second transmission paths is inverted by the operational amplifier 157, this added signal is subtracted from the transmitted signal from the high pass filter 133 at the inverting input of the operational amplifier 159. The resulting signal is further inverted by the operational amplifier 159 and supplied to the output terminal 131*b* of the encoder circuit 130. A negative feedback resistor is connected between the output and input terminals of the operational amplifier 159 for stabilizing the gain thereof.

In other words, as shown in Figure 22, the output from the pre-emphasis circuit 132 is supplied through a first transmission path comprising the compression circuit 137 and the limiter circuit 138 and through a second transmission path comprising the resistor 134, and the output signals from the first and second transmission paths are added in an adding circuit 139 to produce an added output signal. Moreover, the pre-emphasized signal from the pre-emphasis circuit 132 is supplied through a third transmission path comprising the high pass filter 133 where it is effectively subtracted from the added output signal from the adding circuit 139 in a second adding circuit 140 and the resultant signal is supplied to the output terminal 131*b*. It should be realised that the use of an adding circuit 140 in Figure 22 in which the signal from the third transmission path is supplied to a negative input thereof and the combined signal from the first and second transmission

paths is supplied to a positive input thereof is equivalent to the circuit of Figure 21 comprising the amplifiers 157 and 159.

As a result of the arrangement of the circuit of Figure 21, a frequency characteristic, as illustrated in Figure 23, is obtained. In particular, when the input information signal supplied to the input terminal 131*a* is of a relatively high value, the gain of the first and second transmission paths comprising the compression circuit 137 and the resistor 134, respectively, is only slightly greater than the gain of the third transmission path comprising the high pass filter 133. However, when the input information signal is of a relatively high level, the addition of the signals from the first and second transmission paths has a relatively flat characteristic due to the predominance of the second transmission path over the first transmission path. Since the pre-emphasis circuit 132 pre-emphasizes the high frequency components of the information signal, the resulting signal through the second transmission path, that is, through the resistor 134, has the high frequency components thereof emphasized. The third transmission path comprising the high pass filter 133 only passes the high frequency components of the pre-emphasized information signal and the output from the high pass filter 133 is effectively subtracted from the information signal transmittted through the resistor 134 which also has the high frequency components of the signal pre-emphasized. The resulting signal at the output terminal 131*b* therefore has a substantially flat frequency characteristic as shown by the 0 dB input level on Figure 23.

In compression, when the level of the input information signal is of a relatively low value, the gain across the first and second transmission paths is more than 30 dB greater than the gain across the third transmission path so that the signal from the high pass filter 133 can effectively be ignored. At low signal levels, the first transmission path comprising the compression circuit 137 and the limiter circuit 138 predominates over the second transmission path comprising the resistor 134, so that the signal supplied to the output terminal 131*b* has its level compressed as a result of the compression circuit 137 and the high frequency components pre-emphasized as a result of the pre-emphasis circuit 132 as shown, for example, by the —60 dB input level in Figure 23. This result is required in the embodiments and has the effect of improving the signal-to-noise ratio of the information signal. Since back-ground noise is more predominant at low input levels than at high input levels and since background noise is of a relatively high frequency, the low level, high frequency components of the information signal are emphasized in comparison to the low level, low frequency components as shown, for example, at the —60 dB input level in Figure 23. This results in the low level, high frequency components providing a relatively high-signal-to-noise ratio when recorded on a magnetic tape.

It should be appreciated that the first and second transmission paths of Figure 21 operate in a substantially identical manner to the encoder circuit 30 of Figure 9. Thus, for example, the first transmission path comprising the compression circuit 137 and the limiter circuit 138 has an input-output characteristic as shown by the solid lines in Figure 24 for frequencies of 1KHz, 5KHz and 10KHz, in each of which the bent-linear input-output characteristic shown therein is largely dependent on the non-linear characteristic of the non-linear circuit 145. In addition, the second transmission path provides a substantially flat pass characteristic which transmits the information signal with substantially unity gain as shown by the dot-dash line in Figure 24.

Referring now to Figure 25, there is shown one particular circuit arrangement that may be used as the non-linear circuit 145. In the circuit 145 of Figure 25, a level detected *dc* voltage from the level detecting circuit 144 (Figure 21) is supplied through an input terminal 165 to the non-inverting input of an operational amplifier 166, the output of which is connected to the bases of NPN transistors 167 and 168, to the collector of the transistor 168 and to the inverting input of an operational amplifier 170 through a resistor 169. The collector of the transistor 167 is supplied with a voltage from a voltage source and the emitter thereof is connected to ground through a resistor 171 and to the inverting input of the operational amplifier 166. The emitter of the transistor 168 is connected to ground through a resistor 172 and to the inverting input of the operational amplifier 170 through a resistor 173. Moreover, the non-inverting input of the operational amplifier 170 is connected to ground through a resistor and a negative feedback resistor 174 connects the output of the operation amplifier 170 to the inverting input thereof.

Thus, when the level of the detected output signal supplied to the input terminal 165 is less than a predetermined value, the transistors 167 and 168 are rendered inoperative so that the output of the operational amplifier 166 is supplied to the inverting input of the operational amplifier 170 through the resistor 169 only. However, when the level of the signal supplied to the input terminal 165 is greater than the predetermined value, the transistors 167 and 168 are turned ON and the output from the operational amplifier 166 is supplied to the inverting input of the operational amplifier 170 through the parallel combination of the resistors 169 and 173 so as to vary the gain of the variable gain amplifier 135. As a result of such operation, a bent-linear input-output characteristic as shown in Figure 26 is obtained. It should be appreciated that, as a result of the inverting nature of the operational amplifier 170, the bent-linear input-output characteristic of Figure 26 is inverted with respect to the input-output characteristic shown in Figure 10. However, the characteristic of Figure 26 may be inverted to correspond to the characteristic of

Figure 10 by arranging the operational amplifier 170 to provide the resultant output signal at an output terminal 175 of the non-linear circuit 145 in non-inverted form.

As previously discussed with regard to Figure 9, and as applied to Figure 21, the limiter circuit 138 limits the output level of the compression circuit 137 without affecting the input-output characteristic of the compression circuit 137. Therefore, the input-output characteristic for the first and second transmission paths can be represented by the solid line curves of Figure 27 for frequencies of 1KHz, 5KHz and 10KHz. The resultant input-output characteristic between the input terminal 131*a* and the output terminal 131*b* of the encoder circuit 130 as a result of all three transmission paths can be obtained, as shown by the corresponding broken lines of Figure 27 by subtracting the output from the third transmission path from the output from the first and second transmission paths. Thus, as the level of the information signal in the high frequency range increases, the level of the output signal at the output terminal 131*b* also increases but at a decreasing rate.

Referring now to Figure 28, there is shown a second decoder circuit 180 of an embodiment of the invention which provides a complementary characteristic to the encoder circuit 130 of Figure 21. In other words, the decoder circuit 180 acts to restore the encoded signal to its original state. As shown therein, the decoder circuit 180 includes three transmission paths, that is, a first transmission path comprising an expansion circuit 187 and a limiter or coring circuit 188, a second transmission path comprising a resistor 184 in parallel with the first transmission path and a third transmission path comprising a high pass filter 183.

The encoded signal at the input terminal 181*a* of the decoder circuit 180 is supplied to the inverting input of an operational amplifier 191 through a resistor. The output from the operational amplifier 191 is supplied to the first transmission path which comprises the limiter circuit 188 followed by an expansion circuit 187. The limiter circuit 188 includes an operational amplifier 355 having an inverting input thereof supplied with the output from the operational amplifier 191. The non-inverting input of the operational amplifier 355 is connected to ground through a capacitor 361 and resistor 362. The output from the operational amplifier 355 is supplied to the inverting input of another operational amplifier 347 through a resistor 348 and also through a series combination of a capacitor 349 and a resistor 350 in which the latter series combination is in parallel with the resistor 348. A resistor 351, a first diode 352 and a second diode 353 are connected in parallel with each other and are each connected between the inverting input and output terminals of the operational amplifier 347, with the diodes 352 and 353 being arranged in opposing relation. The output of the operational amplifier 347 is supplied to the non-inverting input of the operational amplifier 355 through a resistor 354.

It should be appreciated that the coring function of the limiter circuit 188 can be obtained by utilizing the principles of the negative feedback loop of Figure 20. In other words, the limiter circuit 138 of Figure 21 may be transformed into a negative feedback loop by supplying the output of the operational amplifier 191 to the inverting input of the operational amplifier 155 and supplying the output from the operational amplifier 155 to the inverting input of the operational amplifier 147 through the resistor 148 which is in parallel with the series combination of the capacitor 149 and the resistor 150. This result may be attained by a relatively simple switching mechanism (not shown).

The expansion circuit 187 of the first transmission path is shown to include an operational amplifier 185 supplied at its inverting input with the output from the operational amplifier 355 through a resistor 341. The output from the operational amplifier 355 is also supplied to a weighting circuit 343 through the resistor 341 and the output of the weighting circuit 343 is supplied to a level detecting circuit 344. A non-linear circuit 345 receives the detected output signal from the level detecting circuit 344 and supplies a control voltage through an inverter 189 to a light emitting element (not shown), such as a light emitting diode. The light emitting element transmits light to a negative feedback resistor 342 connected between the output and inverting input terminals of the operational amplifier 185 and which may be a CdS photoconductive cell having a resistance value which varies when irradiated by light from the light emitting element. The constructions of the weighting circuit 343, the level detecting circuit 344, and the non-linear circuit 345 are substantially identical to their respective counterpart circuits in Figure 21. It should, therefore, be appreciated, that, as the resistance value of negative feedback resistor 342 changes, the gain of the operational amplifier 185 and consequently, of the expansion circuit 187, also changes. It should further be appreciated that the input-output characteristic of the first transmission path comprising the limiter circuit 188 and the expansion circuit 187 is the inverse or reciprocal of the input-output characteristic of the first transmission path of Figure 21.

The output from the expansion circuit 187 is supplied through the second transmission path comprising the resistor 184 to the inverting input of the operational amplifier 191. Moreover, the output from the expansion circuit 187 is supplied to the inverting input of an operational amplifier 192 through a resistor and the inverted output signal from the operational amplifier 192 is supplied to the inverting input of the operational amplifier 191 through the third transmission path comprising the high pass filter 183 having a frequency characteristic substantially identical to

the frequency characteristic of the high pass filter 133 of Figure 21.

In other words, as illustrated in Figure 29, the encoded signal from the input terminal 181*a* is effectively added in an adding circuit 190 to the output of the second transmission path comprising a resistor 184 which supplies a substantially flat pass characteristic and to the output of the high pass filter 183 of the third transmission path. The added signals are supplied to the inverting input of the operational amplifier 191 which performs an inverting function and the inverted signals are then supplied to the first transmission path, and, more particularly, to the limiter circuit 188 and the expansion circuit 187 thereof. The output from the expansion circuit 187 is inverted by the operational amplifier 192 and supplied to the de-emphasis circuit 182 which de-emphasizes the high frequency components of the signal supplied thereto in a manner substantially complementary to the pre-emphasis circuit 132 of Figure 21 so as to restore the information signal to its original form whereby it is supplied to the output terminal 181*b* of the decoder circuit 180.

The basic relationship between the encoder circuit 130 (Figure 21) and the decoder circuit 180 (Figure 28) will now be discussed in relation to Figures 30 and 31, with Figure 30 corresponding to the encoder circuit 130 and Figure 31 corresponding to the decoder circuit 180. As shown in Figure 30, an encoder circuit 200 is supplied at its input terminal 205 with an information signal *x*. The information signal *x* is supplied to respective adding inputs of an adding circuit 204 through a first transmission path 203 having a transmission function γ and through a second transmission path 202 having a transmission function β in which the first transmission path 203 corresponds to the first transmission path of Figure 21 comprising the compression circuit 137 and the limiter circuit 138 and the second transmission path 202 corresponds to the second transmission path of Figure 21 comprising the resistor 134. The input information signal *x* is also supplied to a subtracting input of the adding circuit 204 through a third transmission path 201 having a transmission function α and which corresponds to the third transmission path of Figure 21 comprising the high pass filter 133. Accordingly, the encoded output signal *y* of the decoder circuit 200 at output terminal 205′ thereof can be represented as follows:

$$y=(-\alpha+\beta+\alpha)x \qquad (17)$$

Referring now to Figure 31, there is shown a decoder circuit 210 having a complementary characteristic to the encoder circuit 200 for restoring encoded information signal *y* to its original form. The encoded information signal *y* is supplied through an input terminal 215 of the decoder circuit 210 to an adding input of an adding circuit 214 thereof. The output from the adding circuit 214 is supplied through a first transmission path 213 having a transmission function $1/\gamma$ which is the reciprocal or inverse of the characteristic of the first transmission path 203 of the encoder circuit 200. The output from the first transmission path 213 is supplied to a subtracting input of the adding circuit 214 through a second transmission path 212 having a transmission function β and to a second adding input of the adding circuit 214 through a third transmission path 211 having a transmission function α. It should be appreciated that the first, second and third transmission paths 213, 212 and 211 of the decoder circuit 210 correspond to the first, second and third transmission paths of the decoder circuit 180 of Figure 28. It is to be noted that the second transmission path 212 which comprises the resistor 184 is connected to the subtracting input of the adding circuit 214. This results because the encoded signal from the input terminal 181*a* in Figure 28 is supplied through three inverting operational amplifiers 191, 355 and 185 to supply an inverted signal through the resistor 184. In like manner, the third transmission path 211 provides a signal to the adding input of the adding circuit 214 since the signal supplied through the high pass filter 183 from the input terminal 181*a* is transmitted through four inverting operational amplifiers 191, 355, 185 and 192. The decoded output signal *z* is supplied to an output terminal 216 of the decoder circuit 210 from the first transmission path 213 and can be represented as follows:

$$z=\frac{1}{\gamma}y+(\alpha-\beta)z \qquad (18)$$

Equation (18) can be rearranged as follows:

$$\gamma z=y+(\alpha-\beta)z$$

$$(-\alpha+\beta+\gamma)z=y \qquad (19)$$

When equations (17) and (19) are combined, as follows:

$$(-\alpha+\beta+\gamma)x=(-\alpha+\beta+\gamma)z \qquad (20)$$

$$x=z \qquad (21)$$

it is seen that the original information signal is restored by the decoder circuit 210.

Claims

1. In apparatus for recording an information signal on a recording medium by a recording device, gain control means comprising:

means for defining a first transmission path for compressing said information signal;

means defining a second transmission path for transmitting said information signal with substantially unity gain; and

means for supplying the information signal to said recording device by way of said first path when the level of said information signal is below a predetermined value and for supplying said

information signal to said recording device by way of said second path with substantially unity gain when the level of said information signal is above said predetermined value.

2. Gain control means according to claim 1 wherein said means defining the first transmission path includes variable gain amplifier means having a gain which varies in response to a control signal supplied thereto and which compresses said information signal as a function of said information signal, and control means response to the compressed information signal from said variable gain amplifier means for producing said control signal.

3. Gain control means according to claim 2 wherein said variable gain amplifier means compresses said information signal in a logarithmic manner.

4. Gain control means according to claim 2 wherein said control means includes level detecting means for detecting the level of said compressed information signal from said variable gain amplifier means and for producing a detected output signal in response thereto, and non-linear means for producing said control signal in response to said detected output signal.

5. Gain control means according to claim 4 wherein said level detecting means includes means for logarithmically converting said compressed information signal from said variable gain amplifier means, and amplifier means for producing said detected output signal in response to the logarithmically converted signal.

6. Gain control means according to claim 4 wherein said non-linear means has an input-output level characteristic with a first linear gradient when the level of said detected output signal is less than second predetermined value corresponding to the first-mentioned predetermined value, and a second linear gradient greater than said first gradient when the level of said detected output signal is greater than said second predetermined value.

7. Gain control means according to claim 6 wherein said non-linear means includes first and second resistive elements forming a voltage divider for voltage dividing said detected output signal so as to produce said first linear gradient, and means for varying the resistance value of one of said resistive elements for changing the voltage dividing ratio of said voltage divider so as to produce said second linear gradient.

8. Gain control means according to claim 7 wherein said means for varying the resistance value includes a series circuit of a diode, means for reverse biasing said diode, and a third resistive element, and said series circuit is connected in parallel to said one resistive element.

9. Gain control means according to claim 2 wherein said means defining the first transmission path further includes limiter means for limiting said compressed information signal from said variable gain amplifier at two independent levels.

10. Gain control means according to claim 9 wherein said limiter means includes a diode limiter circuit having first and second diodes, each connected in parallel between the output of said variable gain amplifier means and a reference potential, and each being arranged in opposing relation to the other.

11. Gain control means according to claim 10 wherein said limiter means further includes a capacitive element connected between said reference potential and said first and second diodes for providing a second reference potential higher than said first mentioned reference potential for low frequency components of said information signal.

12. Gain control means according to claim 11 wherein said limiter means further includes a first resistive element connected between the output of said variable gain amplifier means and said first and second diodes and a series circuit of a capacitive element and a resistive element connected in parallel with said first resistive element so as to reduce the effective resistance between the output of said variable gain amplifier and said first and second diodes for high frequency components of said information signal.

13. Gain control means according to claim 9 wherein said limiter means includes at least one transistor having a collector-emitter path connected between the output of said variable gain amplifier means and a reference potential.

14. Gain control means according to claim 13 wherein said limiter means further includes another transistor connected between the output of said variable gain amplifer means and a reference potential, and a capacitive element connected between the output of said variable gain amplifier means said transistors for imparting a frequency dependency to said limiter means.

15. Gain control means according to claim 1 wherein said means defining the second transmission path includes a resistive element connected in parallel with said first transmission path.

16. Gain control means according to claim 15 further comprising amplifier means having an input supplied with the compressed information signal from said first transmission path and with said information signal with substantially unity gain from said second transmission path whereby said compressed information signal and said information signal with substantially unity gain are added at the input of said amplifier means.

17. Gain control means according to claim 16 further comprising pre-emphasis means connected to said first and second transmission paths for pre-emphasizing the high frequency components of said information signal.

18. Gain control means according to claim 17 further comprising means defining a third transmission path for de-emphasizing high level, high frequency components of the information signal whereby a substantially flat frequency characteristic is imparted by said apparatus to high level components of said information signal.

19. Gain control means according to claim 18

wherein said means defining a third transmission path includes high pass filter means for transmitting only high frequency components of said information signal, and means for subtracting said high frequency components of said information signal from the added signal produced by the addition of said compressed information signal and said information signal with substantially unity gain for high levels of said information signal.

20. In apparatus for reproducing an information signal from an encoded information signal which has been recorded on a recording medium with the information signal effectively compressed for levels thereof below a predetermined value and with the information signal effectively transmitted with substantially unity gain for levels thereof above said predetermined value; gain control means for reproducing said information signal from said encoded information signal, the gain control means comprising;

means defining a first transmission path for expanding said encoded information signal into an expanded signal; and

means defining a second transmission path for negatively feeding back said expanded signal to said first transmission path with substantially unity gain.

21. Gain control means according to claim 20 wherein said means defining a first transmission path includes variable gain amplifier means having a gain which varies in response to a control signal supplied thereto and which produces said expanded signal as a function of said encoded information signal, and control means responsive to said encoded information signal for producing said control signal.

22. Gain control means according to claim 21 wherein said variable gain amplifier means expands said encoded information signal in a logarithmic manner.

23. Gain control means according to claim 21 wherein said control means includes level detecting means for detecting the level of said encoded information signal and for producing a detected output signal in response thereto, non-linear means for producing an output signal in response to said detected output signal, and inverting means for producing said control signal in response to said output signal from said non-linear means.

24. Gain control means according to claim 23 wherein said non-linear means has an input-output level characteristic with a first linear gradient when the level of said detected output signal is less than a second predetermined value corresponding to the first-mentioned predetermined value, and with a second linear gradient when the level of said detected output signal is greater than said second predetermined value.

25. Gain control means according to claim 21 wherein said means defining a first transmission path further includes limiter means for coring said encoded information signal.

26. Gain control means according to claim 25 further comprising an input terminal; and wherein said limiter means includes first and second diodes connected in parallel and opposing relation between said input terminal and said variable gain amplifier means.

27. Gain control means according to claim 26 wherein said limiter means includes additional amplifier means having input and output terminals, said first and second diodes are connected in parallel between said input and output terminals of said amplifier means, a capacitive element connects said input terminal of the additional amplifier means to a reference potential, and a series circuit of a resistive element and another capacitive element is connected in parallel with another resistive element between the output terminal of said additional amplifier means and said first and second diodes for imparting a frequency characteristic to said limiter means.

28. Gain control means according to claim 20 wherein said means defining the second transmission path includes a feedback resistor for negatively feeding back said expanded signal to said first transmission path.

29. Gain control means according to claim 20 further comprising a de-emphasis circuit connected to said first and second transmission paths for de-emphasizing the high frequency components of said encoded information signal.

30. Gain control means according to claim 29 further comprising a third transmission path for positively feeding back the high frequency components of said expanded signal to said first transmission path.

31. Gain control means according to claim 1 and substantially as any one of the variants hereinbefore described with reference to the accompanying drawings.

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