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(54) **ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL**

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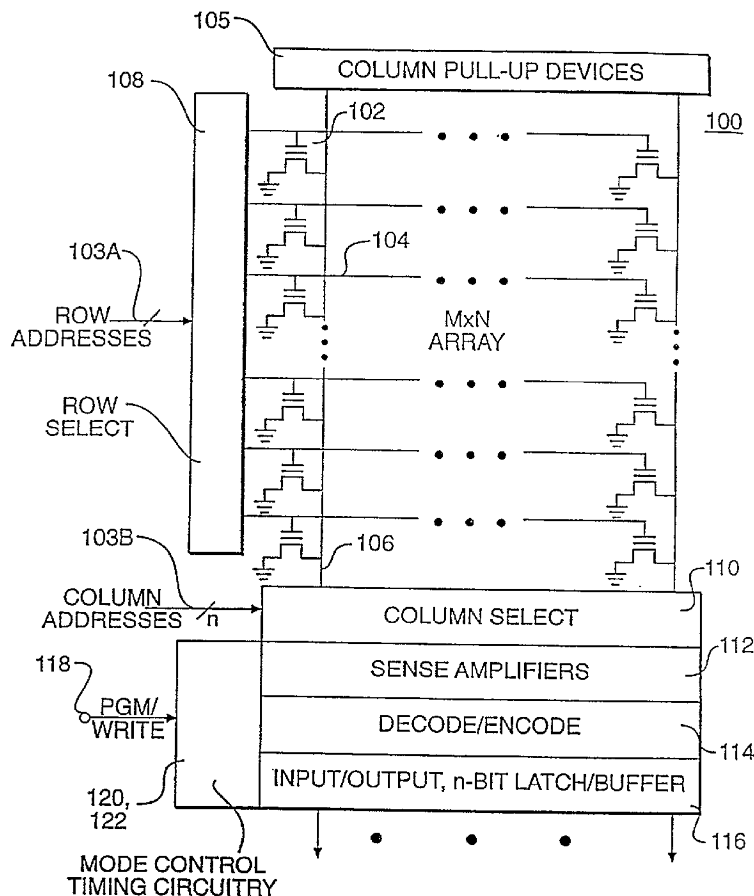
(52) **U.S. Cl.** **365/185.03**

(57) **ABSTRACT**

A multi-bit memory device with a memory cell means for storing input information for an indefinite period of time. The multi-bit memory means stores information in up to K^n memory states ($K^n>1$). A memory cell programming means and comparator means is also included. The present multi-bit memory device also includes a voltage divider arrangement with pull-up devices in a memory array to provide stable and accurate reference voltages over process, temperature, and voltage variations.



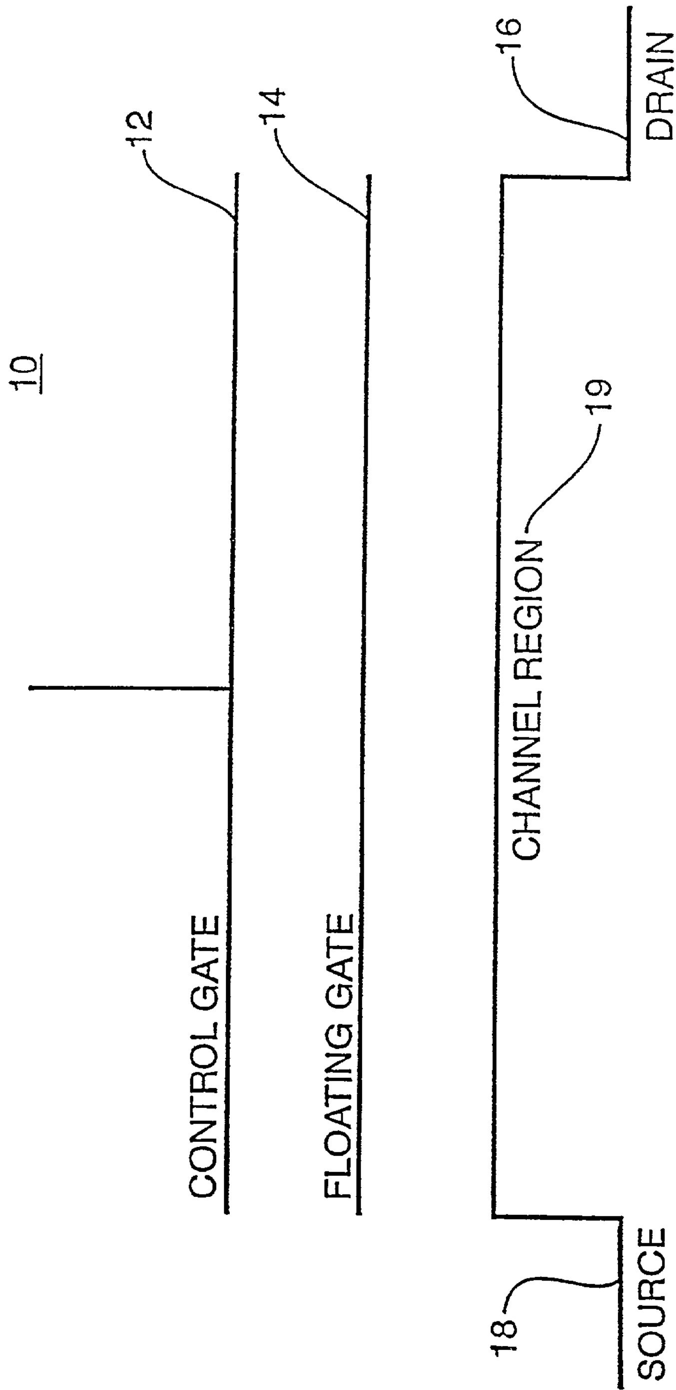


FIG. 1

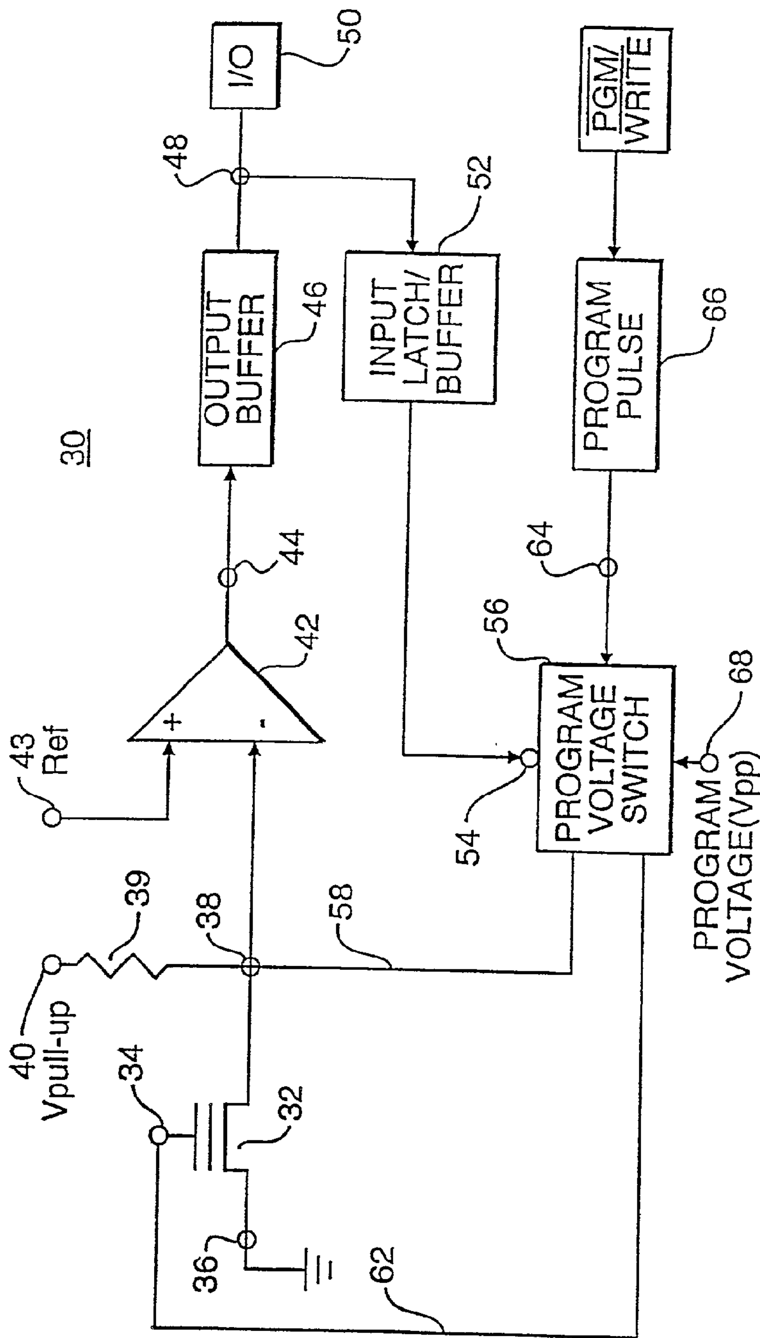


FIG. 2
PRIOR ART

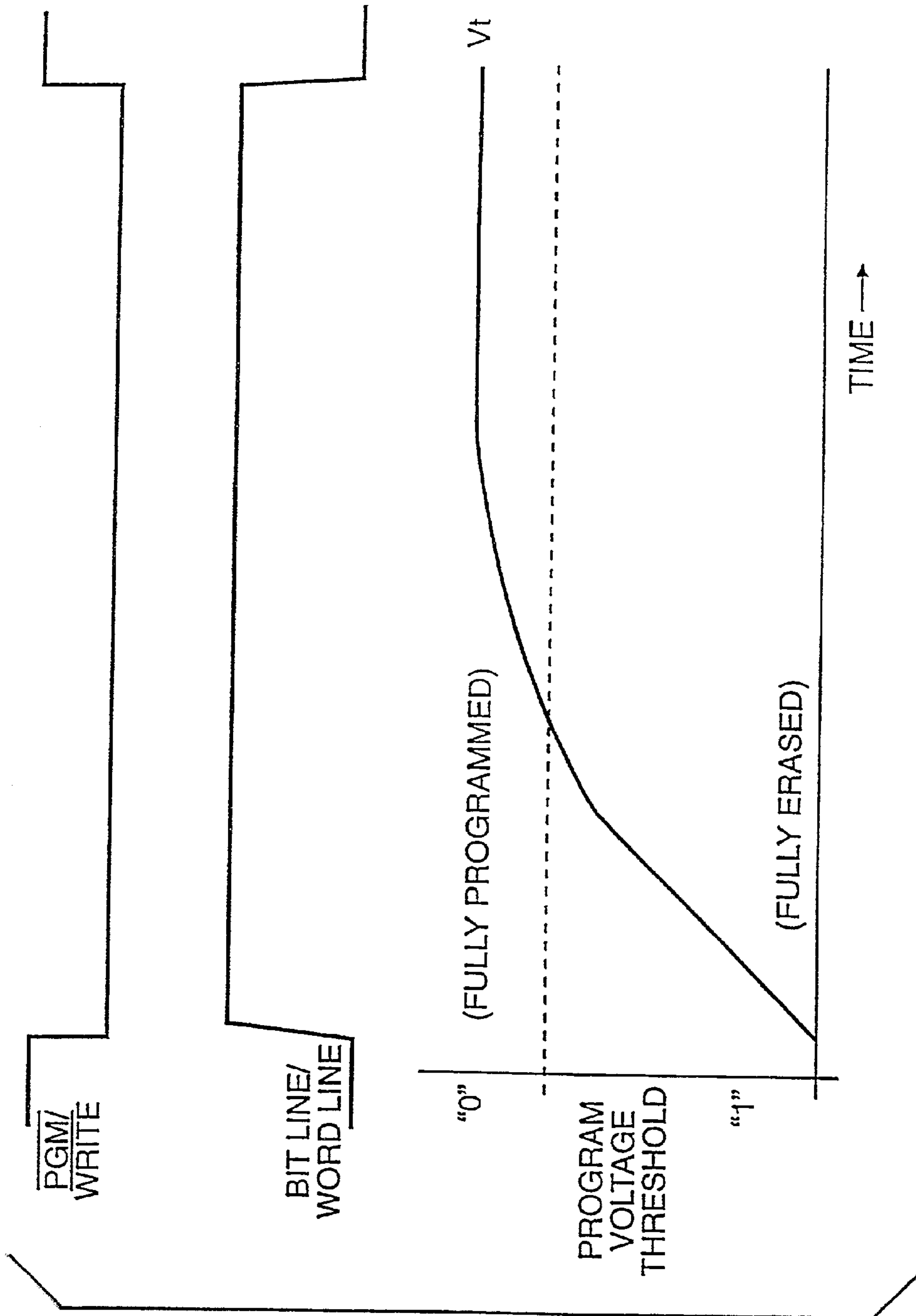


FIG. 3

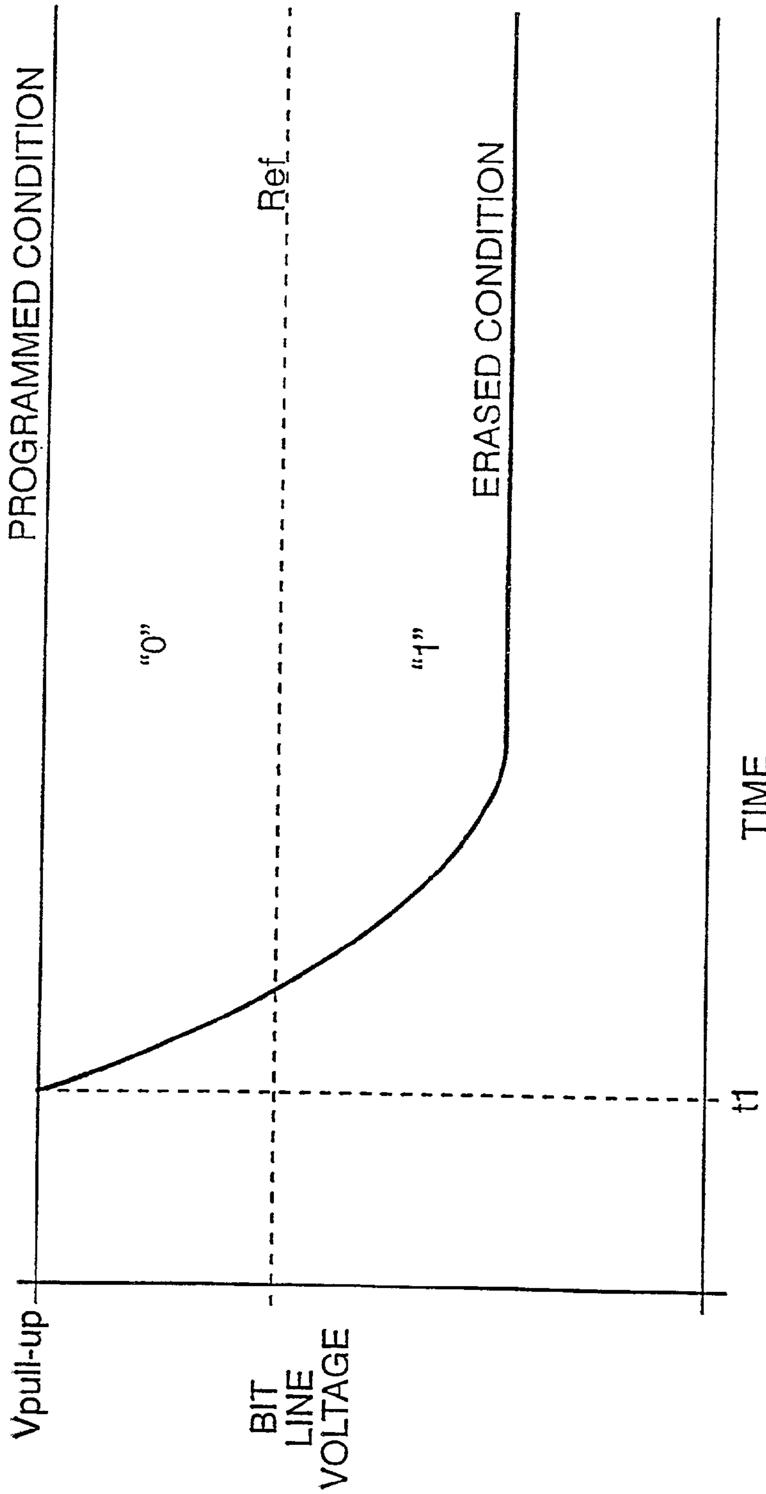


FIG. 4
PRIOR ART READ

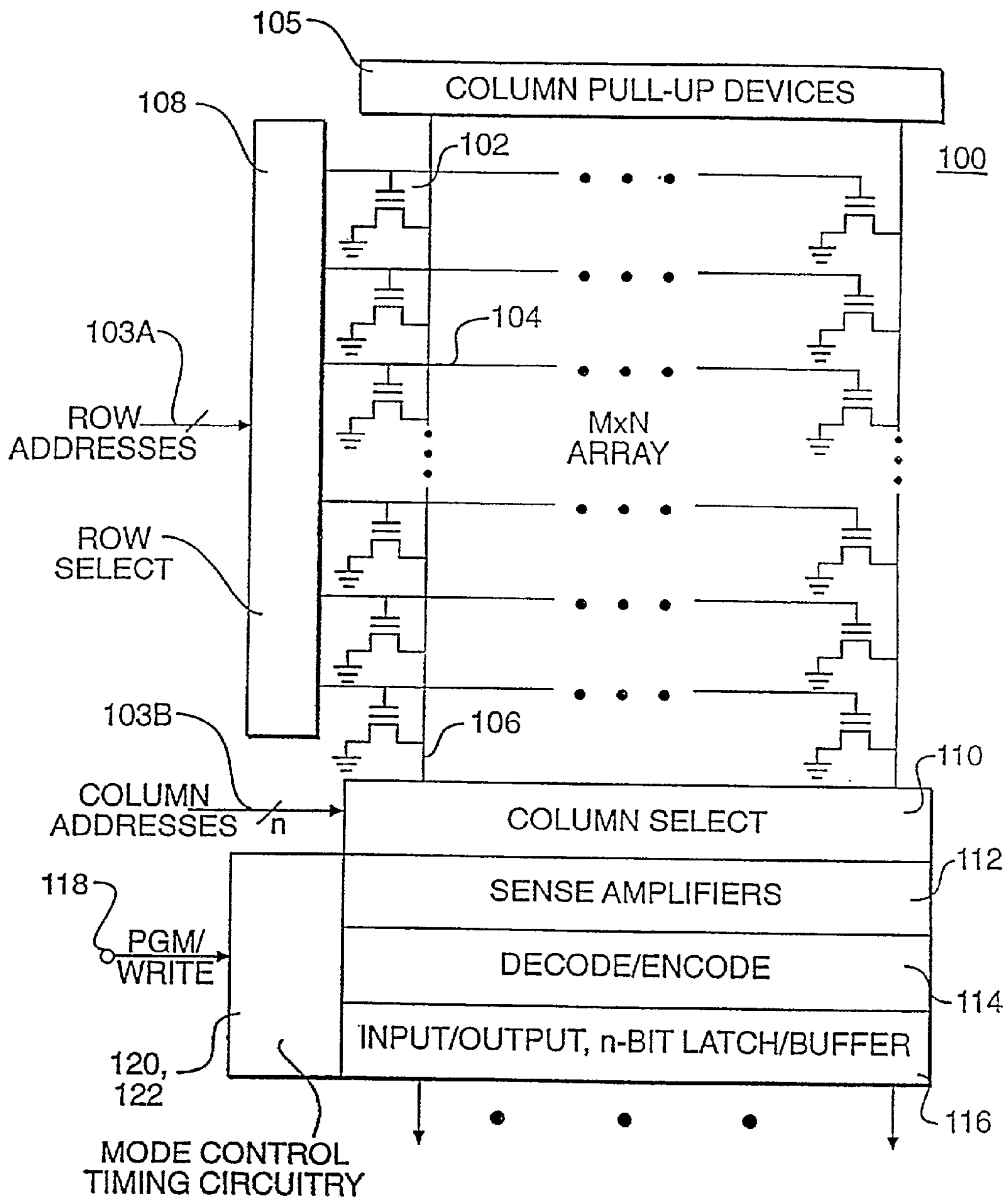


FIG. 5

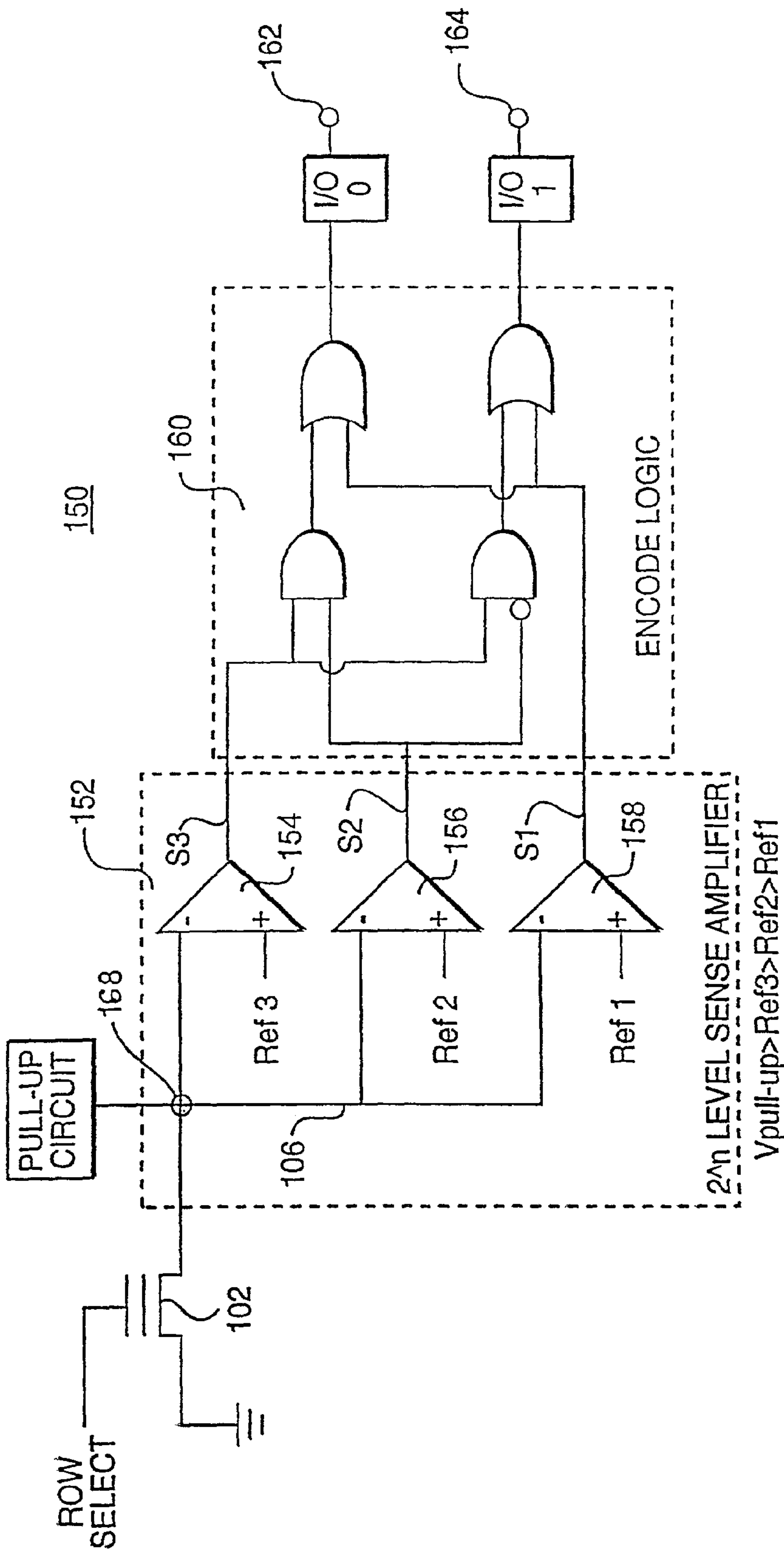


FIG. 6

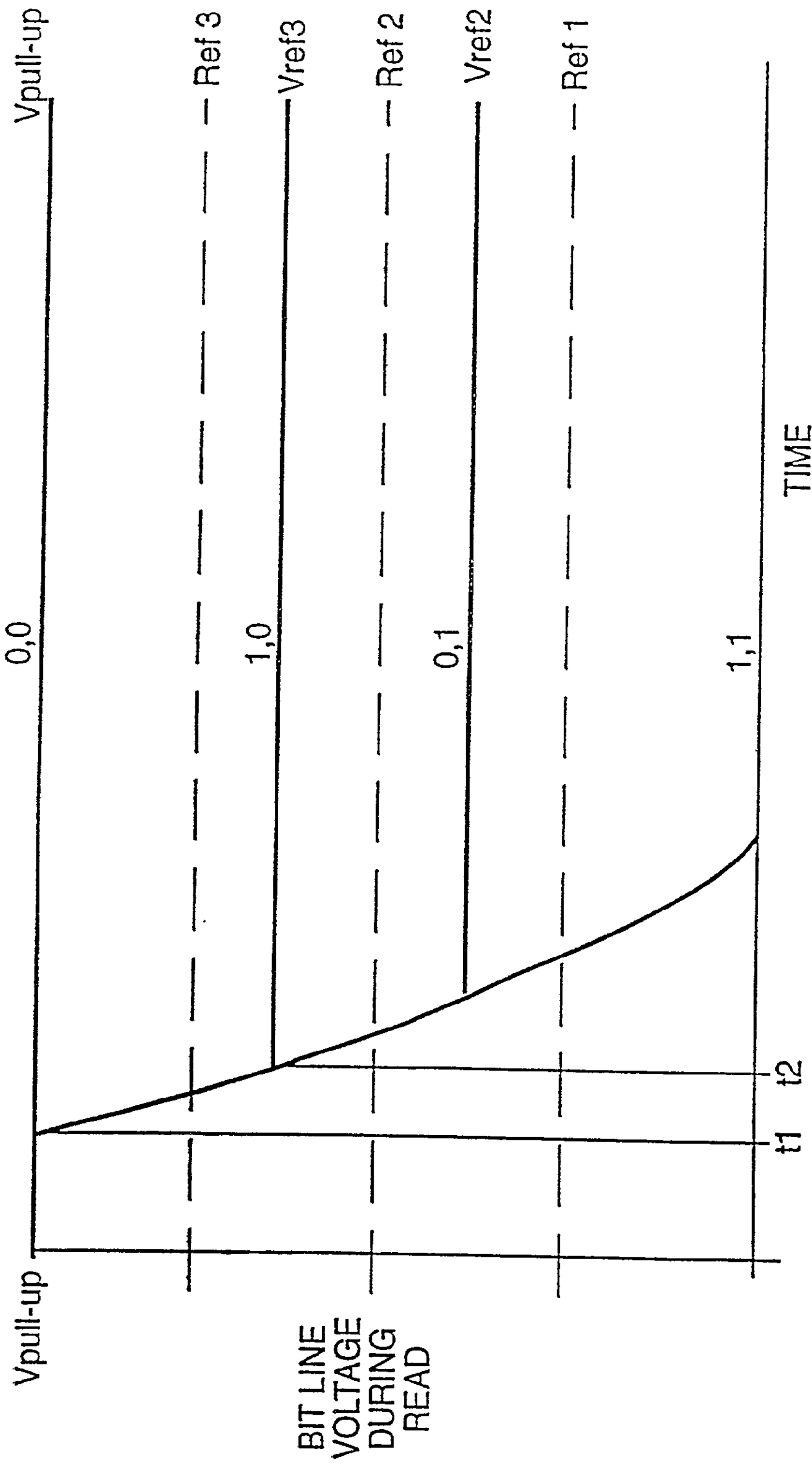


FIG. 7

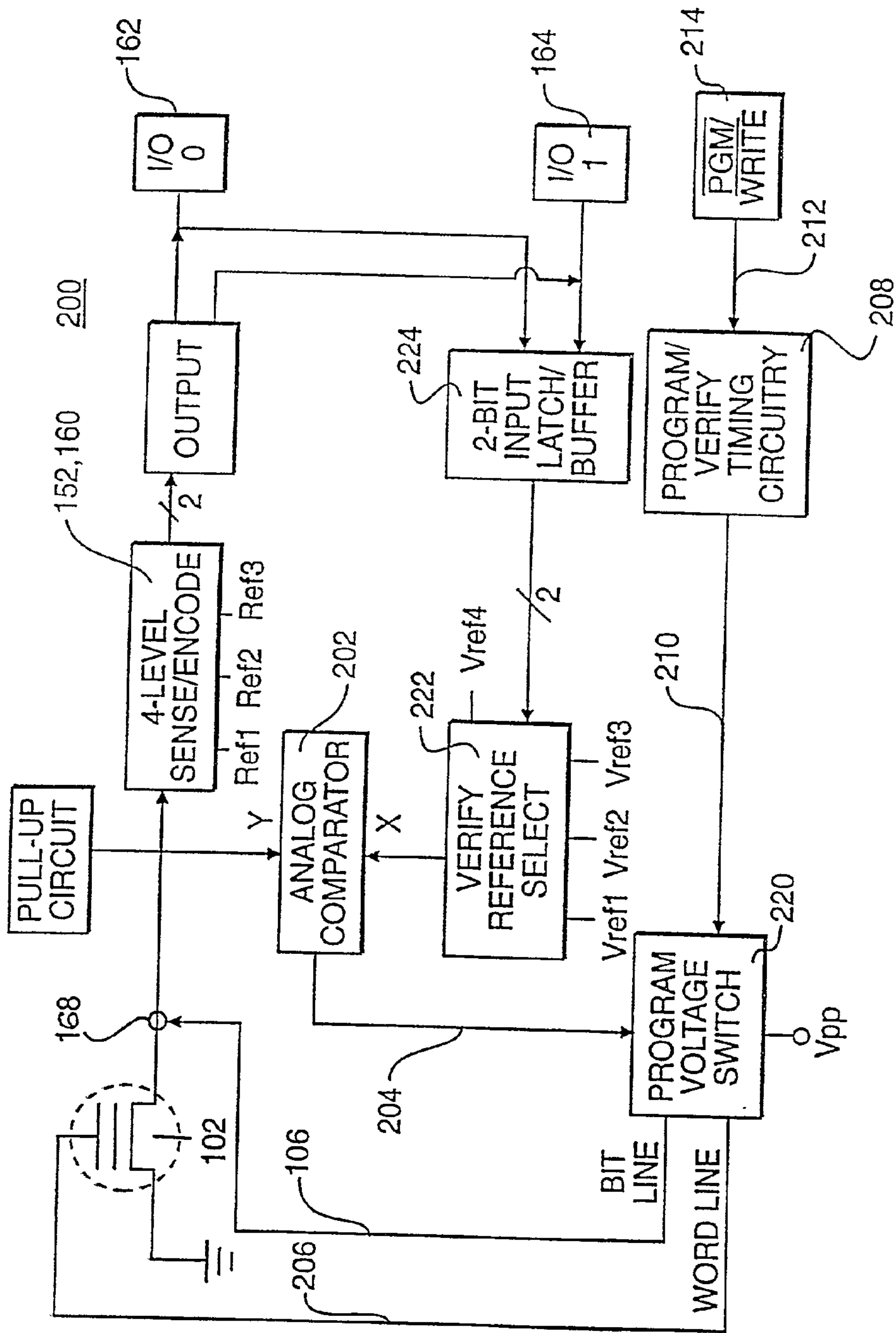


FIG. 8

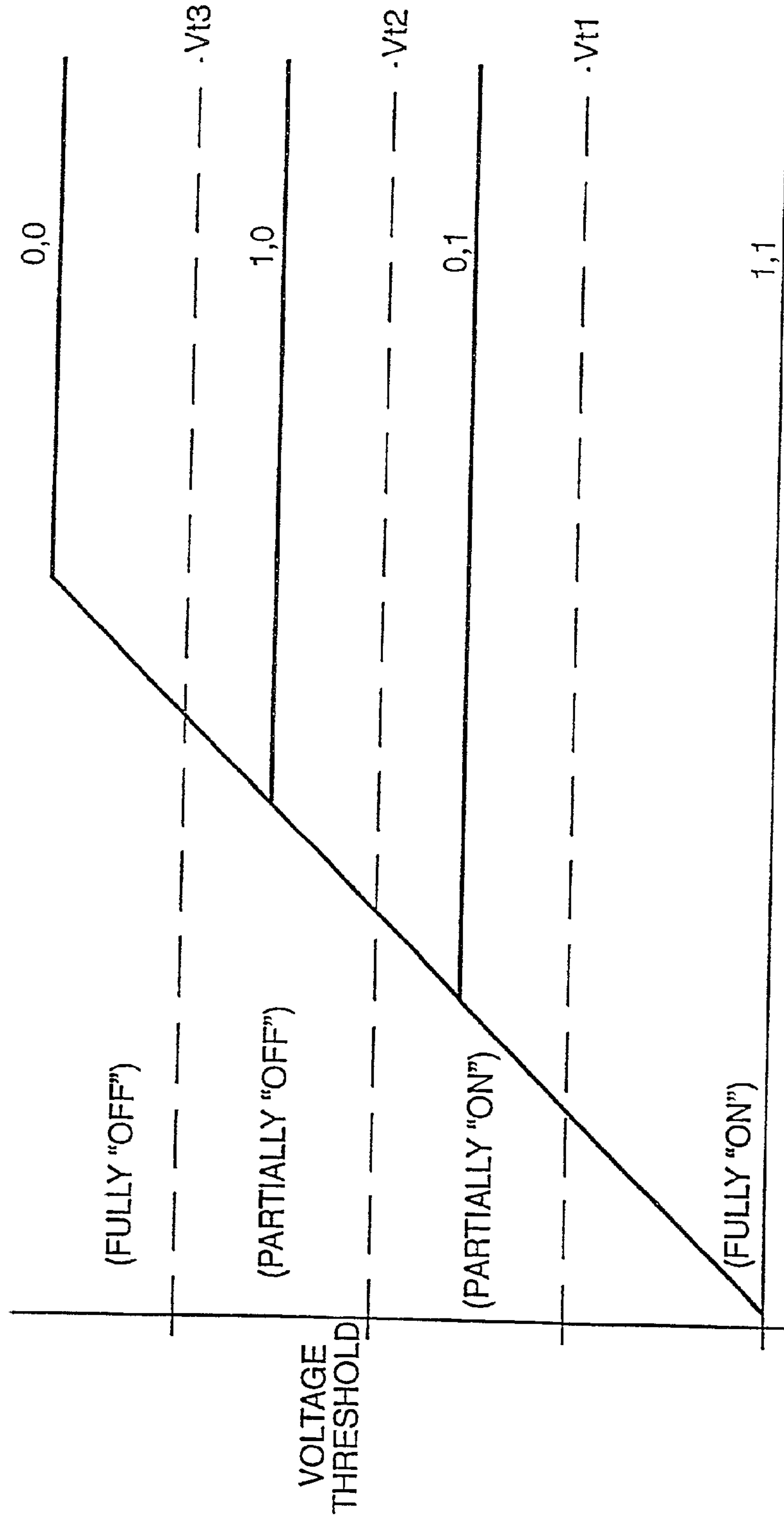


FIG. 9

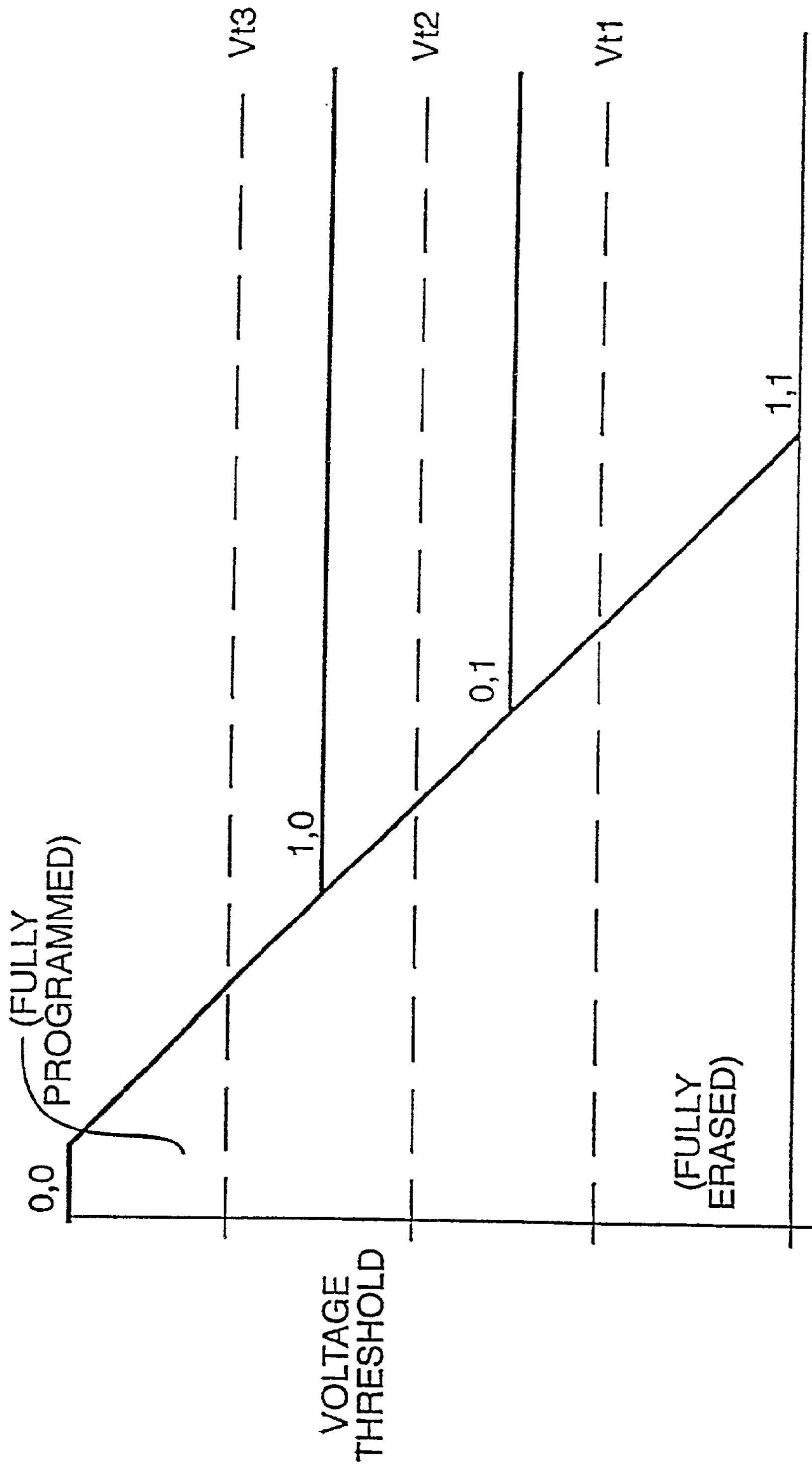


FIG. 10

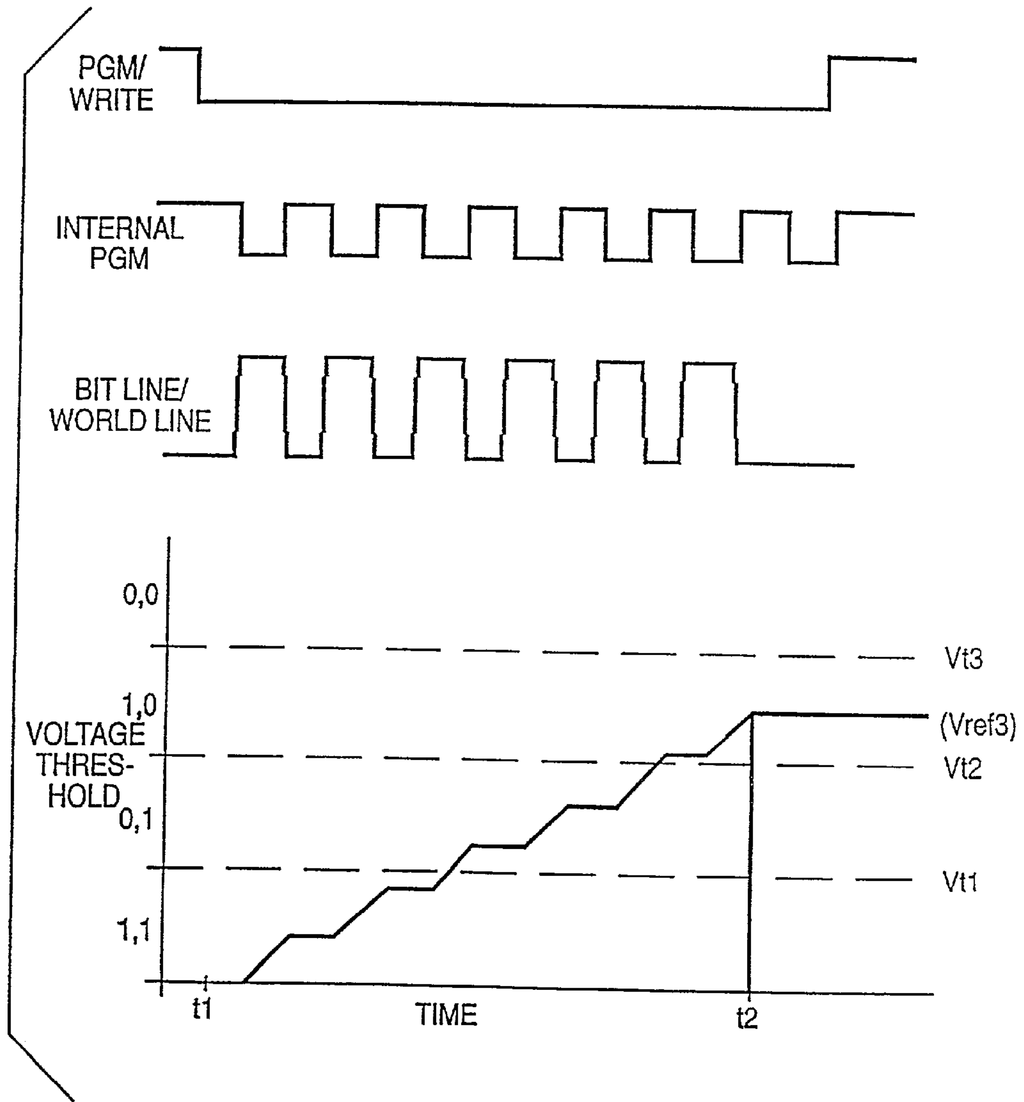


FIG. 11

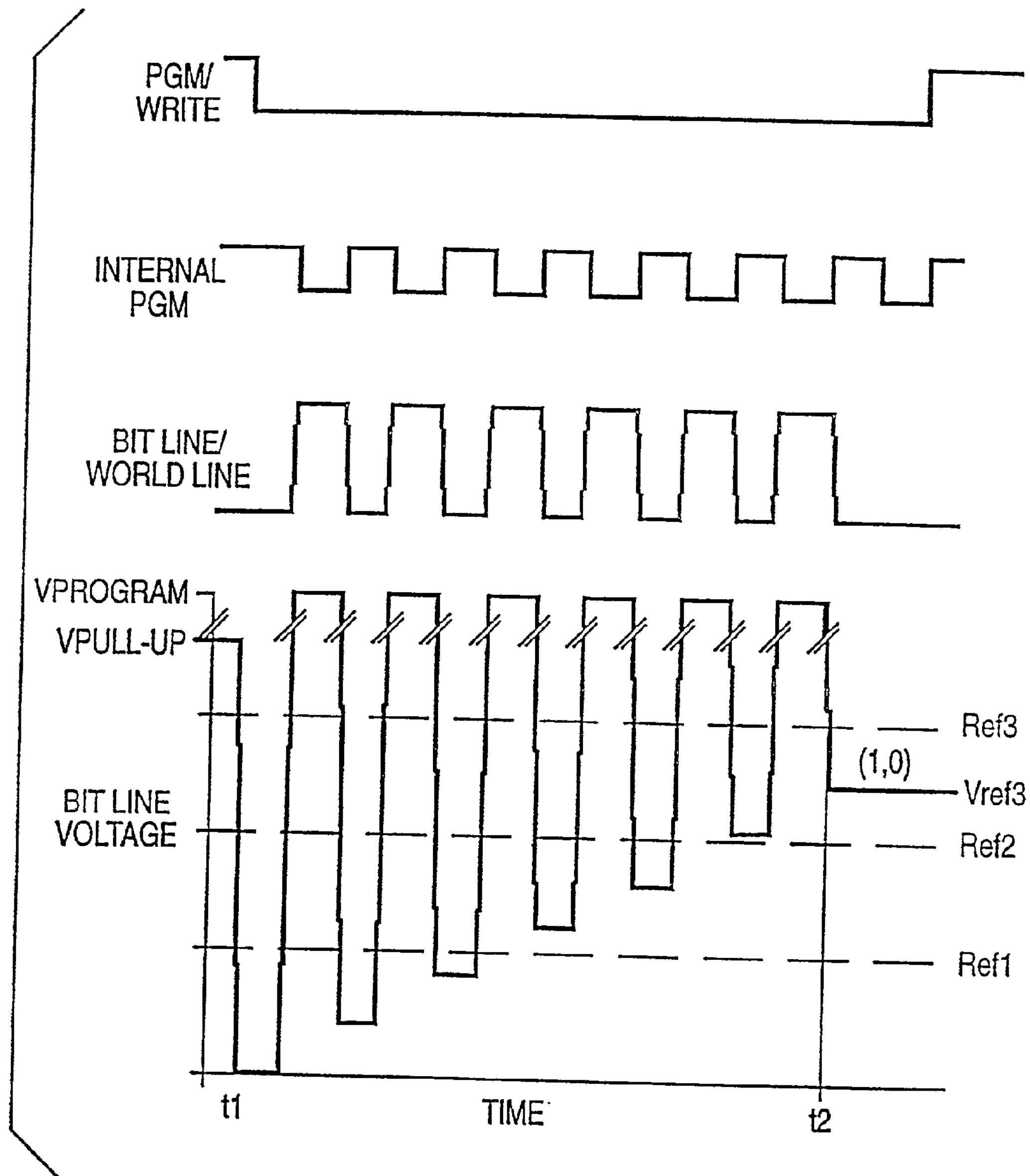


FIG. 12

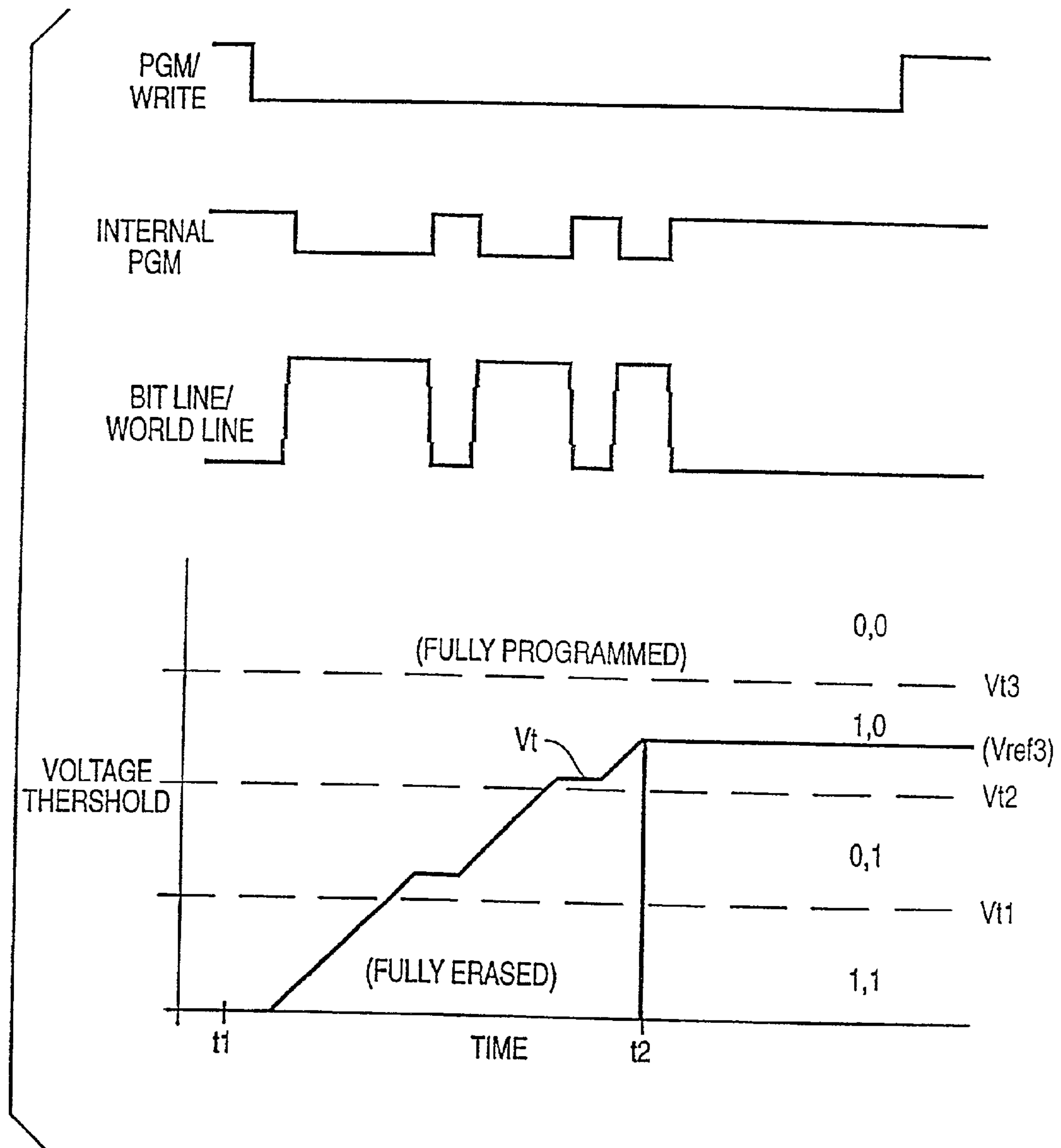


FIG. 13

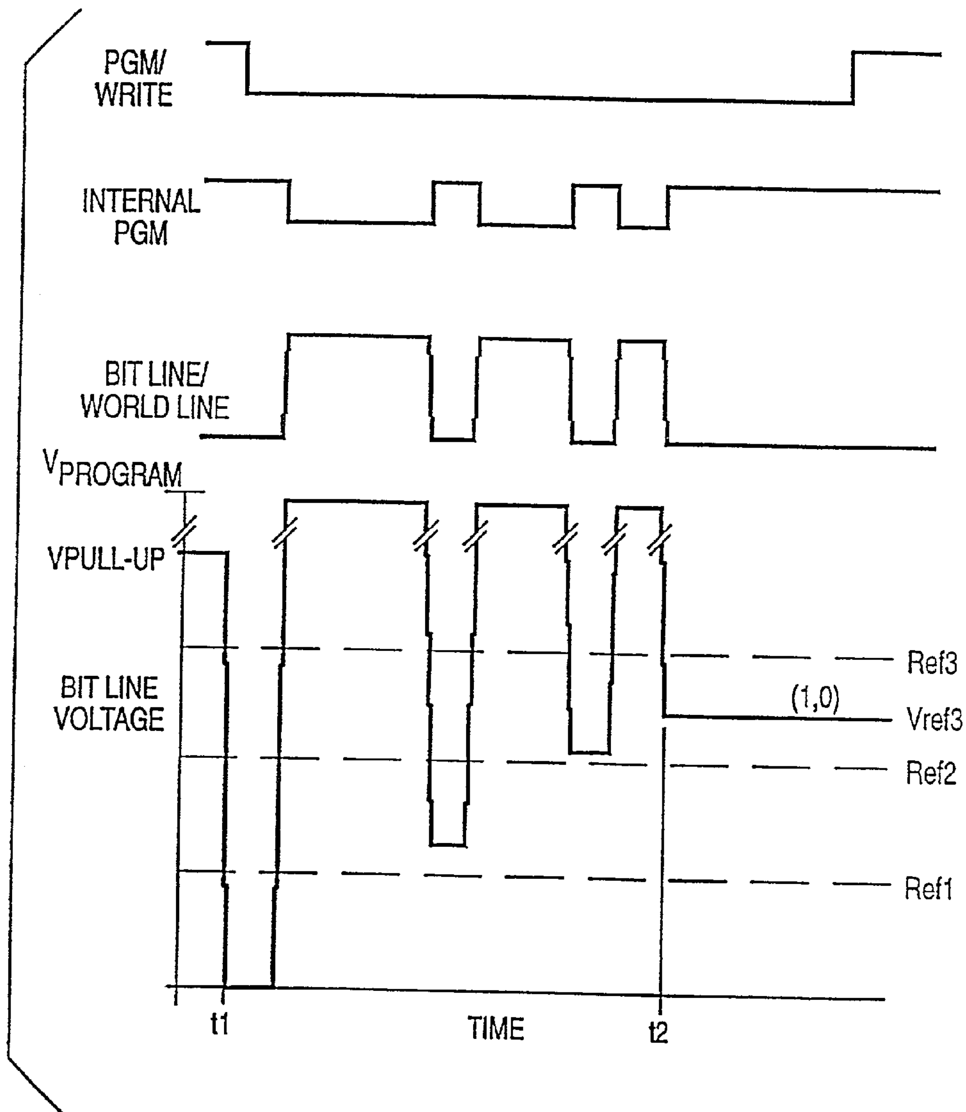


FIG. 14

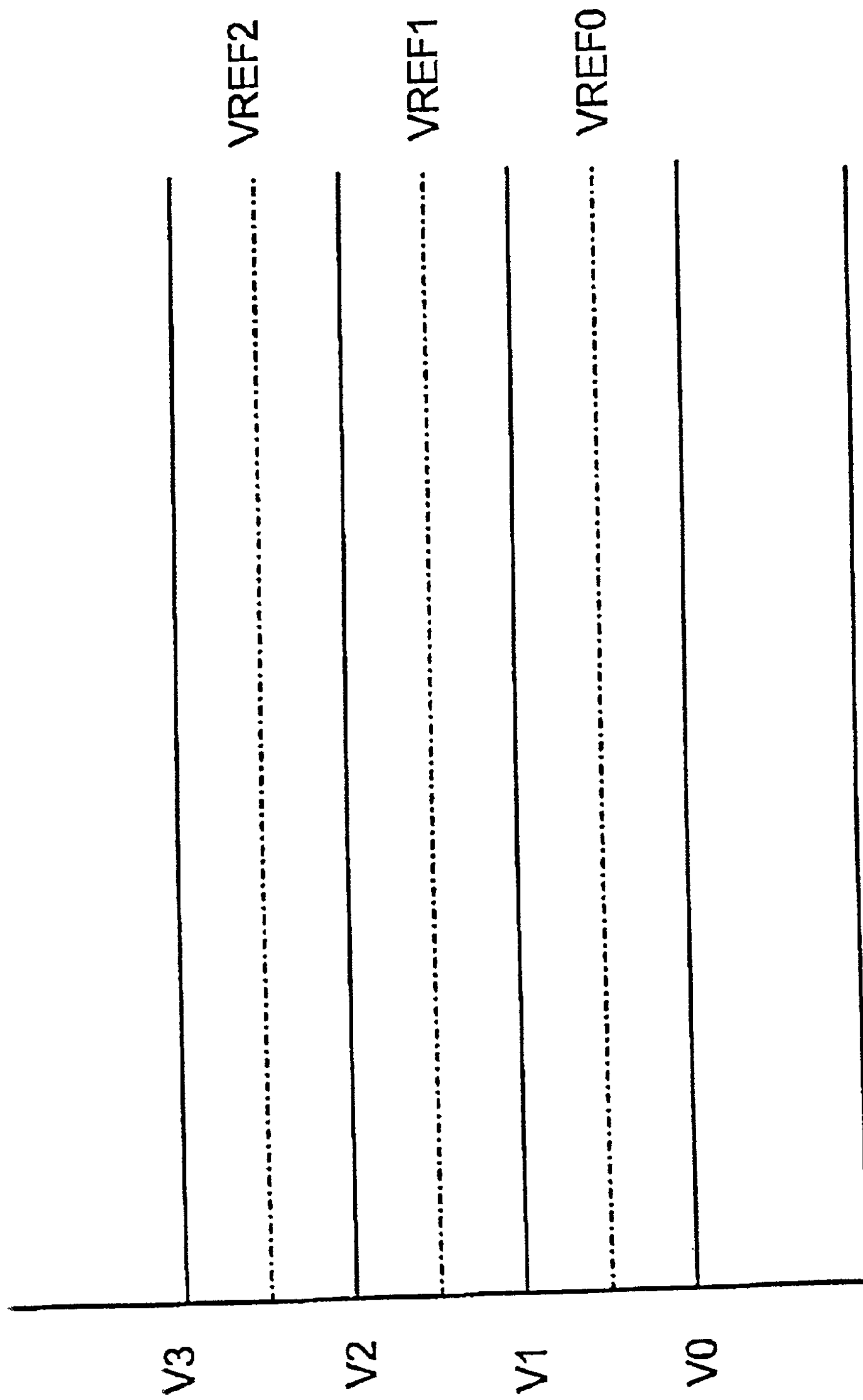


FIG. 15

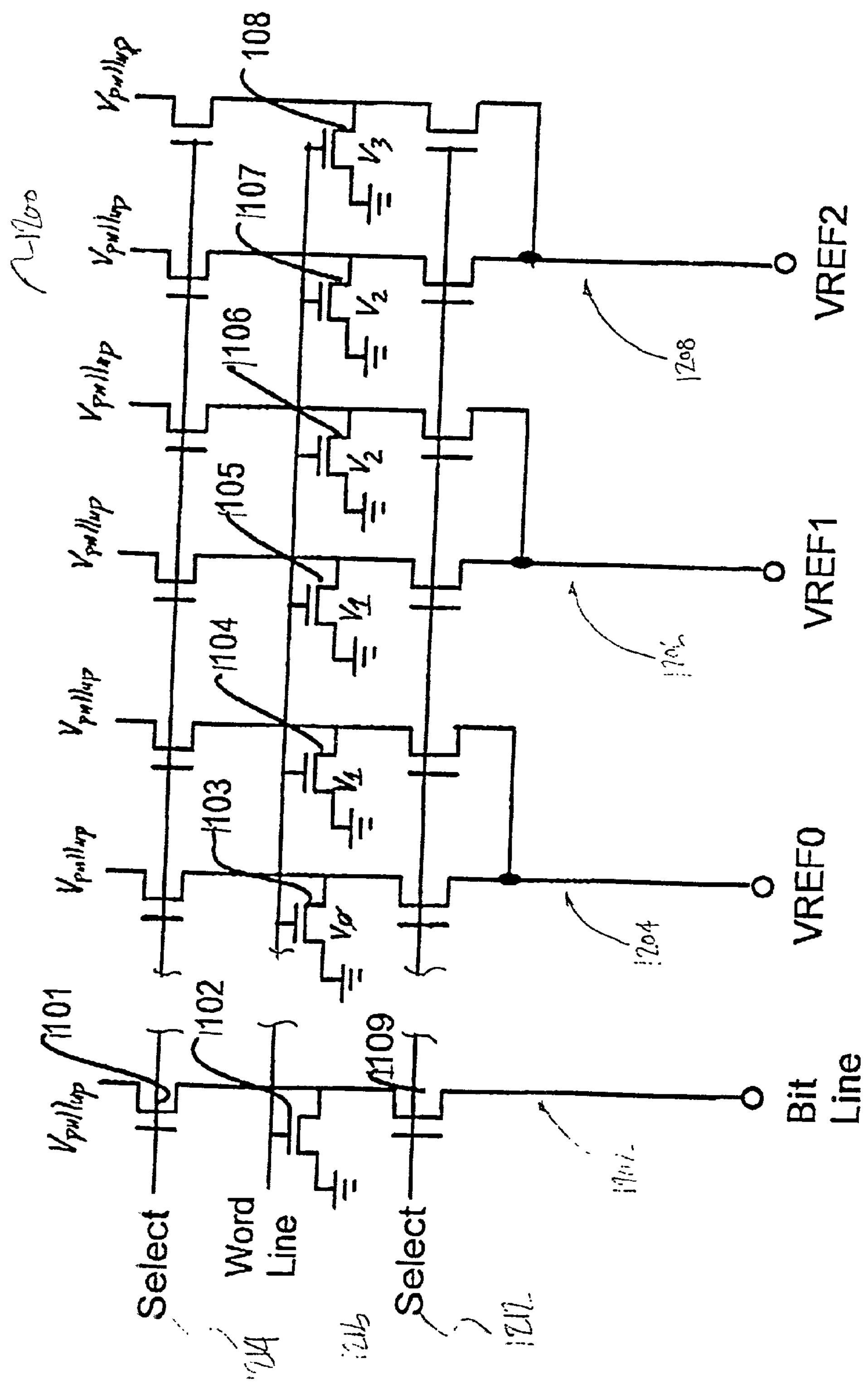


FIG. 16

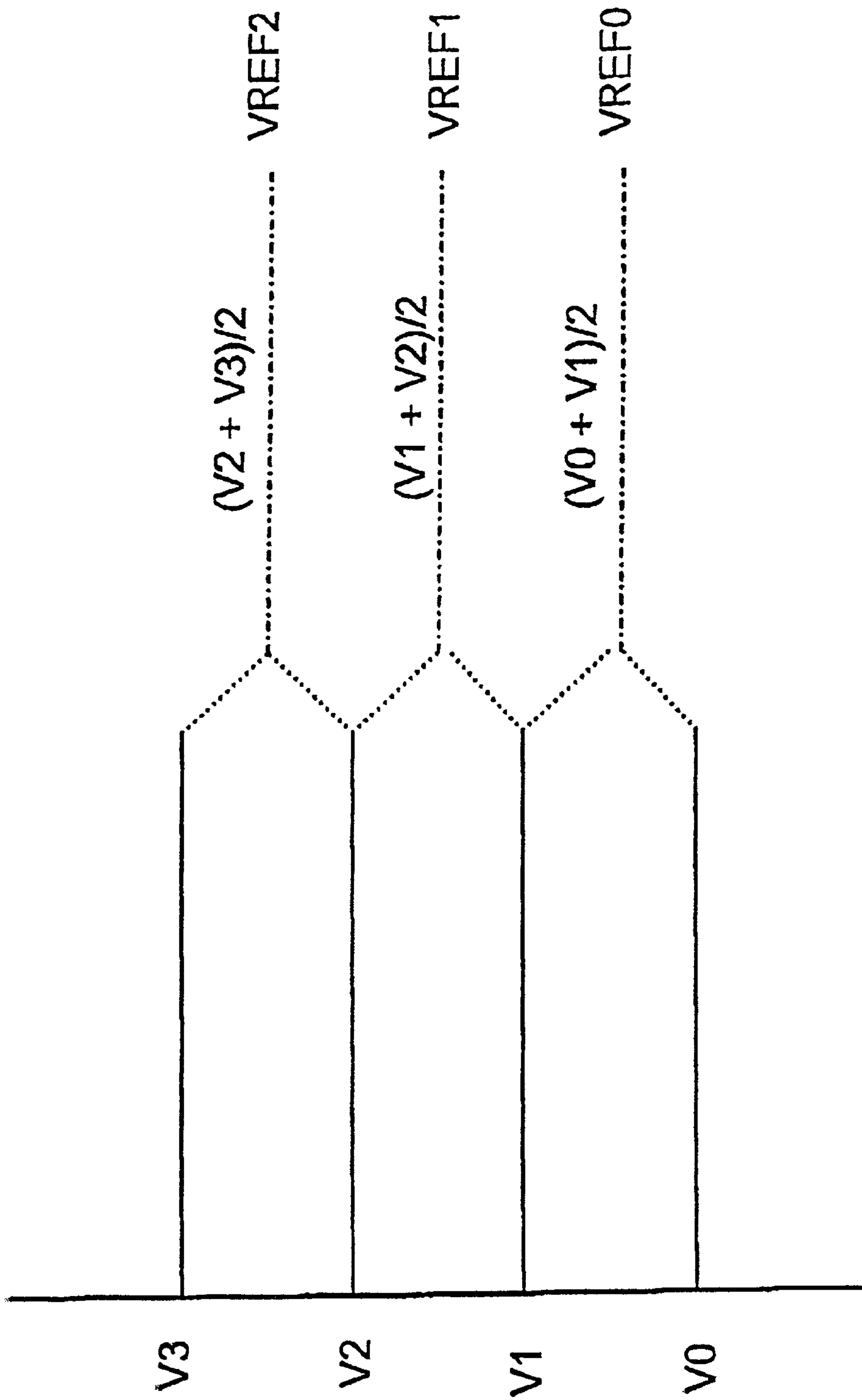


FIG. 17

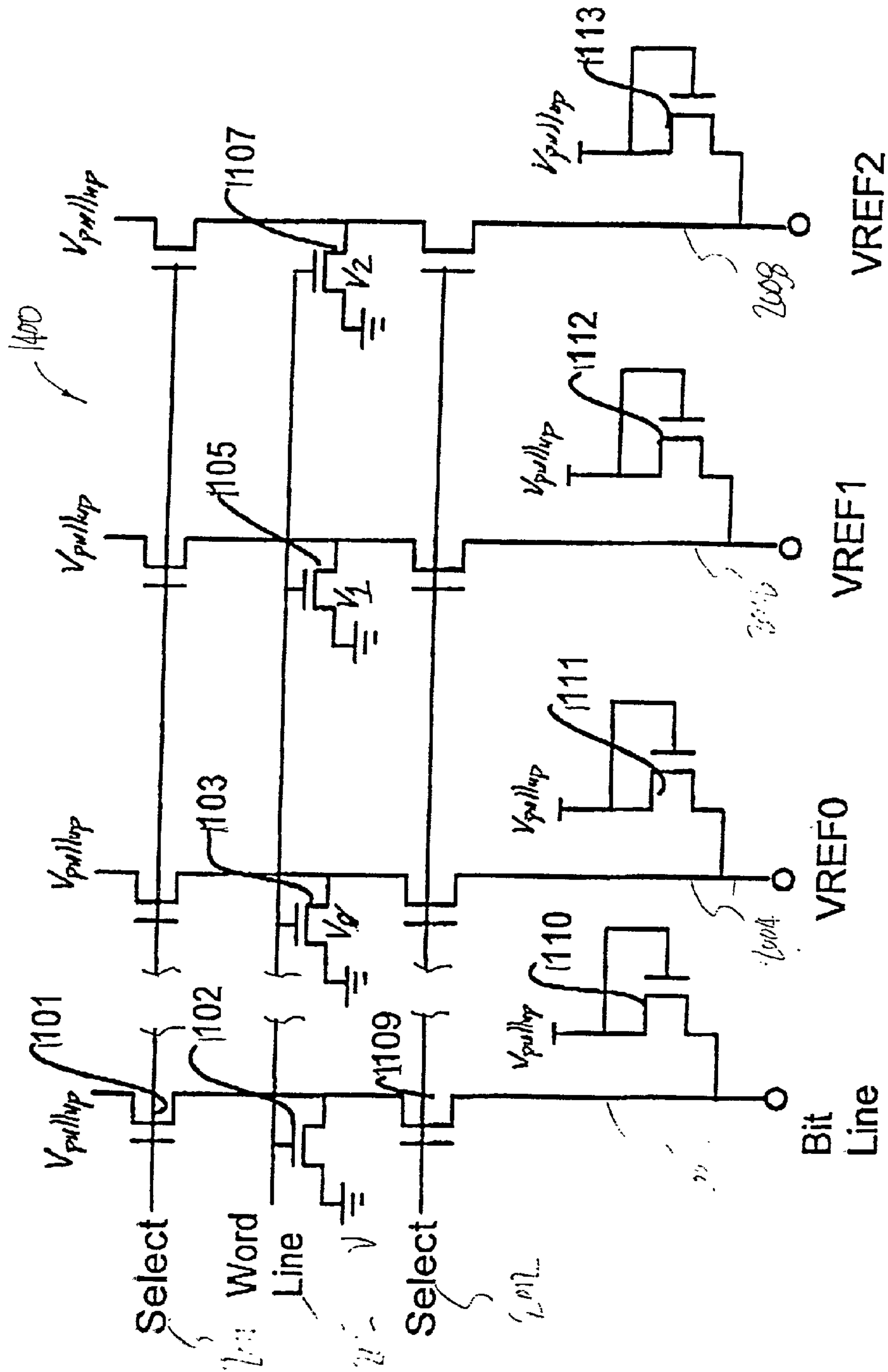


FIG. 18

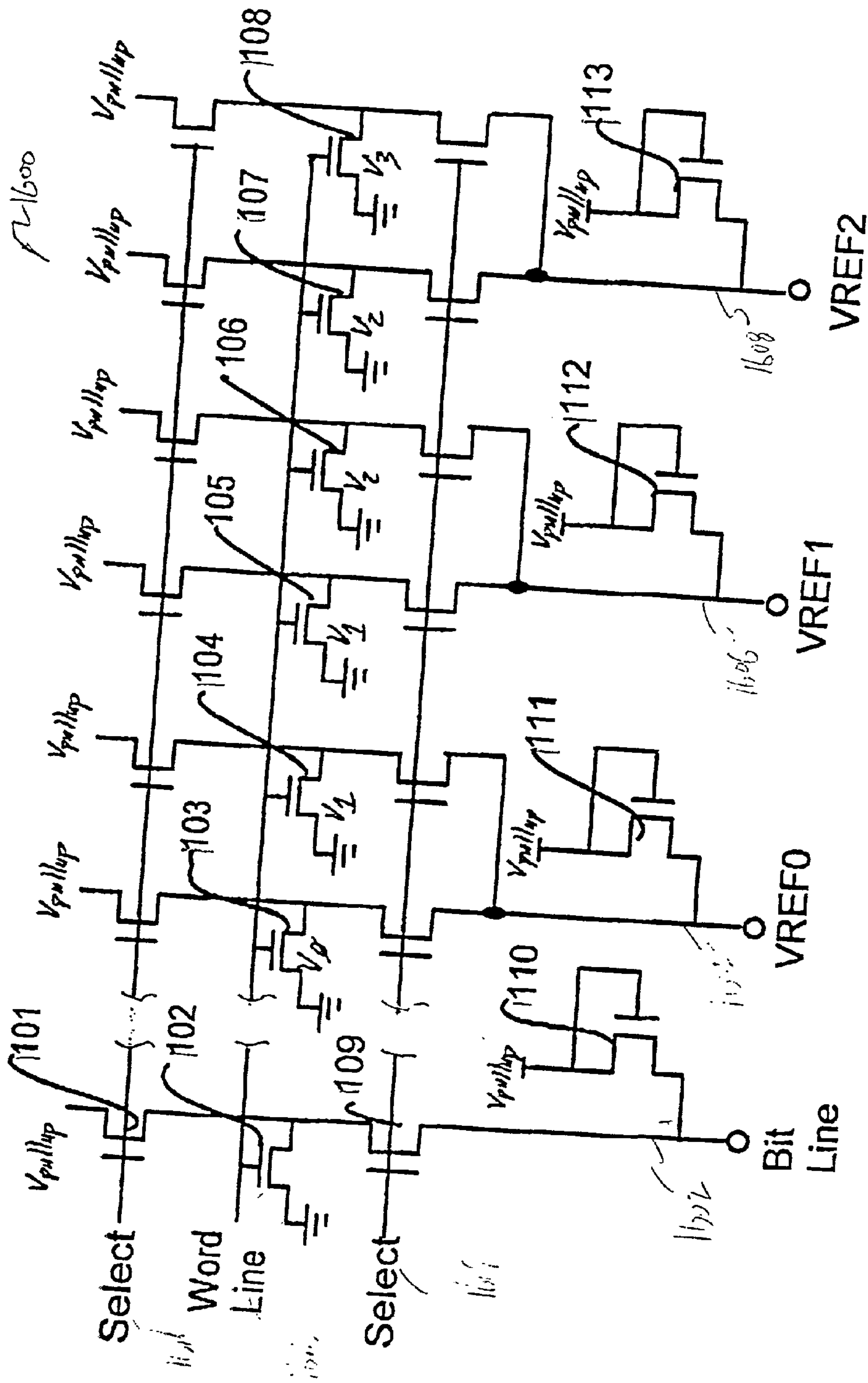


FIG. 19

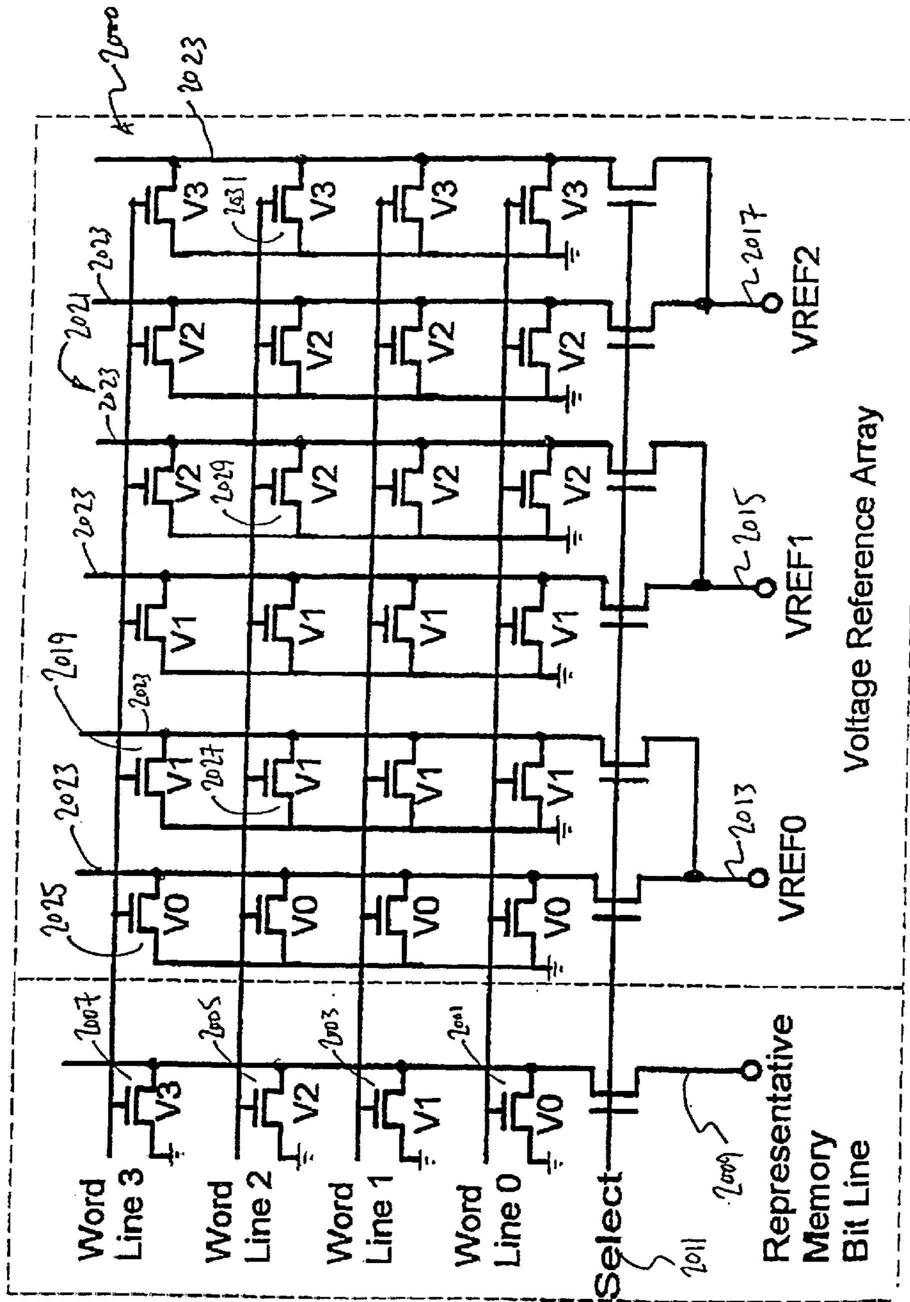


FIG. 20

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. patent application Ser. No. 08/071,816, filed Jun. 4, 1993 entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Memory Cell," which is a continuation of U.S. patent application Ser. No. 07/652,878, filed Feb. 8, 1991 (now U.S. Pat. No. 5,218,569) entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Cell."

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to non-volatile memory (NVM) devices; and, more particularly, is concerned with an apparatus and method for providing a multi-level NVM device with stable reference voltages.

[0004] 2. Description of the Background Art

[0005] In conventional single-bit per cell memory devices, the memory cell assumes one of two information storage states, either an "on" state or an "off" state. This combination of either "on" or "off" defines one bit of information. As a result, a memory device which can store n-bits of data requires n separate memory cells.

[0006] Increasing the number of bits which can be stored in a single-bit per cell memory device relies upon increasing the number of memory cells on a one-for-one basis with the number of bits of data to be stored. Methods for increasing the number of memory bits in a single memory device have relied upon the following advanced manufacturing techniques: manufacture larger die which contain more memory cells; or use improved lithography techniques to build smaller memory cells and allow more memory cells to be placed in a given area on a single chip.

[0007] An alternative approach to the single-bit per cell approach involves storing multiple-bits of data in a single memory cell. Previous approaches to implementing multiple-bit per cell non-volatile memory devices have only involved mask programmable read only memories (ROMs). In one of these approaches, the channel width and/or length of the memory cell is varied such that 2^n different conductivity values are obtained which correspond to 2^n different states corresponding to n-bits of data which can be stored on a single memory cell. In another approach, the ion implant for the threshold voltage is varied such that the memory cell will have 2^n different voltage thresholds (Vt) corresponding to 2^n different conductance levels corresponding to 2^n different states corresponding to n-bits of data which can be stored on a single memory cell. Examples of memory devices of these types are described in U.S. Pat. No. 4,192,014 by Craycraft, U.S. Pat. No. 4,586,163 by Koike, U.S. Pat. No. 4,287,570 by Stark, U.S. Pat. No. 4,327,424 by Wu, and U.S. Pat. No. 4,847,808 by Kobatake.

[0008] Single-bit per cell read-only-memory devices are only required to sense, or read, two different levels or states per cell, consequently they have need for only one voltage reference. Sensing schemes for multi-level memory devices are more complex and require 2^n-1 voltage references. Examples of such multiple state sensing schemes for ROMs are described in U.S. Pat. No. 4,449,203 by Adlhoch, U.S. Pat. No. 4,495,602 by Shepard, U.S. Pat. No. 4,503,578 by Iwahashi, and U.S. Pat. No. 4,653,023 by Suzuki. A limitation with the conventional sensing schemes is often inaccurate and unstable reference voltage levels. The conventional sensing schemes have reference voltage levels which cannot accurately track bit line voltage levels through process, temperature, and voltage variations.

[0009] These approaches to a multi-bit ROM commonly have one of 2^n different conductivity levels of each memory cell being determined during the manufacturing process by means of a customized mask that is valid for only one data pattern. Thus, for storing n different data information patterns, a minimum of n different masks need to be produced and incorporated into a manufacturing process. Each time a data information pattern needs to be changed a new mask must be created and a new batch of semiconductor wafers processed. This dramatically increases the time between a data pattern change and the availability of a memory product programmed with that new data pattern.

[0010] Prior art electrically alterable multiple-bit per cell memory approaches store multiple levels of charge on a capacitive storage element, such as is found in a conventional dynamic random access memory (DRAM) or a charge coupled device (CCD). Such approaches are described in U.S. Pat. No. 4,139,910 by Anantha, U.S. Pat. No. 4,306,300 by Terman, U.S. Pat. No. 4,661,929 by Aoki, U.S. Pat. No. 4,709,350 by Nakagome, and U.S. Pat. No. 4,771,404 by Mano. All of these approaches use volatile storage, that is, the charge levels are not permanently stored. They provide 2^n different volatile charge levels on a capacitor to define 2^n different states corresponding to n-bits of data per memory cell. All of these approaches have the common characteristic that whatever information is stored on such a memory cell is volatile because such a cell loses its data whenever power is removed. Furthermore, these types of memory cells must be periodically refreshed as they have a tendency to lose charge over time even when power is maintained.

[0011] It would be advantageous to develop a multi-bit semiconductor memory cell that has the non-volatile characteristic of a mask programmable read-only-memory (ROM) and the electrically alterable characteristic of a multi-bit per cell DRAM. These characteristics combined in a single cell would provide a multi-bit per cell electrically alterable non-volatile memory (EANVM) capable of storing K^n bits of data, where "K" is the base of the numbering system being used and "n" is the number of bits to be stored in each memory cell. Additionally, it would be advantageous if the EANVM described above was fully compatible with conventional industry standard device programmers/erasers and programming/erasing algorithms such that a user can program/erase the multi-bit per cell memory in a manner identical to that used for current single-bit per cell memory devices.

SUMMARY OF THE INVENTION

[0012] The present invention provides a multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two distinct states and such states are compared to stable reference voltages. The stable reference voltages are gener-

ated by way of cells made during the same (or similar) process steps as the memory device.

[0013] In a specific embodiment, the present invention provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in K^n memory states, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n>2$. The present multi-level memory device also includes a memory cell programming means for programming the multi-level cell means to a state corresponding to the input information. A comparator means for comparing the memory state of the multi-level cell means with the input information is also included. The input information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information.

[0014] An alternative specific embodiment also provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in K^n memory states, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n>2$. A memory cell programming means for programing the multi-level cell means to a state corresponding to the input information is also included. The present multi-level memory device further includes a comparator means for comparing the memory state of the multi-level cell means with the input information. The input information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information. A reference voltage means for defining the plurality of reference voltages is also included. The present reference voltage means is operably coupled to the comparator means.

[0015] In an alternative specific embodiment, the present invention provides an integrated circuit with a plurality of multi-level cells. The present integrated circuit includes a multi-level memory cell for storing input information for an indefinite period of time as a discrete state of said multi-level memory cell. The multi-level memory cell stores information in K^n memory states, where K is a base of a predetermined number system and n is a number of bits stored per multi-level memory cell, wherein $K^n>2$. The present integrated circuit also includes a memory cell programming circuit for programming the multi-level memory cell to a memory state corresponding to the input information. A comparator for comparing the memory state of the multi-level memory cell with the input information is also included. The input information corresponds to one of a plurality of reference voltages. The comparator means further generates a control signal indicative of the memory state as compared to the input information. The present integrated circuit also includes a reference voltage cell for providing the one plurality of reference voltages. The reference voltage cell is operably coupled to the comparator. The multi-level memory cell is defined by one of the plurality of multi-level cells and the reference voltage cell is defined by another of the plurality of multi-level cells.

[0016] A further embodiment provides an integrated circuit device with a plurality of multi-level cells. The plurality of multi-level cells defines a multi-level memory cell and a reference voltage cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

[0018] **FIG. 1** is a generic schematic representation of a non-volatile floating gate memory cell.

[0019] **FIG. 2** is a block diagram of a prior art single-bit memory system.

[0020] **FIG. 3** is a timing diagram of the voltage threshold of a prior art single-bit per cell EANVM system being programmed from an erased "1" state to a programmed "0".

[0021] **FIG. 4** is a timing diagram of the bit line voltage of a prior single-bit per cell EANVM during a read operation. It illustrates waveform levels for both the programmed and erased conditions.

[0022] **FIG. 5** is a block diagram of an M×N memory array implementing a multi-bit per cell EANVM system.

[0023] **FIG. 6** is a block diagram for reading a multi-bit per cell EANVM system.

[0024] **FIG. 7** shows the bit line voltage during a read cycle as a function of time for a 2-bit per cell EANVM which has been programmed to one of four possible states, (0, 0), (1, 0), (0,1) and the fully erased condition (1,1). Four separate voltage levels are represented on this figure, each representing one of the four possible states. Only one of these would be present for any given read operation.

[0025] **FIG. 9** is a timing diagram which illustrates the voltage threshold of a 2-bit per cell EANVM being erased from a fully programmed (0,0) state to one of the other three possible states.

[0026] **FIG. 8** is a block diagram of a multi-bit per cell system combining program/verify and read circuitry.

[0027] **FIG. 9** is a timing diagram for the voltage threshold for a 2-bit per cell EANVM being programmed from a fully erased (1,1) state to one of the other three possible states.

[0028] **FIG. 11** is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using fixed width program pulses.

[0029] **FIG. 12** is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses fixed width program pulses.

[0030] **FIG. 13** is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using variable width program pulses.

[0031] **FIG. 14** is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses variable width program pulses.

[0032] **FIG. 15** is a simplified diagram of voltages for a 2-bit per memory cell according to the present invention.

[0033] **FIG. 16** is a simplified voltage generator circuit diagram of a voltage divider arrangement for generating multiple reference voltages according to the present invention.

[0034] **FIG. 17** illustrates the reference voltages of **FIG. 16** according to the present invention.

[0035] **FIG. 18** is a simplified voltage generator circuit diagram for an array showing reference voltage columns connected to pull-up devices according to the present invention.

[0036] **FIG. 19** is a simplified voltage generator circuit diagram for obtaining reference voltages with use of pull-up devices and a voltage divider according to a preferred embodiment of the present invention.

[0037] **FIG. 20** is a simplified diagram of a voltage generator circuit according to an alternative embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0038] Reference will now be made in detail to the specific embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the specific embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover various alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

[0039] In general, the invention described here allows n-bits of information to be stored on and read from an Electrically Alterable Non-Volatile Memory (EANVM). This is accomplished by electrically varying the conductivity of the channel of a floating gate FET to be within any one of K^n conductivity ranges where "K" represents the base of the numbering system being employed (in a binary system, "K" equals 2). The conductivity range is then sensed and encoded. This forms the basis of an n-bit EANVM memory cell. The floating gate FET conductivity is electrically modified by using conventional external programming hardware and algorithms which supply conventional signals and voltages to the EANVM memory device.

[0040] These external signals and voltages are then modified internal to the device to provide an internally controlled program/verify cycle which incrementally stores electrons on the floating gate until the desired conductivity range is achieved. For the purpose of illustration, the n-bit per cell descriptions will assume a binary system which stores 2-bits per memory cell.

I. Prior Art Single-bit EANVM Devices

[0041] **FIG. 1** is a generic schematic representation of a non-volatile floating gate memory cell **10**. It is not intended that this schematic drawing is in any way indicative of the device structure. It is used to illustrate the fact that this invention refers to an FET memory cell which uses an electrically isolated, or floating, gate **14** to store charged particles for the purpose of altering the voltage threshold and hence channel conductivity of the FET memory cell **10**.

[0042] The FET memory cell **10** includes a-control gate **12** which is used either to select the memory cell for reading or is used to cause electrons to be injected onto the floating gate **14** during the programming process. Floating gate **14** is an electrically isolated structure which can indefinitely store electrons. The presence or absence of electrons on floating gate **14** alters the voltage threshold of the memory cell **10** and as a result alters the conductivity of its channel region. A drain region **16** of the FET is coupled to a source region **18** by a channel region **19**. When the floating gate **14** is fully erased and the control gate **12** has been selected, the channel region **19** is in the fully "on", or high conductivity, state. When the floating gate **14** is fully programmed the channel region **19** is in the fully "off", or low conductivity state.

[0043] **FIG. 2** is a block diagram of a prior art conventional single-bit EANVM memory system **30**. The memory system **30** stores a single bit of information in an EANVM cell **32**. The cell **32**, as described in **FIG. 1**, is selected for reading or writing when a row, or word, select signal is applied to a control gate terminal **34**. A source terminal **36** for the FET of the cell **32** is connected to a reference ground potential. A drain terminal **38** is connected through a pull-up device **39** to a voltage Vpull-up at a terminal **40**. Terminal **38** serves as the output terminal of the cell **32**. When the cell **32** stores a "1" bit, the channel of the FET is in a low conductivity, or high impedance, state so that the voltage at terminal **38** is pulled-up to the voltage level Vpull-up on terminal **40**. When the cell **32** stores a "1" bit, the channel of the FET is in a high conductivity, or low impedance, state so that the voltage at terminal **38** is pulled-down by the ground potential at terminal **36**.

[0044] For reading the value of the single-bit stored in the cell **32**, a sense amplifier **42** compares the voltage at terminal **38** with a reference voltage Vref at terminal **43**. If a "0" is stored on the EANVM cell **32**, the cell will be in a low conductivity state and as a result the voltage at terminal **38** is above the reference voltage at terminal **43**. For a "0" stored in the cell **32**, the output terminal **44** of the sense amplifier **42** will be a low voltage which will be transmitted through an output buffer **46** to a terminal **48** and then coupled to the I/O terminal **50** as a logical "0". If a "1" is stored on the EANVM cell **32**, the cell is in a high conductivity state and as a result the voltage at terminal **38** is below the reference voltage at terminal **43**. The output of the sense amplifier **42** will be a high voltage which will be transmitted to the I/O terminal **50** as a logical "1".

[0045] For writing the value of an information bit stored in the cell **32**, it is assumed that the cell **32** is in the erased, or fully "on", state which corresponds to a logical "1". The I/O terminal **50** is connected to the input terminal of an input latch/buffer **52**. The output of the input latch/buffer **52** is connected to an enable/disable terminal **54** of a program voltage switch **56**. The program voltage switch **56** provides a bit-line program voltage on a signal line **58** connected to terminal **38**. Another output from the program voltage switch **56** is the word line program voltage on a signal line **62**, which is connected to the control gate **34** of the EANVM cell **32**. When a logical "0" is present at terminal **54** of the program voltage switch **56** from the output of Input Latch/Buffer **52** and when the program voltage switch **56** is activated by a program pulse on a signal line **62** from a program pulse **66**, activated by a PGM/Write signal, the program voltage switch **56** provides the Program Voltage

Vpp from a terminal **68** to the control gate **34** of the EANVM cell **32**. The program voltage switch **56** also biases the drain of the cell **32** to a voltage, typically between 8 to 9 volts, and the gate of the EANVM cell **32** to the program voltage Vpp, typically 12 volts. Under these conditions, electrons are injected onto the floating gate by a phenomenon known as hot electron injection. This programming procedure raises the voltage threshold of the EANVM cell which increases its source-drain impedance. This continues until the FET memory cell **32** is effectively turned off, which corresponds to a "0" state. When a "1" is present on terminal **54** from the output of the Input Latch/Buffer **52** and when the PGM/Write is enabled, the signal line **58** is driven low and programming is inhibited and the "1", or erased, state is maintained.

[**0046**] **FIG. 3** is a timing diagram of a prior-art single-bit EANVM cell **32**, as described in connection with **FIG. 2**. The timing diagram shows the change in voltage threshold of the EANVM cell **32**, as controlled by the word line and bit line programming voltages, which are illustratively shown as a single signal and which are both controlled by the PGM/Write signal. The memory cell is being programmed from the fully erased "1" state to the fully programmed "0" state. For the duration of the PGM/Write pulse, the bit and word line program voltages, which need not be the same, are respectively applied to the source connected to the bit line **38** and to the control gate **34** of the memory cell **32**. As electrons are injected onto the floating gate, the voltage threshold of the memory cell begins to increase. Once the voltage threshold has been increased beyond a specific threshold value as indicated by the dashed horizontal line, the memory cell **32** is programmed to a "0" state.

[**0047**] Note that Fowler-Nordheim tunnelling can also be used instead of hot electron injection to place electrons on the floating gate. The multi-bit EANVM device described here functions with either memory cell programming technique. The prior art programming algorithms and circuits for either type of programming are designed to program a single-bit cell with as much margin as possible in as short a time as possible. For a single-bit memory cell, margin is defined as the additional voltage threshold needed to insure that the programmed cell will retain its stored value over time.

[**0048**] **FIG. 4** is a timing diagram showing the bit line voltage at terminal **38** as a function of time during a memory read operation. In this example, prior to time t**1** the bit line is charged to the Vpull-up condition. Note that it is also possible that the bit line may start at any other voltage level prior to time t**1**. At time t**1**, the EANVM cell **32** is selected and, if the cell **32** is in the erased or tilt state, the cell **32** provides a low impedance path to ground. As a result, the bit line is pulled down to near the ground potential provided at terminal **36** in **FIG. 2**. If the EANVM cell **32** were in the "0" or fully programmed state, the bit line voltage would remain at the Vpull-up voltage after time t**1**. The voltage on the bit-line terminal **38** and the reference voltage Vref at terminal **43** are compared by the comparator **42**, whose buffered output drives I/O terminal **50**. When Vref is greater than the bit line voltage, the output on I/O terminal **50** is a logical "0". When Vref is lower than the bit line voltage, the output on I/O terminal **50** is a logical "0".

II. Memory Array for a Multi-bit EANVM System

[**0049**] **FIG. 5** is a block diagram of a multi-bit per cell EANVM system **100** which includes an M×N array of memory cells. The cells are typically shown as a floating gate FET, or EANVM, **102**, as described in **FIG. 1**. The array uses similar addressing techniques, external control signals, and I/O circuits as are used with currently available single bit per cell EANVM devices such as EPROM, EEPROM, FLASH, etc. devices. Row Address signals are provided at input terminals **103**A and Column Address signals are provided at input terminals **103**B.

[**0050**] Each of the EANVM cells in a row of cells has its source connected to a ground reference potential and its drain connected to a column bit line, typically shown as **106**. Each of the columns is connected to a pull-up device, as indicated by the block **105**. All of the control gates of a row are connected to a row select, or word, line, typically shown as **104**. Rows are selected with a row select circuit **108** and columns are selected with a column select circuit **110**. Sense amplifiers **112** are provided for each of the selected columns. Decode/encode circuits **114** and n-bit input/output latches/buffers **116** are also provided. A PGM/Write signal is provided at an input terminal **118** for activating a mode control circuit **120** and a timing circuit **122**.

[**0051**] A significant feature of this n-bit per cell system **100** as compared to a single-bit per cell implementation is that the memory density is increased by a factor of n, where n is the number of bits which can be stored on an individual multi-bit memory cell.

III. Basic Read Mode of an N-bit Memory Cell

[**0052**] **FIG. 6** shows a binary system **150** for reading the state of an n-bit floating gate memory cell **102**, as described in **FIG. 1**, according to the invention, where n is the number of bits stored in the memory cell. For this example, n is set to 2 and one of four states of the memory cell must be detected. The four possible states being, (0,0), (0,1), (1,0), or (1,1). Detecting which state is programmed requires a 4-level sense amplifier **152**. This amplifier includes three sense amplifiers **154**, **156**, **158** each of which have their negative input terminals connected to the output terminal **106** of the memory cell **102**. Sense amplifier **154** has a reference voltage Ref **3** connected to its positive input terminal. Sense amplifier **156** has a reference voltage Ref **2** connected to its positive input terminal. Sense amplifier **158** has a reference voltage Ref **1** connected to its positive input terminal. The voltage references are set such as follows: Vpull-up>Ref **3**> Ref **2**>Ref **1**. The respective output signals S3, S2, S1 of the three sense amplifiers drive an encode logic circuit **160**, which encodes the sensed signals S3, S2, S1 into an appropriate 2-bit data format. Bit **0** is provided at an I/O terminal **162** and Bit **1** is provided at an I/O terminal **164**. A truth table for the encode logic circuit **160** is as follows:

S3	S2	S1	I/0 1	I/0 0	State
L	L	L	0	0	(0,0)
H	L	L	1	0	(1,0)
H	H	L	0	1	(0,1)
H	H	H	1	1	(1,1)

[0053] During a read operation of an n-bit memory cell, the levels of the respective output signals S3, S2, S1 of the sense amplifiers **154**, **156**, **158** are determined by the conductivity value to which the memory cell had been set during a programming operation. A fully erased EANVM cell **102** will be in its lowest threshold voltage state, or the highest conductivity state. Consequently, all of the reference voltages will be higher in voltage than the bit line voltage at terminal **106**, resulting in a (1,1) state. A fully programmed EANVM cell **102** will be in its highest threshold voltage state, or its lowest conductivity state. Consequently, all reference voltages will be lower in voltage than the bit line voltage at terminal **106**, resulting in a (0,0) state. The intermediate threshold states are encoded as is illustrated in the truth table for the logic circuit **160**. **FIG. 7** shows the bit line voltage as a function of time at terminal **106**, during a read cycle, for a binary 2-bit per memory cell. For purposes of illustration, each of the four possible waveforms corresponding to the four possible programmed states of the memory cell are shown. During a read cycle only the waveform corresponding to the programmed state of the EANVM cell would occur. For example, 25 assume the EANVM memory cell **102** has been programmed to a (1,0) state. Prior to time t**1**, because the EANVM cell **102** has not yet been selected or activated, the bit line **106** is pulled-up to Vpull-up. At time t**1**, 22 the EANVM cell is selected using conventional memory address decoding techniques. Because the EANVM cell has been programmed to a specific conductivity level by the charge on the floating gate, the bit line is pulled down to a specific voltage level corresponding to the amount of current that the cell can sink at this specific conductivity level. When this point is reached at time t**2** the bit line voltage stabilizes at a voltage level Vref**2** between reference voltages Ref **3** and Ref **2** which correspond to a (1,0) state. When the EANVM cell **102** is de-selected, the bit line voltage will return to its pulled-up condition. Similarly, the bit-line voltage stabilizes at Vref**1** for the 0,1 state for the other specific conductivity levels, or at zero volts for the 1,1 state. **FIG. 8** is a block diagram of an n-bit memory cell system **200**. For purposes of illustration a binary 2-20 bit per cell system is shown. However, it is intended that the concepts of the invention extend to systems where n is greater than 2. It is also intended that the invention include any system where the EANVM memory cell has more than two states. For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system. Some of the components of this system **200** are shown and described with the same reference numerals for the components of **FIG. 6** for the read mode of operation. It is intended that these same reference numerals identify the same components. The system **200** includes a memory cell **102**, as described in **FIG. 1**, with a bit line output terminal **106**. For the read mode of operation, a 4-level sense amplifier **152** with read reference voltages Ref **1**, Ref **2**, and Ref **3** and an encoder **160** is provided. Read data is provided at a Bit I/O terminal **162** and at a Bit I 1/0 terminal **164**. For the write mode of operation, a verify reference voltage select circuit **222** provides an analog voltage reference level signal X to one input terminal of the analog comparator **202**. The verify reference voltages are chosen so that as soon as the bit line voltage on bit line **106** is greater than the verify reference voltage the threshold of the EANVM cell **102** is set to the proper threshold corresponding to the memory state to which it is to be programmed. To this end the verify reference voltages Vref**1**, Vref**2**, Vref**3**, and Vref**4** are set such that Vref**4** is above Ref **3**, Vref**3** is between Ref **3** and Ref **2**, Vref**2** is between Ref **1** and Ref **2**, and Vref**1** is below Ref **1**. During a normal read operation, the bit line voltage will settle midway between the read reference voltages to insure that the memory contents will be read accurately. The verify reference voltage select circuit **222** is controlled by the 2-output bits from a 2-bit input latch/buffer circuit **224**, which receives binary input bits from the I/O terminals **162** and **164**. The Y signal input terminal of the analog comparator **5202** is connected to the bit line output terminal **106** of the multi-level memory cell **102**. The output signal from the analog comparator is provided on a signal line **204** as an enable/disable signal for the program voltage switch **220**. An output signal line **206** from the program voltage switch **220** provides the word line program voltage to the control gate of the EANVM cell **102**. Another output signal line **206** provides the bit- line programming voltage to the bit- line terminal **106** of EANVM cell **102**. After the program/verify timing circuit **208** is enabled by a PGM/Write signal provided on signal line **212** from a PGM/Write terminal **214**, the timing circuit **208** provides a series of program/verify timing pulses to the program voltage switch **220** on a signal line **210**. The pulse widths are set to control the programming process so that the voltage threshold of the EANVM cell **102** is incrementally altered by controlling the injection of charge onto the floating gate of the EANVM cell. Each programming cycle increases the voltage threshold and, as a result, decreases the conductance of the memory cell **102**. After each internal program cycle is complete, as indicated by signal line **210** going "high", the program voltages are removed via the Program Voltage Switch **220** and a verify cycle begins. The voltage threshold of memory cell **102** is then determined by using the comparator **202** to compare the bit line voltage at terminal **106** with the selected verify reference voltage from the verify reference voltage select circuit **222**. When the bit line voltage exceeds that supplied by the verify reference voltage select circuit **222**, the output signal **204** from the comparator **202** will then disable the program voltage switch **220** ending the programming cycle. For this embodiment of the invention, during a write operation, comparison of the current memory cell analog contents with the analog information to be programmed on the memory cell **102** is performed by the analog comparator **202**. The verify reference voltage select circuit **222** analog output voltage X is determined by decoding the output of the n-bit input latch/buffer **224**. The Y input signal to the analog comparator **202** is taken directly from the bit line terminal **106**. Note that the 4-level sense/encode circuits **152**, **160**, and reference voltage select circuit **222** may be completely independent, as indicated in the drawing. Alternatively, they may be coupled together to alternately time share common circuit components. This is possible because the 4- level sense/encode circuits **152** and **160** are used in the read mode of operation while the verify reference voltage select circuit **222** is used only in the write/verify mode of operation.

IV. Basic Write Mode for a Multi-bit Per Cell EANVM System

[0054] In the write mode, a binary n-bit per cell EANVM system must be capable of electrically programming a memory cell to 2^n uniquely different threshold levels. In the two-bit per cell implementation, because it is assumed that

the cell starts from the erased (1,1) state, it is only necessary to program three different thresholds (Vt**1**, Vt**2**, and Vt**3**) which define the (0,1), (1,0), and (0,0) states. Vt**1** is the threshold required such that in the read mode, the bit line voltage will fall between Ref **1** and Ref **2**. Vt**2** is the threshold required such that in the read mode, the bit line voltage will fall between Ref **2** and Ref **3**. Vt**3** is the threshold required such that in the read mode, the bit line voltage will be greater than Ref **3**.

[**0055**] **FIG. 9** illustrates the change in voltage threshold for a 4-level, or 2-bit EANVM cell as the floating gate is being charged from an erased (1,1) threshold state to any one of the three other possible states. In prior art single-bit memory cells where there are only two states, the design objective is to provide enough charge to the floating gate to insure that the cell's voltage threshold is programmed as high as possible, as shown in **FIG. 3**. Because there is no upper threshold limit in a single-bit per cell system, over-programming the cell will not cause incorrect data to be stored on the memory cell.

[**0056**] As illustrated by **FIG. 9**, in an n-bit per cell system the memory cell must be charged to a point so that the voltage threshold is within a specific voltage threshold range. In this example, where the cell is being programmed to a (1,0) state, the proper threshold range is defined as being above a threshold level Vt**2** and as being below a threshold level Vt**3**.

[**0057**] To accomplish this n-level programming it is necessary to add to or modify the prior art EANVM circuitry. **FIG. 8** shows the additional or modified circuits, including a reference voltage select, an n-bit latch/buffer, a program/verify timing circuit, and a comparator. The comparator can be either digital or analog.

[**0058**] **FIG. 10** illustrates the voltage threshold of an EANVM cell as the floating gate is being erased from a (0,0) state. Standard EANVM programming operating procedure calls for a memory cell to be erased prior to being programmed. This erasure can be performed at the byte, block, or chip level and can be performed by electrical, UV, or other means. In this type of system the cell would be completely erased to a (1,1) state prior to initiating a programming cycle. If a system has the capability to erase an individual memory cell, then it is not necessary to erase all of the cells of a group prior to initiating a programming operation. It is then possible to incrementally erase an individual memory cell, as necessary, to program the cell to the appropriate voltage threshold as is indicated by the waveforms labelled (1,0) and (0,1).

[**0059**] **FIG. 11** is a timing diagram which illustrates how a 2-bit EANVM cell of **FIG. 8** is programmed from an erased (1,1) state to a (1,0) state using the timing circuitry **208** to generate fixed length timing pulses. A low logic level state of the PGM/Write signal on signal line **212** enables the timing circuit **208**. When enabled at time t**1**, the timing circuit **208** provides an internal fixed-width low level internal PGM timing pulse on signal line **210** to the program voltage switch **220**. For the duration of the low state of the internal PGM timing pulse, the bit line and word line program voltage outputs on lines **216** and **206** will be raised to their respective programming voltage levels as shown in **FIG. 11**. During this programming process, charge is added to the floating gate of the memory cell **102**. When the internal PGM timing pulse from timing circuitry **208** switches to a high level, the programming voltages are removed and a verify cycle begins. For this example, verify reference voltage Vref**3** is compared with the bit line voltage. This internally controlled program/verify cycle repeats itself until the bit line voltage on terminal **106** exceeds Vref**3**. At this time, t**2**, the EANVM cell **102** is verified to have been programmed to a (1,0) state and programming is halted by the comparator **222** providing a disable signal on signal line **204** to the program voltage switch **220**.

[**0060**] **FIG. 12** illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1,1) to a partially "off" state (1, 0) using fixed length program pulses. When the externally applied PGM/Write pulse is applied at time t**1**, the program/verify timing circuit **208** first initiates a verify cycle to determine the current status of the memory cell **102**. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, Vpull-up. Although, prior to time t**1**, the bit line voltage could be pre-set to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage, Vref**3** in this example, corresponding to the data to be programmed, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first fixed length programming pulse ends, a verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between ground potential and Ref**1**. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues until the bit-line voltage exceeds the selected verify reference voltage, in this case Vref**3**, which indicates a memory state of (1,0), at time t**2**.

[**0061**] **FIG. 13** illustrates how a 2-bit EANVM cell is programmed from an erased (1,1) state to a (1,0) state using variable length programming pulses. The internal PGM pulses for this implementation start with a low state longer than for fixed-width implementation of **FIGS. 11 and 12**. The low-state pulse widths grow progressively shorter as the memory cell approaches the appropriate voltage threshold. This approach requires more precise control than the fixed length approach. However, programming times can be greatly reduced on average.

[**0062**] **FIG. 14** illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1,1) to a partially "off" state (1,0) using variable length program pulses. When the externally applied PGM/Write pulse goes to an active low level at time t**1**, the program/verify timing circuit **208** first initiates a verify cycle to determine the current status of the memory cell **102**. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, Vpull-up. Although, prior to time t**1**, the bit line voltage could be preset to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage corresponding to the data to be programmed, Vref**3** in this example, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first variable length programming pulse is over, another verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between Ref**1** and Ref**2**. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues

until the bit-line voltage surpasses the selected verify reference voltage, in this case vref**3** which indicates a memory state of (1,0), at time t**2**.

[**0063**] Accordingly, the programming process for an n-bit per cell EANVM uses program/verify cycles, to incrementally program a cell. The duration of these cycles are determined by the timing circuit **208**. A key element of the system is to provide a programming scheme which provides for accurate programming of the memory cell **102**. This is accomplished by matching the pulse widths of the timing pulses of the timing circuitry **208** to the program time of the EANVM cell being used. As indicated in **FIGS. 11 and 13**, a desired voltage threshold actually falls within a range of threshold voltages If the program pulses are too long, then too much charge may be added to the floating gate of the memory cell **102**. This may result in an overshoot of the target voltage threshold, resulting in incorrect data being stored in the memory cell.

[**0064**] The programming pulse width is set such that if the voltage threshold of the cell **102** after the (n−1) programming pulse is at a point just below the target voltage threshold, then the (n)th, or final, program pulse will not cause an overshoot resulting in an overprogrammed condition for a memory cell.

[**0065**] **FIG. 8** may also use a digital comparator rather than the analog comparator **202** shown in **FIG. 8**. The digital comparator would use the encoded data from the encode circuitry **160** as the input to the comparator represent the current contents of the EANVM cell **102**. The verify reference voltage select **222** would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer **224**, representing the data to be programmed. Otherwise, the function of the comparator within the system remains the same.

V. Embodiments to Establish Reference Voltages

[**0066**] A multi-level (or multi-bit) memory device which contains more than one bit of information per memory cell needs accurate and stable reference voltages. The reference voltages allow a multi-level memory cell to be correctly read over various process, voltage, and temperature ranges. The reference voltages must be implemented into the integrated circuit which can accurately sense the multi-level voltage levels of the memory cells as well as track each memory array voltage level as it drifts with the process, voltage, and temperature variations. An unstable or inaccurate reference voltage tends to cause problems such as an improper voltage level read of a bit line, and the like from a memory cell.

[**0067**] In a 2-bit per memory cell embodiment, the memory cell includes four voltage levels **V0**, **V1**, **V2**, and **V3** at each of the bit lines as illustrated by **FIG. 15**. To uniquely detect each of the four voltage levels, it is necessary to generate at least three reference voltages, each of the reference voltages falling between memory bit line voltage levels. When **V0**, **V1**, **V2**, and **V3** represent the four bit line voltage levels, the reference voltages VREF**0**, VREF1, AND VREF2 fall between **V0** and **V1**, **V1** and **V2**, and **V2** and **V3**, respectively. Preferably, the reference voltages VREF**0**, VREF1, and VREF2 fall halfway between **V0** and **V1**, **V1** and **V2**, and **V2** and **V3**, respectively. Each reference voltage is also set to provide a clear and accurate reference level, which can be used as a reference for the bit line voltage.

[**0068**] In a specific embodiment, a method for establishing reference voltages for a non-volatile multi-bit memory array is provided. Merely by way of example, the present method is applied to the manufacture of a non-volatile multi-bit memory array such as a masked ROM array, an EANVM memory array, and the like. The present method calls for reference voltage sources and in particular reference voltage lines and cells which are fabricated simultaneously with the standard memory cell array. Alternatively, the present method may call for reference voltage sources and in particular reference voltage lines and cells which are fabricated by way of the same method (but at a different step) as the standard memory cell array. By way of the present method, stable reference voltages are established which track bit line voltages in memory cells through voltage, temperature, and process variations.

[**0069**] In a masked ROM embodiment, for example, the present method calls for reference voltages to be generated using memory cells which have been programmed in the same fashion and preferably in exactly the same fashion as the cells in the standard memory array itself. In the present masked ROM embodiment whose memory cells are programmed using a Vt implant, the memory cells within the reference voltage generator circuit will be implanted at the same time with preferably the same implant dosage as the ROM cells within the standard memory array. This means the implant dosage of the reference voltage cell is substantially the same as the memory cell for the bit line in the standard memory array. The reference voltage level is also substantially the same as the bit line voltage level, that is, assuming the same voltage is applied to both the reference voltage cell and the bit line cell. As show in **FIG. 16** for example, memory cells within the reference voltage generator circuit include field effect transistors **1103**, **1104**, **1105**, **1106**, **1107**, and **1108**. A ROM cell in a memory array may include transistor **1102** coupled to a bit line.

[**0070**] In the present embodiment, the reference voltage is moved to a voltage point away from the bit line voltage. This allows the multi-bit memory device to sense the relative voltage difference between the bit line and the reference voltage line, and then decode the programmed cell accordingly. By way of the same implant step, the reference voltage tracks the bit line voltage over process, voltage, and temperature variations, and is therefore stable.

[**0071**] In the present invention, a selected voltage difference exists between the voltage reference levels and memory bit line voltage levels such that they do not interfere with each other. The voltage reference and sensing circuitry are able to detect a single unique voltage level out of four possible levels, in a 2-bit per memory cell configuration for example. Referring to **FIG. 15**, if VREF**0** was inadvertently raised to the level of VREF1, a non-programmed memory state of (1,1) is easy read. Unfortunately, if the memory cell was programmed to an intermediate state of (1,0), the relation between VREF**0** to VREF**1** makes it difficult to differentiate between the two levels. As a result, the output is often unreliable and the like. Accordingly, the present invention relies upon either a voltage divider arrangement, a pull-up device arrangement, or the like, and combinations thereof to create desired reference voltage levels. Although the present invention is described in the masked ROM

embodiment, the present invention may also be applied to any multi-bit memory array such as an EANVM memory array, and the like.

[**0072**] **FIG. 16** is a simplified reference voltage generator circuit in a voltage divider arrangement **1200** for generating multiple reference voltages according to the present invention. In a 2-bit per cell embodiment, a multi-level memory cell includes at least four bit line voltage levels **V0**, **V2**, **V3**, and **V4**. Each of the four bit line voltage levels is detected by way of three reference voltage levels, each of which falls between two adjacent bit line voltage levels. The voltage divider arrangement includes a VREF**0** column **1204**, a VREF**1** column **1206**, and a VREF**2** column **1208**. Each column includes at least a pull-up voltage VPULLUP. A bit line column **1202** is also shown for illustrative purposes. The bit line column is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either **V0**, **V1**, **V2**, or **V3**, depending upon the particular application. A plurality of rows **1212**, **1214** (or SELECT lines) are also shown. The SELECT line **1212** includes a plurality of field effect transistors **1109**, and the SELECT line **1214** includes a plurality of field effect transistors **1101**. Each of the columns also includes a WORD line **1216** operably coupled to each column through field effect transistors **1102**, **1103**, **1104**, **1106**, **1107**, and **1108**. The field effect transistors **1102**, **1103**, **1104**, **1106**, **1107**, and **1108** include a source/drain region at V, **V0**, **V1**, **V1**, **V2**, **V2**, **V3**, respectively. The field effect transistors may include an NMOS device, a PMOS device, and the like.

[**0073**] As shown, each pair **V0** and **V1**, **V1** and **V2**, and **V2** and **V3** connect together with a voltage divider arrangement to generate intermediate reference voltages VREF**0**, VREF**1**, and VREF**2**, respectively. By way of the field effect transistors **1103**, **1104**, and application of voltage at the WORD line and the SELECT line **1212**, the reference voltage VREF**0** is at a voltage level between about **V0** and about **V1**. By way of application of voltage at the WORD line and SELECT line **1212**, the reference voltage VREF**1** is between about **V1** and about **V2**. Similarly, by way of application of voltage at the WORD line and the SELECT line **1212**, the reference voltage VREF**2** is between about **V2** and about **V3**.

[**0074**] **FIG. 17** illustrates the reference voltage levels of for example **FIG. 16** according to the present invention. The voltage divider arrangement defines the reference voltages as follows:

[**0075**]

$$VREF0=(V0+V1)/2$$

$$VREF1=(V1+V2)/2$$

$$VREF2=(V2+V3)/2$$

[**0076**] The reference voltages VREF**0**, VREF**1**, and VREF**2** fall between **V0** and **V1**, **V1** and **V2**, and **V2** and **V3**, respectively. Accordingly, the present multi-bit memory device provides reference voltages which do not overlap with the bit line voltages. In addition, the references voltages VREF**0**, VREF**1**, and VREF**2** track well with the memory bit lines over process, voltage, and temperature variations. Preferably, each of the reference voltages fall exactly halfway between adjacent bit line voltage levels.

[**0077**] **FIG. 18** is a simplified voltage generator circuit diagram **1400** of an array showing reference voltage columns connected to pull-up devices according to the present invention. Each of the pull-up devices is a field effect transistor such as an NMOS device, a PMOS device, and the like. Preferably, the pull-up device is a PMOS device. A bit line column **2002** is also shown for illustrative purposes. The bit line column is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either **V0**, **V1**, **V2**, or **V3**, depending upon the particular application. The bit line also includes a field effect transistor **1102** and a word line **2016** operably coupled to the field effect transistor.

[**0078**] The voltage generator circuit includes a plurality of reference voltage column lines **2004**, **2006**, **2008**, each at the same voltage level on one end VPULLUP, a plurality of field effect transistors **1101**, **1109**, and a reference voltage at the other end VREF**0**, VREF**1**, and VREF**2**. Between field effect transistors **1101**, **1109** are cells which include field effect transistors **1103**, **1105**, and **1107**. The field effect transistors **1103**, **1105**, and **1107** include source/drain regions coupled to **V0**, **V1**, and **V2**, and source/drain regions coupled to column lines **2004**, **2006**, and **2008**, respectively. A WORD line connects in parallel to each of the field effect transistor (**1103**, **1105** and **1107**) gates. A plurality of SELECT lines **2012**, **2014** connect to the transistor (**1109**, **1101**) gates. The bit line and reference voltage lines include pull-up devices **1110**, **1111**, **1112**, and **1113**, respectively. The pull-up devices create the reference voltage levels and memory bit line voltage level for sensing multi-levels on the memory bit line.

[**0079**] The pull-up devices are defined on the reference voltage lines. A pull-up device is also defined on the bit lines in the memory array. The desired reference voltages VREF**0**, VREF**1**, and VREF**2** can be made by modifying the size and/or number of pull-ups such as field effect transistors and the like. The reference voltages are preferably at voltage levels corresponding to ones illustrated by **FIG. 16** for example. Preferably, the pull-ups are added at the point where reference signals (corresponding to reference voltages) feed directly into a sense amplifier circuit, and not on each bit line. Determining the appropriate pull-up device size can occur on a trial and error basis during the course of circuit simulation. Other types of pull-up devices or circuitry such as capacitor and resistor combinations, and the like may also be used. Of course, the type of pull-up device and its configuration depend upon the particular application.

[**0080**] The embodiment of **FIG. 18** generally provides a wider voltage range, than the embodiment of **FIG. 17**. The circuit for each reference voltage is no longer substantially dependent upon a maximum voltage range on the bit line. The effective voltage range can be scaled up across a wider range through use of selected pull-up devices. This provides for a greater margin of manufacture by the wider range between the voltages. The increased voltage range insures that an adequate signal is available to sense the difference between the memory bit line voltage and that of the reference voltage. As previously noted, the pull-up device is preferably a PMOS device and the like.

[**0081**] **FIG. 19** is a simplified voltage generator circuit diagram **1600** for obtaining reference voltages with use of

pull-up devices and a voltage divider according to a preferred embodiment of the present invention. A bit line column **1602** is also shown for illustrative purposes. The bit line column is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either **V0**, V1, V2, or **V3**, depending upon the particular application. The bit line also includes a field effect transistor **1102** and a word line **1616** operably coupled to the field effect transistor.

[**0082**] The voltage generator circuit diagram includes a plurality of reference voltage columns **1111**, **1112**, **1113**, a plurality of field effect transistors **1612**, **1614** coupled to SELECT lines, and a plurality of field effect transistors **1103**, **1104**, **1105**, **1106**, **1107**, **1108** in each cell coupled to a WORD line **1616**. Also shown are a plurality of pull-up devices **1111**, **1112**, and **1113** for a VREF**0** line **1604**, a VREF**1** line **1606**, and a VREF**2** line **1608**, respectively. The embodiment provides for a voltage divider arrangement such that each reference voltage tracks the bit line voltage in variations to process, temperature, voltage, and the like. In addition, the embodiment provides for each of the reference voltages VREF**0**, VREF**1**, and VREF**2** to be conditioned by way of respective pull-up devices. A pull-up device **1110** may also condition the voltage at the bit line **1602**.

[**0083**] **FIG. 20** illustrates a simplified reference voltage generator circuit diagram **2000** according to the present invention. A bit line **2009** with four memory cells **2001**, **2003**, **2005**, and **2007**, each of which is programmed to one of four different threshold voltages (V**0**, V1, V2, V3) representing the possible states in a two bit per cell memory array is shown for illustrative purposes. The bit line is operable coupled through field effect transistors in the memory cells **2001**, **2003**, **2005**, and **2007**. The bit line also includes a select line, and word lines **0**, **1**, **2**, and **3**.

[**0084**] The reference voltage generator circuit includes reference voltage lines **2013**, **2015**, and **2017**, for VREF**0**, VREF**1**, and VREF**2**, respectively. The reference voltage generator circuit includes cells **2019** which define a reference voltage array **2021**. The reference voltage array includes bit lines **2023** (or reference voltage lines **2013**, **2015**, and **2017**) which were preferably identical in fabrication to the bit lines such as the bit line **2009** in the memory array. For example, the bit lines **2023** in the reference voltage array and the memory array are made by way of the same (or similar) processing steps.

[**0085**] The cells **2019** in the reference voltage array are programmed to one of four possible voltage thresholds **V0**, V1, V2, and V3. Optionally, the bit line in the reference voltage array which contains cells programmed to the highest threshold voltage **V3** may be omitted, as cells programmed to a voltage threshold higher than the voltage on the word line will effectively be an open circuit. This memory bit line in the reference voltage array may be replaced by a voltage source, typically representing the highest voltage potential used in the particular integrated circuit.

[**0086**] In the present embodiment, the cell (or cells **2001**, **2003**, **2005**, and **2007**) in the memory array is programmed by way of a selected threshold voltage such as **V0** and the like. All of the cells in the reference voltage array using the same threshold voltage is preferably programmed at the same time (or the same method) as the cell (or cells) in the memory array. For example, a cell(s) **2001** at a threshold voltage of **V0** in the memory array is programmed by way of implant or the like at the same step as the cells **2025** at a threshold voltage of **V0** in the reference voltage array. The cell(s) **2003** at a threshold voltage of **V1** in the memory array is programmed by way of implant or the like at the same step as the cells **2027** at a threshold voltage of **V1** in the reference voltage array. The cell(s) **2005** at a threshold voltage of **V2** in the memory array is programmed by way of implant or the like at the same step as the cells **2029** at a threshold voltage of V2 in the reference voltage array. Other threshold voltages **2007** may be programmed into the cells by way of similar programming techniques and the like. The selected programming technique may include a single threshold voltage implant or multiple threshold voltage implants corresponding to a series programming steps. An example of such programming step can be any suitable technique known in the art.

[**0087**] The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

The invention claimed is:

1. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation for settling the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell by applying at least one programming pulse supplied to the bit line, and

wherein the program operation of the one non-volatile multi-level memory cell is carried out by a plurality of programming pulses, the plurality of programming pulses includes at least a first programming pulse and a second programming pulse after the first program-

ming pulse, the first programming pulse has a first electric parameter and the second programming pulse has a second electric parameter so that a first voltage threshold value change of the one non-volatile multi-level memory cell between after applying the first programming pulse and before applying the first programming pulse is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell between after applying the second programming pulse and before applying the second programming pulse.

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