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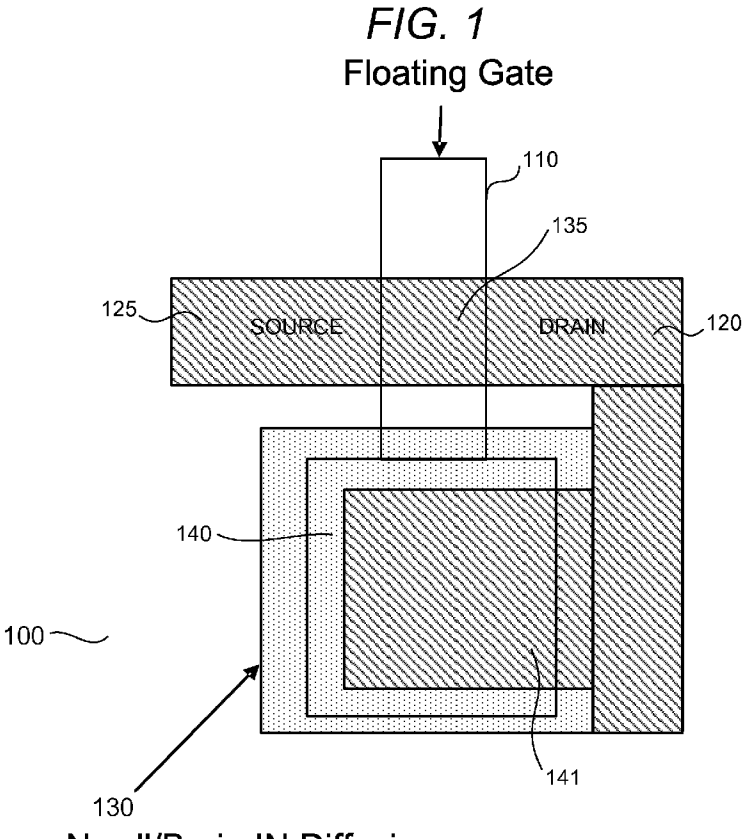
(54) Title: INTEGRATED CIRCUIT EMBEDDED WITH NON-VOLATILE ONE-TIME-PROGRAMMABLE AND MULTIPLE-TIME PROGRAMMABLE MEMORY



(57) Abstract: A programmable non-volatile device uses a floating gate that functions as a FET gate that overlaps a portion of a source/drain region. This allows a programming voltage for the device to be imparted to the floating gate through capacitive coupling, thus changing the state of the device. The invention can be used in environments such as data encryption, reference trimming, manufacturing ID, security ID, and many other applications.

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INTEGRATED CIRCUIT EMBEDDED WITH NON-VOLATILE ONE-TIME - PROGRAMMABLE AND MULTIPLE-TIME PROGRAMMABLE MEMORY

RELATED APPLICATION DATA

The present application claims the benefit under 35 U.S.C. 119(e) of the priority date of Provisional Application Serial no. 60/984,615 filed November 1, 2007 which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to non-volatile memories which can be programmed one time, or multiple times in some instances. The invention has particular applicability to applications where is it desirable to customize electronic circuits.

BACKGROUND

One time programmable (OTP) and multi-time programmable (MTP) memories have been recently introduced for beneficial use in a number of applications where customization is required for both digital and analog designs. These applications include data encryption, reference trimming, manufacturing ID, security ID, and many other applications. Incorporating OTP and MTP memories nonetheless typically comes at the expense of some additional processing steps.

An NMOS OTP implementation is disclosed by USP 6,920,067, incorporated by reference herein. The device in this reference is programmed with channel hot-hole-injection. The disclosure teaches that the device is programmed into conducting state, after the channel hot hole injection. However, it is unclear whether the device actually works in the way the inventors claim. That is, it is not apparent that the channel current will be initiated to induce hot-hole-injection since the state of the floating gate is unknown and there is no available means to couple a voltage unto the floating gate. An NMOS device will conduct a channel current to initiate the hot hole injection only when the floating gate potential is sufficient to turn on the

device, or when the threshold voltage is always low initially to allow channel current conduction. The only way to ensure either scenario is to introduce an additional process step to modify the turn on characteristics of the NMOS. Now assuming the channel is conducting initially and hot holes are injected, the holes injected on the floating gate will make the device more conductive. So the device basically goes from a conductive state (in order to initiate channel current for hot hole injection) to a highly conductive state. This is not a very optimal behavior for a memory device.

Another prior art device described in U.S. publication no. 2008/0186772 (incorporated by reference herein) shows a slightly different approach to the problem of providing a programming voltage to a floating gate embodiment of an OTP device. In this design, shown in FIG. 4, the drain border length L1 is increased relative to the source side length L1 to increase a coupling ratio to the eraseable floating gate 416. By increasing the coupling ratio, the amount of channel current is increased; therefore the charge injection into the floating gate will also increase. The drawbacks of this cell, however, include the fact that the cell and channel 412 must be asymmetric, and the coupling is only controlled using the length dimension of the active regions. Because of these limitations, it also does not appear to be extendable to a multi-level architecture. Moreover, it apparently is only implemented as a p-channel device.

Accordingly there is clearly a long-felt need for a floating gate type programmable memory which is capable of addressing these deficiencies in the prior art.

SUMMARY OF THE INVENTION

An object of the present invention, therefore, is to overcome the aforementioned limitations of the prior art.

A first aspect of the invention concerns a programmable non-volatile device situated on a substrate comprising: a floating gate; wherein the floating gate is comprised of a material that is also used as a gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory; a source region; and a drain region; and an n-type channel coupling the source region and drain region; wherein the drain region overlaps a sufficient portion of the gate such that a programming voltage for the device applied to the drain can be imparted to the floating gate through capacitive coupling.

Preferably the programming voltage is greater than 5 volts. In some instances the floating gate can be erased to allow for reprogramming. The floating gate is eraseable by an erase voltage applied to the source region.

The state of the floating gate can be determined by a read signal applied to the drain which is preferably less than about 1 volt.

The inventive device can be part of a programmable array embedded with separate logic circuits and/or memory circuits in an integrated circuit. The data stored in the memory can be used as a part of (or by) a data encryption circuit; a reference trimming circuit; a manufacturing ID; a security ID or other similar applications.

In some embodiments the capacitive coupling can be configured to place in a first trench situated in the substrate. A separate set of second trenches in the substrate can be used as embedded DRAM.

The programmable device can be coupled to a second programmable device in a paired latch arrangement such a datum and its compliment are stored in the paired latch.

In some embodiments the floating gate is being comprised of a material that includes impurities acting as charge storage sites and is also used as an insulating layer for other non-programmable devices situated on the substrate, such as an oxide. In other applications the floating gate is comprised of a material that is also shared by an interconnect and/or another gate for a transistor device also situated on the substrate and associated with

a logic gate and/or a volatile memory.

Another aspect of the invention concerns a one-time (OTP) or multi-time (MTP) programmable memory device incorporated on a silicon substrate with one or more other additional logic and/or non-OTP memory devices, characterized in that the OTP memory device has an n-type channel; any and all regions and structures of the OTP memory device are derived solely from corresponding regions and structures used as components of the additional logic and/or non-MTP/OTP memory devices.

Another aspect of the invention concerns a method of forming the above NV OTP/MPT device situated on a substrate comprising the following steps: forming a gate for non-volatile programmable memory device from a first layer; the first layer being shared by the non-volatile programmable memory device and at least one other device also situated on the substrate and associated with a logic gate and/or a volatile memory; forming a drain region; and capacitively coupling the gate with the drain region by overlapping a portion of the gate with the drain region.

As noted above, the first layer is preferably polysilicon, or an insulating layer which has impurities introduced during a source or drain implant step. The device is formed with n-type channel.

Preferably the non-volatile programmable memory device is embedded in a computing circuit and formed entirely by CMOS processing and masks used to form other logic and/or memory n-channel devices in the processing circuit.

The non-volatile memory can be programmed during manufacture if desired to store one or more identification codes for a wafer, and/or can be associated with one of the following: a data encryption circuit; a reference trimming circuit; a manufacturing ID; and/or a security ID.

In other embodiments all regions and structures of the OTP memory device are formed in common with corresponding regions and structures used as components of the additional logic and/or non-OTP memory devices.

A further aspect concerns a method of operating a non-volatile programmable (NVP) device situated on a substrate comprising: providing a floating gate, which floating gate is comprised of a layer and material that is shared by gates of at least some other non-NVP devices on the substrate;

programming the NVP device to a first state with channel hot electrons that alter a voltage threshold of a floating gate; reading the first state in the OTP device using a bias current to detect the voltage threshold; and erasing the NVP device with band-band tunneling hot hole injection.

In preferred embodiments the floating gate is comprised of a material that is also used as a gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory. A substantial portion of the programming voltage applied to the drain is also imparted to the floating gate through the capacitive coupling. In preferred embodiments the threshold of the floating gate is set by a current of channel hot electrons to store data in the OTP device.

It will be understood from the Detailed Description that the inventions can be implemented in a multitude of different embodiments. Furthermore, it will be readily appreciated by skilled artisans that such different embodiments will likely include only one or more of the aforementioned objects of the present inventions. Thus, the absence of one or more of such characteristics in any particular embodiment should not be construed as limiting the scope of the present inventions. While described in the context of a non-volatile memory array, it will be apparent to those skilled in the art that the present teachings could be used in any number of applications.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a top down view of a preferred embodiment of a non-volatile memory cell of the present invention;

FIG. 2 is a side cross section view of the preferred non-volatile memory cell;

FIG. 3 is an electrical diagram illustrating the electrical relationship of the structures of the preferred non-volatile memory cell;

FIG. 4 depicts a prior art non-volatile memory cell which uses a floating gate for an OTP application;

FIG. 5 is an electrical diagram showing a preferred embodiment of a latch circuit constructed with the NV memory cells of the present invention.

DETAILED DESCRIPTION

The present disclosure concerns a new type of non-volatile memory device structure (preferably single poly) that can be operated either as an OTP (one time programmable) or as an MTP (multiple time programmable) memory cell. The preferred device structure is fully compatible with advanced CMOS logic process, and would require, at the worst case, very minimal additional steps to implement.

A unique aspect of the present device is that the floating gate of the memory cell structure is electrically coupled strongly through one of the S/D junctions of the transistor, whereas traditional single poly nonvolatile memory cells require either an additional interconnect layer to couple to the floating gate, or the floating gate has virtually none or minimal electrical coupling to any of the existing electrical signals. Moreover, unlike the 2008/0186772 reference, the coupling ratio can be more specific and precise. That is, by exactly controlling the coupling ratio (through areal means) the amount of charge, and thus the final programmed Vt, are directly proportional to the product of the coupling ratio and the drain voltage. It can be more precisely controlled such that the coupling ratio is dictated or designed by the desired programming threshold level (V_t) of the memory cell. This allows for a design that evolves easily into a multi-level version of an OTP since different coupling ratios yield different programmed V_t.

FIG. 1 illustrates the top view of the layout of a preferred structure used in the present invention. FIG. 2 illustrates a representative cross-sectional view of the device structure. It will be understood that these drawings are not intended to be set out to scale, and some aspects of the device have been omitted for clarity.

The device includes a typical NMOS transistor 100 which is modified so that the gate (poly in a preferred embodiment) 110 of the device is not electrically connected to a voltage source. A drain 120 of the device is bent around and is preferably joined by an N-type well 130 that typically already exists in a conventional advanced CMOS process. As an alternative, the N-Well 130 can be replaced with an n-type diffusion layer introduced so as to be beneath the poly floating gate. A conventional source region 125 is also utilized.

The floating gate poly 110 is extended beyond a typical transistor channel region 135 and includes an overlap region 140 which overlaps an active region extending from the drain junction. The active region portion 141 that is surrounded by the N-Well region serves as an effective capacitive coupling to the floating gate. Thus any voltage applied to the drain junction will be effectively coupled onto the floating gate.

As seen in the electrical diagram of FIG. 3, if the coupling ratio of the drain to the floating gate is sufficiently high – which is determined by the ratio of the area of the gate channel region and the area of the Poly extension overlapping the drain extension region - the floating gate can effectively acquire and have a high percentage of the value of the drain voltage.

A key advantage of the preferred embodiment, as seen in FIGs. 1 and 2, is that it is formed from same layers conventionally used to make active n-channel devices in a CMOS process. The only difference is that the poly (or metal as the case may be) gate layer is not interconnected with such other formed active devices or coupled to a gate signal. The other implants for the source/drain are also part of a CMOS conventional process. Thus, in most applications the invention can be integrated without any additional processing costs, because the only alteration is to an existing mask for each relevant layer of the wafer being processed.

One other optional variation of this device structure is to make the drain-to-gate coupling capacitor area on the sidewall of a trench. This will greatly reduce the area of the drain-to-gate coupling capacitor. This reduction in cell area may come at the expense of significantly increase the manufacturing process complexity. However, again, in applications where the invention is integrated with certain types of DRAM architectures (especially embedded types), it is possible to incorporate the conventional processing steps for such memories to avoid additional processing costs. Other techniques for coupling a voltage to the floating gate and achieving a desired coupling ratio will be apparent to those skilled in the art.

While the floating gate is shown as a single polysilicon layer, it will be appreciated by skilled artisans that other materials could be used as well. In some applications for example it may be possible to exploit the formation of other structures/devices which while part of other main underlying

logic/memory structures, can be exploited for purposes of making a floating gate of some kind. In this respect it should be noted that floating gates can typically be formed of a number of different materials, including through techniques in which impurities are implanted/diffused into a dielectric/insulating layer.

Moreover while the preferred embodiment depicts the NVM cell as part of a conventional lateral - planar FET structure on a substrate, it will be apparent to those skilled in the art that other geometries/architectures can be used, including non-planar structures. Thus the invention could be used in SOI substrates, in thin film structures, at other levels of the device than the substrate, in multi-gate (FINFET type) orientations, and in vertical/non-planar configurations. In such latter instances the floating gate would be embedded and oriented vertically with respect to the substrate.

The preferred operation of device 100 will be described. The non-volatile device structure preferably has the physical features of a conventional I/O transistor implemented in an advanced CMOS logic process. At present, such I/O transistor is nominally operated at 3.3V but it will be understood that this value will change with successive generations of manufacturing.

This type of I/O transistor typically has a threshold voltage of 0.5V to 0.7V, with a typical electrical gate oxide thickness of 70A. With a drain coupling to floating gate ratio of 0.90, and a read drain voltage of 1.0V applied to the device, the floating gate will effectively be coupled with a voltage of about 0.90V. This is sufficient to turn on the un-programmed NMOS device 100, and a channel current can be detected by typical means of sense circuitry to identify the state of the device. It will be understood to those skilled in the art that the particular coupling ratio, read voltage, etc., will vary from application to application and can be configured based on desired device operating characteristics.

The device is originally in a unprogrammed state, which in the preferred embodiment is characterized by a low resistance coupling between the source and drain through channel region 135. This means that the channel region 135 can be substantially uniform and current flow is reliable. While the preferred embodiment is shown in the form of a symmetric cell/channel, it will be understood that the invention could be used in non-

symmetric forms such as shown in the aforementioned 20080186722 publication.

To program the device into a programmed state, the device must be shut off by reducing carriers in the channel region, and increasing the threshold voltage. To do this a drain voltage of 6.0V can be applied and this will effectively couple a voltage of about 5.4V to the floating gate. This bias condition will placed the device into a channel hot electron injection regime. The electrons injected into the floating gate effectively increase the threshold voltage of the device. When a subsequent read voltage of 1.0V is applied again on the drain, the device does not conduct current due to its high threshold voltage, and this second state of the device is thus determined. As with the read characteristics, it will be understood to those skilled in the art that the particular coupling ratio, program voltage, etc., will vary from application to application and can be configured based on desired device operating characteristics.

The prior art referred to above is primarily a one time programmable device, since there is no disclosed mechanism for removing the charge on the floating gate. In contrast, some embodiments of the present invention can be made to be capable of multiple-time-programming. To do this, an erase operation can be introduced to remove or neutralize the electrons that have been injected into the floating gate. The mechanism for removing or neutralizing electrons is preferably through band-band tunneling hot hole injection from the other non-coupling junction 125 of the device. The preferred bias condition would be as followed: the non-coupling junction (source junction) is biased with 6V to cause the junction to initiate band-band tunneling current. The band-band tunneling current causes hot holes to be injected into the floating gate and neutralize the electrons that are stored on the floating gate. Thus it is (re)programmed from a non-conducting, or even a low conducting state, into a conducting state. The device is then able to conduct channel current when a subsequent read voltage is applied to the coupling junction during the read operation. It will be understood that programming from a low conducting state to a conducting state may have a limited operating sense window.

As an additional optional operation, to facilitate erase operation and

enhance band-band tunneling current, the coupling junction can be supplied with a negative voltage so that the floating gate is made more negative to cause higher band-band tunneling current across the source junction.

Thus the operating characteristics are preferably as follows:

OPERATION	Drain	Source	Substrate
Program	6.0V	0V	0V
Read	1.0V	0V	0V
Erase	Float or –Vcc	6.0V	0V

In some embodiments, additional protection can be implemented to ensure the OTP and MTP device have sufficient immunity against the loss of charge stored on the floating gate. To do this, the device can be configured into a paired latch 500 – as shown in FIG. 5 - where the data and its complement are stored into the latch, thus effectively doubling the margin in the stored data. As seen therein, a top device 510 couples a node 530 to a first voltage reference (Vcc) while a second bottom device 520 couples the node to a second voltage reference (Vss). By placing charge on the top device floating gate, the top device 510 is programmed into a non-conductive state, thus ensuring that node 530 is pulled down by bottom device 520 to Vss, representing a first logical data value (0). Similarly, by placing charge on the bottom device floating gate, the bottom device 520 is programmed into a non-conductive state, thus ensuring that node 530 is pulled up by top device 510 to Vcc, representing a second logical data value (1).

Another useful advantage of the present preferred embodiment is that it is implemented with an NMOS device structure, whereas most traditional single-poly OTPs are commonly implemented with a PMOS device structure. This means that the device can be formed at the same time as other n-channel devices on a wafer. Another advantage of an NMOS device structure in this invention is that it behaves similar to an EPROM device, i.e., the device is programmed into a non-conducting state from a conducting state. In contrast, the prior art 20080186722 type device – and other commonly used PMOS OTP devices - are programmed from a non-conducting state into a conducting state. This aspect of the invention thus can eliminate the need of an additional masking step that is commonly associated with a PMOS OTP device in order to make sure that PMOS device is in a non-conducting state

coming out of the manufacturing fab.

In addition, since an NMOS device's programming mechanism with channel hot electrons injection is self-limiting, unlike that case of a PMOS with channel hot electron programming, the amount of energy consumption during programming is self-limited for this invention.

As seen in the present description therefore, the particular configuration of the floating gate is not critical. All that is required is that it be structurally and electrically configured to control channel conduction and also be capacitively coupled to an electrical source of charge carriers. The particular geometry can be varied in accordance with any desired layout or mask. In some instances it may be desirable to implement the floating gate as a multi-level structure for example. Moreover, since capacitive coupling is a function of the materials used, the invention allows for significant flexibility as the composition of the floating gate can also be varied as desired to accommodate and be integrated into a particular process. An array of cells constructed in accordance with the present teachings could include different shapes and sizes of floating gates so that cells having threshold cells could be created.

The above descriptions are intended as merely illustrative embodiments of the proposed inventions. It is understood that the protection afforded the present invention also comprehends and extends to embodiments different from those above, but which fall within the scope of the present claims.

What is claimed is:

1. A programmable non-volatile device situated on a substrate comprising:
   a floating gate;
   wherein said floating gate is comprised of a material that is also used as a gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory;
   a source region; and
   a drain region; and
   an n-type channel coupling said source region and drain region;
   wherein the drain region overlaps a sufficient portion of said gate such that a programming voltage for the device applied to said drain can be imparted to said floating gate through capacitive coupling.

2. The programmable device of claim 1 wherein said programming voltage is greater than 5 volts.
3. The programmable device of claim 1 wherein said floating gate can be erased.
4. The programmable device of claim 3 wherein said device can be re-programmed.
5. The programmable device of claim 3 wherein said floating gate is eraseable by an erase voltage applied to said source region.
6. The programmable device of claim 1 wherein a state of said floating gate can be determined by a read signal applied to said drain.
7. The programmable device of claim 1, wherein said read signal is less than about 1 volt.
8. The programmable device of claim 1 wherein said device is part of a programmable array embedded with separate logic circuits and/or memory circuits in an integrated circuit.
9. The programmable device of claim 8 wherein said device is associated with one of the following: a data encryption circuit; a reference trimming circuit; a manufacturing ID; and/or a security ID.
10. The programmable device of claim 1, wherein said capacitive coupling takes place in a first trench situated in the substrate.
11. The programmable device of claim 10, wherein a set of second trenches in said substrate are used as embedded DRAM.

12. The programmable device of claim 11, further including a second programmable device coupled in a paired latch arrangement such that a datum and its complement are stored in said paired latch.

13. A programmable device situated on a substrate comprising:

a floating gate; said floating gate being comprised of a material that includes impurities acting as charge storage sites and is also used as an insulating layer for other non-programmable devices situated on the substrate;

a source region; and

a drain region; and

an n-type channel coupling said source region and drain region;

wherein the drain region overlaps a sufficient portion of said gate such that a programming voltage applied to said drain can be imparted to said floating gate through capacitive coupling.

14. A one-time programmable (OTP) device situated on a substrate comprising:

a floating gate;

wherein said floating gate is comprised of a material that is also shared by an interconnect and/or another gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory;

a source region; and

a drain region overlapping a portion of said floating gate and capacitively coupled thereto; and

an n-type channel coupling said source region and drain region;

wherein a threshold of said floating gate can be permanently altered by channel hot electrons to store data in the OTP device.

15. A one-time programmable (OTP) memory device incorporated on a silicon substrate with one or more other additional logic and/or non-OTP memory devices, characterized in that:

a. said OTP memory device has an n-type channel;

b. any and all regions and structures of said OTP memory device are derived solely from corresponding regions and structures used as components of the additional logic and/or non-OTP memory devices.

16. A programmable memory device with a gate, an n-type impurity source and an n-type impurity drain on a silicon substrate comprising:

an n-type channel; and

wherein the n-type impurity drain overlaps a sufficient portion of said gate such that a programming voltage applied to said n-type impurity drain can be imparted to said gate through capacitive coupling;

said gate being adapted to function as a floating gate so that the device has a programmed state defined by an amount of charge stored on said gate by said programming voltage;

further wherein said charge on said floating gate can be erased so as to permit the device to be re-programmed.

17. A one-time programmable (OTP) memory device with a gate, an n-type impurity source and an n-type impurity drain on a silicon substrate comprising:

an n-type channel; and

wherein the n-type impurity drain overlaps a sufficient portion of said gate such that a voltage applied to said n-type impurity drain can be imparted to said gate through capacitive coupling;

said gate being adapted so that the OTP device has a programmed state defined by a charge state of said gate.

18. A method of forming a non-volatile programmable memory device situated on a substrate comprising:

forming a gate for non-volatile programmable memory device from a first layer;

wherein said first layer is shared by the non-volatile programmable memory device and at least one other device also situated on the substrate and associated with a logic gate and/or a volatile memory;

forming a drain region; and

capacitively coupling said gate with said drain region by overlapping a portion of said gate with said drain region.

19. The method of claim 18 wherein said first layer is polysilicon.

20. The method of claim 18 wherein said first layer is an insulating layer.

21. The method of claim 20 wherein said gate further includes impurities, which impurities are introduced during a source or drain implant step.

22. The method of claim 18 wherein said device is formed with n-type channel.

23. The method of claim 18 wherein said non-volatile programmable memory device is embedded in a computing circuit and formed entirely by masks used to form other logic and/or memory n-channel devices in said processing circuit.

24. The method of claim 23 wherein said non-volatile programmable memory device is embedded in a computing circuit and formed entirely by CMOS processing steps used to form other logic and/or memory devices in said computing circuit.

25. The method of claim 18 wherein said non-volatile programmable memory device is associated with one of the following: a data encryption circuit; a reference trimming circuit; a manufacturing ID; and/or a security ID.
26. The method of claim 1, wherein said capacitive coupling takes place in a first trench situated in the substrate.
27. The method of claim 26 wherein a set of second trenches in said substrate are used as embedded DRAM.
28. The method of claim 18 further including a step: forming a second programmable device coupled in a paired latch arrangement such a datum and its compliment can be stored in said paired latch.
29. The method of claim 18 wherein said non-volatile programmable memory device can only be programmed once.
30. The method of claim 18 wherein said non-volatile programmable memory device can be erased and re-programmed.
31. The method of claim 18 wherein said non-volatile programmable memory device is used to store an identification code for a wafer.
32. The method of claim 18 further including a step: programming said non-volatile programmable memory device during manufacture of a wafer to store an identification code.
33. The method of claim 31 further including a step: programming a second non-volatile programmable memory device during manufacture of the wafer to store a second identification code.
34. The method of claim 18 wherein said non-volatile programmable memory device has a non-conducting channel at a completion of manufacturing of such device.
35. The method of claim 18 wherein said non-volatile programmable memory device is part of an array.

36. A method of forming a one-time programmable (OTP) memory device incorporated on a silicon substrate with one or more other additional logic and/or non-OTP memory devices, characterized in that:

a. said OTP memory device is formed with an n-type channel;

b. any and all regions and structures of said OTP memory device are formed in common with corresponding regions and structures used as components of the additional logic and/or non-OTP memory devices.

37. A method of forming a one-time programmable (OTP) memory device with a gate, an n-type impurity source and an n-type impurity drain on a silicon substrate comprising:

forming an n-type channel; and

forming the n-type impurity drain to overlap a sufficient portion of said gate such that a voltage applied to said n-type impurity drain can be imparted to said gate through capacitive coupling;

forming said gate as a floating gate so that the OTP device has a programmed state defined by a charge state of said gate.

38. A method of operating a non-volatile programmable (NVP) device situated on a substrate comprising:

providing a floating gate, which floating gate is comprised of a layer and material that is shared by gates of at least some other non-NVP devices on said substrate;

programming the NVP device to a first state with channel hot electrons that alter a voltage threshold of a floating gate;

reading the first state in the OTP device using a bias current to detect said voltage threshold; and

erasing the NVP device with band-band tunneling hot hole injection.

39. A method of operating a programmable non-volatile device comprising:

providing a floating gate;

wherein said floating gate is comprised of a material that is also used as a gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory;

providing a source region; and

providing a drain region; and

providing an n-type channel coupling said source region and drain region;

capacitively coupling a portion of said gate to said drain;

providing a programming voltage to said drain, wherein a substantial portion of said programming voltage is also imparted to said floating gate through said capacitive coupling.

40. A method of operating a one-time programmable (OTP) device situated on a substrate comprising:

providing a floating gate;

wherein said floating gate is comprised of a material that is also shared by an interconnect and/or another gate for a transistor device also situated on the substrate and associated with a logic gate and/or a volatile memory;

providing a source region; and

providing a drain region overlapping a portion of said floating gate and capacitively coupled thereto; and

an n-type channel coupling said source region and drain region;

setting a threshold of said floating gate by a current of channel hot electrons to store data in the OTP device.

FIG. 1

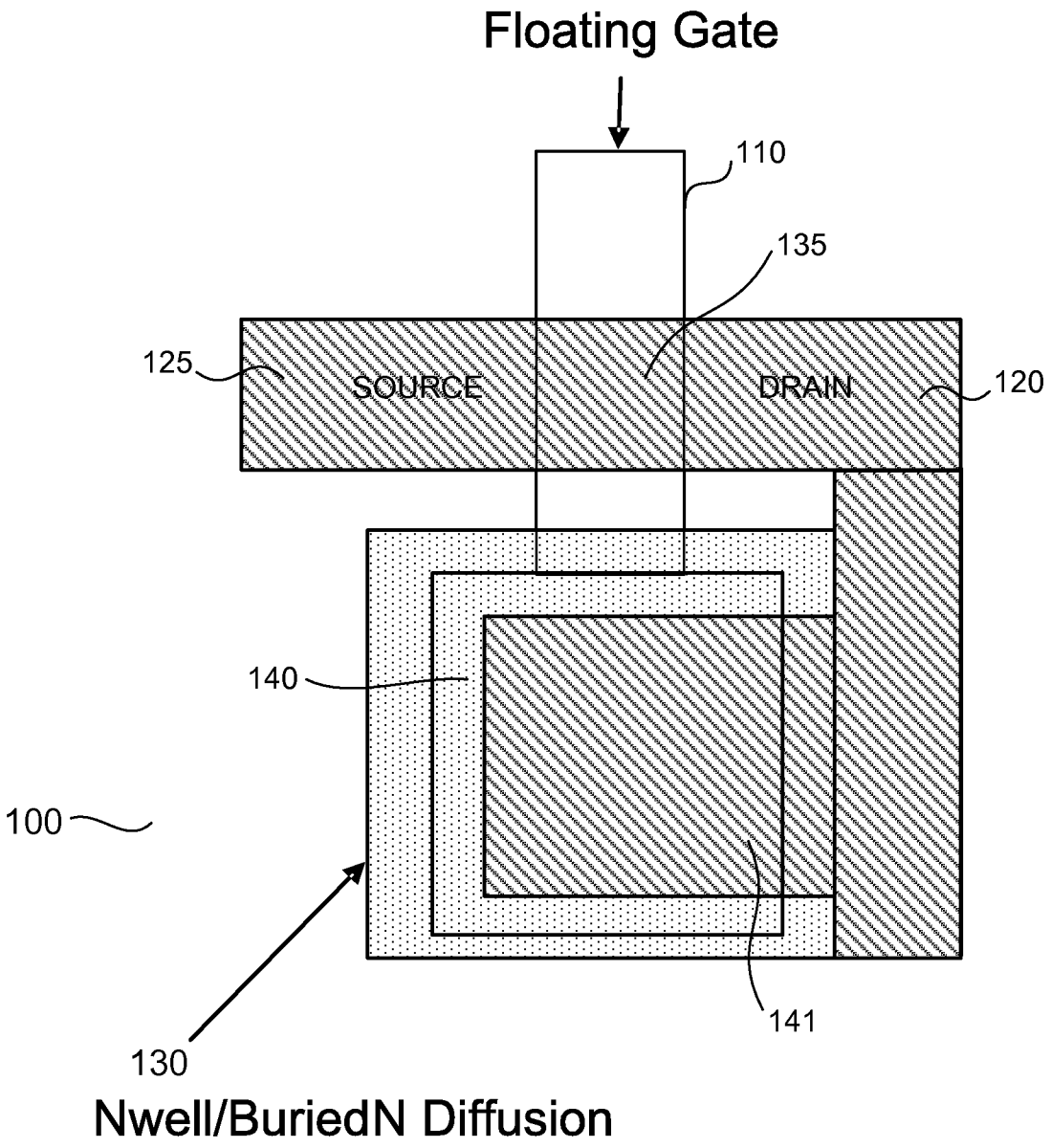

Floating Gate
110
135
125
SOURCE
DRAIN
120
140
100
141
130
Nwell/BuriedN Diffusion

FIG. 2

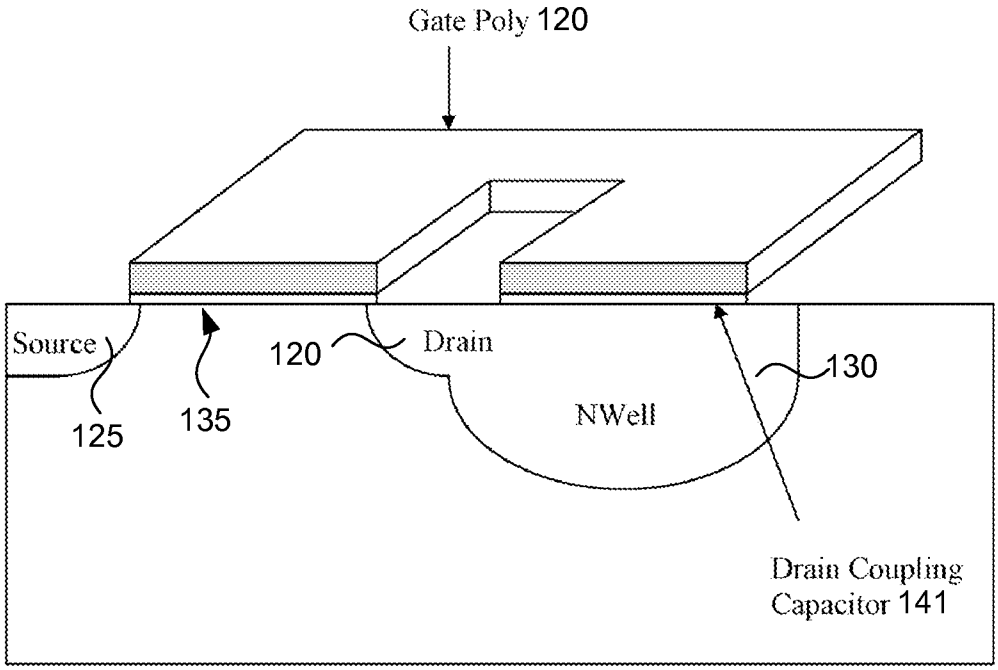

Gate Poly 120
Source
125
135
120
Drain
NWell
130
Drain Coupling
Capacitor 141

FIG. 3

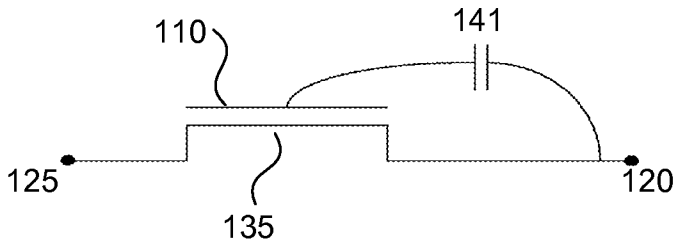
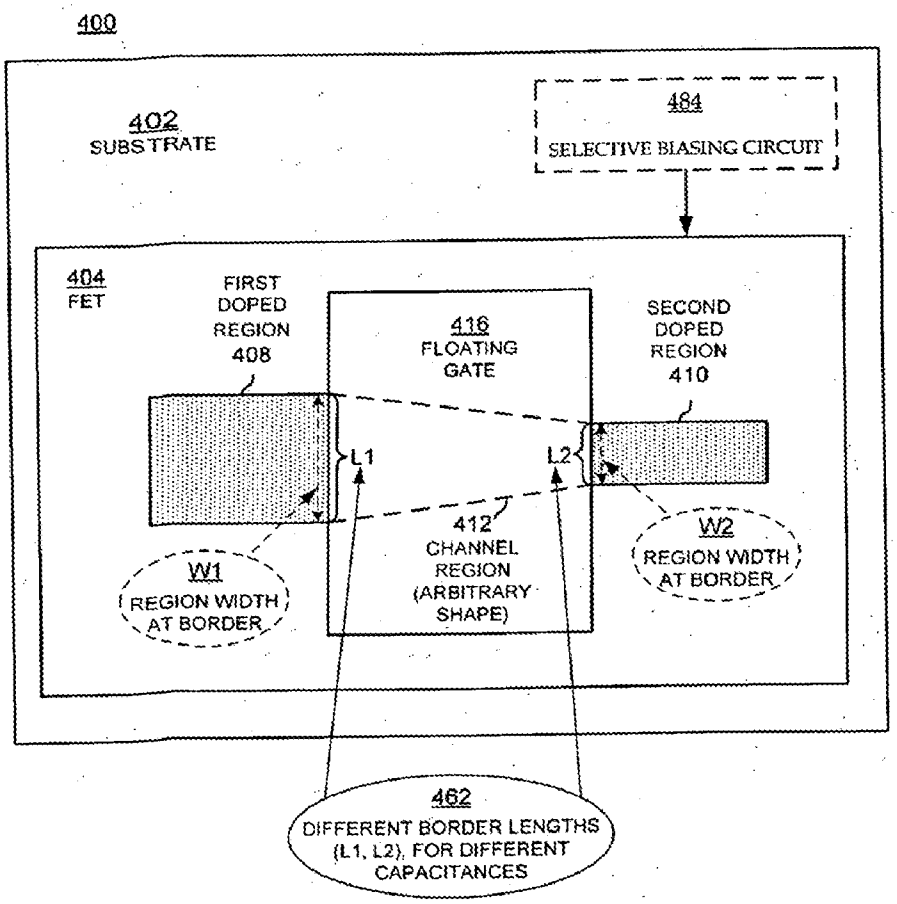
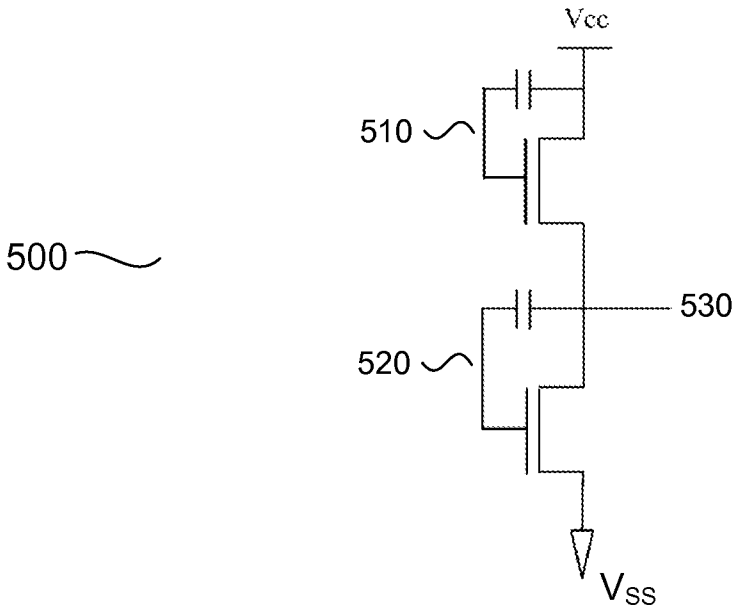


FIG. 4
Prior Art



NON-VOLATILE MEMORY CELL WITH ASYMMETRIC FET

FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/82294

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G11C 17/18 (2008.04)
USPC - 365/225.7
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 365/225.7

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 365/225.7, 185.01, 189.011 (View search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar
Search terms: substrate, insulate, floating gate, transistor, logic gate, volatile memory, source, drain, n-type channel, capacitive coupling, erase, reprogram, read, circuit, encryption, reference trimming, manufacturing ID, security ID, trench, channel, DRAM, etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/0067124 A1 (Lee et al.) 30 March 2006 (30.03.2006) (abstract, para [0006], [0011], [0016], [0031], [0032], [0033], [0034], [0041], [0043], [0044], [0052])	1 - 40
A	US 2007/0247902 A1 (Chen et al.) 25 October 2007 (25.10.2007) (abstract, para [018], [0019], [0020], [0026], [0027], [0054], [0056], [0057])	1 - 40

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 December 2008 (10.12.2008)	19 DEC 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)