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(54) **Title:** METHODS AND APPARATUS FOR SUPPLY VOLTAGE TRANSIENT PROTECTION

(57) **Abstract:** Methods and apparatus for an integrated circuit that includes a supply voltage transient detection module (102) to activate a hold output signal (HOLD_OUT) that causes the output (109) to remain in its present state and to activate a hold processing signal (HOLD_PROC) that causes a signal processing module (106) to remain in its present state. In one embodiment, the output remains in that state until the supply voltage returns to a normal operating range and the hold signal transitions to an inactive state.

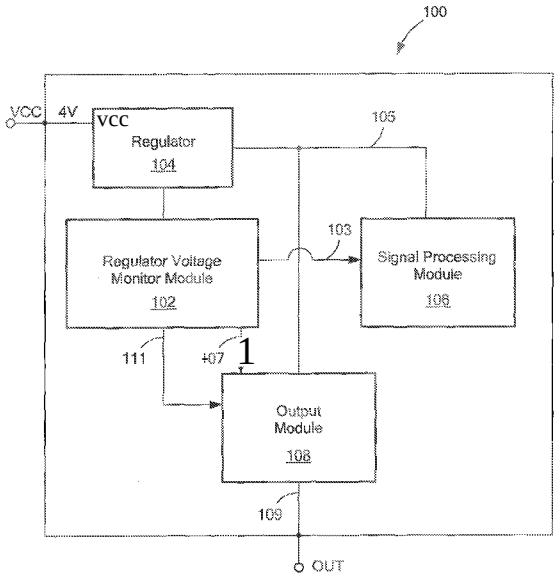


FIG. 1

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METHODS AMD APPARATUS FOR SUPPLY VOLTAGE TRANSIENT PROTECTION

BACKGROUND

[0001] As is known in the art, integrated circuits (ICs) in a package and/or circuit board typically require a regulated supply voltage to enable operation. Voltage transients, such as voltage drops, in a regulator output voltage, for example, can cause outputs and/or signal processing cirojitry to reset or transition to unknown processing states and/or output states. For relatively minor transients, it may be desirable to prevent a reset from occurring. For example, in certain applications, such as vehicle power systems, the environment is inherently noisy. In addition, test protocols can require testing the response of a sensor and/or IC to supply voltage transients. In such environments, it is undesirable to reset a sensor and/or IC for relatively minor voltage transients.

SUMMARY

[0002] Embodiments of the present invention provide methods and apparatus for an integrated circuit that includes a supply voltage transient detection module to activate a hold signal that causes the output to remain in its present state. In one embodiment, the output remains in that state until the supply voltage returns to a normal operating range and the hold signal transitions to an inactive state. With this arrangement, transient supply voltage drops do not reset the output. While exemplary embodiments of the invention are shown and described in conjunction with certain types of ICs, it is understood that embodiments of the invention are applicable to circuits in general for which It. Is desirable to prevent supply voltage transients from resetting output signals and/or interrupthg internal signal processing.

[0003] In one aspect of the invention, a sensor comprises a regulator voltage monitor module to receive a regulated output voltage and transition a first hold signal to an active state when the regulated output voltage drops below a first threshold and transition a second hold signal to an active state when the regulated output voltage drops below a second threshold, a signal processing module to receive the first hold signal from the regulator voltage monitor module and hold processing in a state corresponding to a time the first hold signal transitions to the active state, and an output module for outputni ng a sensor output signal, the output module to receive the second hold signal from the

regulator voltage monitor module and to maintain a state of the sensor output signal at the time the second hold signal transitions to an active state.

[0004] The sensor *can* further including one or more of die following features: the regulator voltage monitor is configured to generate a third hold signal for the output module to cause the output module to transition the sensor output signal to a high impedance state, the third hold signal to transition to an active state when the regulator voltage drops below a third threshold lower than the first threshold, the first and. second thresholds are the same, a regulator to provide die regulated output voltage, the first hold signal remains in the active state until the regulated voltage signal rises above the first threshold, the sensor resets *when* the regulated output voltage drops below a reset threshold voltage level, a magnetic field sensor, and/or a signal processing module includes at least one counter that does sot change in value during a time in which the first hold signal is in die active state,

[0005] In another aspect of the invention, a sensor comprises a regulator voltage monitor means to receive a regulated output voltage and transition a first hold signal to an active state when the regulated output voltage drops below a first threshold and transition a second hold signal to an active state when the regulated output voltage drops below a second threshold, a signal processing means to receive the first hold signal from the regulator voltage monitor means and hold processing in a state corresponding to a time the first hold signal transitions to the active state, and an output means for outputting a sensor output signal, the output module to receive the second hold signal .from the regulator voltage monitor means and to maintain a state of the sensor output signal at the time the second hold signal transitions to an active state. The sensor can further include an output switch and/or signal processing means comprising a magnetic field sensor.

[0006] In a further aspect of the invention, a method comprises receiving a regulated output voltage, transitioning a first hold signal to an active state when the regulated output voltage drops below a .first threshold, transitioning a second hold signal to an active state when the regulated output voltage drops below a second threshold, receiving the first hold signal and holding signal processing in a state corresponding to a time at which the first hold signal transitioned to the active state, receiving the second hold signal, and outputting

a sensor output signal for a sensor and maintaining a state of the sensor output signal present at the time at which the second hold signal transitioned to the active state.

[0007] The method can flirther include one or more of the following features: generating a third hold signal to transition the sensor output signal to a high impedance state, tire third hoid signal to transition to an active state when the regulator voltage drops below a third threshold lower than the first threshold, the first and second thresholds are the same, the first hold signal ren.iai.ns in the active state until the regulated voltage signal rises above the first threshold, the sensor resets when the regulated output voltage drops below a reset threshold voltage level, processing information from a magnetic field sensor; and/or the signal processing includes at least one counter that does not change in value during a time in which the first hold signal is in the active state,

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following description of the drawings in which:

[0009] FIG. 1 shows an exemplary integrated circuit having voltage supply monitoring in accordance with exemplary embodiments of the invention;

[0010] FIG. 1A shows an alternative integrated circuit having voltage supply monitoring in accordance with exemplary embodiments of dic invention;

[0011] FIG. 1B shows a further alternative integrated circuit having voltage supply monitoring in accordance with exemplary embodiments of the invention;

[0012] FIG. 2 is a timing diagram of signals to provide voltage supply monitoring in accordance with cxc.rn.pMy embodiments of the invention;

[0013] FIG. 3 is a schematic representation of an exemplary embodiment to generate hold signals for voltage supply monitoring in accordance with exemplary erxibodinients of the invention;

[0014] FIG. 4 is an exemplary schematic representation of voltage supply monitoring in accordance with exemplary embodiments of the invention; and

[0015] FIG, 5 is an exemplary schematic implementation of voltage supply monitoring in accordance with exemplary embodiments of the invention.

DETAILED DESCRIPTION

[0016] FIG.1 shows an exemplary integrated circuit (IC) 100 having a regulator voltage monitor module 102 coupled to a regulator 104 in accordance with exemplary embodiments of the invention. The regulator 104 is coupled to a supply voltage signal, such as a 4V VCC signal, to provide a regulated voltage 105 to the regulator voltage monitoring module 102, a signal processing module 106, an output module 108, and other circuitry requiring a regulated voltage.

[0017] The regulator voltage monitor module 102 generates a hold processing signal 103 for the signal processing module 106 and a hold output signal 107 for the output module 108, which provides the IC output signal 109. It is the understood that the hold processing signal 103 and the hold output signal 107 can be generated as distinct signals having different thresholds and/or timing, or can be essentially the same signal. In one embodiment, the regulator voltage monitoring module 102 generates an optional high out signal 111 for the output module 108. When the high out signal 111 goes active, the output signal 109 goes to a high impedance state. In an alternative embodiment shown in FIG. 1A, the signal processing module 106' generates a hold output signal 112 and/or a high out signal 111' for the output module 108'.

[0018] It is understood that the regulator can be external to the IC, as shown in FIG. 1B. In addition, it should be understood that some supplies, such as a battery, are sufficiently stable without any explicit regulator circuitry.

[0019] In general, exemplary embodiments of the present invention prevent a transient drop in the voltage regulator output 105 from causing output errors. It Is understood that a full reset may cause an output error in many situations, but preventing the reset doesn't necessarily prevent output errors. It is further understood that a partial reset does not always cause an error.

[0020] If the voltage regulator output 105 drops below a hold threshold the regulator voltage **monitor** module 102 **transitions** the hold output signal 107 to an active state so that the current output state of the output module 108 is maintained until the voltage regulator output 105 rises above the hold threshold or other threshold, as determined by the regulator voltage monitor module 102. The **regulator** voltage monitor module 102 also **transitions the** hold **processing** signal 103 sent to the signal processing module 106. Processing in the signal processing **module** 106, which can **include** a state .machine, can be maintained at the present state instead of resetting,, as in **conventional** sensors. By preventing a reset of the device due to a relatively minor voltage **transient, signal** processing can continue when the voltage regulator **output** 105 **returns** to normal voltage levels. If the voltage regulator output 105 drops **further** to below an optional high **impedance** threshold **the** high out signal 111 becomes active and the **output** module 108 transitions the output signal 109 to a high Impedance state.

[0021j FIG. 2, in conjunction with the diagram of FIG. 1, shows an **exemplary** signal diagram including a regulator output voltage signal Vregout (105) having a transient drop TD. in an exemplary embodiment, when the regulator output voltage Vregout (105) fails below a first down threshold **THH,** the hold **output** signal **HOLD__OUT** (107), **which** is coupled to the output module 108, **transitions** to **an** active state. The hold processing **signal** HOLD_PROC (103), which can have the same or different threshold as the hold **output** signal HOLD_OUT, also transitions to **an active** state. In response to the **transition** of the hold output signal HOLD__OUT, the output module 108 holds the output signal OUT (109) in its present state. While a **further** and/or sustained drop in the voltage regulator output Vregout (**105)** below a reset **threshold** THR will reset the **device,** which is desired, **transient** voltage drops will not reset the device to allow continued operation as the transient dissipates,

[0022] If the regulator voltage Vregout falls below a second down threshold THI, the optional high out signal **HI_OUT** (111) is activated to cause the output module 108 to transition the output 109 to a high impedance state. It *is* understood that without the second down threshold **THI,** the output **signal** OUT would not go to a high **impedance**

state, but rather, would remain in the state at the time the voltage regulator output Vregout goes below the first down threshold THH.

[0023] A power valid POK signal is also shown to indicate that the transient drop in the voltage regulator output 105 should not reset the device. In the illustrated embodiment, the POK signal does not transition since the transient is not significant enough to reset the device. In general, a voltage drop below THE. will reset the device. The threshold for THE. should he set for a voltage drop of a level and duration such that the internal circuit states, e.g., a value held in a flip-flop, cannot he trusted. This level and duration depends on details of process and circuit implementation, as will he readily appreciated by one of ordinary skill in the art,

[0024] An exemplary DIFF signal, which is described below, is also shown having a dip during the regulator output transient.

[0025] It is understood that a variety of circuits well known to one of ordinary skill in the art can be used to monitor and detect the voltage regulator output dropping below one or more thresholds.

[0026] FIG. 3 shows an exemplary circuit to detect a voltage drop of the regulator output voltage Vregout below a given threshold. A first comparator 300 receives the voltage regulator output Vregout and a voltage VOLT_THH set to the first down threshold THH (see FIG. 2), which defines the voltage below which the hold output signal HOLD_OUT (107) should become active. The output of the first comparator 300 provides the hold output signal HOLD_OUT (107) to the output module 108.

[0027] Similarly, if the voltage regulator output Vregout drops below a high impedance threshold VOLT_THL the output of a second comparator 302 transitions to activate a high out signal HI_OUT (111) *causing the output* module 108 to transition the output signal 109 to a high impedance state

[0028] A further comparator 304 can he used to generate a HOLD_PROC signal (103) that has a different threshold VOLT_THP than for the HOLD_OUT signal. As shown in

FIG, 1, a hold output signal 107 is provided to the output module 108 and a bold processing signal 103 is provided to the signal processing module 106,

[0029] In other embodiments, transient voltage drops in the regulator output voltage are handled in a variety of ways. For example, a hold signal can he active for a predetermined duration, an event, such as teeth counts, or the like. In another embodiment, further processing of input signals, such as from magnetic sensor elements, e.g., Hall elements, can be prevented. hn a further embodiment, an oscillator in the signal processing module can be held or ignored to hold a given logic state. Other embodiments can latch and hold the output state, reduce the bandwidth of an analog chain to .filter transients, trigger a recalibration to facilitate recovery from a transient event, perform a foil chip reset under certain conditions, partially reset the device, such as recalibrating only the data potentially affected, e.g., move the threshold to a safer place until a few switches have past, return the device to a previously saved state, enable a watchdog-type feature that has no effect in normal operation but recalibrates the sensor if a problem condition is detected, reduce Icc to mitigate the severity of the regulator output transient, stop the oscillator to eliminate digital currents, place analog circuits in low power 'sleep' state, inform a user of low Vcc condition, change output levels, generate output pulses with predetermined error pulse widths, modulates Iee, and/or provide a specific error condition signal on the test pin,

[0030] FIG. 4 shows an exemplary sensor 400 having supply voltage transient protection in accordance with exemplary embodiments of the invention. It is understood that the sensor 400 is one particular embodiment of a magnetic sensor having transient protection. Other sensor embodiments having other signal processing and output configurations with inventive transient protection are well within the scope of the invention.

[0031] A magnetic article detector 400 includes regulator voltage transient protection in accordance with exemplary embodiments of the invention. A magnetic field sensor 414 provides a magnetic field sensor signal 416 that is proportional to an ambient magnetic field. The detector 400 is positioned in proximity to a magnetic article, for example a gear 12, so that the magnetic field sensor signal 416 is indicative of the profile of the magnetic article 12. The detector 400 provides a detector output signal 438 indicative of the magnetic article 1.2 subject to regulator voltage transient processing, as described herein. As the gear 12 passes through the ambient magnetic field a pulse train is generated

indicating edges of the gear teeth 12a-12n.

[0032] The detector 400 reduces phase error in the detector output signal 438 occurring at the transition from a power up detection mode to a running detection mode and includes a first circuit 424, herein referred to as the True Power On State (TPOS) detector, that is responsive to the magnetic field sensor signal 416 to provide a first output signal 428 indicative of the passing magnetic article 12 and a second circuit 426, herein referred to as the running mode detector, that is responsive to the magnetic field sensor signal 416 to provide a second output signal 430 indicative of the passing magnetic article 12. The first output signal 428 provides the detector output signal 438 during a first time interval and the second output signal 430 provides the detector output signal 438 doring a second time interval following the first time interval, as will be described.

[0033] An Automatic Gain Control (AGC) circuit 420 adjusts the gain of the magnetic field sensor signal 416 to provide a gain-adjusted version of the signal, referred to herein as the DIFF signal 418. Thus, in the illustrative embodiment, the running mode detector 426 is more directly responsive to the DIFF signal 418. The TPOS detector 424 is responsive to the AGC circuit 420 via a signal 422 for use in adjusting the TPOS threshold signal, as described below.

[0034] A phase comparator, or detector 432 is responsive to the first and second output signals 428, 430 to provide a phase detector output signal, or control signal 436 indicative of a change in the phase relationship between the first and second output signals and. an output switch. 434 provides the detector output signal 438 in the form of the first output signal or the second output signal in response to the control signal 436. More particularly, the phase detector output signal 436 is at a first logic level when a rising edge of the TPOS detector output signal 428 leads a rising edge of the running mode detector output signal 430 and is at a second logic level when a rising edge of the TPOS detector output signal 428 lags a rising edge of the running mode detector output signal 430. The control signal 436 is also coupled to the TPOS detector 424 as shown for use hi adjusting a TPOS threshold signal, as will he described.

[0035] A HOLD_OUT signal and an optional HI_OUT signal are provided to the output switch. 434 by a regulator voltage monitor module 450, which can be similar to the regulator voltage module 102 of FIG. I, to control the output daring regulator voltage transients. A regulator 452 can provide a regulated output to the legislator voltage monitor module 450 and other components. As shown in FIG. 2, if the HOLD_OUT signal output from the regulator voltage monitor module 450 becomes active, the output switch 434 maintains the state of the switch at the time the HOLD_OUT signal transitions to the active state. If the HIjQUT signal becomes active, the output switch 434 transitions to a high impedance stale.

[0036] In an exemplary embodiment, a HOLD_PROC signal, which can be similar to that shown in FIG. 2, can be coupled to the TPOS detector 424 and/or running mode detector 426 to halt further signal processing.

[0037] FIG. 5 shows an exemplary implementation 500 of the block diagram 400 of FIG. 4. A regulator voltage monitor module 550 receives an external regulated voltage supply signal Vcc_reg and generates a HOLD_PROC signal, a HOLD_OUT signal, and a HI_OUT signal, which are described above in FIG. 2, for example. These signals control output states and hold processing during transients drops in the regulated voltage signal Vregout.

[0038] A magnetic field sensor 514 includes a magnetic field sensing element 540. The sensing element 540 may take various forms known in the art, including but not limited to a Hall effect element, a vertical Hall effect element, a Giant Magnetoresistive (GMR) element, an Anisotropic Magnetoresistive (AMR) element, and a Tunnel Magnetoresistive (TMR) element. Also, the magnetic field sensing element 540 may comprise a single magnetically responsive element or, alternatively, may comprise a plurality of elements arranged in various configurations. In the illustrative embodiment, the magnetic field sensing element 540 is a single Hall effect element.

[0039] Various circuits and techniques may he used to process the signal provided by the magnetic field sensing element 540. In the illustrative embodiment, the signal from the Hall effect element 540 is amplified by a Hall amplifier 542 and provided to a summing

node 544 for DC offset cancellation. Various conventional techniques for DC offset cancellation are possible. In the illustrative embodiment, a 5 hit offset trim and a 3 bit temperature compensation trim 548 are provided, as may be implemented with fuses and trimmed during manufacture in order to center the signal from the Hall amplifier 540 within the voltage rails of the detector 510, A low pass filter 552 is coupled to the summing node 544 to provide the magnetic field sensor signal 516, as shown,

[0040] The AGC circuit 520 adjusts the gain of the magnetic field sensor signal 516 to provide the D1FF signal 518. In larger airgap installations, the magnetic field sensor signal 516 has a lower magnitude than in smaller airgap installations. It is generally advantageous to "normalize" the size of the magnetic field sensor signal 516 for further processing and detection. To this end, the AGC circuit 520 includes a dual differential amplifier (DDA) 560 that is responsive to the differential magnetic field sensor signal 516 and to an adjustable resistive feedback element 564, as shown. The feedback element 564 is adjustable in response to an auto gain adjust circuit 570.

[0041] Various schemes are possible to provide the auto gain adjust circuit 570 and more generally, to provide automatic gain control. In the illustrated embodiment, the circuit 570 includes a comparator 572 for comparing the DIFF signal *518* to an AGC threshold signal, **TOOJBIG,** and for providing an output signal to a one shot 576. The one shot 576 controls a counter 574 that is incremented every time the DIFF signal 518 exceeds the level of the AGC threshold signal. The counter output 522 is used to control the resistance of element 564 via a resistor control circuit 578.

[0042] In operation, the resistance of element 564 is initially set to provide a maximum gain to the magnetic field signal 516. If the resulting DIFF signal 518 is greater than the TOOJBIG signal, indicating clipping, then the output of the comparator 572 transitions and the one shot. 576 provides a pulse to increment the counter 574, The incremented counter output 522 is provided to the resistor control circuit 578 for adjustment of the resistor 564 in a manner that causes the magnitude of the magnetic field signal 516 to be reduced. This comparison of the DIFF signal to the TOOJBIG signal occurs until a predetermined number of gear teeth have passed following power up, a reset of the detector 510, or an initial gear rotation (i.e., zero speed). In the illustrative embodiment,

the AGC circuit 520 is active until three gear teeth, or six gear tooth edges pass the detector 510, after which the value of resistor 564 remains constant.

[0043] Once AGC operation ends, the output signal 522 of the AGC counter 574 remains at a fixed value representative of how many gain reductions, or decrements occurred during the AGC process (i.e., how many one shot pulses occurred). For example, in the case of a large airgap, no gain decrements may occur, thereby causing the counter output 522 to remain at a value of 0000 in the illustrative 4 bit counter embodiment Whereas, *in* the case of a small airgap, several gain decrements may occur, thereby causing the counter output 522 to remain at the value corresponding to the number of gain decrements occurring during AGC. The AGC counter output signal 522 is coupled to the TPOS detector 524 for use in adjusting the TPOS threshold signal, as will be described.

[0044] As is known, the use of differential elements and differential signals can be advantageous for common mode noise reduction reasons. In the illustrative embodiment, the elements and signals before the AGC circuit 520 are differentia! and, after the gain stage, the elements and signals, such as the BIFF signal 518, are single ended, as shown. It will be appreciated by those of ordinary skill in the art however that such design choices are based on particular circuit specifications and can be readily varied to meet different requirements.

[0045] The TPOS detector output signal 528 provides the detector output signal 538 for a first time interval, for example following power up or reset of the detector 510 because, as will become apparent, the running mode detector output signal 530 (referred to herein alternatively as the POSCOMP signal 530) may not provide accurate target detection, at least until the AGC process has been completed.

[0046] The TPOS detector 524 includes a comparator 580 having a first input (or pair of differential inputs in the case of the illustrative embodiment) responsive to the magnetic field sensor signal 516 and a second input (again, here a pair of differential inputs) responsive to a threshold signal 584. The TPOS threshold signal. 584 is initially set to a predetermined level and Is adjusted from the predetermined level in order to reduce phase error once it is determined that the running mode detector output signal 530 is accurate.

More particularly, the TPOS threshold signal 584 is at the predetermined level during a first portion of the first time interval and is adjusted during a second portion of the first time interval so as to minimize the phase error between edge detection by the TPOS detector and edge detection by the running mode detector.

[0047] The predetermined level to which the TPOS threshold signal 584 is initially set is selected to ensure switching on each gear tooth 512a-12η, regardless of airgap and other tolerances. This may be achieved with a TPOS trim 592 coupled to a digital-to-analog converter (DAC) 594, as shown. During manufacture, the detector 510 is tested with a target, or gear 512 positioned at the maximum specified airgaps and the TPOS detector output signal 528 is monitored to ensure switching on each gear tooth. Puses in a resistor network are then selectively blown in order to provide a voltage level for the TPOS threshold signal 584 that ensures switching on each gear tooth regardless of airgap. In one illustrative embodiment, the TPOS threshold signal 584 is initially set to a value on fee order of 50 millivolts.

[0048] The TPOS threshold signal 584 remains at the predetmnined level for a first portion of the first time interval, until the running mode detector output signal 530 is accurate, following which the TPOS threshold signal is adjusted during a second portion of the first time interval. Various schemes are possible in order to determine that the running mode detector output signal 530 is accurate and thus, that the TPOS threshold signal 584 should he adjusted so as to minimize the phase error between detection by the TPOS detector and detection by the running mode detector. In one illustrative embodiment, the first portion of the first time interval ends after a predetermined number of gear tooth detections (i.e.. after a predetermined number of transitions occur in. the TPOS detector output signal 528). For example, in one embodiment, the predetermined number of TPOS detector output signal transitions is ten, corresponding to six transitions (i.e., three gear teeth) during which AGC is active and four transitions (i.e., two gear teeth) thereafter to ensure that the ranning mode detector output signal 530 is accurate.

[0049] Referring to FIG. 5 in conjunction with FIG. 2, if the regulated voltage signal Vregout decreases below a first voltage threshold THH, the HOLD_PR.QC and the HOLD_OUT signals transition to active states. It is understood that in other

embodiments, the HOLD_PROC and HOLD_OUT signals are controlled with separate thresholds and/or timing, In an exemplary embodiment, when the HOLD_PROC goes active, the counter 588 and resistor control 578 hold their respective values dining the time that the HOLD_PROC signal is active. With this arrangement, the state of signal processing is held until the supply voltage transient dissipates. Similarly, while the HOLD_QUT signal is active, the output switch 534 maintains the same output until the HOLD__OUT signal is no longer active. If the regulated voltage Vregout drops below a second threshold THI, the HI__GUT signal transitions to an active state and the output switch 534 goes to a high impedance state until the HI__OUT signal goes inactive.

[0050] Having described exemplary embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may also be used. The embodiments contained herein should not. he limited to disclosed embodiments but rather should he limited only by the spirit and scope of the appended claims. All publications and references cited herein are expressly incorporated herein by reference in their entirety.

What is claimed is:

1 L A sensor, comprising:
2 a voltage monitor module to receive a regulated output voltage and transition a
3 first hold signal to an active state when the regelated output voltage drops below a first
4 threshold and transition a second hold signal to an active state when die regulated output
5 voltage drops below a second threshold;
6 a. signal processing module to receive the first hold signal from die regulator
7 voltage monitor module and hold processing in a state corresponding to a time the first
8 hold signal transitions to the active state; and
9 an output module for outpntxing a sensor output signal, the output module to
10 receive the second hold signal from.the regulator voltage monitor module and to maintain
11 a state of the sensor output signal at tlie time die second hold signal transitions to an active
12 state,

1 2. The sensor according to claim 1, wherein the regulator voltage monitor is configured
2 to generate a third hold signal for the output module to cause the output module to
3 transition the sensor output signal to a high impedance state, the third hold signal to
4 transition to an active state when tlie regulator voltage drops below a third threshold lower
5 than the first threshold,

1 3. The sensor according to claim 1, wherein the first and second thresholds are the same.

1 4. The sensor according to claim 1, further including a regulator to provide the regulated
2 output voltage.

t 5, The sensor according to claim 1, wherein the first hold signal remains in the active
2 state until die regulated voltage signal rises above the first threshold.

t 6. The sensor according to claim 1, wherein tlie sensor resets when the regulated output
2 voltage drops below a reset threshold voltage level.

t 7. The sensor according to claim. 1, further including a magnetic field sensor.

8. The sensor according to claim 1, **wherein** the a signal processing **module** includes at bast one coimter that does not change in value during a time in which the first hold signal is in the active state,

9, A sensor, comprising:

a regulator voltage monitor means to receive a regulated output voltage and **transition** a first hold signal to **an** active state when the **regulated** output voltage drops below a **first** threshold and transition a second hold signal to **an** active state when the regulated output voltage drops below a second threshold;

a **signal** processing means **to** receive the first hold signal from the regulator voltage monitor means and hold processing in a state corresponding to a time the first hold signal **transitions** to **the** active state; and

an. output **means** for outpatting a sensor output signal, the **output** module to receive the second hold signal from the regulator voltage monitor means and to maintain a state of the sensor output signal at the **time the** second hold signal transitions to an active state,

10, The sensor according to claim 9, **wherein** the **output** means comprises a switch.

11. The sensor according to claim 9, wherein the signal processing means comprises a magnetic field sensor.

12. A **method,** comprising;

receiving a regulated output voltage;

transitioning a first hold signal to an active state when **the** regulated output voltage drops below a first threshold;

transitioning a second hold signal to an active state when **the regulated** output voltage drops below a second threshold;

receiving the first hold **signal** and holding signal processing in a state corresponding to a time at which the first hold signal transitioned to **the** active state;

receiving the second hold signal; and

outputting a sensor output signal for a sensor and maintaining a state of the sensor output signal present at the time at which the second hold signal transitioned to the active state.

13. The method according to claim 12, further including generating a third hold signal to transition the sensor output signal to a high impedance state, the third hold signal to transition to an active state when the regulator voltage drops below a third threshold lower than the first threshold.

14. The method according to claim 12, wherein the first and second thresholds are the same.

15. The method according to claim 12, wherein the first hold signal remains in the active state until the regulated voltage signal rises above the first threshold.

16. The method according to claim 12, wherein the sensor resets when the regulated output voltage drops below a reset threshold voltage level,

17. The method according to claim 12, further including processing information from a magnetic field sensor.

18. The method according to claim 1, wherein the signal processing includes at least one counter that does not change in value during a time in which the first hold signal is in the active state.

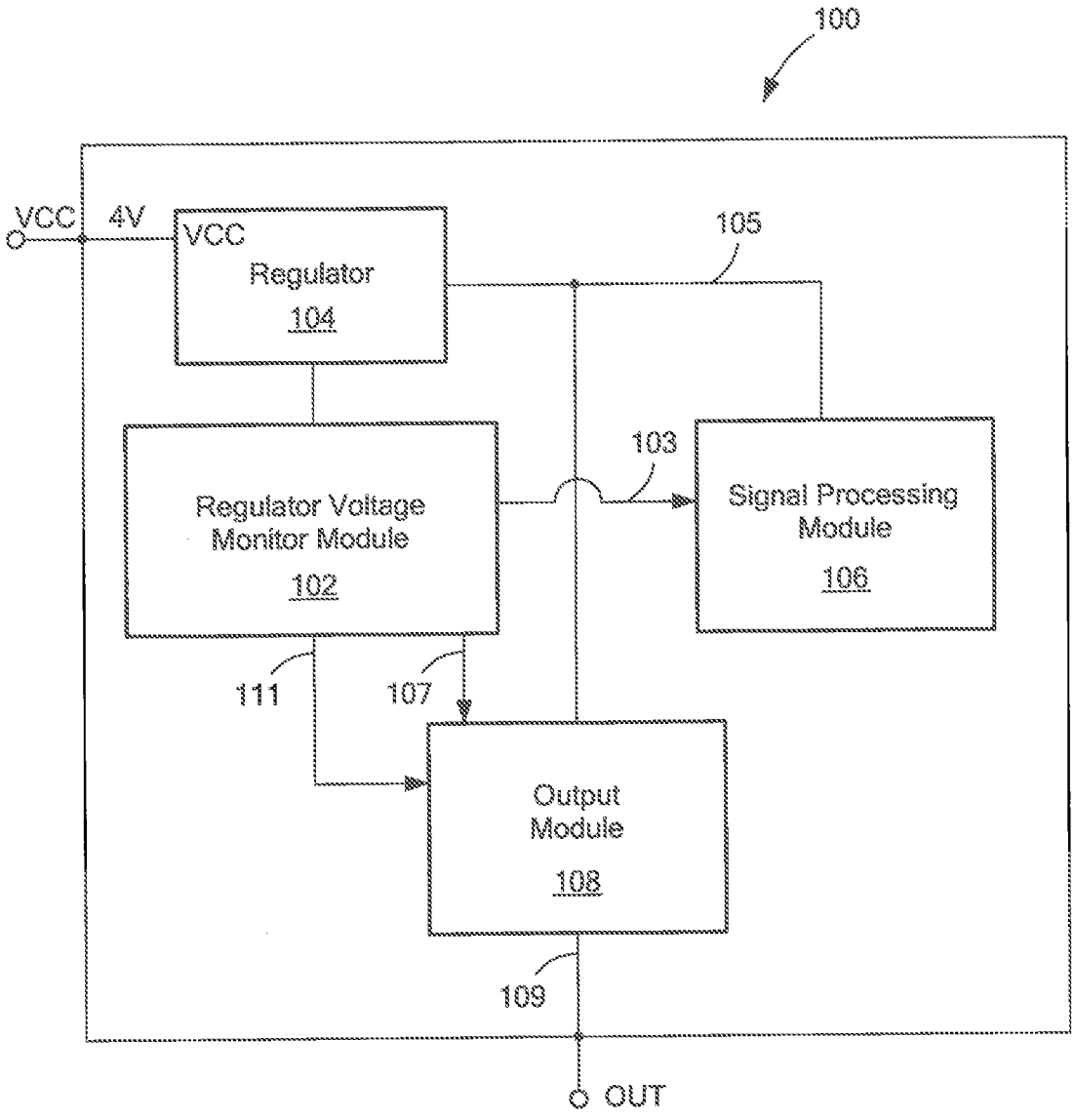

100
VCC
4V
VCC
Regulator
104
105
Regulator Voltage
Monitor Module
102
103
Signal Processing
Module
106
111
107
Output
Module
108
109
OUT

FIG. 1

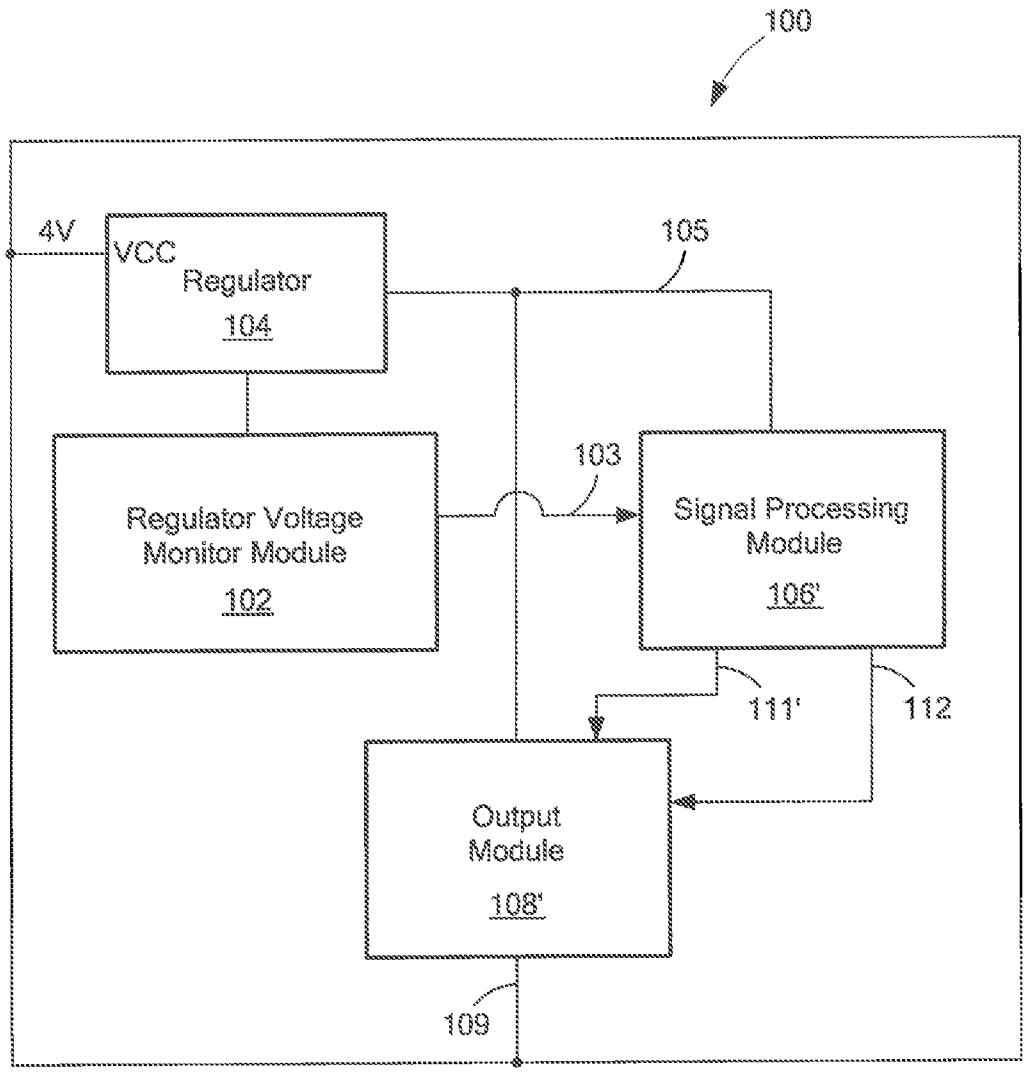

100
4V
VCC
Regulator
104
105
Regulator Voltage
Monitor Module
102
103
Signal Processing
Module
106'
111'
112
Output
Module
108'
109

FIG. 1A

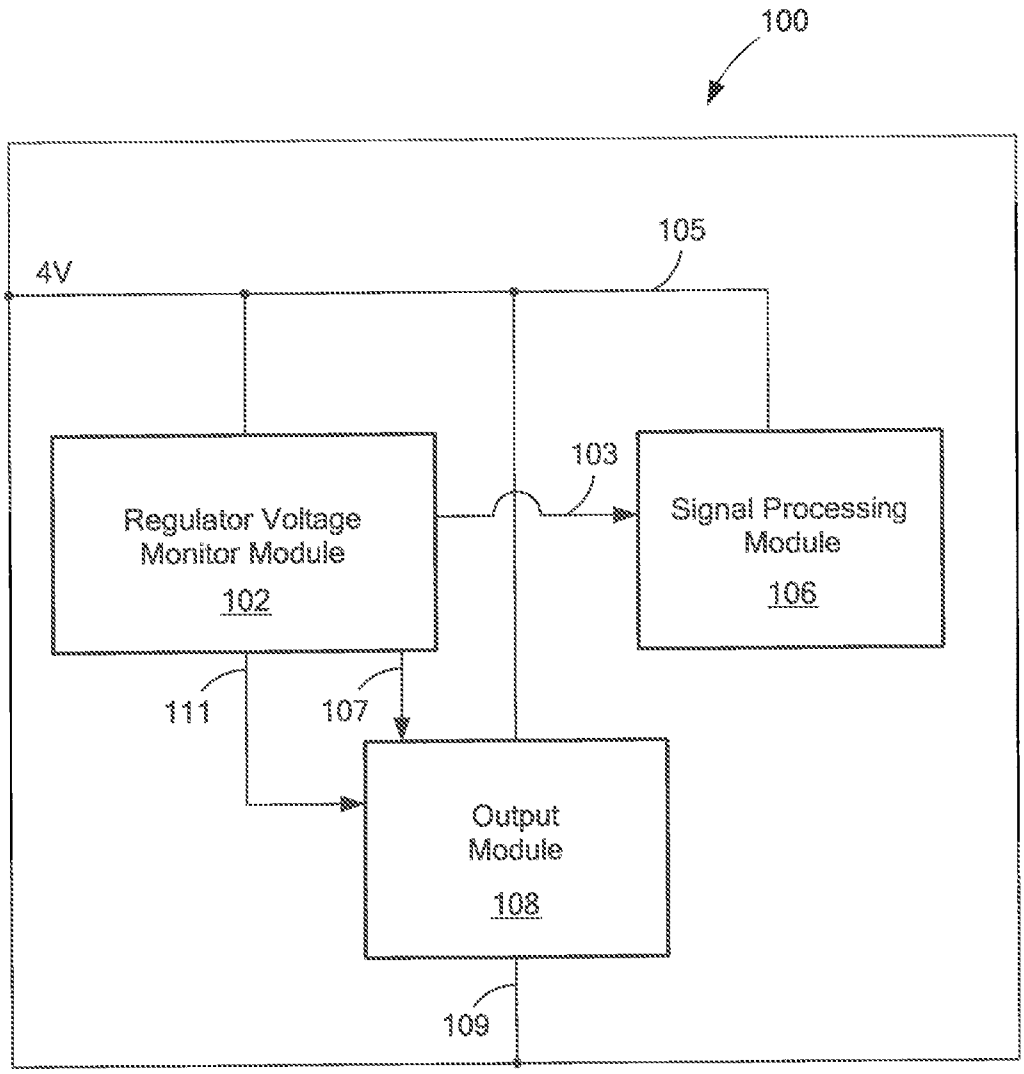

100
105
4V
Regulator Voltage Monitor Module
102
103
Signal Processing Module
106
111
107
Output Module
108
109

FIG. 1B

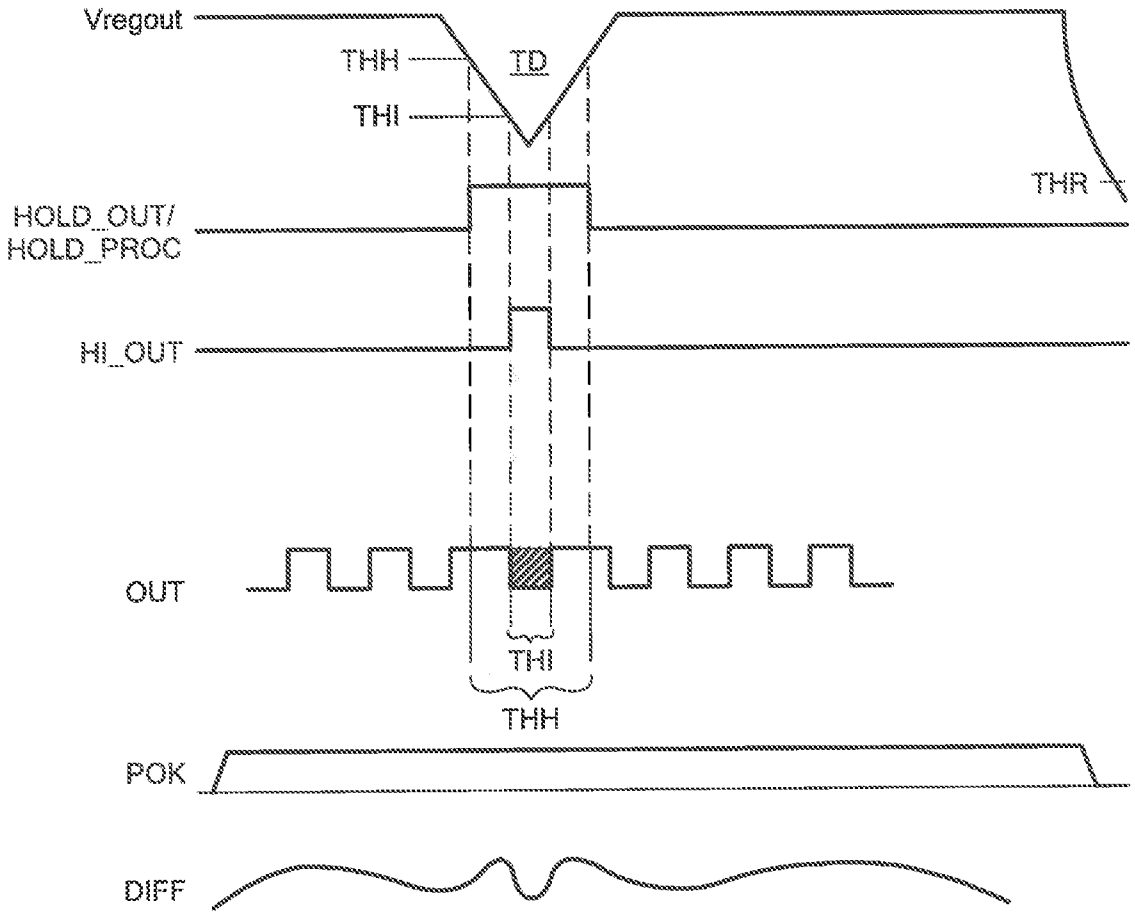

Vregout
THH
TD
THI
THR
HOLD_OUT/
HOLD_PROC
HI_OUT
OUT
THI
THH
POK
DIFF

FIG. 2

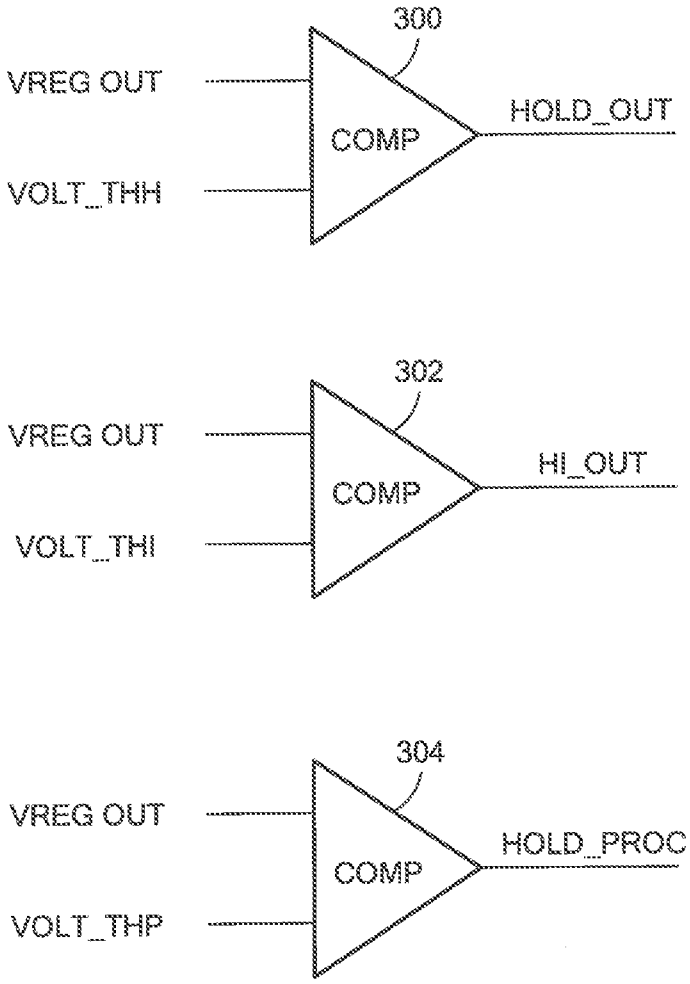

300
VREG OUT
COMP
HOLD_OUT
VOLT_THH
302
VREG OUT
COMP
HI_OUT
VOLT_THI
304
VREG OUT
COMP
HOLD_PROC
VOLT_THP

FIG. 3

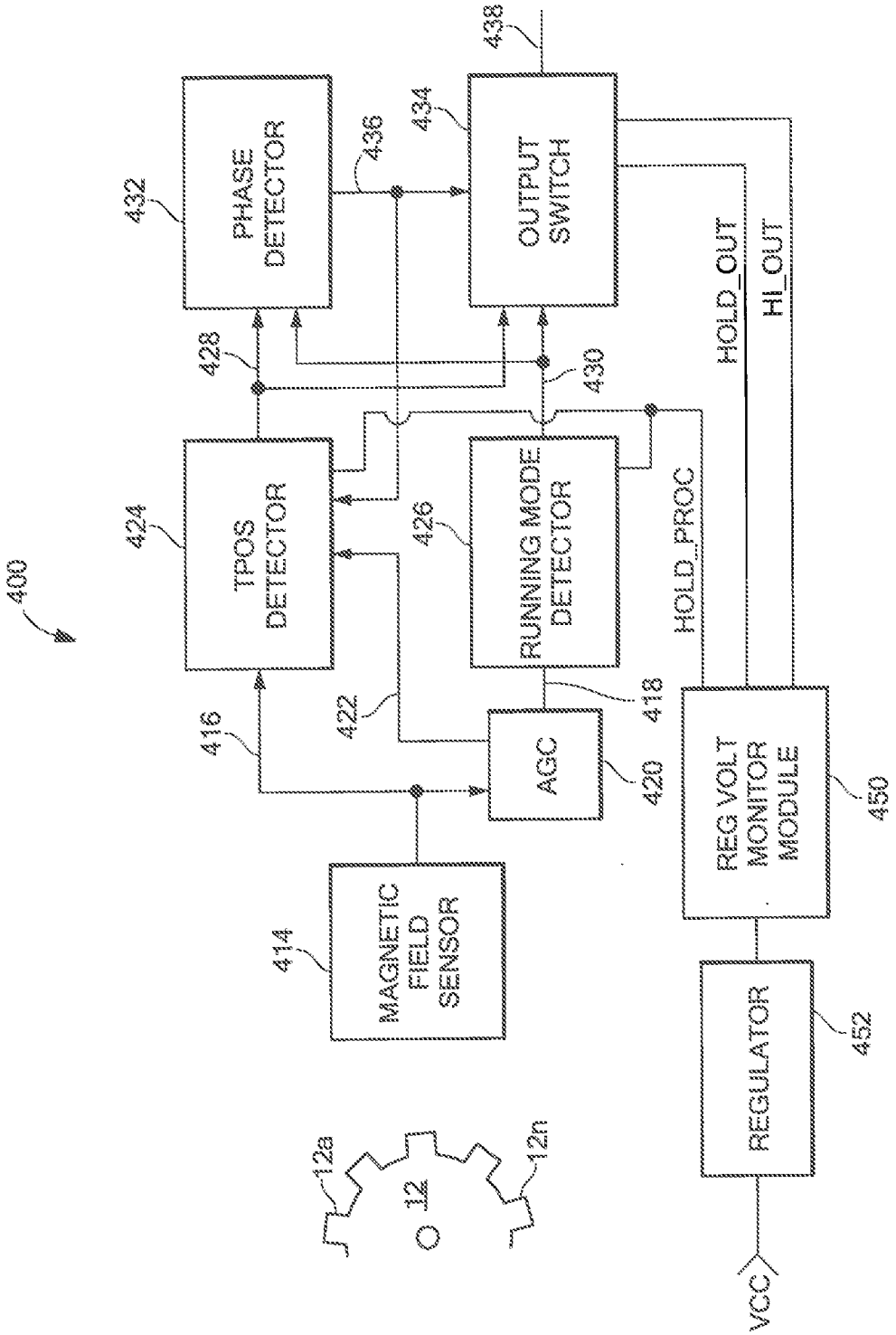

400
PHASE DETECTOR
432
436
OUTPUT SWITCH
434
438
HOLD_OUT
HI_OUT
428
430
TPOS DETECTOR
424
RUNNING MODE DETECTOR
426
HOLD_PROC
416
422
AGC
420
418
REG VOLT MONITOR MODULE
450
MAGNETIC FIELD SENSOR
414
REGULATOR
452
12a
12
12n
VCC

FIG. 4

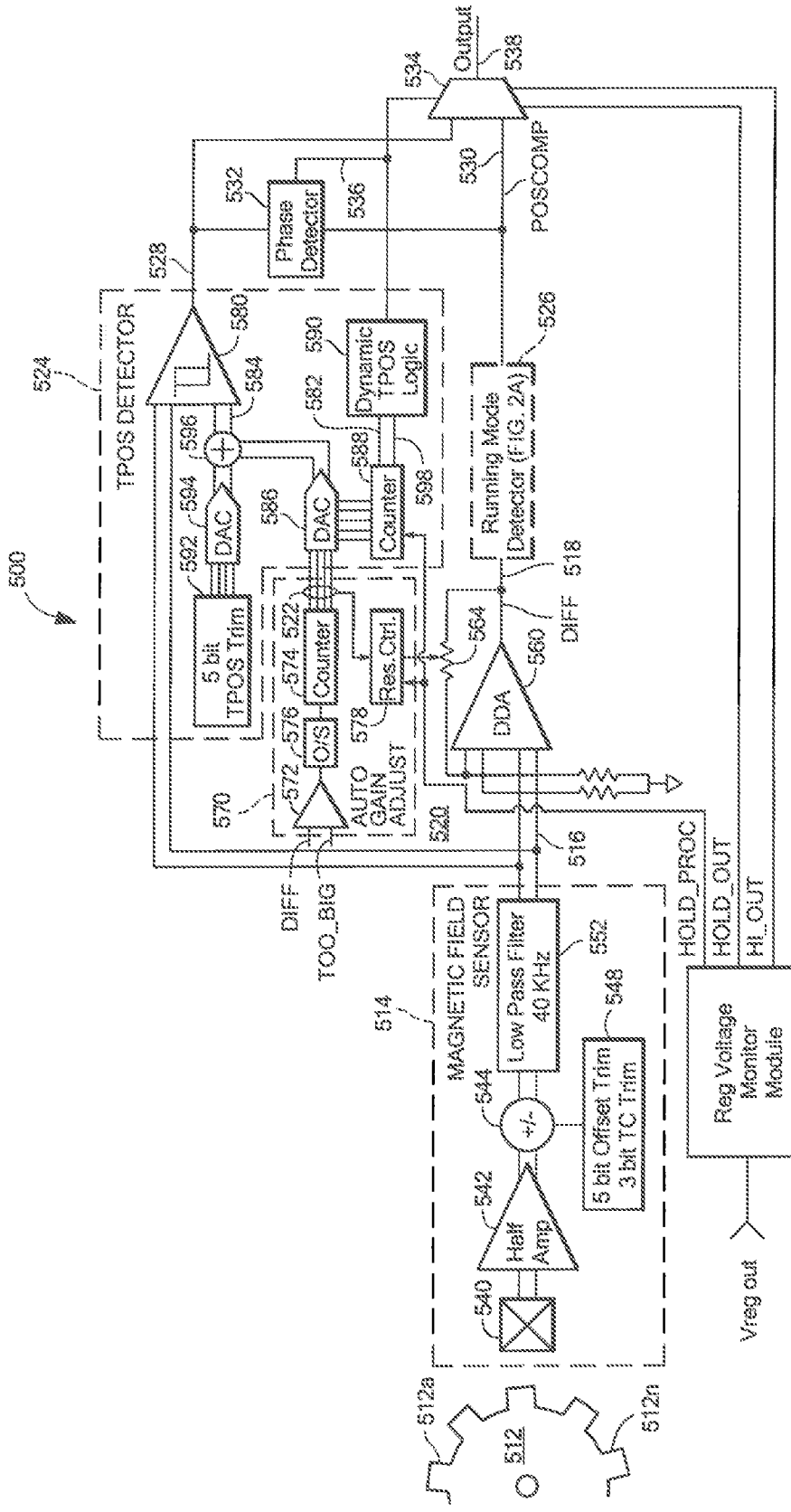

500
TPOS DETECTOR
524
528
580
584
582
590
Dynamic TPOS Logic
588
598
Counter
586
DAC
592
594
DAC
596
5 bit TPOS Trim
574
522
Counter
Res Ctrl
578
576
OVS
572
AUTO GAIN ADJUST
570
520
516
DIFF
TOO_BIG
514
MAGNETIC FIELD SENSOR
Low Pass Filter 40 KHz
552
544
+/-
542
Half Amp
540
5 bit Offset Trim
3 bit TC Trim
548
512a
512
512n
Phase Detector
532
536
534
Output
538
530
POSCOMP
526
Running Mode Detector (FIG. 2A)
518
DIFF
564
560
DDA
HOLD_PROC
HOLD_OUT
HI_OUT
Reg Voltage Monitor Module
550
Vreg out

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/068850

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/24
ADD. H03K17/94

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 003 532 A2 (DENSO CORP [JP]) 17 December 2008 (2008-12-17) figures 1,2	1-18
A	US 2007/164732 A1 (V0ISINE CORY [US] ET AL) 19 July 2007 (2007-07-19) figure 2	1-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 March 2013	25/03/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Simon, Volker

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2012/068850

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