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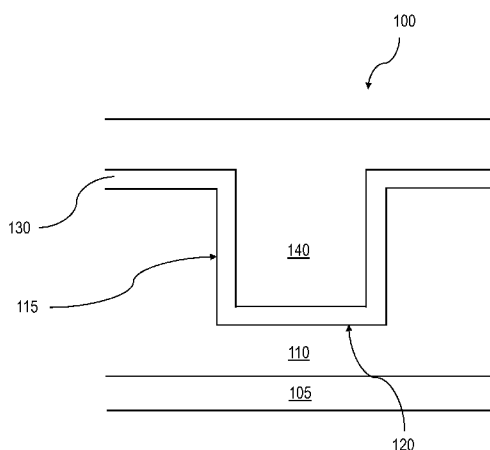
(54) **Title:** DOPED TANTALUM NITRIDE FOR COPPER BARRIER APPLICATIONS

FIG. 1B

(57) **Abstract:** Described are doped TaN films, as well as methods for providing the doped TaN films. Doping TaN films with Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and/or V allows for enhanced copper barrier properties of the TaN films. Also described are methods of providing films with a first layer comprising doped TaN and a second layer comprising one or more of Ru and Co, with optional doping of the second layer.



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## DOPED TANTALUM NITRIDE FOR COPPER BARRIER APPLICATIONS

## FIELD

[0001] The present invention relates generally to barrier layers in semiconductor devices, and methods of forming such barrier layers. More particularly, the disclosed method relates to  
5 films comprising TaN and selected dopants.

## BACKGROUND

[0002] Microelectronic devices, such as semiconductors or integrated circuits, can include millions of electronic circuit devices such as transistors, capacitors, etc. To further increase the density of devices found on integrated circuits, even smaller feature sizes are desired. To  
10 achieve these smaller feature sizes, the size of conductive lines, vias, and interconnects, gates, etc. must be reduced. Reliable formation of multilevel interconnect structures is also necessary to increase circuit density and quality. Advances in fabrication techniques have enabled use of copper for conductive lines, interconnects, vias, and other structures. However, electromigration in interconnect structures becomes a greater hurdle to overcome, with  
15 decreased feature size and the increased use of copper for interconnections.

[0003] Tantalum nitride (TaN) is a copper barrier at film thicknesses greater than 10Å, where the film is continuous. However, because a Ta atom is about 4Å in diameter, TaN films around 5Å thick are not continuous. For smaller nodes where thinner TaN is required, TaN by itself may be a discontinuous film, thus limiting its copper barrier properties. Current methods  
20 include a Ta layer on top of a TaN layer, which acts as a wetting layer for copper and provides the continuity of a barrier film. For smaller nodes (less than 32nm), however, this method leads to larger line resistance and hence is not an adequate solution.

[0004] Therefore, there is a need for thin layers that are effective copper barriers.

## SUMMARY OF THE INVENTION

25 [0005] One aspect of the current invention pertains to a method for forming interconnections in a microelectronic device comprising: providing a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom; depositing a barrier layer comprising TaN and one

or more dopants on at least a portion of the sidewall and/or bottom of the trench and/or via to provide a lined trench and/or via; and depositing a conductive material comprising Cu into the lined trench and/or via. According to one or more embodiments of this aspect, the one or more dopants are selected from Ru, Cu, Cu, Mn, Al, Mg, Cr, Nb, Ti and V. In some embodiments, the dopant comprises Mn. In other embodiments, the dopant comprises one or more of Ru, Cu and Co. According to one or more embodiments, the conductive material further comprises Mn.

[0006] One or more embodiments provide that depositing the barrier layer comprises depositing alternating layers comprising TaN and dopant. In other embodiments, depositing the barrier layer comprises depositing a TaN layer and diffusing the dopant into the TaN layer.

[0007] In one or more embodiments, the method further comprises exposing the barrier layer to plasma treatment prior to depositing the conductive material comprising Cu. In certain embodiments, the plasma comprises one or more of He, Ar,  $N_3^+$ ,  $H_2$  and  $N_2$ .

[0008] Another aspect of the invention pertains to a method for forming interconnections in a microelectronic device comprising: providing a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom; depositing a first layer comprising TaN and one or more first dopants on at least a portion of the sidewall and/or bottom of the trench and/or via to provide a lined trench and/or via; depositing a second layer comprising one or more of Ru and Co upon the first layer; and depositing a conductive material comprising Cu into the lined trench and/or via.

[0009] According to one or more embodiments of this aspect, the one or more first dopants are selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V. In some embodiments, the first dopant comprises Mn. In other embodiments, the first dopant comprises one or more of Ru, Cu and Co. According to one or more embodiments, the conductive material further comprises Mn. One or more embodiments provide that the second layer further comprises one or more second dopants selected from Mn, Al, Mg, Cr, Nb, Ti and V.

[0010] In one or more embodiments, the first layer is deposited by depositing alternating layers comprising TaN and the first dopant. In certain embodiments, the second layer is deposited by depositing alternating layers comprising Ru or Co and the second dopant.

[0011] According to one or more embodiments, the method of this aspect further comprises exposing the first layer and/or the second layer to plasma treatment prior to depositing the conductive material. In certain embodiments, the plasma comprises one or more of He, Ar, NH<sub>3</sub>, H<sub>2</sub> and N<sub>2</sub>.

5 [0012] Yet another aspect of the invention provides a microelectronic device comprising: a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom; a first layer lining at least a portion of the sidewall and/or bottom of the trench and/or via, the first layer comprising TaN and one or more dopants selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V; a second  
10 layer comprising one or more of Ru and Co overlying the first layer; and a conductive material comprising Cu filling the lined trench and/or via. According to one or more embodiments, the first layer has a thickness less than 10 Angstroms.

[0013] In one or more embodiments of this aspect, the conductive material further comprises Mn. In certain embodiments, the conductive material comprises less than wt. 2% Mn.

15 [0014] One or more embodiments of this aspect provide that the second layer further comprises one or more dopants selected from Mn, Al, Mg, Cr, Nb, Ti and V.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0015] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized  
20 above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0016] FIGS. 1A and 1B illustrate a dielectric layer before and after deposition of a barrier  
25 layer and conductive fill material in accordance with one or more embodiments of the invention; and

[0017] FIG. 2 illustrates a dielectric layer having a first layer, a second layer, and conductive fill material in accordance with one or more embodiments of the invention.

[0018] FIG. 3 shows the results from a biased thermal stress test of various barrier films.

#### DETAILED DESCRIPTION

[0019] Before describing several exemplary embodiments of the invention, it is to be understood that the invention is not limited to the details of construction or process steps set forth in the following description. The invention is capable of other embodiments and of being practiced or being carried out in various ways. Although specific reference is made to trenches in the following description, it is to be understood that the processes, films and devices described herein may involve similar structures such as vias, through-silicon-vias (TSVs), dual damascene structures and the like.

[0020] One aspect of the invention relates to a microelectronic device comprising a substrate, a dielectric layer, a barrier layer, and a conductive material. FIG. 1A depicts an embodiment of a microelectronic device 100 comprising a substrate 105 and a dielectric layer 110. The dielectric layer 110 is disposed upon the substrate 105, and the dielectric layer 110 has a trench 150 defined by a trench bottom 120, sidewalls 115, and opening 160.

[0021] In one or more embodiments, the dielectric layer 110 is a low-k dielectric layer. In certain embodiments, the dielectric layer comprises  $\text{SiO}_x$ . Further embodiments provide that the dielectric layer comprises porous carbon-doped  $\text{SiO}_x$ . In some embodiments, the dielectric layer is a porous carbon-doped  $\text{SiO}_x$  layer with a k value less than 3.

[0022] FIG. 1B shows the same microelectronic device 100 after deposition of a barrier layer 130, which covers at least a portion of the sidewall 115 and/or trench bottom 120. As shown in FIG. 1B, the barrier layer 130 may cover the entirety of the sidewall 115 and trench bottom 120. The barrier layer 130 may comprise TaN and one or more dopants such as Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti or V. According to one or more embodiments, the barrier layer comprises TaN and Mn. In other embodiments, the barrier layer comprises TaN and one or more of Ru, Cu and Co.

[0023] In one or more embodiments, the barrier layer comprises 0.1 to 10 % dopant, based on the weight of the TaN layer. In certain embodiments, the barrier layer comprises 0.2 to 8 wt. % dopant. In some embodiments, the barrier layer comprises 0.5 to 5 wt. % dopant, such

as about 0.5, about 1, about 1.5, about 2, about 2.5, about 3, about 3.5, about 4, about 4.5, or about 5 wt. % dopant.

[0024] According to one or more embodiments, as used herein, "barrier layer" refers to a discrete layer formed by depositing TaN and one or more dopants, and excludes a region in which a second element or dopant diffuses into only a portion of the barrier layer. In other words, some embodiments provide that the dopant is present throughout the entire thickness of the TaN layer, and not only at a surface portion thereof.

[0025] A conductive fill material 140 fills at least a portion of the trench 150 lined with barrier layer 130. According to one or more embodiments, the conductive fill material comprises copper or a copper alloy. In further embodiments, the conductive fill material also comprises Mn. In other embodiments, the conductive fill material further comprises Al.

[0026] Although the conductive fill material 140 in FIG. 1B is shown in direct contact with the barrier layer 130, intermediate layers may be in between the conductive fill material 140 and the barrier layer 130, such as adhesion layers or seeding layers. According to one or more embodiments, the microelectronic device further comprises an adhesion layer comprising one or more of Ru and Co. In addition to Ru and/or Co, the adhesion layer may comprise one or more dopants such as Mn, Al, Mg, Cr, Nb, Ti or V. In some embodiments, the adhesion layer comprises Ru and Mn. In other embodiments, the adhesion layer comprises Co and Mn.

[0027] In certain embodiments, a seeding layer is deposited on top of the barrier layer. According to one or more embodiments, the seeding layer comprises an alloy of copper, such as a Cu-Mn alloy. In certain embodiments, the seeding layer comprises less than 2 wt. % Mn. In some embodiments, the seeding layer comprises about 1 wt. % Mn. The line resistance of copper alloys containing 1 wt. % Mn is expected to be the same as or similar to the line resistance of pure copper.

[0028] While not wishing to be bound to any particular theory, it is thought that the dopant can selectively diffuse through the barrier layer 130 to the dielectric layer 110 and form a complex with the dielectric material that will be resistant to electromigration. Thus, in embodiments where the dopant is Mn and the dielectric layer comprises  $\text{SiO}_x$ , the Mn can diffuse through the barrier layer and form  $\text{MnSiO}_x$ . This self-forming barrier layer of  $\text{MnSiO}_x$

can then prevent copper electromigration from the conductive material 140 to the dielectric layer 110.

[0029] When the barrier layer is greater than 10Å, such as 25Å, undoped TaN is effective as a copper barrier layer. However, TaN layers of this thickness are often too thick for use in smaller nodes, such as those less than 32 nm.

[0030] Depending on the dopant used, the penetration depth of the dopant may be less than 10Å. Thus, for TaN layers of about 10Å, the dopant may not penetrate to the dielectric layer to form the dopant-dielectric complex. However, the copper penetration depth may be more than 10Å, thus rendering the barrier layer ineffective. Accordingly, one or more embodiments of the present invention provide that the TaN layer is less than 10Å. In certain embodiments, the TaN layer is in the range of 4Å to 10Å.

[0031] In addition to being a copper barrier, doped TaN may also be a barrier to oxygen diffusing from the dielectric layer 110 to the conductive material 140. Oxygen diffusion from the dielectric layer 110 to the conductive material 140 can result in oxygen reacting with components in the conductive material and/or seed layer. For example, if the conductive material 140 comprises Mn, then oxygen can react with the Mn at the interface of the barrier layer 130 and the conductive material 140, thus "pinning" the Mn to the barrier layer/conductive material interface. As a result, the Mn cannot segregate throughout the conductive material. Similarly, if a seed layer comprising Mn is present, then oxygen can react with the Mn in the seed layer at the seed layer/barrier layer interface and pin the Mn to the interface.

[0032] It is believed that oxygen diffusing into the TaN layer will react with the dopant and will prevent oxygen from diffusing into the conductive material 140. As a result, oxygen will not be available to react with the seed layer or the conductive material.

[0033] FIG. 2 illustrates a microelectronic device 200 with a substrate 205 and a dielectric layer 210. The dielectric layer 210 has sidewalls 215 and trench bottom 220, which are at least partially covered by a first layer 230. The first layer 230 may be a barrier layer comprising TaN and one or more dopants such as Ru, Cu, Co, Mn, Al, Mg, Nb, Ti or V. In some



embodiments, the first layer comprises TaN and Mn. In other embodiments, the first layer comprises TaN and one or more of Ru, Cu and Co.

[0034] A second layer 235 is disposed upon the first layer 230, and may comprise one or more of Ru and Co. The second layer may further comprise one or more dopants such as Mn, Al, Mg, Cr, Nb, Ti or V. In some embodiments, the second layer comprises Ru and Mn. In other embodiments, the second layer comprises Co and Mn.

[0035] A conductive fill material 240 is deposited in the remainder of the trench defined by sidewall 215 and trench bottom 220. According to one or more embodiments, the conductive fill material comprises copper or a copper alloy. In further embodiments, the conductive fill material also comprises Mn. The conductive material 240 may be deposited directly on the second layer 235, or may be deposited on a seeding layer (not shown) on top of the second layer 235. According to one or more embodiments, the seeding layer comprises an alloy of copper, such as a Cu-Mn alloy. In certain embodiments, the seeding layer comprises less than 2% Mn. In some embodiments, the seeding layer comprises about 1% Mn.

[0036] In addition to the films described above, another aspect of the invention relates to a method for forming interconnections in a microelectronic device comprising providing a substrate with a dielectric layer disposed thereon, depositing a barrier layer upon the dielectric layer, and depositing a conductive material upon the barrier layer. According to one or more embodiments of this aspect, the barrier layer comprises TaN and a dopant selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V. In some embodiments, the dopant is Mn. In other embodiments, the dopant comprises one or more of Ru, Cu and Co.

[0037] The doped TaN layer may be formed by any appropriate deposition process. For example, the TaN can be deposited by an alternating layer deposition (ALD) process or a plasma enhanced atomic layer deposition (PEALD). The dopant can then be deposited by chemical vapor deposition (CVD), physical vapor deposition (PVD) or ALD. The dopant is then diffused into TaN layer to form an integrated TaN dopant layer. The dopant may be diffused into the TaN layer through various processes, including by plasma treatment and by heating.

[0038] Alternatively, the TaN and the dopant can be deposited in alternating layers. In accordance with this embodiment, a first TaN layer, such as a TaN monolayer, is deposited on the dielectric film. A first dopant layer, such as a layer of dopant, dopant alloy or other dopant-containing compound, is then deposited on top of the first TaN. This first dopant layer  
5 can also be a monolayer. A second TaN layer is then deposited on top of the first dopant layer. This process is repeated until a doped TaN film of the desired thickness is produced.

[0039] Notably, certain embodiments of these processes will result in a film with dopant interspersed throughout the entire TaN layer, instead of a separate barrier layer such as Mn on top of the TaN barrier layer. As the dopant is already present in the TaN layer, it may be easier  
10 for the dopant to diffuse to the dielectric layer to form the dopant-barrier layer complex, such as  $\text{MnSiO}_x$ . In contrast, if the dopant is only present as a separate barrier layer on top the TaN layer, the dopant must diffuse through the entire thickness of the TaN layer before reaching the dielectric layer.

[0040] Suitable precursors for depositing a TaN film include Ta-containing precursors and  
15 N-containing precursors. For example, the Ta-containing precursor may be pentakis(dimethylamino)tantalum (PDMAT) and the N-containing precursor may be ammonia. Other suitable precursors are known to those skilled in the art. Organic species in organic-containing precursors for TaN may get partially incorporated into the dielectric layer, which may increase the adhesion at the TaN-dielectric layer interface.

[0041] For depositing the dopant metal, an appropriate metal-containing precursor may be  
20 used. Examples of suitable precursors include metal complexes containing the desired dopant, such as dopant metals coordinated with organic or carbonyl ligands. A suitable dopant precursor should have sufficient vapor pressure to be deposited in the appropriate process, such as ALD, CVD and PVD. Depending on the dopant precursor used, a co-reactant may be used  
25 to deposit the dopant. For example, reducing gases such as hydrogen and ammonia can be used as co-reactants for depositing some dopants.

[0042] Certain embodiments of the invention provide that the doped TaN film is treated with a plasma prior to depositing the conductive material. According to one or more  
30 embodiments, the plasma comprises one or more of He, Ar,  $\text{NH}_3$ ,  $\text{H}_2$  and  $\text{N}_2$ . In some embodiments, the plasma may comprise a mixture of Ar and  $\text{H}_2$ , such as a mixture having a

Ar:H<sub>2</sub> molar ratio in the range from 1:1 to 1:10. The plasma power may be in the range from about 400 to about 1000 Watts. The plasma treatment time may vary from 5 second to 60 seconds, such as in the range from 10 seconds to 30 seconds. In some embodiments, the pressure during plasma treatment may be in the range from 0.5 to 50 Torr, such as from 1 to 10 Torr. Alternatively, in some embodiments the barrier layer is not doped TaN. In these embodiments, the barrier layer may comprise MnN<sub>x</sub> or TaN that is subsequently exposed to a plasma treatment as described herein.

[0043] The conductive material may be deposited in a variety of ways, including by an electroless deposition process, an electroplating (ECP) process, a CVD process or a PVD process. In certain embodiments, a first seed layer is deposited upon the barrier layer, and a bulk conductive layer is then formed upon the seed layer.

[0044] Another aspect of the invention pertains to a method for forming interconnections in a microelectronic device comprising providing a substrate with a dielectric layer disposed thereon, depositing a first layer upon the dielectric layer, depositing a second layer upon the first layer, and depositing a conductive material upon the second layer. In embodiments of this aspect, the first layer may comprise TaN and one or more dopants selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V. In some embodiments, the first layer comprises TaN and Mn. In other embodiments, the first layer comprises TaN and one or more of Ru, Cu and Co. The doped TaN layer may be formed by any appropriate deposition process, such as those described above.

[0045] According to one or more embodiments, the second layer comprises one or more of Ru and Co. In certain embodiments, the second layer further comprises one or more dopants selected from Mn, Al, Mg, Cr, Nb, Ti and V. In some embodiments, the second layer comprises Ru and Mn. In other embodiments, the second layer comprises Co and Mn.

[0046] The second layer may be deposited by any appropriate deposition process, including CVD, PVD, ALD, and PEALD. In embodiments where the second layer comprises cobalt, suitable precursors for the second layer include, but are not limited to, cobalt carbonyl complexes, cobalt amidinates compounds, cobaltocene compounds, cobalt dienyl complexes, cobalt nitrosyl complexes, and derivatives and combinations thereof. In embodiments where the second layer comprises ruthenium, suitable precursors include, but are not limited to,

pyrrolyl ruthenium precursors such as a pentadienyl pyrrolyl ruthenium precursor, a cyclopentadienyl pyrrolyl ruthenium precursor, an alkylpentadienyl pyrrolyl ruthenium precursor or an alkylcyclopentadienyl pyrrolyl ruthenium precursor.

[0047] As with the doping of TaN films, the second layer may be doped by depositing a layer comprising one or more of Ru and Co, and then diffusing a dopant into the Ru and/or Co layer. Alternatively, the Ru and/or Co and the dopant may be deposited in alternating layers until a film of the desired thickness is formed.

[0048] Additionally, the conductive material may be deposited in any appropriate process, including those described above. The doped TaN may be treated with a plasma prior to depositing the conductive material, such as a plasma comprising one or more of He, Ar, NH<sub>3</sub>, H<sub>2</sub> and N<sub>2</sub>

[0049] The films in accordance with various embodiments of this invention can be deposited over virtually any substrate material. A "substrate surface," as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, silicon nitride, doped silicon, germanium, gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Barrier layers, metals or metal nitrides on a substrate surface include titanium, titanium nitride, tungsten nitride, tantalum and tantalum nitride, aluminum, copper, or any other conductor or conductive or non-conductive barrier layer useful for device fabrication. Substrates may have various dimensions, such as 200 mm or 300 mm diameter wafers, as well as, rectangular or square panes. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers, III-V materials such as GaAs, GaN, InP, etc. and patterned or non-patterned wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal and/or bake the substrate surface.

[0050] As embodiments of the invention provide a method for depositing or forming doped TaN films, a processing chamber is configured to expose the substrate to a sequence of gases and/or plasmas during the vapor deposition process. The processing chamber would include separate supplies of reactants, along with any supply of carrier, purge and inert gases such as argon and nitrogen in fluid communication with gas inlets for each of the reactants and gases. Each inlet may be controlled by an appropriate flow controller such as a mass flow controller or volume flow controller in communication with a central processing unit (CPU) that allows flow of each of the reactants to the substrate to perform a deposition process as described herein. The central processing unit may be one of any forms of a computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The CPU can be coupled to a memory and may be one or more of readily available memory such as random access memory (RAM), read only memory (ROM), flash memory, compact disc, floppy disk, hard disk, or any other form of local or remote digital storage. Support circuits can be coupled to the CPU to support the CPU in a conventional manner. These circuits include cache, power supplies, clock circuits, input/output circuitry, subsystems, and the like.

[0051] The co-reactants are typically in vapor or gas form. The reactants may be delivered with a carrier gas. A carrier gas, a purge gas, a deposition gas, or other process gas may contain nitrogen, hydrogen, argon, neon, helium, or combinations thereof. The various plasmas described herein, such as the nitrogen plasma or the inert gas plasma, may be ignited from and/or contain a plasma co-reactant gas.

[0052] In one or more embodiments, the various gases for the process may be pulsed into an inlet, through a gas channel, from various holes or outlets, and into a central channel. In one or more embodiments, the deposition gases may be sequentially pulsed to and through a showerhead. Alternatively, as described above, the gases can flow simultaneously through gas supply nozzle or head and the substrate and/or the gas supply head can be moved so that the substrate is sequentially exposed to the gases.

[0053] In another embodiment, a doped TaN film may be formed during plasma enhanced atomic layer deposition (PEALD) process that provides sequential pulses of precursors and plasma. In specific embodiments, the co-reactant may involve a plasma. In other

embodiments involving the use of plasma, during the plasma step the reagents are generally ionized during the process, though this might occur only upstream of the deposition chamber such that ions or other energetic or light emitting species are not in direct contact with the depositing film, this configuration often termed a remote plasma. Thus in this type of PEALD process, the plasma is generated external from the processing chamber, such as by a remote plasma generator system. During PEALD processes, a plasma may be generated from a microwave (MW) frequency generator or a radio frequency (RF) generator. Although plasmas may be used during the deposition processes disclosed herein, it should be noted that plasmas are not required. Indeed, other embodiments relate to deposition processes under very mild conditions without a plasma.

[0054] Another aspect of the invention pertains to an apparatus for deposition of a film on a substrate to perform a process according to any of the embodiments described above. In one embodiment, the apparatus comprises a deposition chamber for deposition of a film on a substrate. The chamber comprises a process area for supporting a substrate. The apparatus includes a precursor inlet in fluid communication with a supply of a Ta precursor, such as pentakis(dimethylamino)tantalum (PDMAT). The apparatus also includes a reactant gas inlet in fluid communication with a supply of nitrogen-containing precursor, such as ammonia. The apparatus also includes a reactant gas inlet in fluid communication with a supply of dopant precursor, such as a dopant-containing metal complex. The apparatus further includes a purge gas inlet in fluid communication with a purge gas. The apparatus can further include a vacuum port for removing gas from the deposition chamber. The apparatus can further include an auxiliary gas inlet for supplying one or more auxiliary gases such as inert gases to the deposition chamber. The deposition can further include a means for heating the substrate by radiant and/or resistive heat.

[0055] In some embodiments, a plasma system and processing chambers or systems which may be used during methods described here for depositing or forming the films can be performed on either PRODUCER®, CENTURA®, or ENDURA® systems, all available from Applied Materials, Inc., located in Santa Clara, Calif. A detailed description of an ALD processing chamber may be found in commonly assigned U.S. Pat. Nos. 6,878,206, 6,916,398, and 7,780,785.

## EXAMPLES

**[0056]** A biased thermal stress (BTS) test was performed on various barrier films. The compositions of each film are shown in Table 1 below:

Table 1: Barrier Film Compositions

Film No.	Composition	Deposition Process	Thickness
1	MnN <sub>x</sub>	Thermal ALD	10 Angstroms
2	MnN <sub>x</sub>	Thermal ALD	15 Angstroms
3	MnN <sub>x</sub>	Thermal ALD with plasma post-treatment	10 Angstroms
4	Mn-doped TaN	Thermal ALD	10 Angstroms
5	Mn-doped TaN	Thermal ALD with plasma post-treatment	10 Angstroms
6	TaN	Thermal ALD with plasma post-treatment	10 Angstroms
7	TaN	Thermal ALD with plasma post-treatment	15 Angstroms
8	Ta	Thermal ALD	30 Angstroms
9	TaN	PEALD	20 Angstroms

5

**[0057]** The films subjected to a plasma post-treatment were exposed to a plasma containing an Ar:H<sub>2</sub> mixture of 1:1 to 1:10 for 10 to 30 seconds. The plasma power was 400 to 1000 W and the pressure was 1 to 10 Torr.

**[0058]** The Mn-doped TaN films contained about 10A of TaN and about 1A of Mn. The TaN films were exposed to Mn precursor doping for 1 to 5s and optionally had a NH<sub>3</sub> soak for 5 to 30s.

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[0059] The results of the BTS test are shown in FIG. 3. Films 8 and 9 were the baseline with an eWF shift of 0V. A lower eWF shift in FIG. 3 demonstrates that a barrier film had better barrier properties. As can be seen from FIG. 3, film 4 (corresponding to 10A Mn-doped TaN) exhibited superior barrier properties compared to film 1 (10A MnN<sub>x</sub>) and had comparable barrier properties to a MnN<sub>x</sub> film with a larger thickness (film 2). The plasma post-treatment enhanced the barrier properties of all films.

[0060] Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0061] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present invention without departing from the spirit and scope of the invention. Thus, it is intended that the present invention include modifications and variations that are within the scope of the appended claims and their equivalents.



What is claimed is:

1. A method for forming interconnections in a microelectronic device comprising:  
providing a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom;  
5 depositing a barrier layer comprising TaN and one or more dopants selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V on at least a portion of the sidewall and/or bottom of the trench and/or via to provide a lined trench and/or via; and  
depositing a conductive material comprising Cu into the lined trench and/or via.
- 10 2. The method of claim 1, wherein the dopant comprises Mn.
3. The method of claim 1 or 2, wherein the dopant comprises one or more of Ru, Cu and Co.
- 15 4. The method of any of claims 1-3, wherein depositing the barrier layer comprises depositing alternating layers comprising TaN and dopant.
5. The method of any of claims 1-3, wherein depositing the barrier layer comprises depositing a TaN layer and diffusing the dopant into the TaN layer.
- 20 6. The method of any of claims 1-5, further comprising exposing the barrier layer to plasma treatment prior to depositing the conductive material comprising Cu.
7. The method of claim 6, wherein the plasma comprises one or more of He, Ar, N<sup>3/4</sup>, H<sub>2</sub>  
25 and N<sub>2</sub>.
8. A method for forming interconnections in a microelectronic device comprising:  
providing a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom;  
30 depositing a first layer comprising TaN and one or more first dopants selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V on at least a portion of the sidewall and/or bottom of the trench and/or via to provide a lined trench and/or via;

depositing a second layer comprising one or more of Ru and Co upon the first layer;  
and  
depositing a conductive material comprising Cu into the lined trench and/or via.

5 9. The method of claim 8, wherein the first dopant comprises Mn.

10. The method of claim 8 or 9, wherein the second layer further comprises one or more second dopants selected from Mn, Al, Mg, Cr, Nb, Ti and V.

10 11. The method of any of claims 8-10, further comprising exposing the first layer to plasma treatment prior to depositing the conductive material.

12. The method of claim 11, wherein the plasma comprises one or more of He, Ar, N<sup>3/4</sup>, H<sub>2</sub> and N<sub>2</sub>.

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13. A microelectronic device comprising:

a substrate comprising a dielectric layer disposed thereon, the dielectric layer having one or more trenches and/or vias with an opening, a sidewall and a bottom;

20 a first layer lining at least a portion of the sidewall and/or bottom of the trench and/or via, the first layer comprising TaN and one or more dopants selected from Ru, Cu, Co, Mn, Al, Mg, Cr, Nb, Ti and V;

a second layer comprising one or more of Ru and Co overlying the first layer; and

a conductive material comprising Cu filling the lined trench and/or via.

25 14. The microelectronic device of claim 13, wherein the second layer further comprises one or more dopants selected from Mn, Al, Mg, Cr, Nb, Ti and V.

15. The microelectronic device of claim 13 or 14, wherein the first layer has a thickness less than 10 Angstroms.

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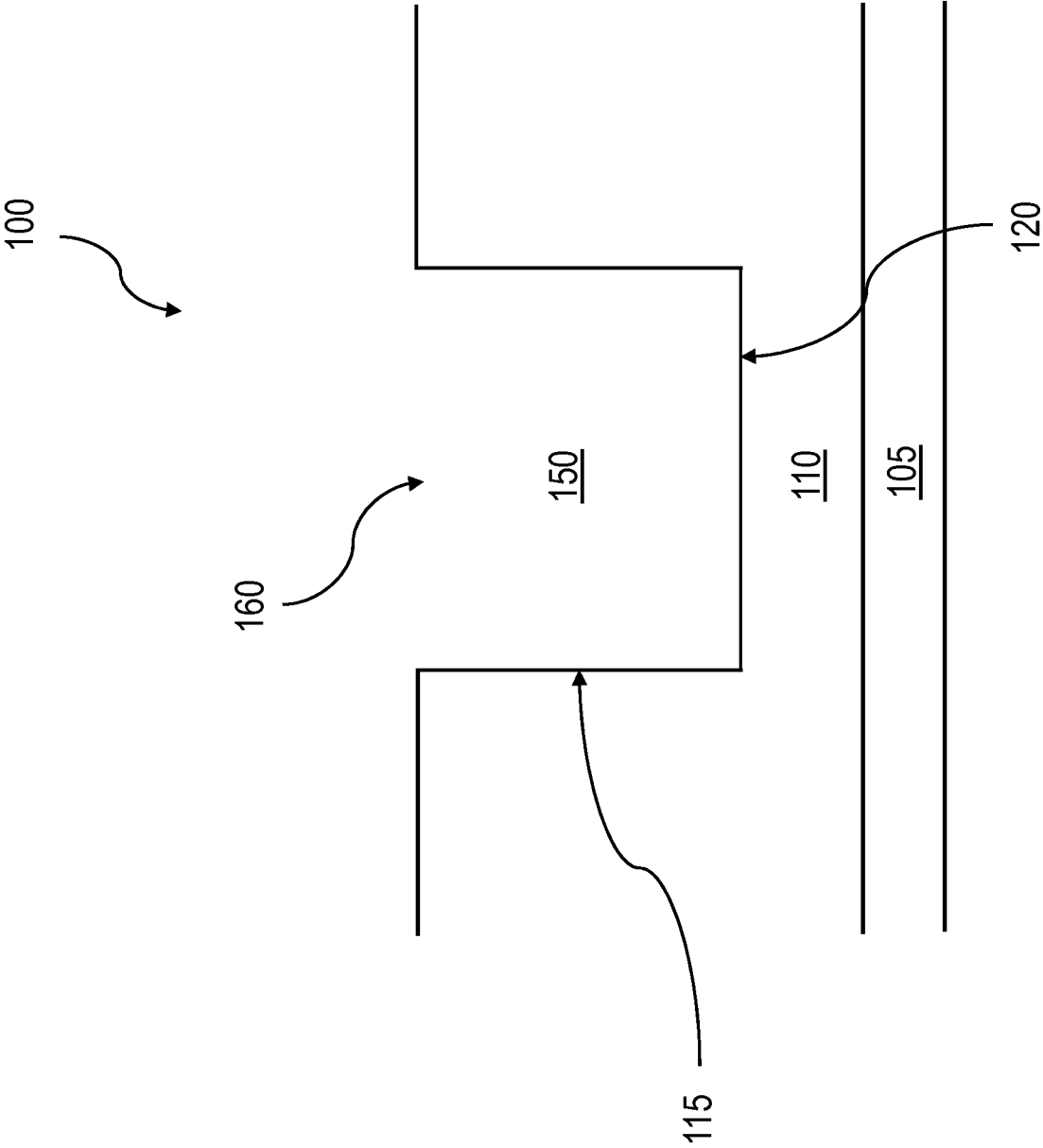


FIG. 1A

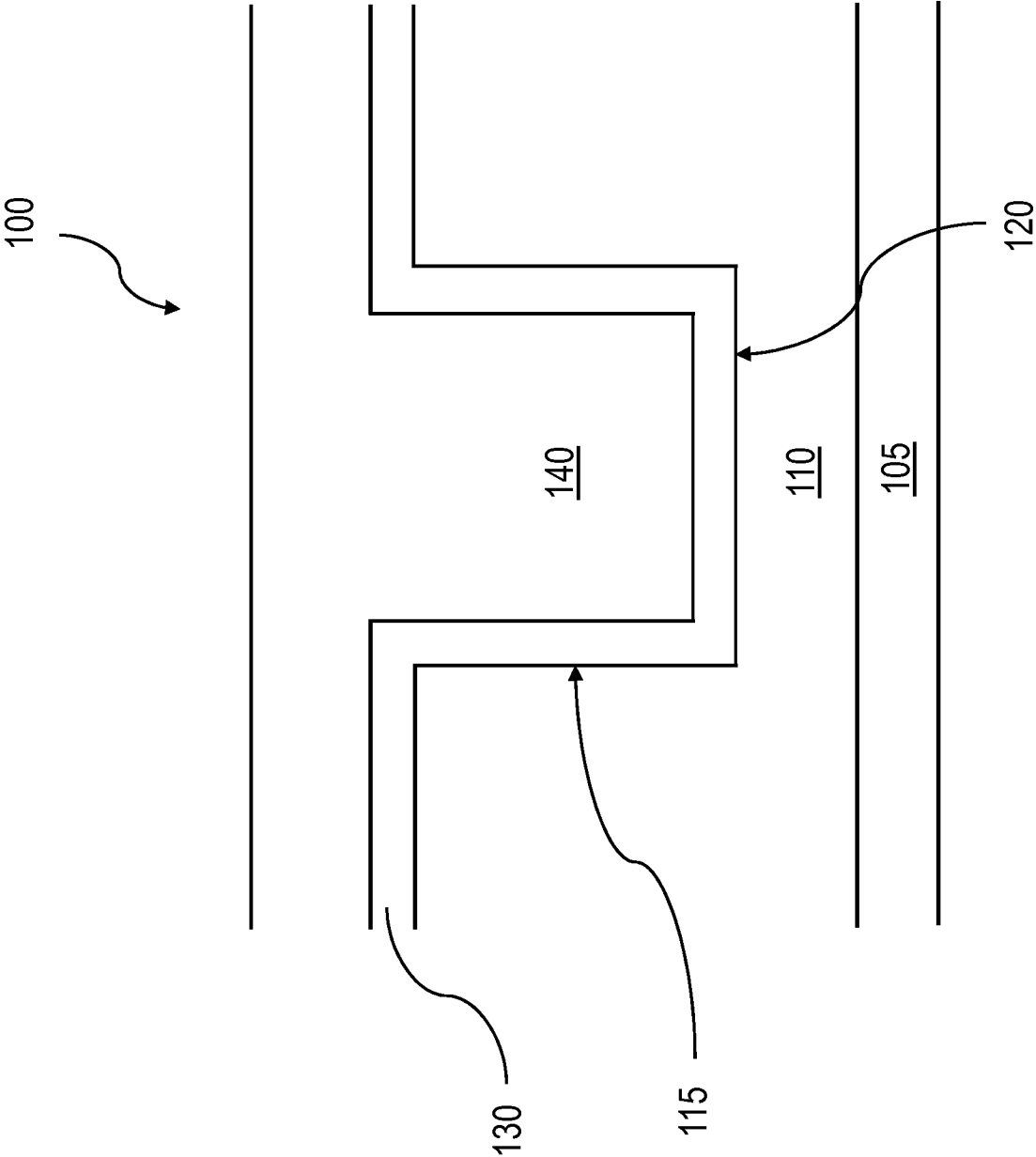


FIG. 1B

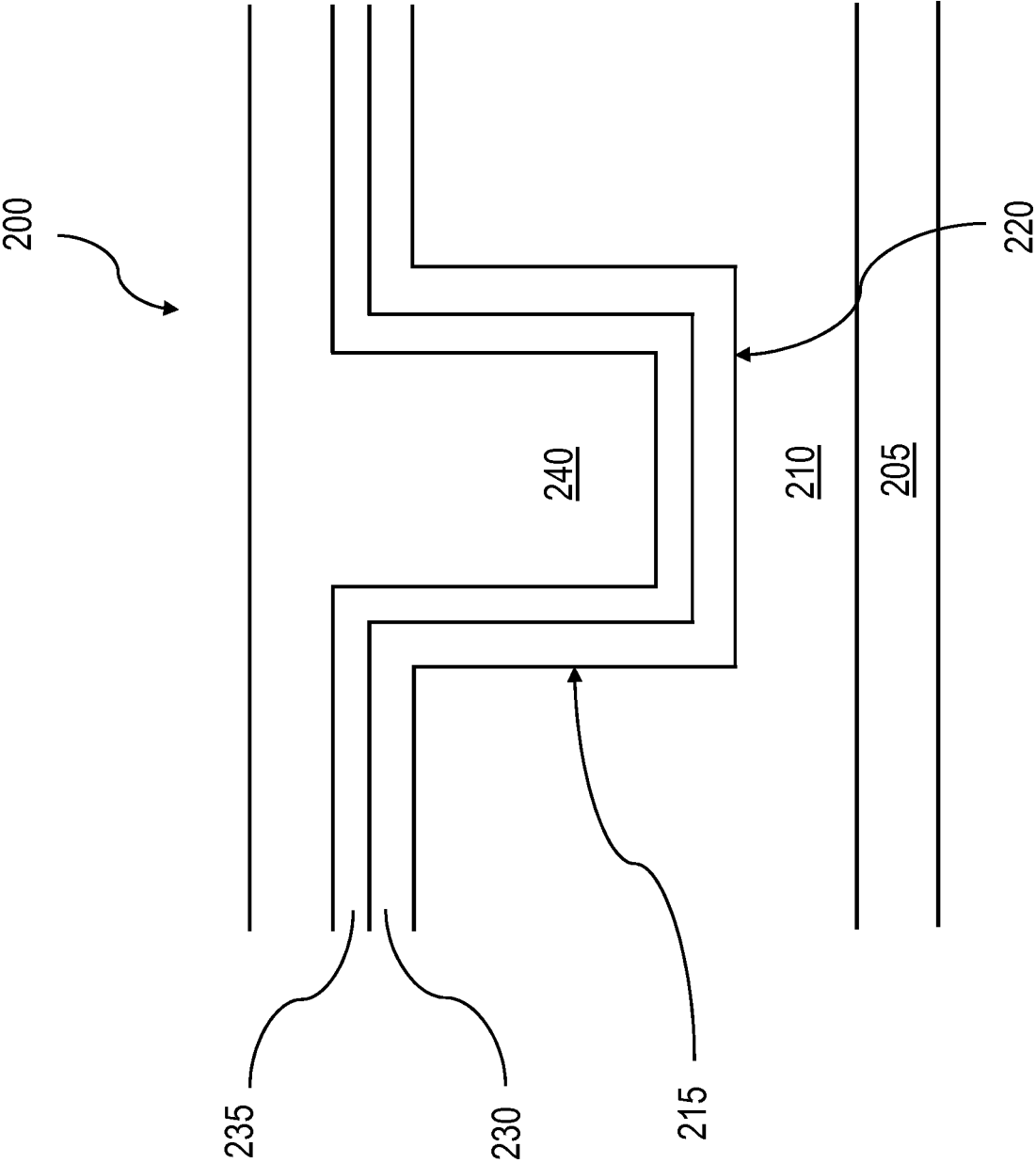


FIG. 2

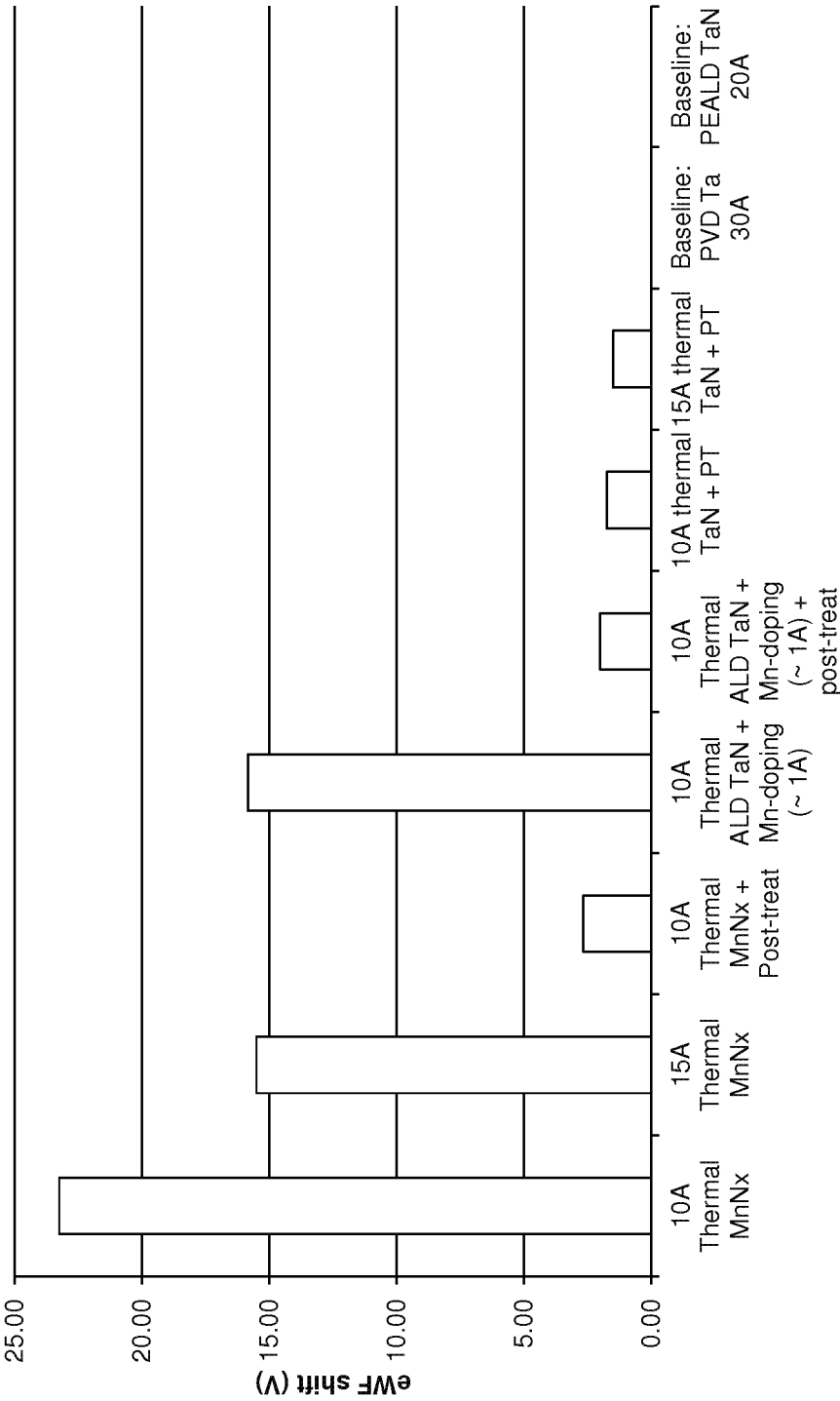


FIG. 3

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2012/067212****A. CLASSIFICATION OF SUBJECT MATTER****HOIL 21/28(2006.01)i, HOIL 21/265(2006.01)1, HOIL 21/318(2006.01)1**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

HOIL 21/28; HOIL 21/768; HOIL 21/4763; HOIL 23/48; HOIL 29/40; C09K 3/14; HOIL 23/532

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
Korean utility models and applications for utility models  
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
eKOMPASS(KIPO internal) & keywords: tantalum, nitride, dopant, trench, barrier, copper**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005-0161817 A1 (MORITZ-ANDREAS MEYER et al.) 28 July 2005 See abstract, paragraphs [0026] -[0039], claims 1, 6, 22, 26-27, 33-37 and figures 1a-1d.	1-3, 8-9, 13
Y		10, 14
A		15
Y	US 2010-0200991 A1 (ROHAN AKOLKAR et al.) 12 August 2010 See abstract, paragraphs [0014], [0019H0023], [0032] and figures 1-4.	10, 14
A	KR 10-2011-0014586 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) 11 February 2011 See abstract, paragraphs [0040], [0046], [0051M0062] and figures 2a-2f.	1-3, 8-10, 13-15
A	US 2004-0188850 A1 (HSIEN-MING LEE et al.) 30 September 2004 See abstract, paragraphs [0019] -[0025] and figures 1A-1C, 1F.	1-3, 8-10, 13-15
A	KR 10-2006-0089219 A (INTEL CORPORATION) 08 August 2006 See pages 2-3, claims 11-12 and figures 1a-1b.	1-3, 8-10, 13-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

25 MARCH 2013 (25.03.2013)

Date of mailing of the international search report

**26 MARCH 2013 (26.03.2013)**

Name and mailing address of the ISA/KR

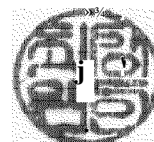
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City 302-70 1 Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

CHOI, Sang Won

Telephone No. 82-42-481-8291



# INTERNATIONAL SEARCH REPORT

International application No.

**PCT/US2012/067212**

## Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2. ☒ Claims Nos.: 7, 12  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:  
  
Claims 7, 12 are not clear, since these claims refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).
  
3. ☒ Claims Nos.: 4-6, 11  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
  
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
  
3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☒ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.



**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2012/067212**

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005-01618 17 A 1	28.07.2005	DE 102004003863 A1 DE 102004003863 B4 US 8039395 B2	18.08.2005 29.01.2009 18.10.2011
US 2010-020099 1 A 1	12.08.2010	US 2008-0223287 A1	18.09.2008
KR 10-2011-0014586 A	11.02.2011	EP 2283513 A1 EP 2283513 A4 JP 2011-523780 A TW 201013840 A US 2009-0289365 A1 WO 2009-142655 A1	16.02.2011 14.11.2012 18.08.2011 01.04.2010 26.11.2009 26.11.2009
US 2004-0188850 A1	30.09.2004	US 7101790 B2	05.09.2006
KR 10-2006-0089219 A	08.08.2006	CN 1618909 A CN 1618909 CO CN 1992179 A CN 1992179 CO EP 1673416 A2 JP 2007-508692 A TW 1313294 A TW 1313294 B US 2005-0070109 A1 US 2006-0097347 A1 US 2006-0099817 A1 WO 2005-033234 A2 WO 2005-033234 A3	25.05.2005 30.05.2007 04.07.2007 04.07.2007 28.06.2006 05.04.2007 11.08.2009 11.08.2009 31.03.2005 11.05.2006 11.05.2006 14.04.2005 26.01.2006