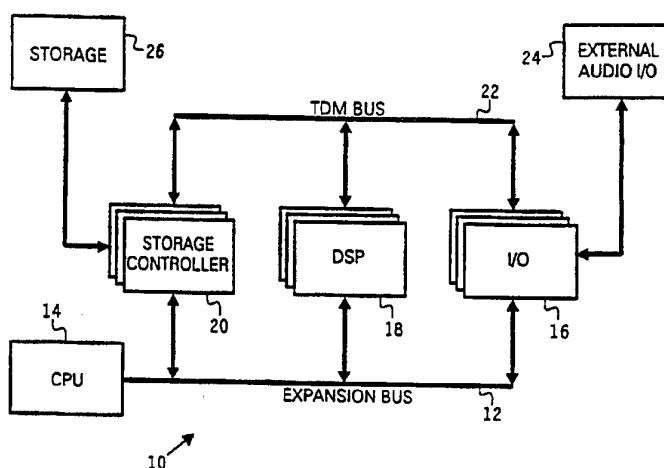




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(21) International Application Number: PCT/US94/04146 (22) International Filing Date: 15 April 1994 (15.04.94)  (30) Priority Data: 049,267                      19 April 1993 (19.04.93)                      US  (71) Applicant: CUSTOM BUSINESS SYSTEMS, INC. [US/US]; 115 S. 20th, Reedsport, OR 97467 (US).  (72) Inventors: WOLNIAKOWSKI, James; 430 - 16th Street, Bellingham, WA 98225 (US). UPPIANO, Karl, A.; 2098 Jeffcott Place, Ferndale, WA 98248 (US).  (74) Agents: BECKER, Mark, L. et al.; Klarquist, Sparkman, Campbell, Leigh & Whinston, One World Trade Center, Suite 1600, 121 S.W. Salmon Street, Portland, OR 97204 (US).		(81) Designated States: AU, BR, CA, FI, JP, KR, NO, NZ, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report.</i>

(54) Title: DIGITAL AUDIO SYSTEM HAVING A TDM BUS FOR SIMULTANEOUSLY TRANSFERRING PLURALITY OF DIGITAL AUDIO SIGNALS



## (57) Abstract

A digital audio system for digitally recording, processing and playing single or multiple audio programs through a computer system. The audio system includes an input/output device (16), a digital processing device (14) and a time division multiplexing ("TDM") bus (22). The TDM bus (22) may simultaneously transfer a plurality of digital audio signals between the digital processing device (14) and the input/output device (16). The digital processing device may include a digital signal processing board (18) for processing digital audio signals or a storage device (20) for storing and playing back a plurality of digital audio signals simultaneously.

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Digital audio system having a TDM bus for simultaneously transferring plurality of digital audio signals.

#### FIELD OF THE INVENTION

The invention relates generally to digital audio signal processing. More specifically, the invention relates to a method and apparatus for digitally recording, processing and playing  
5 single or multiple digital audio programs through a computer system.

#### BACKGROUND OF THE INVENTION

The increasing speed and versatility of personal computers ("PCs") coupled with the advantages of digital media for the storage and transmission of audio signals make the combination of computers and digital signal processing an attractive option. Unfortunately, the  
10 present computer architecture of personal computers significantly limits the capacity of the computer to control simultaneous processing, recording, and playback of multiple digital audio signals. Such control is particularly valuable in, for example, the radio broadcasting and music studio industries where multiple stereo channels are often simultaneously recorded, processed, and transmitted.

Existing computer-based digital audio systems, because they use the PC expansion bus for both control and manipulation of digital audio programs, have limited capacity. The bandwidth of the expansion bus can support no more than three low fidelity programs simultaneously. This capacity is barely adequate to support a single music studio, requiring the installation of multiple systems to support the multiple studios found in a typical recording or  
20 broadcast facility. This leads to wasteful duplication of storage and other computer resources.

In addition, the typical storage format of the computer system's hard disk is not optimal for digital audio. Although it is possible to install a second disk with the appropriate formatting, this does not solve the bus bandwidth problem.

A typical radio station, for example, may wish to record simultaneously from several  
25 external program feeds (such as an audio network), in addition to multiple production sections and transmitter feeds, any of which may require different digital sample rates. It is not uncommon for a radio station to simultaneously operate dozens of active transmission channels to support these multiple activities.

Because of the limitations of the existing computer-based digital audio systems, there  
30 is a need for an improved digital audio system that can control processing, recording, and transmission of digital audio signals simultaneously. This improved system should have the capability to transfer simultaneously a large number of digital signals having various sample rates. Such a system would be useful in radio broadcasting to control many radio stations simultaneously from a single computer server. In addition, such a system would be useful in  
35 other audio processing applications such as in the music studio industry.

SUMMARY OF THE INVENTION

It is the object of the invention, therefore, to provide a digital audio system that may process, record, and transmit several digital audio signals simultaneously, such that multiple audio facilities may have access to common storage and processing devices.

5           Another object of the invention is to provide a digital audio system that may transfer several digital audio signals simultaneously and at various sample rates.

Still another object of the invention is to provide a digital audio system with a dedicated audio storage device that formats audio data in a manner that saves storage space and enhances accessibility of the data.

10           To achieve these objects, the invention provides a digital audio system and a method for providing simultaneous control of a plurality of digital audio signals in a computer system. The digital audio system includes an input/output device, a digital processing device, and a time division multiplexing ("TDM") bus. The TDM bus may simultaneously transfer a plurality of digital audio signals between the digital processing device and the input/output device. The  
15           digital processing device may include a digital signal processing board for processing digital audio signals or a storage device for storing and playing back a plurality of digital audio signals simultaneously.

A TDM bus, separate from the expansion, or computer bus, increases the data transfer capability of the system. The TDM bus may allow the simultaneous and bidirectional  
20           transfer of a plurality of digital audio signals between an input and output of a single input/output device as well as among an input/output device and a plurality of input/output devices or digital processing devices. The TDM bus also may allow the simultaneous and bidirectional transfer of a plurality of digital audio signals among a plurality of input/output devices and digital processing devices, including either storage devices or digital signal  
25           processing boards. The TDM bus may transfer digital audio data in a system with only input/output devices, with an input/output device and either a digital signal processing or storage device, or with a digital signal processing and storage device.

The storage device coupled to the TDM bus may be dedicated for the storage of audio data. Each sample of the audio data may be separated into subunits, and these subunits  
30           may be stored contiguously within a storage device. This data formatting increases the efficiency with which audio data, having varying sample lengths, may be stored in a storage device. Additionally, this data formatting may enhance the accessibility of audio data and facilitate "cut and paste" editing without the use of a digital processing board.

The TDM bus may transfer at least two digital audio signals at differing sample rates  
35           simultaneously. The TDM bus may be coupled to a bus master for providing a plurality of sync signals, each possibly having differing sample rates. This feature of the invention enables the system to simultaneously control digital signals operating at a standard sampling rate or any other sampling rate within a wide range of rates.

The advantages and features of the invention will become apparent to those skilled in the art from the following description and accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a digital audio system according to the invention.

5        FIG. 2 is a block diagram of an input/output ("I/O") portion of the digital audio system of FIG. 1.

FIG. 3 is a block diagram of a storage controller portion of the system of FIG. 1.

FIG. 4 is a block diagram of a digital signal processing portion of the system of FIG. 1.

10        FIG. 5 illustrates the waveforms of a TDM bus for transferring audio data within the system of FIG. 1.

FIG. 6 illustrates the waveforms of the frame sync and master clock signals on the TDM bus.

#### DETAILED DESCRIPTION OF THE INVENTION

15        FIG. 1 illustrates a block diagram of a digital audio system 10 according to an embodiment of the invention. The audio system 10 is presently implemented within a personal computer having an expansion bus 12 for coupling peripheral devices known as expansion boards to the central processing unit ("CPU") 14 of the computer. Throughout the description of the embodiment, the term "CPU" is used generally to mean the microprocessor of the computer along with memory and controller devices used to store software or firmware programs and communicate with peripheral devices coupled to the expansion bus 12. The present embodiment of system 10 includes a plurality of expansion boards that plug into the PC along an expansion bus 12. The system includes three expansion boards that correspond to three portions of the system: an input/output ("I/O") board 16, a digital signal processing board ("DSP") 18, and a storage controller board 20. However, the components on the three expansion boards could be integrated into a single board or designed into the computer itself, if desired. The system may include any number of I/O, DSP or storage controller boards 16, 18, 20, but is limited in total number to the maximum number of expansion slots in the computer system.

30        To transfer audio data among the expansion boards, the system has a TDM bus 22 intercoupling each of the portions of the system 10. Running at a clock speed such as 8.33 MHz, the TDM bus 22 is multiplexed into 128 time slots to provide a maximum sample rate per time slot of 65kHz. The maximum sample rate can be varied by changing the number of time slots or the clock speed. The TDM bus 22 may transfer up to 32 bits of audio data in parallel at each time slot. Because the TDM bus 22 in the present embodiment has 128 time slots, up to 128 audio programs may be transferred among expansion boards on the expansion bus 12 simultaneously.

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Physically an expansion board is coupled to the TDM bus 22 through right angle connectors, spaced every 0.9" along the TDM bus 22. The TDM bus 22 is comprised of a 100 conductor ribbon cable. Right angle headers of the expansion boards mate with the connectors on the ribbon cable at the top of the boards.

5 All bus lines may be terminated at each end with a 220 Ohm pull-up resistor to VCC and a 330 Ohm pull-down resistor to ground. If active termination is used, it may have a termination impedance of 110 Ohms, be capable of sourcing 20 milliamps when the line is in the logic low state, and pull the line up to at least 2.5 volts when the line is open or in the logic high state. Since any particular board may be located anywhere along the TDM bus 22, it  
10 should be possible to configure any board to correctly terminate the TDM bus 22.

The I/O, DSP, and storage controller boards 16, 18, 20 each receive control signals from the CPU 14 through the expansion bus 12. In response to control signals from the CPU 14, the I/O board 16 receives or transmits serial digital data to and from external audio I/O 24, respectively. The I/O board 16 may receive input audio data and transfer the data  
15 along the TDM bus 22 to either the DSP board 18 for signal processing or to the storage controller board 20 for storage on a dedicated audio storage device 26. The I/O board 16 may transfer audio data to at least another board, including another I/O board, and may transfer data from an input and an output on a single board.

In response to control signals from the CPU 14, the storage controller board 20 may  
20 play back or record digital audio data. The storage controller board 20 may transfer digital data to the DSP board 18 for processing to the I/O board 16 for transmitting digital data to an external I/O device 24 or to both simultaneously.

Finally, the DSP board 18 responds to control signals from the CPU 14 to execute any number of editing or signal processing functions. The DSP board may transfer data to  
25 several other boards simultaneously, and may receive and transfer data simultaneously. In this manner, the CPU 14 controls the operation of each of the expansion boards through the expansion bus 12.

The CPU 14 and expansion bus 12 are components of a host computer system. The host computer is preferably an IBM compatible personal computer with an EISA ("Extended  
30 Industry Standard Architecture") expansion bus. For convenience, the terms "expansion bus" and "EISA bus" are used interchangeably because the system 10 includes an EISA compatible expansion bus. While a personal computer compatible with an EISA expansion bus is preferred, it should be understood that any suitable data processing unit coupled with other standard or proprietary expansion buses could provide the host processing function for the  
35 system. For example, the system may include an IBM or IBM compatible personal computer with a 386, 486, or more advanced compatible CPU 14 from Intel Corporation. The system 10 also supports M/PS processors from M/PS Corporation, Alpha processors from Digital Equipment Corporation, or even multiple processor computers. The computer typically

includes a hard disk drive or equivalent mass storage device for storage of audio system software. NT operating software from Microsoft or any similar operating software may be used to operate the system 10.

Each of the expansion boards of the system plug into the EISA bus 12 of the computer at standard EISA bus interface circuits. FIGS. 2, 3, 4, showing block diagrams of the I/O, DSP, and storage controller boards 16, 18, 20 respectively, each having a standard EISA bus interface 30, 32, 34 electrically coupling the respective board to the EISA bus 12. Such EISA bus interface are known in the art and readily commercially available. For example, the HD64981F EISA Slave Interface Controller (ESIC) from Hitachi Corporation may serve as an EISA interface for the I/O board 16, storage controller board 18, and DSP board 20.

FIG. 2 illustrates a block diagram of an I/O portion 16 within the audio system 10. The audio system 10 receives serial digital audio at a digital receiver 40 and transmits serial digital audio data at the digital transmitter 42. For simplicity, FIG. 2 illustrates the incoming and outgoing serial audio signals as single serial transmission lines 44, 46. However, the input line 44 represents eight stereo inputs and the output line 46 represents eight stereo outputs. Each stereo input and output typically have left and right channels. For each stereo input, the I/O board includes a digital receiver chip such as a CS8411 from Crystal Semiconductor. Similarly, for each stereo output, the I/O board includes a digital transmitter chip such as an 8401, also from Crystal Semiconductor. For simplicity, the receiver and transmitter chips are each shown as single blocks, digital receiver 40 and digital transmitter 42. Overall, an I/O board 16 has 16 input channels and 16 output channels. The system 10 can accommodate more I/O boards 16 to provide for additional input and output capacity.

The I/O board 16 is electrically connected to the TDM bus 22 through a bus driver 50. The bus driver 50 includes data transceiver chips for passing audio data from input and output registers 54, 56 on the I/O board 16 to the TDM bus 22. The bus driver 50 of the I/O board 16 includes several 8 bit transceiver chips, which may be a standard bus interface IC from the 74F family. For example each 32-bit input and output register 54, 56 may be coupled to four of such chips depending on the word length requirements of a particular application. Certain portions of the I/O board 16, such as the clock oscillator 60 and sync clocks 62 have a tri-state output coupled with an enable in addition to standard discrete buffers. The additional tri-state output is required because only one I/O board 16 may serve as bus master at one time. Finally, the bus driver 50 includes discrete buffers that provide bus driving and isolation functions.

An I/O board 16 of the system 10 serves as the bus master for the TDM bus 22. Generally, the bus master provides the timing for TDM bus 22 operation and synchronization of signals on the bus 22. Timing originates from three primary sources: 1) a clock oscillator 60; 2) frame syncs 70 derived from incoming digital data at the digital receiver 40; and 3) a sync clock 62. The clock oscillator 60 of a single I/O board 16 serves as the bus

master for the system. Producing a square wave running at 8.33 MHz, the clock oscillator 60 provides the master clock signal, TDMCK. The clock oscillator 60 also has an internal 128 counter. When the counter recycles to zero, the clock oscillator 60 provides a TDM channel zero signal, TDMCH0, used to synchronize the TDM bus 22.

5           The sync clock 62 includes three oscillators, each running at 128 times the standard sampling frequencies of 32, 44.1, and 48 kHz. The three clock signals are each divided by 128, using modulo 128 counters, and then are coupled to inputs of five multiplexers along with the eight frame sync signals from each of the receivers. With these five multiplexers, the sync clock 62 can provide five frame sync signals, FS0-FS4, shown in FIG. 5. The frame sync signals  
10 are coupled to the TDM bus 22 through control lines 64 and a tri-state output and buffer in the bus driver 50. Similarly, the output of the three clocks are multiplexed along with master clock signals provided by the eight receiver chips to provide five total master clock signals, MCK0-MCK4. These signals are also coupled to the TDM bus 22 through control lines 64 and tri-state outputs and buffers located in the bus driver 50. The master clock signals,  
15 MCK0-MCK4, may be used in a transmitter 42 and receiver 40 to operate their internal state machines. A device such as a receiver 40 or transmitter 42 that drives a frame sync must also correctly drive an associated master clock line.

A multiplexer in the sync clock 62 is coupled to each of the frame sync signals, FS0-FS4, shown in FIG. 5. This multiplexer is coupled to the frame sync lines of the TDM bus 22 through a buffer between the TDM bus 22 and the sync clock 62. In particular, the  
20 multiplexer is coupled to the TDM bus 22 through control lines 64 on the bus side of the tri-state outputs coupled to the five multiplexers that produce the frame sync signals. Coupled to the EISA bus interface 30 through control lines 65, this final multiplexer provides a frame sync signal for the eight transmitter chips shown as the transmitter 42 in FIG. 2. The transmitter 42  
25 is coupled to the sync clock 62 through control lines 66 to receive frame sync signals from the final multiplexer. This frame sync signal synchronizes the transfer of data from a transmitter 42 to an external audio I/O device 24.

Just as the multiplexer described in the proceeding paragraph, the five frame sync signals from the TDM bus 22 are each coupled to the sync counter comparator 74 through a  
30 buffer and control lines 68. The sync counter comparator 74 includes a 16-bit counter that is expanded in the CPU 14 to a 64-bit counter through the use of software. The sync counter comparator 74 also includes a matching 16-bit comparator expanded to 64 bits through the use of software and programmed from the EISA bus interface 30 through control and data  
lines 69. By counting the number of frame syncs, the sync counter provides program length  
35 information to the CPU 14. The comparator may be used to signal the end of a transfer with an interrupt when the counter value matches the comparator value loaded into the comparator.

Each of the multiplexers of the sync clock 62 are coupled to the EISA bus interface 30 through control lines 65 to receive the appropriate select signals from the CPU 14.

For example, to transmit an audio program at a sample rate of 44.1 KHz used in CD technology, the CPU would signal the multiplexer to select a frame sync signal driven at 44.1 kHz by the oscillator in the sync clock 62.

5 In addition to serving as the bus master, the I/O board 16 receives and transmits serial digital audio through incoming and outgoing serial transmission lines 44, 46 coupled to the receiver and transmitter, respectively. The transmitter and receiver each have several modes compatible with standard digital formats. For example, serial digital audio may adhere to the Audio Engineers Standard ("AES")/European Broadcasting Union ("EBU") format. This format supports a maximum audio word length of 32 bits, with a possible range of 16 to 10 24 bits of audio data. For example audio data in CD technology has a word length of 16 bits while audio data typical in music studios has a word length of 16 to 24 bits. In the case of studio audio, 24 bits of the 32 bit digital signal is audio data and the remaining 8 bits include user data, control data, parity, validity, and 4 bits of sync preamble information. In the AES/EBU format, the digital signal is a serial stream of bits and each digital signal, including 15 two stereo channels, enters the I/O board 16 in one of 8 serial transmission lines, each carrying a stereophonic digital audio signal.

The serial digital signal enters the system at the digital receiver 40. The digital receiver 40 is a digital receiver IC chip commercially available from Crystal Semiconductor. The receiver 40 is coupled to a serial-to-parallel register 80, hand shake logic 84, a sync 20 clock 62, and the EISA bus interface 30. The receiver 40 transfers data to the serial-to-parallel register 80. The receiver 40 transfers frame sync signals to both the sync clock 62 through control lines 82 and the handshake logic 84 through control lines 70. Finally, the receiver 40 communicates with the EISA bus interface 30 through control and data lines 83.

The digital receiver 40 separates the audio data from the control and user data. 25 Using a phase locked loop circuit, the digital receiver 40 extracts a frame sync signal from the incoming serial signal. Through data and control lines 85, the receiver sends serial audio data to the serial-to-parallel register 80. The receiver 40 either uses its internally generated frame sync or uses frame sync and master clock signals from the sync clock 62 to control transfers.

In response to control signals from the CPU through the EISA bus interface 30, the 30 receiver 40 transmits serial audio data to a serial-to-parallel register 80. The receiver 40 fills the serial-to-parallel register 80 with the left and right channels of incoming audio data. Data is serially shifted into the serial-to-parallel register 80, which has a total length of 48 bits, with 24 bits each for the left and right channel. The receiver chip sends only the audio data portion of the incoming signal, so if the data has length less than 24 bits per channel, then the lowest 35 bits of each 24 bit register are unused. The receiver communicates the non-data portion, including channel status and auxiliary data, to the EISA bus interface 30. With each pulse of the frame sync, the serial-to-parallel register 50 transfers its contents in parallel to an input register 54.

The input register 54 holds a left and right channel of audio data and awaits an address signal from a channel map 90 to transfer the audio data through 32 data lines 86 and transceiver chips in the bus driver 50 to an active time slot on the TDM bus. The channel map 90 includes RAM for storing channel mapping information downloaded from the EISA bus interface 30 through control and data lines 87. Specifically, the channel map 90 contains the address of an input register 54 if data is to be written from the I/O board 16 to the TDM bus 22. The channel map 90 has 5 lines 89 coupled to a decoder for selecting one of the 16 output registers 56 to write data from the TDM bus 22 through the bus driver 50. The channel map 90 contains the address of an output register 56 if data is to be read from the TDM bus 22. The channel map 90 has 16 separate lines 88 for this reading function to drive each of the input registers 54.

The output register 56 reads data when the I/O board 16 transmits audio data to an external audio I/O 24. The I/O board 16 includes circuitry that performs essentially the reverse operation of the receiver 40 and input registers 54. Through the EISA bus interface 30, the CPU 14 sets the channel map 90, selects the frame sync from the bus using the multiplexer of the sync clock 62, and controls the operation of the transmitter 42.

In response to a signal from the channel map 90, the output register 56 begins to read data from the TDM bus 22 through transceiver chips of the bus driver 50 and through data lines 92. With each pulse of the frame sync signal, the output register 56 shifts data in parallel to a parallel to serial register 96. This frame/sync signal, which is selected from one of the TDM frame sync lines, is sent to a set/reset flip flop inside the handshake logic 84 to produce a data request signal to the TDM bus 22. In response to the data request, the output register 56 may read the next data from the appropriate time slot on the TDM bus 22.

At the same time, the transmitter 42 is serially clocking in data from the parallel to serial register 96. The transmitter 42 is coupled to the parallel to serial register 96 through control and data lines 99. The transmitter clocks in serial digital data at 64 times a frame sync rate derived from a frame sync signal from the sync clock 62. The transmitter then transmits serial audio data at a sampling rate specified by the CPU 14 to an external audio I/O device 24. In general, the transmitter may be controlled through control lines 101 coupling the transmitter 42 to the EISA bus interface 30.

In addition to serving as the bus master and providing system input and output, the I/O board 16 synchronizes the TDM bus 22. To synchronize the TDM bus 22, the I/O board 16 includes synchronizing maps 100 and an address counter 102.

The I/O board 16 has an address counter 102 coupled to the TDMCK, and TDMCH0 signals 104 of the TDM bus through a buffer in the bus driver 50. The address counter 102 is a modulo 128 counter that begins counting at zero in response to the TDMCH0 signal. The TDM clock runs the counter such that the counter corresponds to the current

active time slot of the TDM bus 22. The address counter 102 communicates the active time slot to both the channel map 90 and the synchronizing maps 100 through control lines 106.

The I/O board 16 includes synchronizing maps 100 implemented with two 1 x 128 RAM devices. The I/O board 16 has two synchronizing maps because one map is active while the other is being set up by the CPU 14. The synchronizing maps 100 are coupled to the TDM bus 22 through a buffer in the bus driver 50. The synchronizing maps are also coupled to the hand shake logic 84 and the address counter 102. Using the address counter 102, a synchronizing map 100 provides a signal, TDMOK (108), indicating which time slots are enabled. Each synchronizing map has 128 one bit memory units corresponding to the 128 time slots of the TDM bus 22. The TDMOK signal (108) from the synchronizing map provides a means for simultaneously starting and stopping data transfers on multiple time slots of the TDM bus 22. The synchronizing maps 100 communicate the TDMOK signal (108) to the TDM bus 22 and to hand shake logic on the I/O board.

The system 10 in general controls transfers among boards with the use of handshake logic on each board. Each board may act as a bus reader or bus writer to the TDM bus 22. The bus readers and writers each have a double memory buffer to synchronize transfers on the bus 22. Different components on each board play the role of the double memory buffer. For example, on the I/O board 16, the input and serial-to-parallel registers 54, 80 serve as double buffers of a bus writer, and the output and parallel to serial registers 56, 96 serve as double buffers of a bus reader.

The control signals for a bus transfer are frame sync (FS0-FS4), TDMOK, TDMRD, and TDMWR. TDMWR is asserted by a bus writer when an address counter 102 on the writer indicates that a time slot is active, and when a data available flag is set. TDMRD is asserted by a bus reader when the time slot is active, and when the bus reader sets a data request flag. The bus master, an I/O board 16, asserts TDMOK during an active time slot if the synchronizing map contains an enabling signal for that time slot.

The transfer of data to the TDM bus 22 using double buffering can be described by way of example on the I/O board 16. To transfer data from the I/O board, the process begins when the serial-to-parallel register 80 transfers data to the input register 54. This transfer occurs with each frame sync transition from low to high. This transition sets a "data available" flag in the hand shake logic. At the same time, the double buffer of a reader transfers data between its buffers and a data request flag is set. During the active time slot for a channel, if data available is set, then the I/O board enables the TDMWR signal. Similarly, if the data request is set on the reader, then the reader enables the TDMRD signal. Finally, if the synchronizing map asserts a TDMOK for the time slot, then a transfer occurs. The handshake logic 84 combines the TDMOK, TDMRD, and TDMWR signals through an AND gate to produce a signal that enables the transfer and also clears the data available flip flop.

Analogous hand shake circuitry in the bus reader clears the data request flag. In this manner, the handshake logic facilitates the transfer of data on the TDM bus 22.

Possible designs for the I/O board are not limited to the discrete components described above. Several of the devices on the I/O board are implemented within a field programmable grid array (FPGA). The input and serial-to-parallel registers 54, 80 conceptually include 16 separate 24-bit registers. Each of these registers are implemented within a FPGA chip. Similarly, the output and parallel to serial registers 56, 96, including 16 separate 24-bit registers, are implemented within an FPGA. Both the channel map 90 and the synchronizing maps 100 are implemented within a FPGA chip. The FPGA may be a 4010 from Xilinx Corporation, but any equivalent FPGA or applications specific integrated circuit ("ASIC") with similar memory capabilities may suffice. In general, the invention should not be limited to the implementation described because many equivalent circuit designs, using a variety of discrete and/or programmable logic elements could perform the function of the I/O board 16.

In summary, one I/O board 16 in the system 10 serves as the bus master, and each I/O board 16 may be used to transmit and receive serial digital audio signals from the system 10. The I/O board may transfer audio data over the TDM bus 22 to the DSP board 18 for processing, to the storage controller board 20 for storage on a dedicated storage device, to another I/O board, or to a transmitter on the same I/O board 16.

FIG. 3 shows a block diagram of the storage controller board 20. The storage controller board 20 controls the transfer of up to 32 channels of audio data to and from a storage device 26, which in this embodiment includes up to seven SCSI storage devices. The particular storage controller board 20 in this system 10 is designed to control recording and playback from a SCSI storage device 110, but the underlying principle of the invention is not limited to SCSI compatible devices. The storage controller board 20 shown in FIG. 3 may control any SCSI compatible storage device. The storage device should have sufficient storage capacity and data transfer speed depending on the amount of data to be stored and the number of channels to be transferred.

Generally, the storage controller board 20 includes the following components: a bus driver 112, dual ported static RAM ("SRAM") 114, DRAM 116, SCSI control and interface 118, an EISA bus interface 32, and control and handshake logic 120.

The bus driver 112 provides buffering and isolation between the board and the TDM bus 22. The bus driver 112 couples the TDM bus 22 to the dual ported SRAM 114 and to the control and handshake logic 120. The data lines, TDM0-31, on the TDM bus are coupled to four 8-bit transceiver chips in the bus driver 112. These transceiver chips drive the TDM bus 22 and provide isolation between the data lines 122 of the dual ported SRAM 114. Buffers

in the bus driver 112 couple the signals TDMCK, TDMCHO, TDMRD, TDMWR, and TDMOK on the TDM bus to the control and handshake logic 120 through control lines 121.

5 The dual ported SRAM 114 performs a remapping function of data transferred from the DRAM 116. The dual ported SRAM 114 is coupled to the DRAM 116 through a common data bus 124 shared by the dual ported SRAM 114, the DRAM 116, and the SCSI control and interface 118. The dual ported SRAM is also coupled to the control and handshake logic through two sets of control and address lines 126, 128. One set of control and address lines 126 corresponds to the TDM port 130 while the other set 128 corresponds to the DRAM port 132 of the dual ported SRAM 114.

10 The DRAM 116 temporarily stores sections of data passing between the SCSI controller and interface 118 and the dual ported SRAM 114. The DRAM 116 is coupled to the control and handshake logic through address and control lines 134. The DRAM is coupled to the SCSI controller and interface 118 through the common data bus 124.

15 The control and handshake logic 120 controls the transfer of data among the SRAM 114, DRAM 116, TDM bus 22, and SCSI control and interface 118. The control and handshake logic 120 communicates with the CPU 14 through the EISA bus interface 32 to receive and transmit data transfer information. To facilitate the control of the SCSI control and interface 118, the control and handshake logic 120 includes chip selection logic and is coupled to the SCSI control and interface 118 through control lines 140. In response to control signals through control lines 138, the control and handshake logic 120 transfers the appropriate control and data transfer information between the SCSI interface 118 and the EISA bus interface 32. To control the transfer of audio data from the memory of the SRAM 114 and DRAM 116 devices, the control and handshake logic 120 includes a TDM controller and a direct memory address controller ("DMA").

25 The TDM controller specifically controls the transfer of data between the TDM bus 22 and the SRAM 122. To coordinate transfers to the TDM bus 22, the TDM controller is coupled to the TDMCK, TDMCHO, and TDMOK signals from the bus and is capable of driving or receiving TDMRD and TDMWR signals. Like the I/O board 16, the TDM controller includes a modulo 128 address counter to keep track of the active TDM time slot. 30 The TDM controller also includes handshake logic that uses the TDMRD, TDMWR, and TDMOK signals to control transfers to and from the bus. The TDM controller is coupled to the control and address lines 126 of the SRAM that correspond to the TDM port 130. By providing the appropriate address and control to the TDM port 130 of the dual ported SRAM, the TDM controller can transfer audio data to and from the TDM bus 22.

35 To control transfers of data between the DRAM 116 and the dual ported SRAM 114, the DMA is coupled between the address and control lines of the DRAM 126, 128 and the DRAM port 132 of the dual ported SRAM 114. The DMA is event driven such that it will initiate transfer of data when, for example, a certain boundary or threshold in memory has

been crossed. As the SRAM 114 fills or empties, it will trigger the DMA to transfer data between the SRAM 114 and the DRAM 116.

While many variations are possible, the DRAM 116 typically will be designed to store relatively large sections of data in the DRAM 116 than in the dual ported SRAM 114.

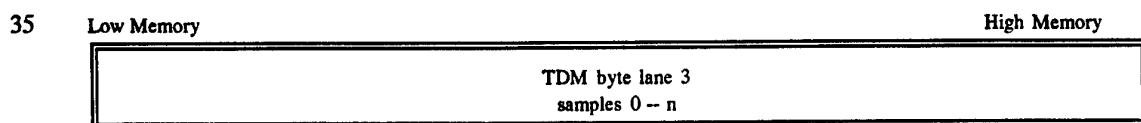
5 Because DRAM 116 is relatively inexpensive compared to SRAM 114, it is cost effective to use more DRAM 116 for temporary storage during transfers rather than using solely SRAM. It is possible, for example, to use only the dual ported SRAM 114 to transfer data between storage and the TDM bus 22, but this alternative is significantly more costly than using both a large DRAM portion and a smaller SRAM portion.

10 To implement the control and handshake logic 120, the storage controller board has a FPGA. The FPGA is programmed to provide the TDM controller, the DMA, and the chip selection logic described above. While several commercially available FPGA chips may be suitable, this particular embodiment includes a 4010 from Xilinx Corporation. It should be understood that the hand shake and control logic 120 could be implemented in various ways  
15 using either ASICS programmable logic chips, discrete devices, or a combination of each.

The SCSI control and interface 118 controls the operation of up to seven SCSI storage devices. The SCSI control is coupled to the DRAM through address and control lines 136 and is coupled to up to seven SCSI storage devices through data lines 142. Through the EISA bus interface 32 and chip selection logic, the CPU 14 may control the SCSI control  
20 and interface 118. The SCSI control and interface 118 may be a 53C720 chip commercially available from NCR Corporation. This chip is easily programmable to control data transfer from a SCSI storage device 110. Other SCSI controller chips could be readily substituted for this application.

In operation, the storage controller uses a unique data storage format. This data  
25 storage format increases the efficiency of storing data samples with varying word length. While standard hard drive controllers typically transfer data in either 8, 16, or 32-bit words from the hard drive, this board 20 is optimized for transfer of 32-bit words. Audio data samples, however, may have a word length of 8, 16, or 24 bits. This data format maximizes the use of storage of data having varying lengths by breaking the data into 8-bit bytes. The data format  
30 also makes audio data more accessible on the SCSI storage device and simplifies editing of stored audio programs.

Section format for 8 bits/sample (k=1):



Section format for 16 bits/sample (k=2):



TDM byte lane 3 samples 0 – n/2	TDM byte lane 2 samples 0 – n/2
------------------------------------	------------------------------------

Section format for 24 bits/sample ( $k=3$ ):

5

Low Memory		High Memory
TDM byte lane 3 samples 0 – n/3	TDM byte lane 2 samples 0 – n/3	TDM byte lane 1 samples 0 – n/3

10

Section format for 32 bits/sample ( $k=4$ ):

Low Memory			High Memory
TDM byte lane 3 samples 0 – n/4	TDM byte lane 2 samples 0 – n/4	TDM byte lane 1 samples 0 – n/4	TDM byte lane 0 samples 0 – n/4

15

**TABLE 1**

TABLE 1 graphically represents the manner in which data samples are formatted for storage. Under the format, a sample is separated into 8 bit segments known as bytes. The dual ported SRAM 114 of the storage controller board 20 operates as a mapping buffer in that it divides audio samples into bytes depending on the length of the sample. The mapping buffer conceptually has four byte lanes: TDM byte lane 0, TDM byte lane 1, TDM byte lane 2 and TDM byte lane 3. If the audio sample has 8 bits, all samples are stored in TDM byte lane 3. If the audio sample has 16 bits, the lower byte of each sample is stored in TDM byte lane 3 and the higher byte is stored in TDM byte lane 2. If the audio sample has 24 bits, the low byte is stored in TDM byte lane 3, the medium byte is stored in TDM byte lane 2, and the high byte is stored in TDM byte lane 1. Finally, if the audio sample has 32 bits, the four bytes of the sample are stored in TDM byte lanes 3 to zero, from low to high, respectively. In this manner, each audio sample having more than one byte is separated into its separate byte components. When stored on a storage device such as a SCSI hard drive, samples are not stored contiguously. Rather, bytes of similar position, for example the lowest bytes, or subunit, of the samples, are stored contiguously. TABLE 1 illustrates specifically how data is stored on a storage device using the format. Each box represents an allocation unit with a storage capacity of  $n$  bytes. A storage unit such as a hard drive stores data in an allocation unit, for example, a disk sector. Each allocation unit is divided into  $k$  subunits, where  $k$  equals the number of bytes in a sample. For example for a 24 bit sample, a disk allocation unit is divided into 3 subunits. Each subunit consists of either all low, medium or high bytes from the 24 bit data. In other words, each 24 bit sample is separated into three parts and is stored in separate subunits of an allocation unit.

To implement this data format, only a single mapping buffer is necessary. However, because this embodiment uses SRAM as well as DRAM, the format will be described in the context of this particular embodiment. It should be understood that the underlying invention could be implemented in various ways without exceeding the scope of the invention.

As noted, the dual ported SRAM 114 serves as the mapping buffer. Because the SRAM has dual ports, the mapping buffer has two perspectives: the TDM view and the DRAM view. Fixed in hardware, the mapping buffer uses addressing at the TDM port 130 to ensure that samples are properly assembled from the perspective of the TDM bus 22 and uses  
 5 addressing at the DRAM port 132 to format the samples for storage as outlined above. The specific manner of storage in the DRAM 116 is not critical. However, the DRAM 116 must store and the SCSI controller 118 must transfer the samples such that the separation of the bytes according to the format is maintained. Because the DRAM memory is relatively flexible in the sense that it is not performing critical mapping, the memory locations may be defined  
 10 and altered using software. For example, if samples have two bytes, then the DRAM may be divided into two sections corresponding to TDM byte lanes 2 and 3. In this example, the mapping buffer would not change, but only memory locations corresponding to TDM byte lanes 2 and 3 would be used.

15		DRAM Byte Lane 0	DRAM Byte Lane 1	DRAM Byte Lane 2	DRAM Byte Lane 3
	{	0	1	2	3
	TDM Byte Lane 3 {	...	...	...	...
		8188	8189	8190	8191
	{	8192	8193	8194	8195
20	TDM Byte Lane 2 {	...	...	...	...
		16380	16381	16382	16383
	{	16384	16385	16386	16387
	TDM Byte Lane 1 {	...	...	...	...
		24572	24573	24574	24575
25	{	24576	24577	24578	24579
	TDM Byte Lane 0 {	...	...	...	...
		32764	32765	32766	32767

**TABLE 2**

30 TABLE 2 shows the mapping buffer from the perspective of the DRAM. The contents of the mapping buffer memory are arranged in four sections corresponding to TDM byte lanes zero through three. This is shown along the vertical border of the mapping buffer. Because the DRAM storage locations have a length of 32 bits or equivalently, four-bytes, the DRAM is shown divided into four-byte words across the horizontal border of the memory  
 35 buffer. Each byte lane includes 2048 four-byte words for a total of 8192 bytes. Since there are four TDM byte lanes, there are a total of 32768 bytes in the mapping buffer. Selected memory locations are numbered starting from zero and ending at 32767 to illustrate the number of memory positions.

		DRAM Byte Lane 0	DRAM Byte Lane 1	DRAM Byte Lane 2	DRAM Byte Lane 3
	{	0	1	2	3
	Channel 0 {	...	...	...	...
		252	253	254	255
5	{	256	257	258	259
	Channel 1 {	...	...	...	...
		508	509	510	511
	{	512	513	514	515
	Channel 2 {	...	...	...	...
10		764	765	766	767
	Channel 3 { through { Channel 28 {	...	...	...	...
	{	7424	7425	7426	7427
15	Channel 29 {	...	...	...	...
		7676	7677	7678	7679
	{	7680	7681	7682	7683
	Channel 30 {	...	...	...	...
		7932	7933	7934	7935
20	{	7936	7937	7938	7939
	Channel 31 {	...	...	...	...
		8188	8189	8190	8191

**TABLE 3**

TABLE 3 illustrates, from the DRAM perspective, that each TDM byte lane is divided into 32 channels, each containing 64 four-byte words. The channels are shown along the vertical border starting from channel zero and ending with channel 31. This section of the memory map corresponds to TDM byte lane 3 shown in TABLE 2. From the DRAM perspective, channels zero through 31 in byte lane three contain the low bytes of a sample having more than one byte.

30

		DRAM Byte Lane 0	DRAM Byte Lane 1	DRAM Byte Lane 2	DRAM Byte Lane 3
	{	0	1	2	3
	Section 0 {	...	...	...	...
		124	125	126	127
35	{	128	129	130	131
	Section 1 {	...	...	...	...
		252	253	254	255

**TABLE 4**

TABLE 4 illustrates the DRAM perspective of each channel of data. The 64 four-byte words of a single channel are divided into two sections containing 32 four-byte words each.

Specifically, channel 0 of TDM byte lane 3 is shown separated into two sections: Section 0 and

5 Section 1. Each channel of data is separated into two sections in the mapping buffer to allow for simultaneous writing of data to one section and reading of data from the other section.

		TDM Byte Lane 0	TDM Byte Lane 1	TDM Byte Lane 2	TDM Byte Lane 3
	{	0	1	2	3
10	Channel 0 {	...	...	...	...
		1020	1021	1022	1023
	{	1024	1025	1026	1027
	Channel 1 {	...	...	...	...
		2044	2045	2046	2047
15	{	2048	2049	2050	2051
	Channel 2 {	...	...	...	...
		3068	3069	3070	3071
20	Channel 3 {	...	...	...	...
	through {				
	Channel 28				
	{	29696	29697	29698	29699
	Channel 29 {	...	...	...	...
		30716	30717	30718	30719
	{	30720	30721	30722	30723
25	Channel 30 {	...	...	...	...
		31740	31741	31742	31743
	{	31744	31745	31746	31747
	Channel 31 {	...	...	...	...
30		32764	32765	32766	32767

**TABLE 5**

TABLE 5 illustrates the TDM perspective of the mapping buffer. From this perspective, the TDM byte lanes are shown across the horizontal axis and the channels of data are shown down the vertical axis. The channels of data are coupled through data lines 122 to the transceiver chips in the bus driver 112. From the TDM perspective, the samples of data are remapped. This remapping is illustrated by observing that each channel includes four-bytes from each of the TDM byte lanes 0-3. For example, the first row of channel 0 has, starting from the left and moving horizontally, a byte from each byte lane. Each channel in the mapping buffer has 256 four-byte words for a total of 1024 bytes.

	TDM Byte Lane 0	TDM Byte Lane 1	TDM Byte Lane 2	TDM Byte Lane 3
{	0	1	2	3
Section 0 {	...	...	...	...
	508	509	510	511
	512	513	514	515
Section 1 {	...	...	...	...
	1020	1021	1022	1023

**TABLE 6**

Finally, TABLE 6 illustrates that each channel from the TDM perspective is subdivided into two 128 four-byte word sections. As described from the DRAM perspective, these two sections allow the mapping buffer to be accessed from the TDM bus 22 and the DRAM 116 simultaneously.

It is helpful to understand the data path from the storage device 110 to the TDM bus 22 by way of an example. To begin, the SCSI control and interface 118 reads or writes data in bunches from or to the DRAM 116. For example, to write data to the DRAM 116, the SCSI control and interface 118 writes several allocation units to the DRAM 116 very rapidly relative to transfers from the DRAM 116 to the SRAM 114. With each write of an allocation unit, the SCSI control and interface 118 in combination with address information separates the allocation unit into its TDM byte lane sections. For 24 bit samples, the DRAM 116 is divided using software into three TDM byte lanes. The SCSI controller, thus, separates the allocation unit data and places it in the appropriate TDM byte lanes in the DRAM 116. The samples still must be remapped so that each sample has a byte from each of the three byte lanes.

The DMA controls the reading and writing of data between the DRAM 116 and the DRAM port 132 of the dual ported SRAM 114. During a write to the SRAM 114, also called the mapping buffer, the samples are transferred from the DRAM 116 one TDM byte lane at a time. Before a channel can be read from the mapping buffer, the DMA must transfer bytes from each TDM byte lane starting with 3 and ending with 1 for a 24 bit sample. It should be noted that only one section of each channel will be filled. TABLES 2, 3, and 4 again illustrates the DRAM perspective. Section 0 of TABLE 4 will be filled with bytes from TDM byte lane 3. To fill one complete section of the mapping buffer for one channel, section 0 for TDM byte lanes 3 through 1 will be written to using the DMA. At the same time, section 1 will be read by the TDM bus 22.

Referring again to TABLE 6 to illustrate the TDM perspective, the TDM reads a previously filled section one. From the TDM perspective shown in TABLE 5, each sample is remapped such that the sample includes three bytes from each TDM byte lane for the 24 bit example. In this manner, the storage controller passes data from the storage device 110 to the

TDM bus 22. Data transfers from the TDM bus 22 to the storage device 110 occur similarly, but in reverse order.

In general, the TDM controller, DMA, and SCSI control and interface 118 function in conjunction with the CPU to control data flow through the storage controller board 20. During  
5 a transfer of data to storage, the TDM controller attempts to keep the SRAM full. When the SRAM is not full, a data request flag is produced. Conversely, during a transfer of data from storage to the TDM bus 22, the TDM controller attempts to keep the SRAM empty. When the SRAM is not empty, a data available flag is produced. The TDM controller provides an interrupt to the CPU 14 whenever data needs to be transferred in or out of SRAM. Similarly,  
10 an interrupt is produced when a boundary in the DRAM memory is crossed. The CPU receives these interrupts and provides the appropriate control to the TDM controller, DMA, and SCSI control and interface 118. The CPU 14 programs the TDM controller, DMA, and SCSI controller and interface 118, to set the boundaries in memory that trigger interrupts.

The data format, generally, has several advantages. Data of varying lengths such as  
15 audio samples having 8, 16, and 24 bits can be stored to minimize waste of memory space in the storage device 110 because data is subdivided into 8 byte sections. The storage controller board 20 may perform cut and paste editing because the format enables the storage controller to access sections of programs without accessing the entire program. This easy access to programs eliminates the need to involve the DSP for cut and paste editing functions. In general, the  
20 format enables the storage controller to access programs more quickly.

The detailed data path described should not be construed to limit the scope of the invention. The manner of separating the data into byte lanes may be altered without departing from the scope of the invention. As noted, the mapping and remapping may be carried out in a single memory device or using a combination of memory devices.

25 FIG. 4 illustrates a block diagram overview of the DSP board 18. The DSP board 18 includes a bus driver 150, control and handshake logic 152, an EISA bus interface 34, dual ported SRAM 154, and a plurality of DSP chips 156.

The bus driver 150 provides buffering and isolation for the TDM data and timing signals. Transceiver chips like those used in the bus drivers of the I/O and storage controller  
30 boards 16, 20 couple the data lines 158 from one port 160 of the dual ported SRAM to the TDM bus 22. Additionally, the bus driver 150 includes discrete buffers for coupling the TDMCK, TDMCH0, TDMRD, TDMWR, and TDMOK signals of the TDM bus 22 to the control and hand shake logic 152. Finally, the bus driver includes discrete buffers for coupling the frame sync (FS0-FS4) signals to the DSP chips 156.

35 The dual ported SRAM 154 acts as a memory buffer between the DSP chips 156 and the TDM bus 22. The TDM port 160 of the dual ported SRAM 154 is coupled through data lines 158 to the transceiver chips of the bus driver 150. The dual ported SRAM 154 is also coupled to the control and handshake logic 152 through address and control lines 162. The DSP

port 164 of the dual ported SRAM 154 is coupled to the DSP chips 156 through address, control, and data lines 166.

The control and handshake logic 152 controls transfers of data from the dual ported SRAM 154 to the TDM bus 22 and communicates with the EISA bus interface 34 through control lines 168. To control the transfers on the TDM bus 22, the control and handshake logic 152 is coupled to TDMCK, TDMCH0, TDMOK, TDMRD, and TDMWR through control lines 170 and buffers in the bus driver 150. The control and handshake logic 152 includes a modulo 128 counter coupled to TDMCK and TDMCH0 for keeping track of the active time slot on the bus. In a similar manner to the handshaking described for the I/O board 16, the control and hand shake logic 152 controls transfers to and from the TDM bus 22. The dual ported SRAM 154 produces data available and data request signals as data passes through the SRAM 154. Conceptually, the SRAM 154 performs the double buffering described previously to facilitate transfers to the TDM bus 22. To provide control of transfers to and from the DSP board 18, the control and handshake logic 156 is coupled to the EISA bus interface through control lines 168.

The DSP board 18 includes a plurality of digital signal processing ("DSP") chips 156. Each DSP board 18 may include up to any number of DSP chips limited by physical board space and addressing and speed requirements. Each of these DSP chips 156 is coupled to the DSP port 164 of the dual ported SRAM 154 through address and control lines. The DSP chips 156 are also coupled to frame sync signals (FS0-4) through isolation and driver circuitry on the bus driver and through control lines 172. The DSP uses the frame sync signals to time transfers of audio data to and from the DSP port 164 of the dual ported SRAM 154. Finally, the DSP chips are coupled to the EISA bus interface through control and data lines 174 for writing programs to the DSP chips, changing parameters such as gain values, and changing addressing information used in transfers between the SRAM 154 and the DSP chips 156.

The DSP chips have their own internal RAM and share a common clock independent from the bus clock, so the DSP chips may perform editing and processing quickly and independently from the TDM bus timing. The DSP chips 156 provide several functions such as gain change, dithering, equalization, summing, stretching, shrinking, and sample rate conversion. Such chips and their capabilities are well-known. For example, the DSP56K family of chips from Motorola may perform these functions.

In sum, the DSP board 18 processes digital audio data transferred to it from other boards. The DSP board 18 communicates with other boards using a similar double buffering scheme as described for the I/O board 16. It should be understood that transfers, while functionally the same, are implemented differently depending on the particular hardware. The DSP board 18 could be implemented in various ways as long as it appropriately communicates with the TDM bus 22.

To describe the operation of the TDM bus 22, FIG. 5 illustrates the waveforms of the TDM bus signals shown relative to the TDM time slots 180. Time slots 126, 127, 0, and 1 provide a representative illustration of the TDM bus operation. The frame sync and master clock signals are shown separate from the other bus signals because it is necessary to truncate both the master clock and frame sync signals to fully illustrate them.

TDMCK 186 is the TDM bus clock and is driven onto the bus by a bus master. An I/O board 16 may serve as a bus master, but only one I/O board 16 may be the bus master at one time. Each cycle of the bus clock defines a time slot. A time slot is divided into two phases: phase 1 begins at the low to high transition, and phase 2 begins at the high to low transition of the bus clock. During data transfer on the TDM bus 22, a 32 bit channel of data is present for one time slot. Each board includes a modulo 128 counter, acting as an address counter, to indicate which of the 128 times slots is active.

TDM31-TDM0 190 are the 32 TDM data lines. TDM31 is the most significant bit and TDM0 is the least significant bit. If an audio data sample has less than 32 bits, then the lower bits are unused on the TDM bus. A board acting as a bus writer begins to drive the data lines for an active channel at the end of phase 1. Conversely, a corresponding bus reader latches this data at the end of phase 2. All data lines switch to a high impedance state 192 in the tri-state outputs of the bus driver throughout phase 1 to prevent contention during the setup time between time slots. During a transfer of data, several boards may act as bus reader, but only one board may be a bus writer.

TDMCH0 194 identifies time slot zero and synchronizes each address counter of the I/O, DSP, and storage controller boards 16, 18, 20. The clock oscillator 60 of the bus master drives TDMCH0 low (196) during time slot 127 so that all address counters 104 may be reset to zero on the next rising clock edge.

TDMRD, TDMWR, and TDMOK each have similar timing characteristics and are shown together in waveforms 198.

TDMRD is a read request generated by a bus reader when the reader's data request flag is set and a selected time slot becomes active. The reader drives TDMRD low during phase one of the selected time slot to signify that it is ready to receive data. At the end of phase 2, the bus reader switches the tri-state output coupled to TDMRD to a high impedance state.

TDMWR is a write request generated by a bus writer when the writer's data available flag is set and a selected time slot becomes active. The bus writer drives TDMWR low during phase 1 of the time slot to signify that the writer is ready to send data. Like the bus reader, the bus writer switches the tri state output coupled to TDMWR to high impedance state at the end of phase 2.

TDMOK identifies an enabled channel. The bus master drives TDMOK low for the duration of an enabled time slot. Each reader or writer of a particular time slot monitors the TDMOK line to determine whether a transfer is allowed during the time slot. By loading a

synchronizing map on the bus master with the appropriate values for TDMOK, the system may simultaneously start and stop data transfers on multiple time slots. A data transfer can take place during a time slot if and only if TDMOK, TDMRD, and TDMWR are all active through phase 2 of the current time slot.

5           FIG. 6 illustrates the waveforms of the frame sync, FS0-FS4 200, and master clock, MCK0-MCK4 202, shown relative to master clock cycles 204. The frame sync and master clock signals 200, 202 are not dependent upon the bus clock signal, so they are shown separately in FIG. 6 relative to master clock cycles 204. FIG. 6 also illustrates the transfer of both the left and right channels of audio data in a stereophonic signal, when frame sync 200 is high, the  
10   receiver 40 transfers the left channel. When frame sync is low, the receiver 40 transfers the right channel. This transfer of left and right channels is a characteristic of the particular receiver chip used in the implementation and is not critical to the operation of the invention.

FS0-FS4 184 are the frame sync lines 0 through 4. Frame sync is used to synchronize data transfers on the TDM bus to a particular sample rate. The rising edge of a frame sync is  
15   used to create data available and request flags that enable writers and readers to transfer data during the next available time slot. Frame sync is also used to swap the synchronizing maps 100. For example, to start or stop a number of channels each tied to a particular frame sync, the frame sync is used to synchronize the swap.

FS0 through FS4 support five simultaneous sample rates at any frequency up to 65  
20   KHz. Devices on the bus can synchronize their transfers to any one of the five, or carry out unsynchronized transfers at rates up to 65 KHz. Any device may drive one or more frame sync lines, however, there can be no more than one device driving any particular frame sync line.

MCK0-MCK4 184 are master clock lines 0 through 4. Paired with FS0-FS4, these lines run at 128 times the associated sample rate. These signals can be used by devices such as  
25   AES/EBU transmitters and receivers to operate their internal state machines. If a device drives frame sync, it must also correctly drive the associated master clock line.

Parameter	Description	Min	Typ	Max	Units
t0	TDMCK L to TDMCK H			15	nsec
t1	TDMCK H to TDMCK L			15	nsec
t2	TDMCK H to TDMD31 - TDMD0 inactive			30	nsec
t3	TDMCK L to TDMD31 - TDMD0 valid			30	nsec
t4	TDMCK H to /TDMCH0 active (channel 127)		15	60	nsec
t5	TDMCK L to /TDMCH0 inactive (channel 0)		15	60	nsec
t6	TDMCK H to /TDMRD valid			30	nsec
	TDMCK H to TDMWR valid				
	TDMCK H to /TDMOK valid		15	30	nsec

Bus Clock Timing Characteristics

t7	MCK0-MCK4 L to MCK0-MCK4 H		15	30	nsec
t8	MCK0-MCK4 H to MCK0-MCK4L		15	30	nsec
t9	MCKn H to FSn H (start left channel)		15		nsec
t10	MCKn H to FSn L (start right channel)		15		nsec

Frame Sync Timing Characteristics

**TABLE 7**

The timing parameters for each wave form of FIG. 5 are listed in TABLE 7. Each of the waveforms have timing parameters such as t0 and t1 showing the transition times of the bus clock. Timing parameters t0-t6 are synchronous with TDMCK while timing parameters t7-t10 are not synchronous with TDMCK because t7-t10 are derived from actual digital audio sample rates. No assumptions should be made regarding the timing relationships between MCK0-4 or FSO-4 and TDMCK because frame syncs need not be synchronized to the TDM bus clock.

1	GND	51	TDMD24
3	TDMD0	53	TDMD25
5	TDMD1	55	TDMD26
7	TDMD2	57	TDMD27
9	TDMD3	59	TDMD28
11	TDMD4	61	TDMD29
13	TDMD5	63	TDMD30
15	TDMD6	65	TDMD31
17	TDMD7	67	FS0
19	TDMD8	69	FS1
21	TDMD9	71	FS2
23	TDMD10	73	FS3
25	TDMD11	75	FS4
27	TDMD12	77	MCK0
29	TDMD13	79	MCK1
31	TDMD14	81	MCK2
33	TDMD15	83	MCK3
35	TDMD16	85	MCK4
37	TDMD17	87	/TDMCH0
39	TDMD18	89	/TDMRD
41	TDMD19	91	/TDMWR
43	TDMD20	93	/TDMOK
45	TDMD21	95	TDMCK
47	TDMD22	97	Reserved 1
49	TDMD23	99	Reserved 2

**TABLE 8**

Table 8 illustrates the pin assignments of a specific implementation of the TDM bus.

TABLE 8 only shows the pin assignments for the odd-numbered pins; all other pins are ground pins.

To control various processing, storing, and transmitting functions, the CPU 14 may be programmed with software. The I/O, DSP, and storage controller boards 16, 18, 20 are readily controlled with the standard EISA bus interface devices 30, 32, 34. Operation of the EISA bus interfaces is well known to those skilled in the art. Various software programs may provide the control of each of the boards in the system 10 to perform the various data transfer, storage, and processing functions described in detail herein.

Programmed with software, the CPU may control the simultaneous transfer of several digital audio signals on the TDM bus 22. Because there are 128 time slots, each operating at an effective rate of about 65 kHz, up to 128 digital signals also known as channels may be transferred among devices simultaneously. The TDM bus 22 also has five sync lines, not necessarily tied to the bus clock, that can provide frame synchronization for up to five different sample rates. Transfers need not be synchronized to the bus clock or one of five frame sync signals on the TDM bus 22.

Though the digital audio system 10 is described in detail, the invention should not be limited to the particular embodiment described. It is not critical that the expansion boards be implemented as described. For example, some of the boards may be combined into a single board and, alternatively, may be interfaced to a personal computer or a CPU through various standard or proprietary bus means. Various functions performed with software using a programmed CPU and interface circuitry may be implemented with hardware alone. The uniquely programmed FPGA chips may be programmed alternatively, used in combination with discrete logic devices, or completely substituted with discrete logic or an ASIC. The bus interface scheme, and specifically the double buffering circuitry, may be implemented various ways. In short, the invention is not limited to the specific implementation described.

Having illustrated and described the principles of the invention in a preferred embodiment, it should be apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and equivalents coming within the spirit and scope of the following claims.

CLAIMS

1. A digital audio system comprising:  
a programmed central processing unit;  
an input/output portion for receiving and transmitting digital audio data;  
5 a storage device;  
an expansion bus for coupling the input/output portion and the storage device to the programmed central processing unit;  
a TDM bus, coupling the input/output portion to the storage device, for simultaneously transferring a plurality of digital audio signals between the storage device and  
10 the input/output portion.
2. The system of claim 1 wherein the storage device includes:  
a mapping buffer to separate n-bit samples of a digital audio signal into at least first and second subunits having k bits where k is less than n;  
and a mass storage device for storing the first subunits contiguously and the second  
15 subunits contiguously.
3. The system of claim 1 further comprising  
a digital signal processing portion coupled to the expansion bus for coupling the digital sound processing portion to the programmed central processing unit;  
the digital signal processing portion being coupled to the TDM bus for  
20 simultaneously transferring a plurality of digital audio signals among the storage device, the input/output portion, and the digital sound processing portion.
4. The system of claim 1 wherein the TDM multiplexing bus is coupled to a bus master for transferring at least two digital audio signals at differing sampling rates simultaneously.
- 25 5. A computer controlled digital audio system comprising:  
an input/output device;  
a digital processing device;  
a TDM bus coupled to the input/output device and the digital processing device for simultaneously transferring a plurality of digital audio signals between the digital processing  
30 device and the input/output device.
6. The system of claim 5 wherein the digital processing device includes a digital signal processing board;  
the TDM bus being coupled to the digital signal processing board for simultaneously transferring a plurality of digital audio signals between the digital signal processing board and  
35 the input/output device.
7. The system of claim 5 wherein the digital processing device includes a storage device;

the TDM bus being coupled to the storage device for simultaneously transferring a plurality of digital audio signals between the storage device and the input/output device.

8. The system of claim 5 wherein the digital processing device includes an additional input/output device;

5 the TDM bus being coupled to the additional input/output device for simultaneously transferring a plurality of digital audio signals between the input/output device and the additional input/output device.

9. The system of claim 5 wherein the input/output device includes a receiver and a transmitter;

10 the input/output device being coupled to the TDM bus for simultaneously transferring at least one digital audio signal from the receiver to the transmitter.

10. The system of claim 5 wherein the digital processing device includes a digital signal processing board and a storage device;

15 the TDM bus being coupled to the digital signal processing board and the storage device for simultaneously transferring a plurality of digital audio signals among the digital signal processing board, the storage device, and the input/output device.

11. The system of claim 4 wherein the TDM multiplexing bus is coupled to a bus master for transferring at least two digital audio signals at differing sampling rates simultaneously.

20 12. The system of claim 4 wherein the digital processing device is a storage device including:

a mapping buffer to separate  $n$ -bit samples of a digital audio signal into first and second subunits having  $k$  bits where  $k$  is less than  $n$ ;

25 and a mass storage device for storing the first subunits contiguously and the second subunits contiguously.

13. A method for providing simultaneous control of a plurality of digital audio signals in a computer system comprising:

receiving or transmitting a digital audio signal through at least one input/output device; and

30 simultaneously transferring on a TDM bus a plurality of digital audio signals between at least one input/output device and a digital processing device.

14. The method of claim 13 further including simultaneously transferring on the TDM bus at least one digital audio signal having a different sample rate than a second digital audio signal.

15. The method of claim 13 further including:  
transferring on the TDM bus a digital audio signal to a storage device;  
separating n-bit samples of the digital audio signal into at least first and second  
subunits having k bits, where k is less than n; and  
5 storing the first subunits contiguously and the second subunits contiguously on the  
storage device.
16. A digital audio system, comprising:  
an input/output portion for receiving and transmitting digital audio data;  
a digital data storage portion;  
10 a digital signal processing portion for processing the digital audio data; and  
a time division multiplexed bus for simultaneously transferring digital audio data  
through multiple time slots among the input/output portion, the digital data storage portion  
and the digital signal processing portion.
17. A method of playing back and recording multiple digital audio data signals  
15 simultaneously in a digital audio system, comprising:  
receiving one or more digital audio data input signals simultaneously;  
time division multiplexing the input signals for recording on a digital data storage  
device;  
playing back one or more digital audio data outputs signals simultaneously from the  
20 digital data storage device; and  
time division multiplexing the output signals simultaneously with the input signals.
18. A method of storing digital audio data samples on a storage device,  
comprising:  
separating n-bit samples of the digital audio signal into at least first and second  
25 subunits having k bits, where k is less than n; and  
storing the first subunits contiguously and the second subunits contiguously on the  
storage device.

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FIG. 1

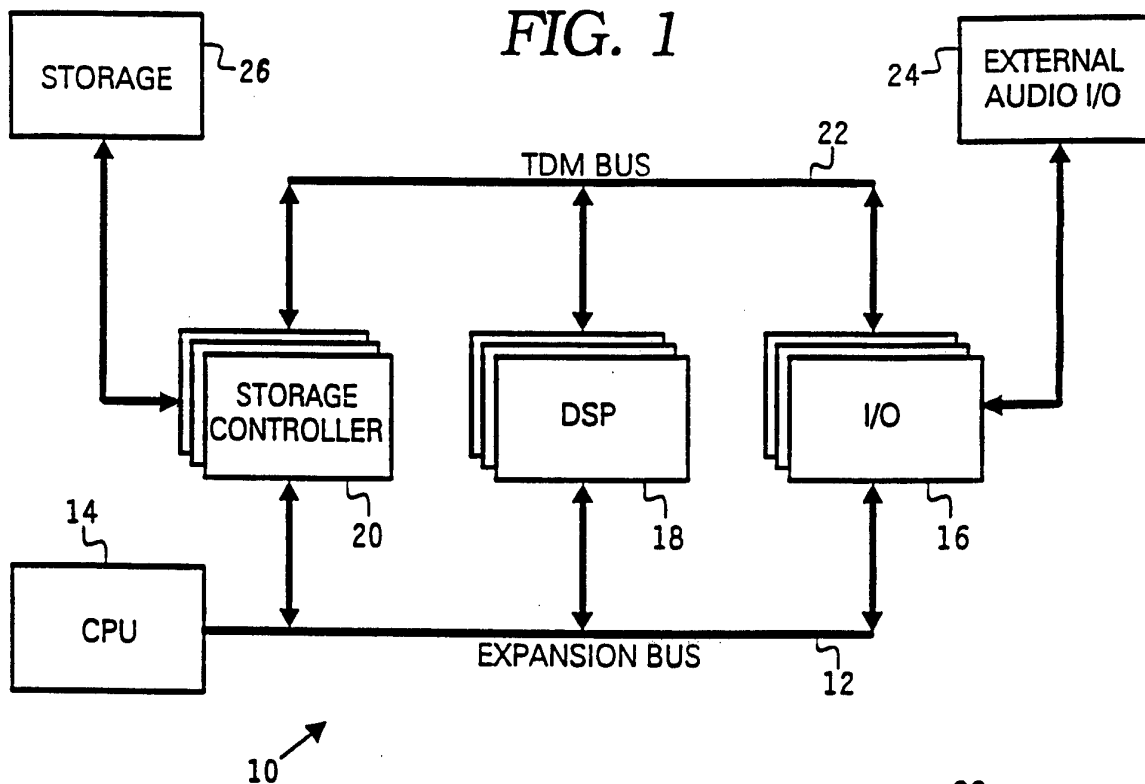
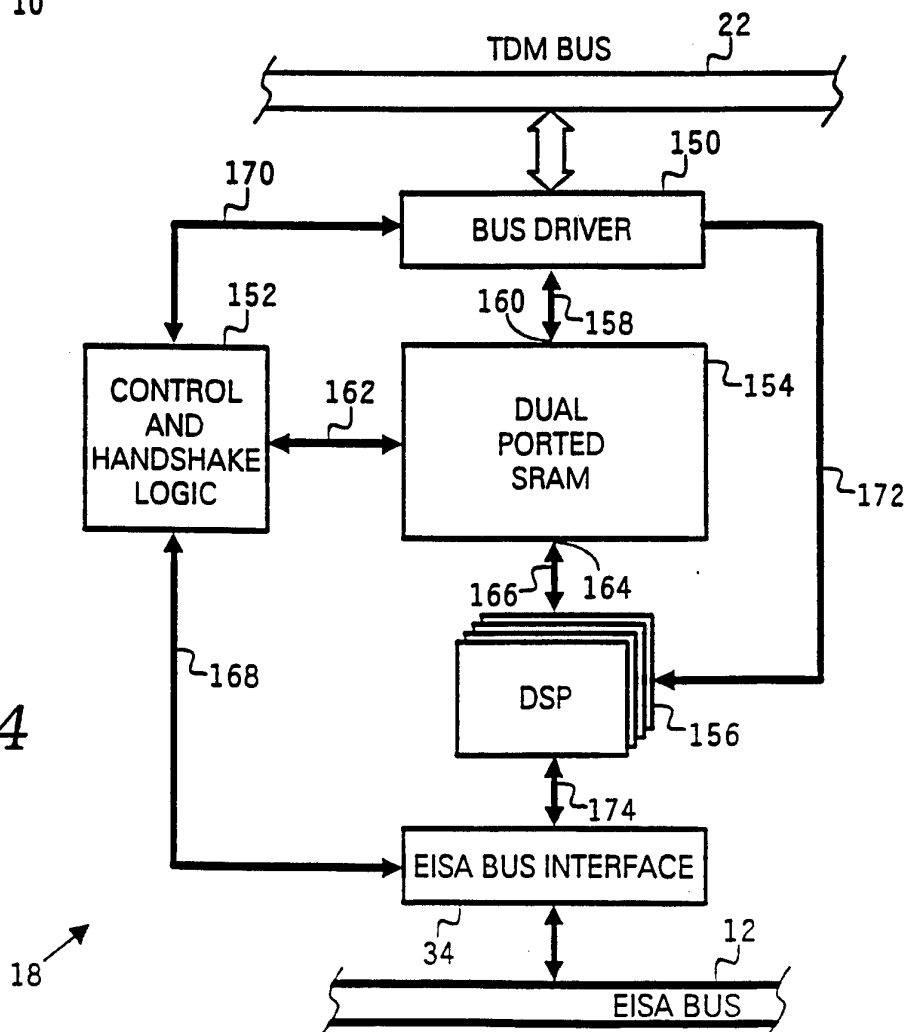
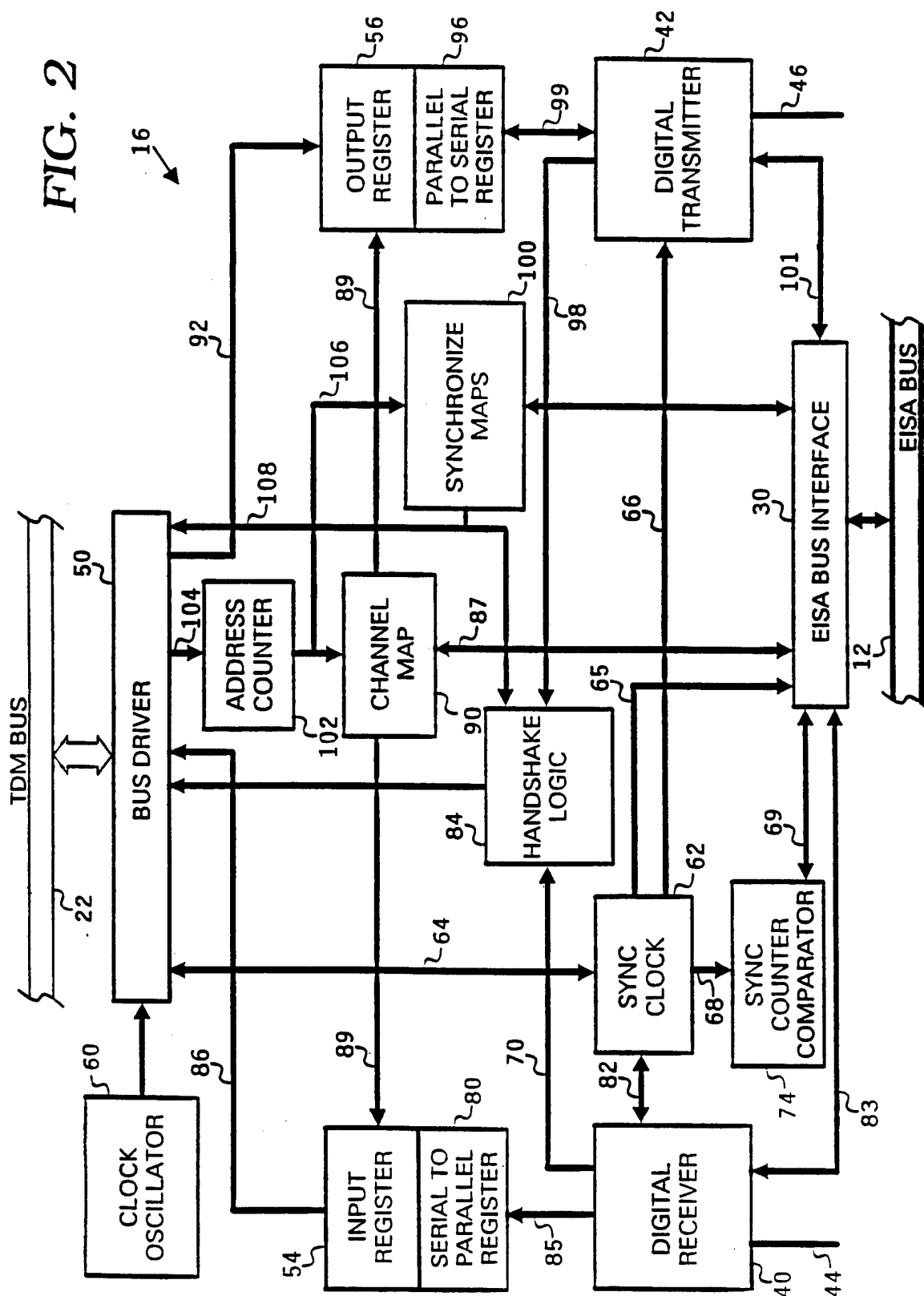


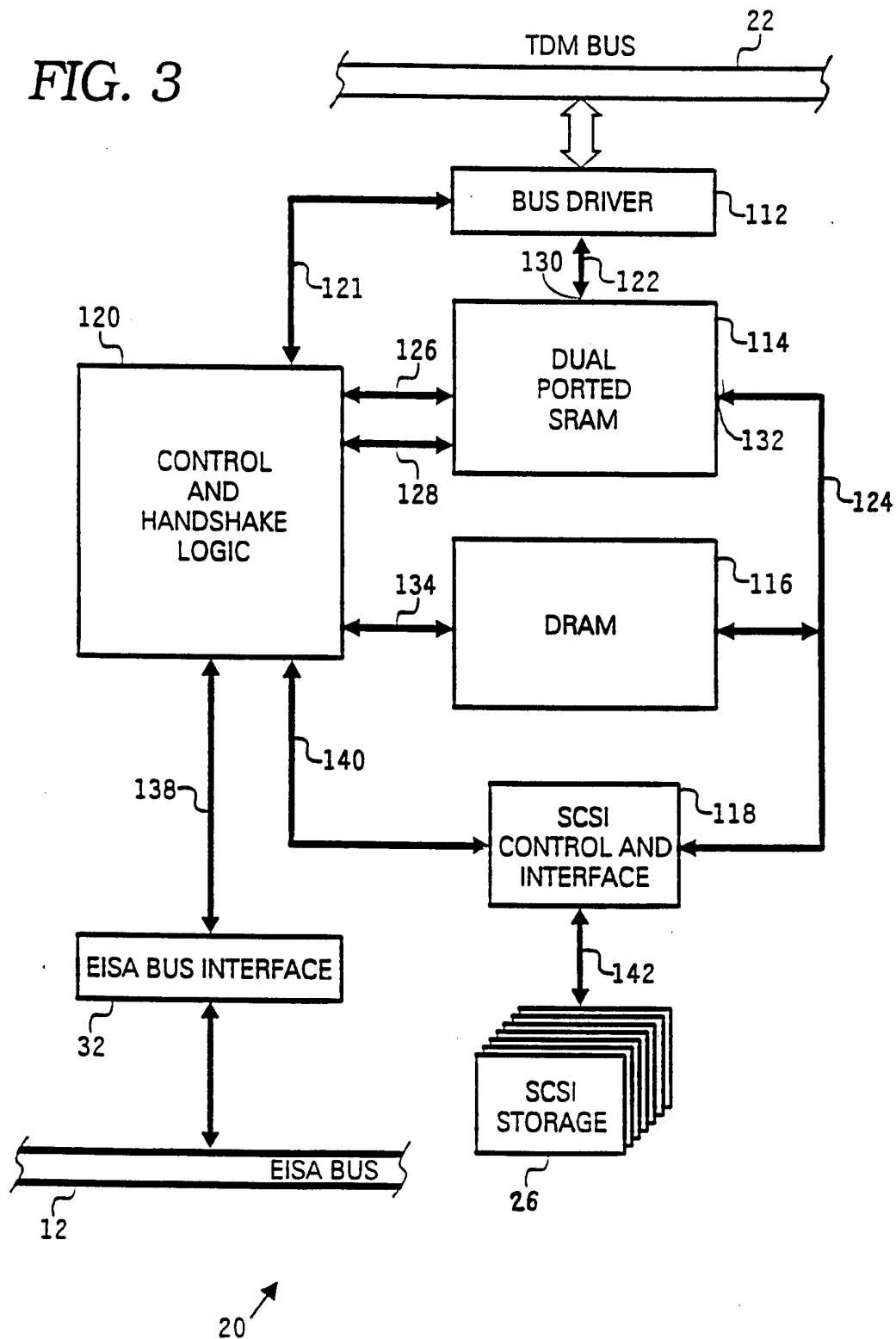
FIG. 4



**FIG. 2**



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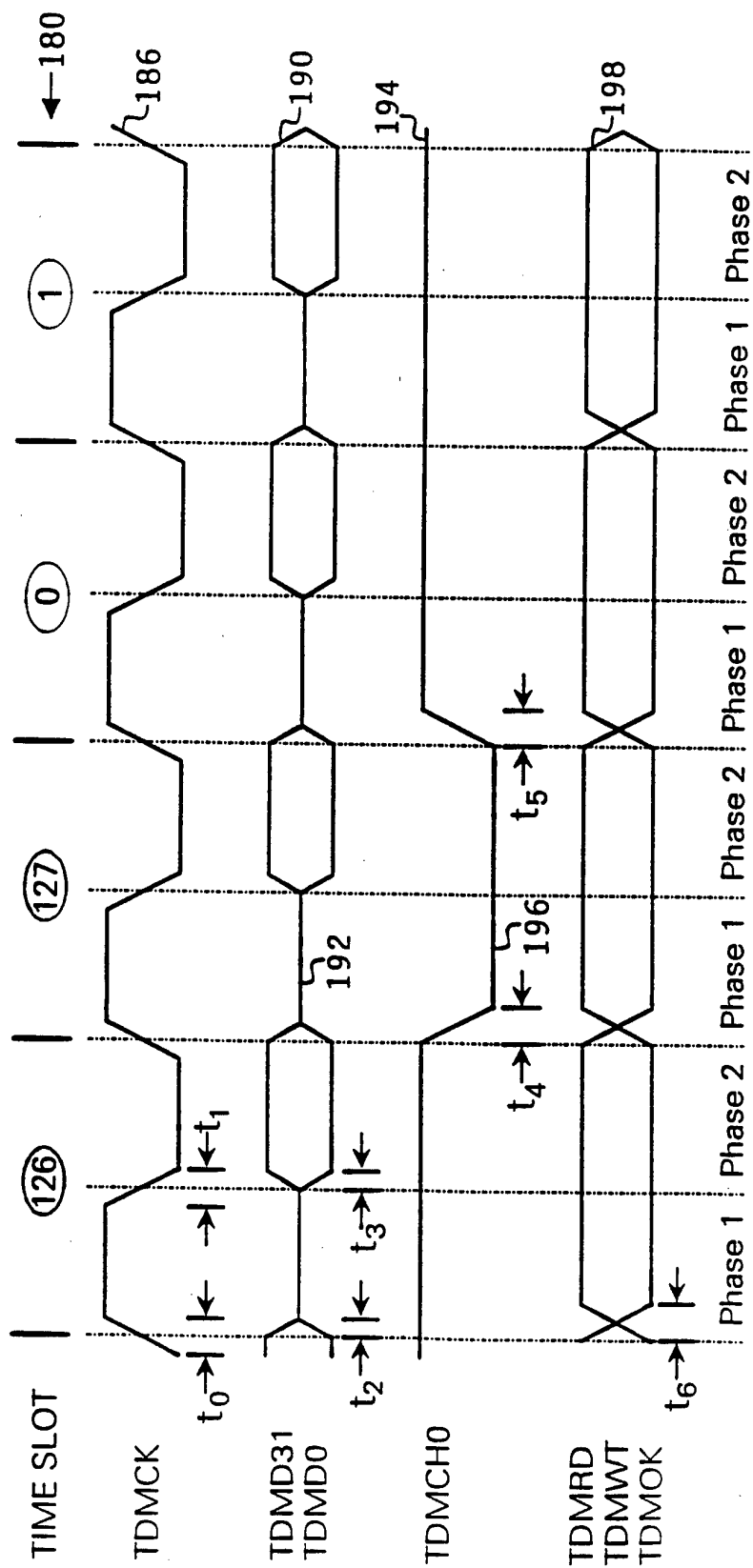


FIG. 5

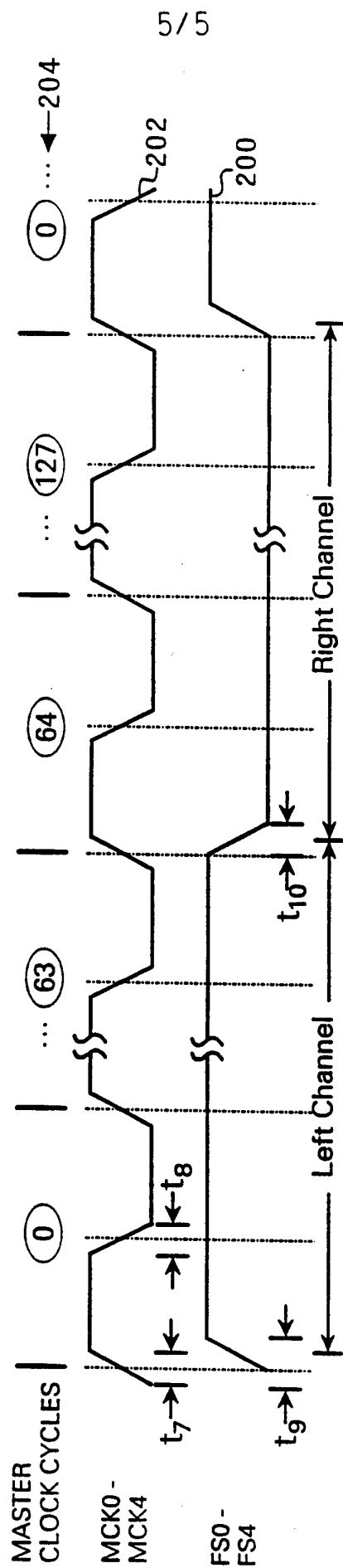


FIG. 6

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US94/04146

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) : G06F 13/00, 13/14, 15/00, 15/16

US CL : 395/800, 275, 200; 370/ 58.1, 77, 85.1; 381/31, 81

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/800,275,200;370/29, 32, 58.1,58.2, 77,85.1,95.3;381/31,81

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,218,710 (Yamaki et al.) 08 June 1993 see abstract and column 3, line 50 to column 6, line 25.	1-18
Y	US, A, 4,811,332 (Carse) 03 March 1989 see column 2, line 55 to column 3, line 41.	1-18
A,P	US, A, 5,212,688 (Gerbehy et al.) 18 May 1993 see column 1, line 45 to column 2, line 35.	1-18
A	US, A, 4,554,658 (Marten et al.) 19 November 1985 see column 2, lines 20-60.	1-18
A,P	US, A, 5,229,989 (Maher et al.) 20 July 1993 see column 3, line 40 to column 4, line 2.	1-18

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be part of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

25 MAY 1994

Date of mailing of the international search report

JUL 12 1994

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## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US94/04146

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,630,263 (Townsend et al.) 16 December 1986 see column 1, lines 25-60.	1-18

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US94/04146

## B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

APS

search terms: audio data, audio signals, DSP, digital signal processing, TDM, time-division, simultaneously or concurrently or parallel.