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Husbands et al.

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[45] **May 8, 1973**

[54] **ELECTRICAL TIMING DEVICE**

[75] Inventors: **Keith Ronald Frederick Husbands**, Sandiacre; **John Dawson**, Kirby-in-Ashfield, both of England

[73] Assignee: **Plessey Handel Und Investments A.G.**

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[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** .....**307/304,** 307/202, 307/293, 307/296, 317/36 TD, 321/45 S, 328/129

[51] **Int. Cl.**.....**H03k 5/153**

[58] **Field of Search**.....307/202, 246, 293, 307/296, 297, 304; 317/36 TD; 320/1; 321/45 S; 328/129, 259

[56] **References Cited**

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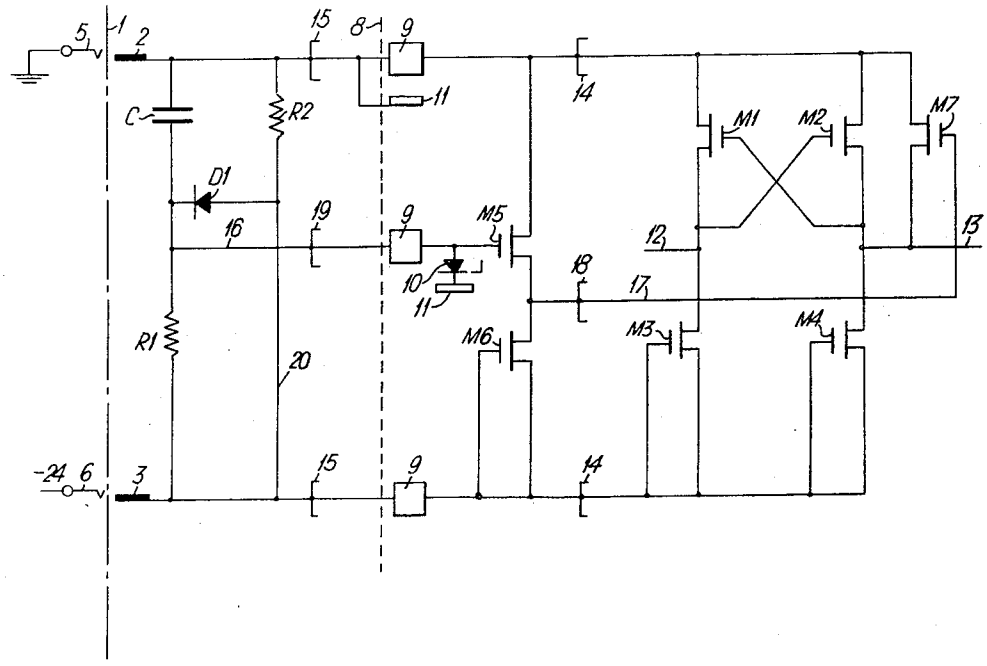
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Primary Examiner—Stanley D. Miller, Jr.
Assistant Examiner—R. C. Woodbridge
Attorney—Alex Friedman et al.

[57] **ABSTRACT**

An electrical timing device comprising a capacitor, a timing resistor and a discharge circuit for the capacitor which is maintained ineffective as long as power supply is not interrupted. In a preferred application, the interval timed exceeds the change-over time of a bistable register, a priming signal applied to bias the register into a preferred state being terminated on the expiry of the interval.

3 Claims, 5 Drawing Figures



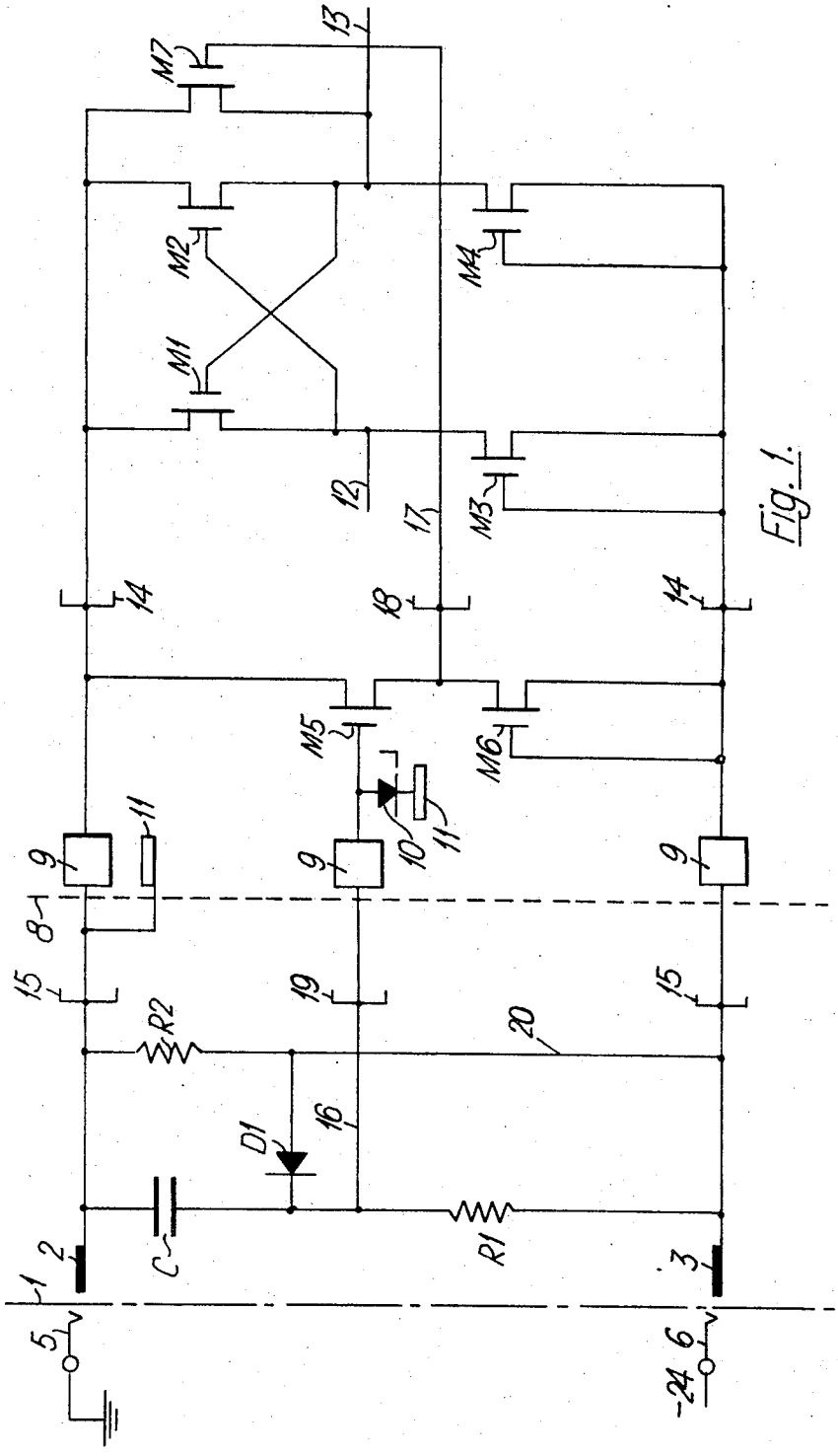

M7
13
M2
M4
M1
M3
12
17
14
18
14
M5
M6
11
10
11
9
9
9
8
15
19
15
R2
20
D1
16
C
R1
2
1
3
5
6
-24

Fig. 1.

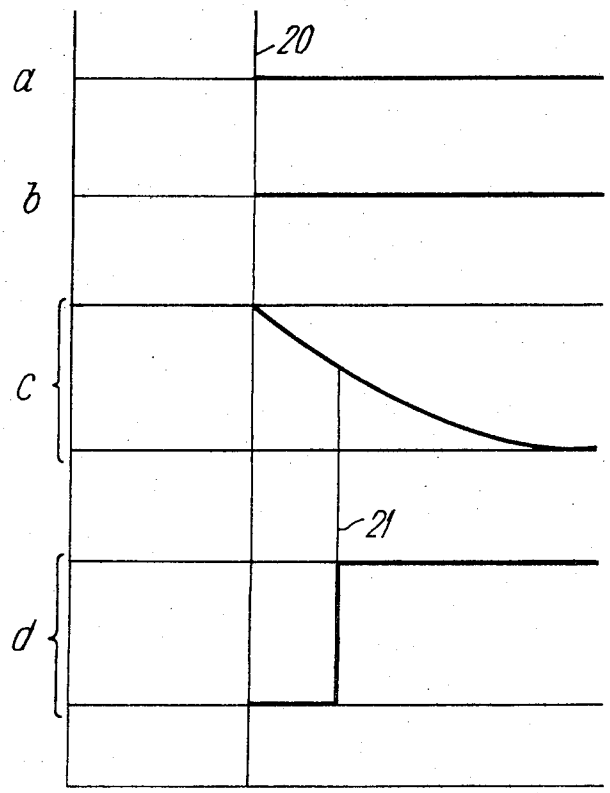


Fig. 2.

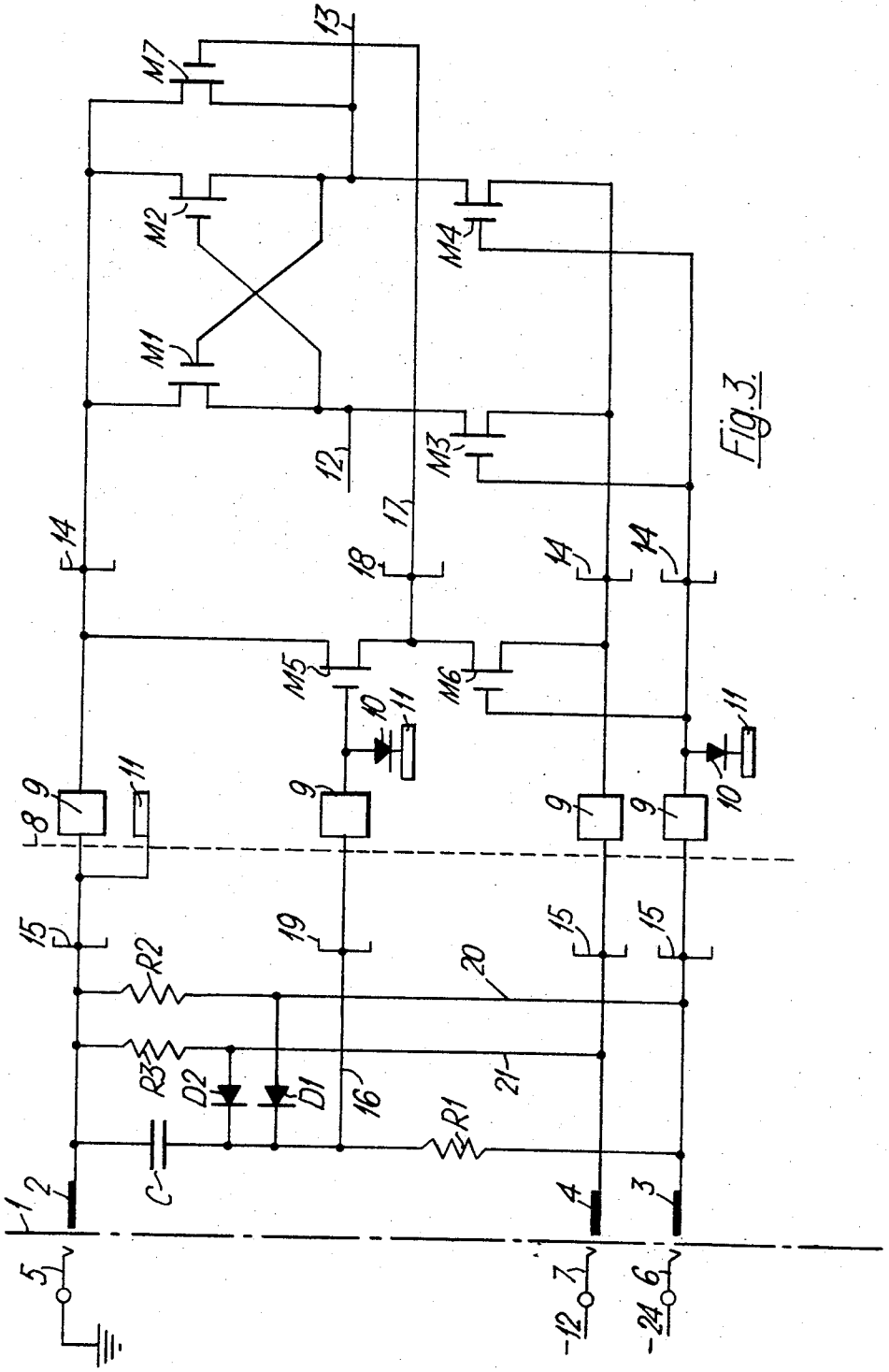

M7
13
M2
M4
M1
M3
12
17
14
18
M5
M6
10
11
9
8
15
19
20
R2
R3
D2
D1
16
21
R1
C
1
2
4
3
5
7
6
-12
-24

Fig. 3.

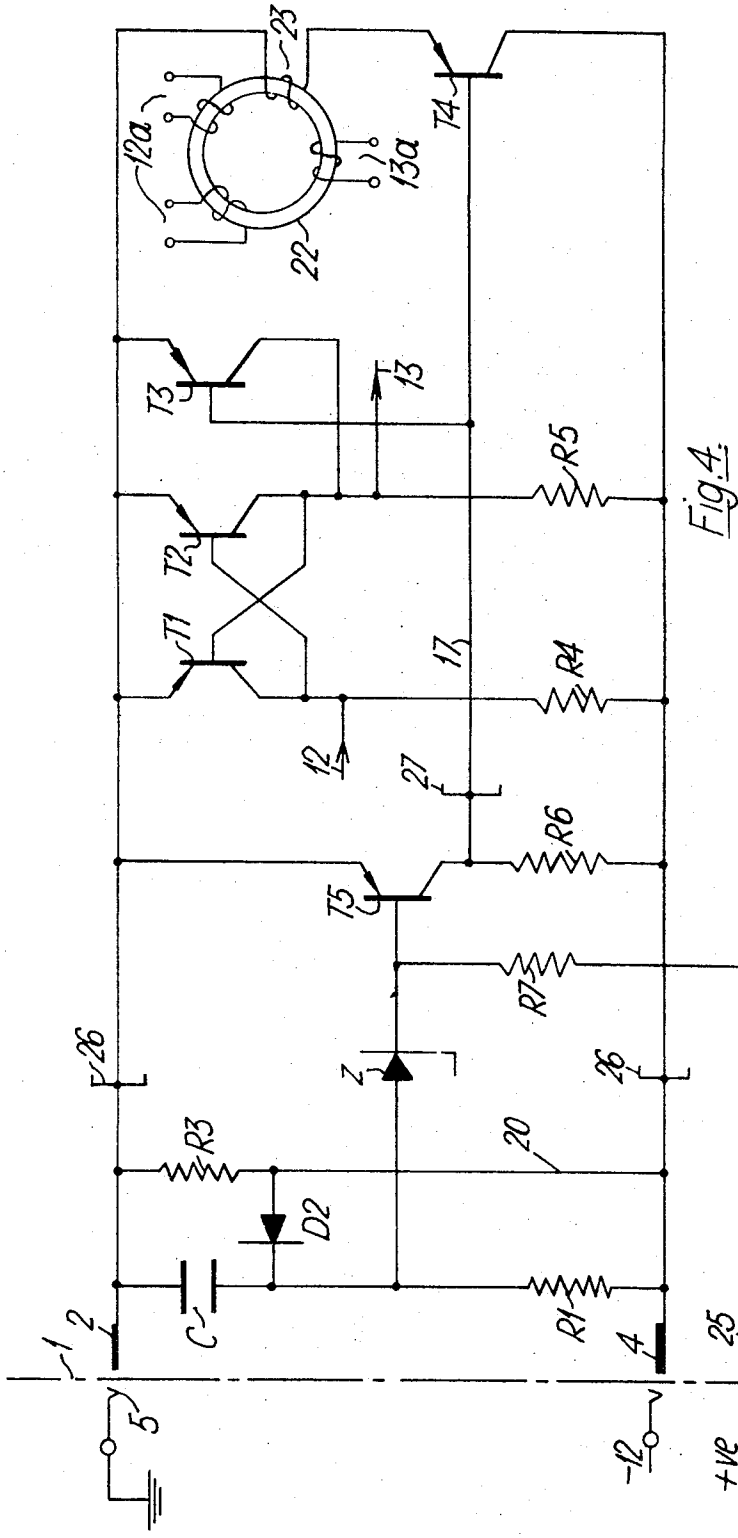

23
12a
13a
T4
22
T3
13
R5
T2
T1
17
R4
12
27
R6
T5
R7
Z
26
26
R3
20
D2
C
R1
1
2
4
25
5
-12
+Ve
24

Fig. 4.

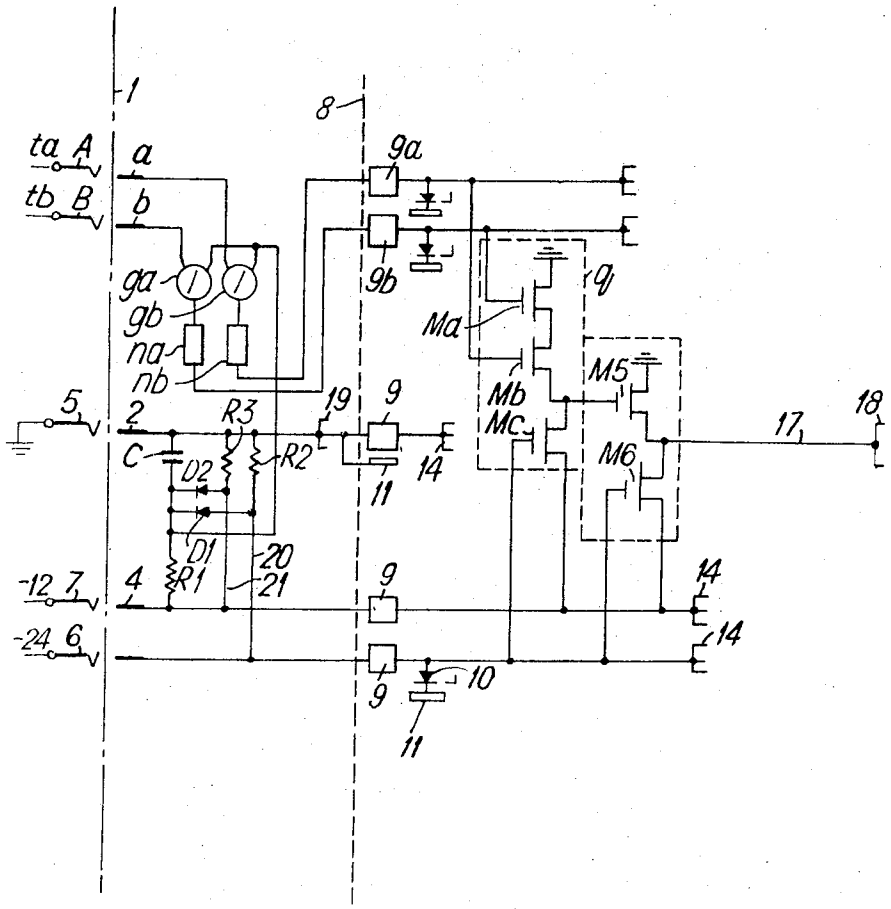

1
8
ta A
a
9a
tb B
b
9b
ga
gb
na
nb
q
Ma
Mb
Mc
M5
M6
5
2
C
R3
R2
19
9
14
11
17
18
D2
D1
R1
20
21
-12 7
4
-24 6
10

Fig.5

ELECTRICAL TIMING DEVICE

This invention relates to electrical timing devices.

According to the invention there is provided an electrical timing device, responsive to the application of power to measure an interval of time starting at the moment of application, which includes a charging circuit comprising a timing capacitor and a timing resistor connected in series with each other, a discharge circuit by which the capacitor may be discharged, and restraining means for maintaining the discharge circuit in an ineffective state while power is applied to the device. The timing device is utilized in conjunction with an electrical plug-in circuit card carrying a circuit having at least one circuit element capable of assuming more than one state, which element must occupy a preferred one of said states before the circuit can be used. Priming bias circuit means delivers a signal responsive to said applied power to one of said elements to bias said one element to a preferred state, the delivery of said signal being terminated in response to a switching device in turn responsive to a switching signal produced by said timing device. Said switching signal is produced at a time interval exceeding the time required for said one element to change from one to another of said alternative states.

The invention will now be described in connection with its application to an electrical plug-in circuit card, and with reference to the accompanying drawings in which:

FIG. 1 shows a first electrical plug-in circuit card carrying a timing device according to the invention,

FIG. 2 is a time chart used in explaining FIG. 1,

FIG. 3 shows a second electrical plug-in circuit card carrying a modification to the timing device shown in FIG. 1,

FIG. 4 shows a third electrical plug-in circuit card carrying a timing device according to the invention, and

FIG. 5 shows a fourth electrical plug-in circuit card carrying the timing device shown in FIG. 3.

In FIG. 1, the part of the drawing to the right of the chain line 1 represents an electrical plug-in circuit card. The card has terminals 2, 3, which form part of one half of a multiple plug-and-socket connector. The other half of the connector is fixed to a rack and offers further terminals 5, 6 which cooperate respectively with the terminals 2, 3, making physical and electrical contact therewith when the card is plugged in at a service position in the rack. In FIG. 1 only two terminals in each half of the multiple connector are shown, but it is to be understood that other terminals may be provided and used as required by the circuit carried on the card. Terminal 5 is connected to a source of reference potential, conveniently earth; and terminal 6 is connected to a source of power potential, conveniently −24 volts.

The card carries an integrated circuit chip, the relevant parts of which are shown to the right of the broken line 8. Electrical connection to the chip is established by means of pads 9, catching diodes 10 being provided where necessary and connected to the chip substrate 11, the substrate 11 being connected to terminal 2.

The integrated circuit includes a bistable device comprising two Mosts M1, M2 having their sources commoned, and their gates and drains cross-connected. The commoned sources of Mosts, M1, M2 are

connectable over terminals 2, 5 to the source of earth potential. The drains of Mosts M1, M2 are connected respectively to the sources of two further Mosts M3, M4 which serve passively as loads. The drains of Mosts M3, M4 are connectable by terminals 3, 6 to the source of power potential. The gates of Mosts M3, M4 are also connectable by terminals 3, 6 to the source of power potential. The bistable device comprising the Mosts M1, M2 is responsive to input signals applied to the gate of Most M2 to deliver output signals from the drain of Most M2 as shown at 12, 13 respectively. Mosts M1, M2 define a bistable register capable of assuming two states. In normal operation, this device should occupy a preferred one of said states before the circuit can be used. Multiple points 14 are provided by which reference and power potentials may be distributed as required within the chip. Multiple points 15 are provided by which these potentials may be distributed to other chips carried by the card. When the card is plugged in at its service position on the rack, reference potential appears at terminal 2 and power potential appears at terminal 3. The bistable device M1, M2 assumes one of its two stable states arbitrarily. Let it be assumed that the Most M2 should be conducting before the integrated circuit can be brought into service. The requirement of placing the device in this preferred state is met in the manner now to be described.

A timing capacitor C is connected in series with a timing resistor R1 across the terminals 2, 3. At the junction of the capacitor and resistor, a lead 16 is provided by means of which the potential of the junction is applied to the gate of a switching Most M5. The source of Most M5 is connected to terminal 2. The drain of Most M5 is connected to the source of a load Most M6 whose gate and drain are connected to terminal 3. A priming bias conductor 17 is run from the drain of the switching Most M5 to the gate of a biasing Most M7, whose source and drain are connected respectively to the source and drain of the Most M2 of the bistable device M1, M2. A multiple point 18 allows for priming bias conductors being run in respect of other devices in the chip which have to occupy a preferred state of a number of alternative states before the integrated circuit in the chip can be brought into service. A multiple point 19 allows the potential of the lead 16 to be used in respect of other chips carried by the card.

As soon as the card is plugged in at its service position in the rack, reference potential (earth) appears at terminal 2 and power potential (−24 volts) appears at terminal 3. The lead 16 assumes earth potential, preventing the switching Most M5 from conducting. The load Mosts M3, M4, M6 all become conductive, causing negative potential to appear at the gates of Mosts, M1, M2, M7. The negative potential applied to the gate of Most M7 constitutes a priming bias signal which biases the bistable device M1, M2 into the state in which the Most M2 is conducting. While the capacitor C starts to charge through resistor R1, the biasing Most M7 conducts and resolves the competition between the Mosts M1, M2 in favour of the Most M2, earth potential being delivered to the gate of the Most M1. These events are illustrated in the time-voltage chart of FIG. 2 where the vertical line 20 represents the instant of plugging-in. The thin horizontal lines to the

left of the line **20** are trace lines for ease of reference. The thick lines to the right of the line **20** depict the events just described, and represent respectively:

a. the potential at terminal **2**,
b. the potential at terminal **3**,
c. the potential of lead **16**, and
d. the potential of the priming bias conductor **17**.

As the capacitor C continues to charge, the potential on lead **16** reaches a value which causes the switching Most **M5** to conduct. This stage is represented by the line **21** in FIG. **2**. When the Most **M5** conducts, the priming bias conductor **17** assumes earth potential. With its gate at earth potential, the biasing Most **M7** becomes ineffective; the bistable device **M1**, **M2** is left with the Most **M2** conducting and is free to respond to input signals **12**.

Once the switching Most **M5** has been operated, the charging process continues until the timing capacitor C is fully charged, as shown in FIG. **2***c*. The timing capacitor C remains fully charged while the card is in service. If now the card is withdrawn from service, for example by withdrawing the card from its service position or otherwise cutting off the power supply, the bistable device **M1**, **M2** is deprived of power. When power is restored, it is fortuitous which of its alternative states is assumed by the bistable device **M1**, **M2**. Since the timing capacitor C is fully charged, the switching Most **M5** is conductive and the delivery of the priming bias signal to the gate of Most **M7** is prevented. To overcome this difficulty, the timing capacitor C is provided with a discharge circuit which becomes effective when the supply of power is interrupted. The discharge circuit comprises a discharge resistor **R2** connected in series with a diode **D1** across the capacitor C, the resistor **R2** being connected to the terminal **2**. The diode **D1** is poled so as to pass discharge current flowing from the timing capacitor C. When power is interrupted, the capacitor C discharges through the diode **D1** and the discharge resistor **R2**. Hence, when power is resumed, a priming bias signal is developed on the priming bias conductor **17** as already described. It is, however, necessary to prevent the discharge circuit from operating while the card is in service, an event which could impair performance of circuits carried by the card. This unwanted discharge is prevented by a connection **20** run from the junction of the diode **D1** and discharge resistor **R2** to the terminal **3**. By the connection **20**, the junction is maintained at the potential of the terminal **3**. And as long as the junction is maintained at the potential of the terminal **3**, the timing capacitor C is unable to discharge.

The value of the discharge resistor **R2** is chosen so that the timing capacitor C will discharge completely during any foreseeable interruption to the power supply. Such interruptions may be due to any cause, including, in the case of plug-in circuit cards, contact-bounce immediately following the act of plugging the card in at a service position. Contact-bounce, however, may be catered for in another way, as will become apparent.

Considering now the charging of the timing capacitor C, it has already been explained that the operation of the switching Most **M5** is deferred for a time exceeding the change-over time of the bistable device **M1**, **M2**. Contact-bounce can be catered for by deferring the operation of the switching Most **M5** for a longer period. This longer period slightly exceeds the sum of the time required for the contacts to attain mechanical stability, and the change-over time of the bistable device **M1**, **M2**. The time required to attain mechanical stability can be calculated from the mechanical features of the contacts.

With integrated circuit chips it is known to employ two sources of negative potential in addition to a source of reference (earth) potential. The two sources are conveniently −12 volts and −24 volts. FIG. **3** shows a circuit card having a chip which employs two sources of negative potential. The second source, i.e., −12 volts is connectable to the card by terminals **4**, **7**, and to the chip by a further pad **9**. Components which have already been described in connection with FIG. **1** are given the same references in FIG. **3** and are not described again. To distribute the −12 volts supply, additional multiple points **14**, **15** are provided. When the card is plugged in, the bistable device **M1**, **M2** is set to its preferred state as already described in connection with FIGS. **1**, **2**. A second discharge circuit is provided comprising a discharge resistor **R3** connected in series with a diode **D2** across the capacitor C; and a connection **21** between the junction of the diode **D2** and the discharge resistor **R3** to the terminal **4**. The diode **D2** is poled so as to pass discharge current flowing from the capacitor C. The second discharge circuit ensures that the charging process can only take place if both the −12 volt and the −24 volt supplies are uninterrupted.

Where the circuit on the card employs discrete components, the arrangement shown in FIG. **4** is adopted. Here again the components mounted on the card appear to the right of the chain line **1**. Components that function as described in connection with FIGS. **1**, **2** bear the references accorded to them in FIG. **1**. The card shown in FIG. **4** shows two circuit elements which must occupy a preferred state before the circuit carried by the card is brought into service. The first circuit element is a flip-flop comprising two transistors **T1**, **T2** having their emitters connected to the terminal **2**, their bases and collectors cross connected and their collectors connected by individual resistors **R4**, **R5** to the terminal **4**. The first element responds to input signals delivered at **12** to deliver output signals at **13**. The second circuit element comprises a so-called square loop core **22** which can be magnetised in one or other sense by an input pulse applied to one or other of the input windings **12***a*. When the core **22** is read out, an output pulse is delivered at the output winding **13***a*.

To prime the flip-flop **T1**, **T2** to the preferred state, which will be assumed to be when the transistor **T2** is conducting, a biasing transistor **T3** has its emitter and collector connected respectively to the emitter and collector of the transistor **T2**, and its base connected to the priming bias conductor **17**. To prime the core **22** to the preferred sense, a bias winding **23**, wound in the sense of the appropriate input coil **12***a*, is connected across the terminals **2**, **4** in series with a biasing transistor **T4** whose base is connected to the priming bias conductor **17**. The priming bias conductor **17** is connected to the collector of a switching transistor **T5**, and, through a resistor **R6**, to the terminal **4**. The emitter of the switching transistor **T5** is connected to the terminal **2**. To achieve a positive switching action

by the switching transistor T5, the junction of the timing capacitor C and the timing resistor R1 is connected to a zener diode Z, the outlet of which is connected to the base of the transistor T5. The zener diode Z is biased from a source of positive potential by way of further terminals 24, 25 and a bias resistor R7. Multiple points 26 allow for the distribution of reference and power potential to other components carried by the card. Multiple points 27 allow for the priming bias signal to be applied to other circuit elements which have to be primed to a preferred state.

The circuit works in a manner similar to that already described. The biasing transistors T3, T4 are conductive while the priming bias conductor 17 is maintained at negative potential. Negative potential is maintained for a time sufficient for the first and second circuit elements T1, T2 and 22 respectively to assume their preferred states. Negative potential is terminated when the switching transistor T5 is switched into conduction. This switching occurs when the potential developed by the timing capacitor C and timing resistor R1 causes the zener diode Z to break down.

In FIGS. 1, 3, a pad 9 has been shown individual to the switching Most M5. The need for this pad can be avoided by using simultaneously two other pads which would not otherwise be used at the same time as each other. Suppose the pads 9*a*, 9*b* carry respectively two consecutive time pulses *ta*, *tb*, which are delivered at co-operating terminals A,*a*; B,*b*. These pads are not normally used simultaneously. Instead of being directly connected to the pads 9*a*, 9*b*, the terminals *a*, *b* are connected as inputs to the respective one of two OR gates *ga*, *gb*. The junction of the capacitor C and resistor R1 is connected as an input to both of the gates *ga*, *gb*. The outlets of the gates *ga*, *gb* are taken respectively to inverters *ma*, *mb* and thence to the pads 9*a*, 9*b*. The gates *ga*, *gb* and inverters *na*, *nb* are made of discrete components. Within the chip, the pads 9*a*, 9*b* are connected respectively to the gates of two Mosts M*a*, M*b*. The two Mosts are connected in series with each other and with a load Most M*c*, and form an AND gate *q*. The outlet of the gate *q* is connected to the gate of the switching Most M5. It will be seen that the application of the time pulses *ta*, *tb* is unaffected by this arrangement, and that the gate *q* does not respond to either time pulse alone. The action of plugging in causes negative potential to appear on the priming bias lead 17 as already described. After a suitable interval the junction of the capacitor C and resistor R1 attains, on account of the charging of the capacitor C, a value which switches both of the gates *ga*, *gb*, thereby opening the gate *q* and switching the Most M5. With the most M5 switched, earth potential is applied to the priming bias lead 17 as already explained.

What is claimed is.

1. In combination with an electrical plug-in circuit card carrying a circuit having at least one circuit element capable of assuming more than one state, which element must occupy a preferred one of said states before the circuit can be used, which card also carries a first terminal and a second terminal at which reference and power potentials respectively appear when the card is plugged-in at a working position, the improvement which comprises at least one priming bias means for applying a signal responsive to said power potential from said second terminal to at least one of said circuit elements to bias said one element to a preferred state; timing device means responsive to the appearance of said reference and power potentials at said first and second terminals respectively to time a time interval exceeding the time required for said one element to change from one to another of said alternative states, and to produce a switching signal on the expiration of said time interval; and switching device means connected between said priming bias means and said timing device means for terminating the delivery of said signal responsive to the power potential by said priming bias means in response to said switching signal from said timing device means.

2. The combination of claim 1, wherein said timing device means includes a timing capacitor, a timing resistor connected in series with said timing capacitor across said first and second terminals; a discharge circuit for said timing capacitor including a discharge resistor and a diode connected in series with said discharge resistor across said timing capacitor, said discharge resistor being connected to said first terminal and said diode being poled to pass discharge current from said timing capacitor; and restraining means interconnecting said second terminal and the junction of said diode and discharge resistor for preventing said discharge circuit from operating as long as the power potential appears at the second terminal.

3. The combination of claim 2, wherein said restraining means is a restraining conductor.

* * * * *