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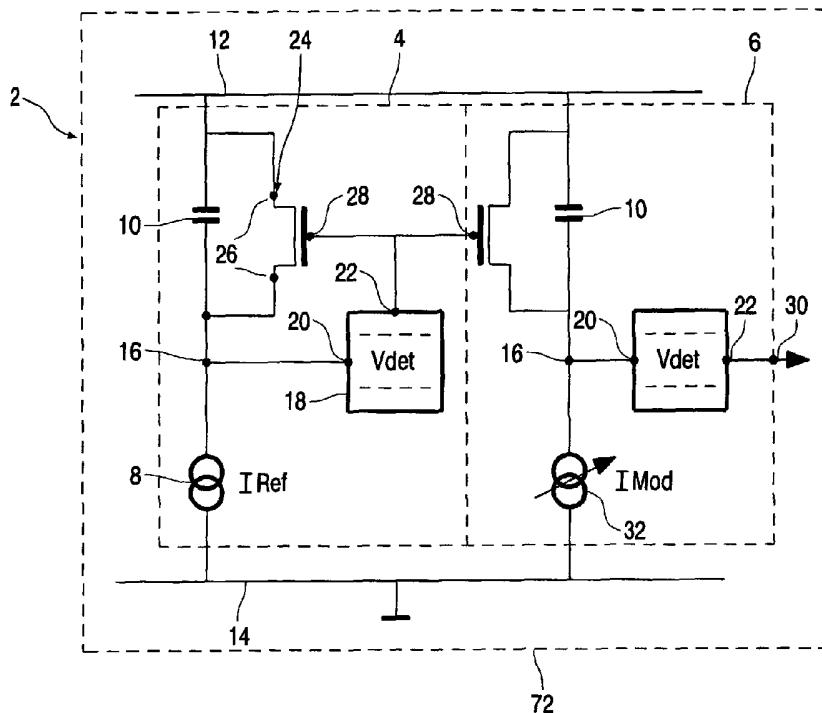
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(54) Title: PULSE WIDTH MODULATION SIGNAL GENERATOR



(57) Abstract: A signal generator has matched reference (4) and modulation (6) ramp circuits, each including current source (8, 32), capacitance (10) charged by the current source, voltage detector (18) and switch (24). The output of one of the voltage detectors (8) controls both switches (24), and the output of the other voltage detector (18) is used as the output.

WO 2004/004123 A1



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- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments* *For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

DESCRIPTION

PULSE WIDTH MODULATION SIGNAL GENERATOR

5 The invention relates to a signal generator, and in particular to a signal generator for producing a pulse width modulated (PWM) signal. The invention also relates to a switched dc-dc converter incorporating the signal generator and to a method of dc-dc conversion.

10 Pulse width modulation circuits are used in a variety of applications, including power devices. Temperature variation can be a real problem in such circuits, especially in the signal generation circuit that delivers a pulse width modulated output. Temperature variation can significantly effect the output making it difficult to achieve an accurate control of the on to off ratio in the
15 PWM output. The on to off ratio is the ratio of time that the signal is on to the time that the signal is off.

 Signal generators for producing pulse width modulated signals are particularly required for driving switching dc-dc voltage generators. Such circuits may be used in a number of fields where temperature variation can be
20 a problem. A particular example of this is in the automotive sector.

 Switching dc-dc circuits may be implemented synchronously, using a pull-up and a pull-down power transistor controlled by the output of a signal generator in such a fashion that only one of the two transistors is on at any one time. The common node between the pull-up and pull-down transistors is
25 known as a drive node, and is connected to the output by means of a filter circuit. The on to off ratio controls the output voltage.

 To use such a circuit in automotive applications to produce a dc voltage different to the input voltage requires that the circuit be rugged and in particular independent of supply voltage, process variation and temperature.

30 Existing designs do not achieve this to a satisfactory level. One example is DE-A-10048593 which discloses a switching circuit for the control

of a number of components. No special arrangements for temperature stabilisation are provided.

There thus remains a need for an improved signal generation circuit and an improved switching voltage converter that provides improved accuracy
5 particularly as temperature varies.

According to the invention there is provided a signal generator for generating a pulse width modulated control signal, comprising: matched reference and modulation ramp circuits, each including a current source, a
10 capacitance arranged to be charged by the current output from the current source, a switch for discharging the capacitance, and a voltage detector for detecting a predetermined charge on the capacitance; wherein the output of the voltage detector of the reference ramp circuit is connected to control the switch of both the reference and the modulation ramp circuits; and the output
15 of the voltage detector of the modulation ramp circuit is connected to an output.

The invention uses the properties of the matched reference and modulation ramp circuits to achieve a high degree of independence from supply voltage, process variation and temperature. Any change in the current
20 source, the capacitor or the voltage level detected in the voltage detector in one of the ramp circuits will in general be matched in the other and cancelled out, thereby leading to no change in the output percentage on to off ratio. Thus, the signal generator is highly suitable for use with power integrated circuits which may operate at high temperature and with uneven supply
25 voltage.

A further advantage of the circuit is that it is open loop and does not need an op-amp in it. This offers a number of advantages. It greatly simplifies the design and operation of the circuit as the performance of the circuit is not limited by the performance of the op-amp. This means that op-amp offset and
30 slew rates which could reduce the performance of existing circuits do not need to be considered. For switching voltage applications, a high frequency is beneficial and so for a good level of accuracy the slew rate on the output

needs to be very high. Thus, providing a suitable op-amp is difficult, a difficulty solved in the present invention which does not require an op-amp.

The other advantage of an open loop system is that the method of charging a capacitance by current sources effectively integrates the input and reference current over the period of the pulse width modulated signal. This means that the system is less sensitive to noise on both the input and the reference currents. This gives improved accuracy over existing designs.

The current source is preferably a fixed current constant current source and the current source of the modulation ramp circuit is preferably a modulated current source having a control input for controlling the output current and hence for controlling the percentage of time the output is on.

If the signal input on the control input is continuously variable the final pulse width modulated output will effectively integrate the input for the whole period, rather than just sample the input voltage at a given moment. Therefore, the signal generator according to the invention will give a better representation of the changing input signal in its control of the output path width modulation pulse stream than an existing design would. This gives the dual charge rate circuit considerable advantages over conventional designs in systems with dynamic inputs.

In embodiments of the invention, in each of the measurement and modulation ramp circuits the current source is connected to the capacitance at a measurement node; the voltage detector has a sense input and a control output with the sense input being connected to the measurement node, for detecting the voltage on the measurement node and outputting a control signal on the control output under predetermined conditions; the switch is arranged across the capacitance; and the switch has a control input, the switch being arranged to be closed by a signal on the control input for discharging the capacitance in response to the signal; the capacitance, voltage detector and switch of the reference and modulation ramp circuits are matched, and the control output of the voltage detector on the measurement node is connected to the control input of the switches of both the reference and modulation ramp circuits.

The switch in each ramp circuit is preferably a transistor having controlled terminals (source and drain) connected across the capacitance and a control terminal (gate) connected to the output of the voltage detector of the reference ramp circuit. The transistor can then simply be switched on to
5 discharge the capacitance through the transistor.

The modulation and reference ramp circuits are preferably integrated on a single semiconductor substrate to ensure good temperature matching and corresponding benefit to the self-cancelling properties of the circuit.

The signal generator may be included in a switching dc-dc converter
10 circuit having a dc input, a dc output, and a switching module connected between the dc input and the dc output and containing at least one switch controlled by the output of the signal generator.

The invention also relates to a power switching device having high and low dc inputs; a filter circuit connected between a drive node and the low
15 voltage dc input, the filter circuit having a filter output; at least one of a first power transistor connected between the high dc input and the drive node and a second power transistor connected between the drive node and a low voltage node; and a signal generator as above connected to drive the at least one of the first and second power transistors for producing a predetermined dc
20 output voltage between the filter output and the low voltage node.

Preferably, the signal generator and at least one power transistor is included in the same device package.

The first and second power transistors may preferably be power MOSFETs.

25 The invention also relates to a method of generating a control signal for a pulse width modulator, including: providing matched reference and modulation ramp circuits; each of the first and second ramp circuits including each including a current source, a capacitance arranged to be charged by the current output from the current source; a switch for discharging the
30 capacitance, and a voltage detector for detecting a predetermined charge on the capacitance; driving a constant current to charge the capacitance of the reference ramp circuit; supplying a modulated constant current to the

measurement node of the modulation ramp circuit; detecting in the voltage detector in each ramp circuit when the voltage across the respective capacitance exceeds a predetermined value; outputting a control signal from the voltage detector in the reference ramp circuit to the inputs of the switches
5 in both modulation and reference ramp circuits to discharge the capacitance when the voltage across the capacitance in the reference ramp circuit exceeds the predetermined value; and outputting the signal from the voltage detector in the modulation ramp circuit as the control signal for a pulse width modulator.

10 Embodiments of the invention will now be described, purely by way of example, with reference to the accompanying drawings in which:

Figure 1 shows a signal generator according to the invention;

Figure 2 shows outputs of the voltage modulation and voltage reference circuits;

15 Figure 3 shows a first embodiment of a switching modulator incorporating the signal generator of Figure 1; and

Figure 4 shows a second embodiment of switching modulator incorporating the signal generator of Figure 1.

20 Referring to Figure 1, signal generator 2 formed on a single semiconductor substrate 70 includes matching reference 4 and modulation 6 ramp circuits. Each circuit includes a current source 8, 32 and a capacitor 10 connected in series between high 12 and low 14 voltage rails. The node between the current source 8 and capacitor 10 will be referred to as the
25 measurement node, and it is connected to voltage detector 18 which has input 20 connected to the measurement node. The voltage detector further includes output 22. Transistor 24 is connected across the capacitor 10. The transistor 24 is in the embodiment a MOSFET having controlled terminals 26 (the source and drain) connected to opposite ends of the capacitor and a control terminal
30 28 (the gate) which is connected in both reference and modulation ramp circuits 4, 6 to the output 22 of the voltage detector 18 in the reference ramp

circuit. The output of the voltage detector in the modulation ramp circuit is connected to output node 30 to form the output of the signal generator.

Each of the voltage detector circuits 18 is arranged to detect the same predetermined voltage on the respective measurement node 16 and output a
5 signal on output 22 suitable for switching on the transistors 24 which act as switches to discharge the capacitor.

The current source 32 in the modulation ramp circuit is adjustable to allow the output on:off ratio of the output pulse width modulation (PWM) signal to be adjusted.

10 The initial cycle of the circuit is as follows at the start of the cycle. The capacitor 10 is reset via the transistor 24 so that both sides of the capacitor 10 are at the same potential. The capacitor 10 is then charged from the current source 8 with the transistor 24 acting as an open switch. The capacitor 10 will continue to charge until the voltage detector 18 detects a predetermined
15 voltage on measurement node 16. At this time, the voltage detector outputs a signal on output 22 suitable to switch on the transistor 24 to short both sides of the capacitor together to discharge the capacitor 10. The discharge of the capacitor 10 in both reference 4 and modulation 6 ramp circuits is controlled by the voltage detector 18 in the reference ramp circuit.

20 The charge rate of the capacitor 10 in the modulation ramp circuit 6 is controlled by current source 32. As the circuits are matched if the current output by current source 32 in the modulation ramp circuit is greater than the current output by current source 8 in the reference ramp circuit then the modulation detector 18 in the modulation ramp circuit will trigger to produce
25 output before the voltage detector 18 in the reference ramp circuit. When the reference voltage detector triggers it discharges the capacitor 10 in the modulation ramp circuit and accordingly resets the voltage detector 18 in the modulation ramp circuit and return the sign of the output to its original sign.

30 The output of the modulation ramp circuit 18 functions as the output of the signal generator. The percentage of pulse rate modulation is given by the amount that the current output by the modulation current source 32 increases that of the reference current source 8. Thus, if both currents are equal, 100%

on pulse width modulation signal will be output. If the modulation current source 32 produces twice as much current as the reference current source 8, then 50% on pulse width modulation will be achieved. This is illustrated in Figure 2 for a 2.5 times ratio producing a 40% on output.

5 Traditional PWM circuits generate the PWM signal by generating a regular reference waveform, usually a sawtooth, and comparing it against a dc voltage with an op-amp. By changing the level of the dc voltage the PWM percentage can be changed. The problem with this approach is that the dc voltage has to carefully match the regular waveform as the two circuits that
10 control these two signals are completely independent. This means that any variation in component values in either circuit can cause errors in the PWM output. To rectify this there is usually a degree of trimming in these types of circuits. The dual charge technique according to the invention is not affected by these problems, because the two circuits that make up the system are the
15 same and are self cancelling. This means that as long as the variation in components is common to the two circuits then a high degree of matching can be obtained, because exactly the same components are used in both. Therefore both halves of the circuit will be affected in the same way and the variation will cancel out. This makes the circuit ideally suited for IC
20 applications where components exhibit good matching.

The self cancelling design of the circuit also means that it has a high degree of temperature independence. Any change in the current source, the capacitor or the voltage level detected in the voltage detector, due to a change
25 in a components characteristics, will be matched in the other circuit and cancelled out, even if the temperature rapidly changes. Therefore the PWM on-ratio will stay more constant compared with existing circuits. This is highly important in power IC's, which have a wide operating temperature range.

A further advantage of this circuit is that it is open loop and as such does not require an op-amp in its design. This offers a number of advantages.
30 Firstly it greatly simplifies the design and operation of the circuit as the performance of the PWM circuit is not limited by the performance of the op-amp. This means that offsets and slew rates which could reduce the

performance of an existing PWM design do not have to be considered. This is especially important in this case, where the PWM system has a very high frequency and to get a good level of accuracy the slew rate on the output will have to be very high, which can make designing a suitable op-amp difficult.

5 Another advantage of this system is that the method effectively integrates the input and reference currents over the period of the PWM signal, by charging the capacitors in the circuit at the rate of the input current. This means that the system is less sensitive to noise on both the input and the reference currents. This gives improved accuracy over existing designs. More
10 importantly, it means that if the input is continually varying the final PWM output will be determined by the input level for the whole period, rather than just sampled the voltage at the moment the input was equal to the reference waveform. Therefore the dual charge circuit will give a better representation of the changing input signal in its control of the output PWM pulse stream, than
15 an existing design would. This gives the dual charge rate circuit considerable advantages over conventional designs, in systems that have dynamic inputs.

Referring to Figure 3, the signal generator 2 may be used to drive the transistor of a switching dc-dc converter. The input dc signal is provided on high 40 and low 42 input dc terminals. Control terminal 44 also feeds into
20 signal generator 2 to control the required output voltage.

The signal generator is connected to switching circuit 72 to control MOSFET switch 46 which is connected between high voltage input 40 and drive node 50. A filter 52 is connected between drive node 50 and low voltage
25 terminal 42, the filter 52 in this case being formed by inductor 54 and capacitor 56 connected in series with filter node 58 between the two. A diode 68 provides a current path to the inductor 54 when the switch 46 is off.

Low voltage output terminal 62 is connected to low voltage input terminal 42, and high voltage output terminal 60 is connected to the filter node 58. The components may all be integrally formed in a single device package
30 66.

The output may be used, for example, to drive a lamp in an automotive application.

Referring to Figure 4, an alternative embodiment includes a synchronous dc-dc converter having two transistors.

The output 30 from the signal generator 2 is used to first 46 and second 48 power transistors, in this case MOSFETs. One of the transistors is driven
5 directly from output node 30, whereas the other transistor is driven through inverter 51. The transistors 46, 48 are connected in series between the input high 40 and low 42 dc voltage terminals. The node joining the two transistors is known as the drive node since the output drive is taken from this point.

A filter 52 is connected between drive node 50 and low voltage terminal
10 42, the filter 52 in this case being formed by inductor 54 and capacitor 56 connected in series with filter node 58 between the inductor 54 and the capacitor 56.

High 60 and low 62 output voltage terminals are connected to filter node 58 and to low voltage input node 42 respectively. Feedback link 64 is used to
15 feed back to control the current output by the modulation current source. The details of how the modulation current signal is controlled from the signal on the feedback link 64 and the input control node 44 are well known to the person skilled in the art and so will not be described further.

Package 66, indicated by a dotted line, includes the whole circuit,
20 including power transistors 46, 48 and signal generator 2. In alternative embodiments, the package 66 may include one of the transistors 46, 48, leaving the other to be supplied as a discrete component, or the signal generator 2 may be separately packaged. Providing the two halves of the signal generator 2 on the same chip and in the same package assists in
25 temperature matching.

The transistors 46, 48 form a switching module. It should be noted that the invention is also applicable to other types of switching module, such as those using only a single transistor. Further, the skilled person will be aware of many alternative filter designs that may be used to replace the filter 52 of the
30 described embodiment.

The signal generator and switching converter according to the invention is particularly suited for applications in which temperature may vary, such as automotive applications.

In particular, the signal generator 2 may be included as the drive for an
5 integrated power device such as the TOPFET (Trade Mark) marketed by Philips.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the
10 design, manufacture and use of a signal generator and/or pulse width modulation circuit and which may be used in addition to or instead of features described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of disclosure also includes any novel feature or any novel combination of
15 features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to any such features and/or combinations of such features during the prosecution of the present application or of any further applications
20 derived therefrom.

CLAIMS

1. A signal generator (2) for generating a pulse width modulated signal, comprising:

5 matched reference (4) and modulation (6) ramp circuits, each including a current source (8, 32), a capacitance (10) arranged to be charged by the current output from the current source (8, 32), a switch (24) for discharging the capacitance, and a voltage detector (18) for detecting a predetermined charge on the capacitance;

10 wherein the output (22) of the voltage detector (18) of the reference ramp circuit (4) controls the switch (24) of both the reference (4) and the modulation ramp circuits (6); and

the output (32) of the voltage detector (18) of the modulation ramp circuit (6) is connected to an output (30) for providing the pulse width
15 modulated signal.

2. A signal generator according to claim 1, wherein

in each of the measurement and modulation ramp circuits the current source (8, 32) is connected to the capacitance (10) at a measurement node
20 (16); the voltage detector (18) has a sense input (20) and an output (22) with the sense input (20) being connected to the measurement node (16), for detecting the voltage on the measurement node (16) and outputting a control signal on the output (22) under predetermined conditions; the switch (24) is arranged across the capacitance (10); and the switch (24) has a control input
25 (28), the switch being arranged to be closed by a signal on the control input (28) for discharging the capacitance in response to the control signal;

the capacitance (10), voltage detector (18) and switch (24) of the reference (4) and modulation (6) ramp circuits are matched; and

the control output (22) of the voltage detector (18) on the reference
30 ramp circuit (4) is connected to the control input (28) of the switches (24) of both the reference (4) and modulation (6) ramp circuits.

3. A signal generator according to claim 1 or 2 wherein the current source (8) of the reference ramp circuit (4) is a fixed current constant current source (32) and the current source of the modulation ramp circuit (6) is a modulated current source having a control input for controlling the output constant current, and in turn for controlling the percentage of time the output is on.

4. A signal generator according to any preceding claim wherein the switch (24) in each ramp circuit is a transistor having controlled terminals (26) connected across the capacitance and the control terminal (28) connected to the output of the voltage detector of the reference ramp circuit.

5. A signal generator according to any preceding claim wherein the modulation (6) and reference (4) ramp circuits are integrated on a single semiconductor substrate (70).

6. A switching dc-dc converter circuit comprising a dc input (40, 42); a dc output (60, 62); a signal generator (2) according to any preceding claim; and a switching module (72) connected between the dc input and the dc output and containing at least one switch (46) controlled by the output of the voltage detector of the modulation ramp circuit of the signal generator (2) to convert an input dc voltage into an output dc voltage.

7. A power switching device according to claim 6 further comprising a device package (66) including the signal generator (2) and at least one power transistor switch (46).

8. A power switching device according to claim 6 or 7 comprising first (46) and second (48) power transistors wherein the signal generator (2) is arranged to switch on the first power transistor (46) only when the second transistor (48) is switched off and to switch on the second transistor (48) only when the first transistor (46) is switched off.

9. A method of generating a control signal for a pulse width modulator, including:

providing matched reference (4) and modulation (6) ramp circuits; each
5 of the first and second ramp circuits (4, 6) including a current source (8, 32), a
capacitance (10) arranged to be charged by the current output from the current
source; a switch (24) for discharging the capacitance, and a voltage detector
(18) for detecting a predetermined charge on the capacitance;

10 driving a constant current to charge the capacitance (10) of the
reference ramp circuit;

supplying a modulated current to charge the capacitance (10) of the
modulation ramp circuit (6);

15 detecting in the voltage detector (18) in each ramp circuit (4, 6) when
the voltage across the respective capacitance (10) exceeds a predetermined
value;

outputting a control signal from the voltage detector (18) in the
reference ramp circuit (4) to the inputs of the switches (24) in both modulation
and reference ramp circuits (4, 6) to discharge the capacitance (10) when the
voltage across the capacitance in the reference ramp circuit exceeds the
20 predetermined value; and

outputting the signal from the voltage detector (18) in the modulation
ramp circuit (6) as the control signal for a pulse width modulator.

25 10. A method according to claim 9 further including adjusting the
modulated constant current to vary the percentage of time the output is on.

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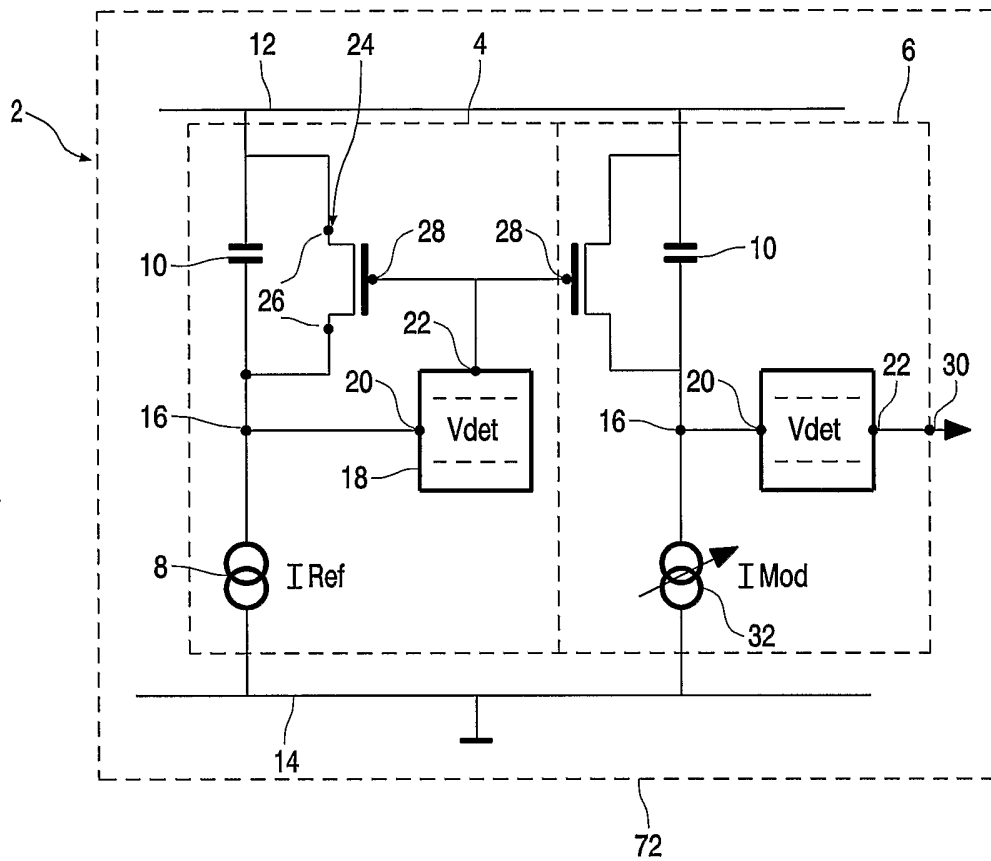


FIG.1

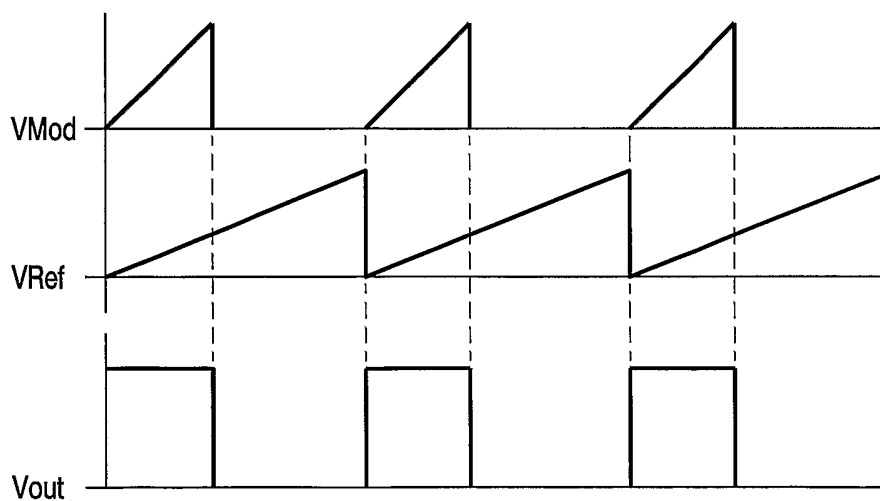


FIG.2

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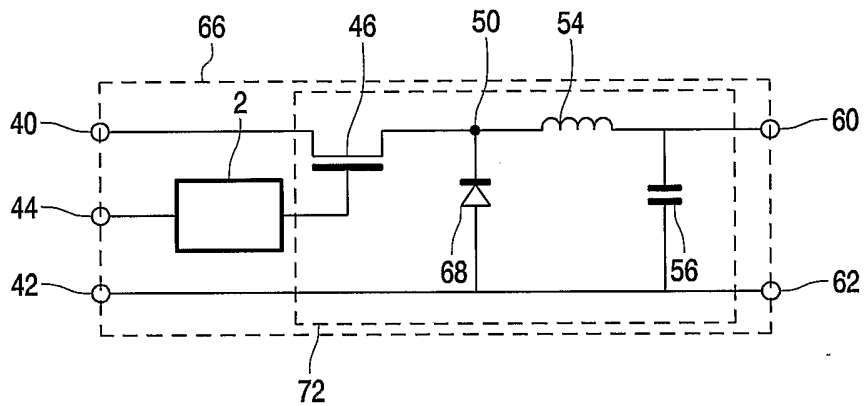


FIG.3

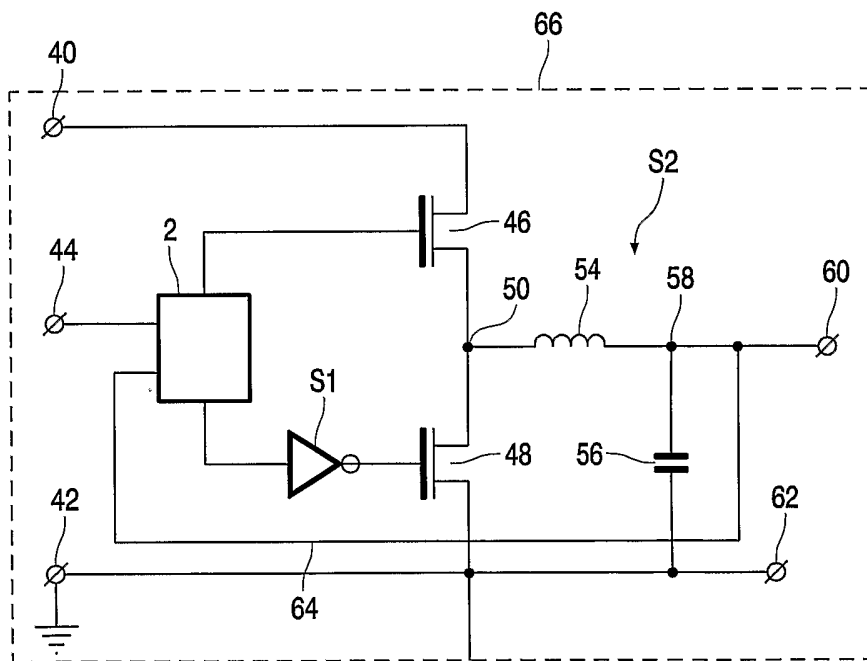


FIG.4

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K7/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 633 168 A (VENEMA HARRY J) 30 December 1986 (1986-12-30) column 1, line 64 -column 3, line 36; figures 1,2 column 4, line 38 - line 41	1,2,4,5
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X	US 4 404 481 A (IDE TOSHIMINE ET AL) 13 September 1983 (1983-09-13) column 5, line 4 - line 15; figures 6,8,9,14 column 5, line 44 -column 7, line 65	1,2
A	---	3-10
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Name and mailing address of the ISA

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INTERNATIONAL SEARCH REPORT

 Internatic plication No
 PCT/IB 03/02862

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 03/02862

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