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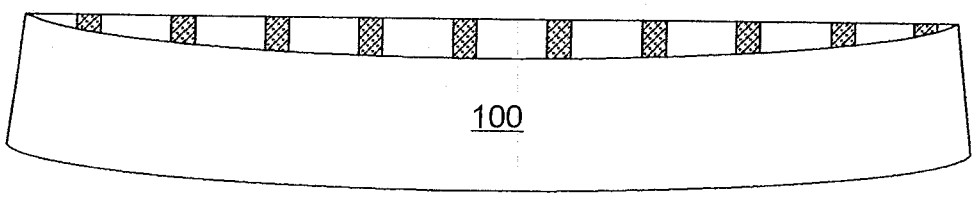

FIG. 5

(57) Abstract: A planarizing method performed on a non-planar wafer involves forming electrically conductive posts extending through a removable material, each of the posts having a length such that a top of each post is located above a plane defining a point of maximum deviation for the wafer, concurrently smoothing the material and posts so as to form a substantially planar surface, and removing the material. An apparatus includes a non planar wafer having contacts thereon, the wafer having a deviation from planar by an amount that is greater than a height of at least one contact on the wafer, and a set of electrically conductive posts extending away from a surface of the wafer, the posts each having a distal end, the distal ends of the posts collectively defining a substantially flat plane.

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TITLE

BOWED WAFER HYBRIDIZATION COMPENSATION

FIELD OF THE INVENTION

[0001] The present invention relates to wafer processing and, more particularly, to wafer processing for electrical connections.

BACKGROUND

[0002] Semiconductor wafers are typically highly polished with very smooth surfaces (i.e. deviations of less than 1 nm). However, they are not necessarily uniformly flat across the extent of the wafer. The same is true for wafers of ceramic or other materials. Flatness variation, called "wafer bow," may be a result of the wafer manufacturing process itself or processing of the wafer (e.g. through depositing of metal or dielectric onto the wafer) and can be on the order of 25μm or more on the concave and/or convex side. If the polished side is concave, the wafer is often referred to as "dished" whereas if it is convex the wafer is called "bowed." Note however, that an individual wafer can concurrently have both types of non-planarities (i.e. one portion is bowed whereas another portion is dished.

[0003] For simplicity herein, the terms "dished," "bowed" and "non-planar" are interchangeably used herein to generically refer to a non-flat wafer of, for example, semiconductor or ceramic, irrespective of whether it would formally be called dished or bowed. FIG. 1 illustrates, in simplified form, a conventional non-planar wafer 100. As shown, the wafer 100 is between 500μm and 750μm thick and has a maximum deviation "δ" at the edges of 25μm from flat. As a result, in the example of FIG. 1, the deviation from highest to lowest point across both sides is 40μm. In most cases, with conventional processes for forming chips and interconnecting them to other chips, this amount of bow is sufficiently small relative to the size

of typical connections that it can be disregarded. However, such variations can render a wafer unsuitable for use where the pitch and/or height of the individual contacts is less than or equal to 25μm, unless further expensive polishing operations are performed to reduce the bow to an acceptable level, if it is possible to do so at all. Moreover, if the same types of connections will be used but the chip will be stacked with another chip, the bowing would be on the order of about 50μm (i.e. taking into account the maximum deviation of 25μm each for both chips and/or on both sides).

[0004] Thus, there is a need for a way to make use of individual wafers that have bow on a side with contacts that are less in height than the bow or on a pitch where such bow could make it impossible to connect to them.

SUMMARY OF THE INVENTION

[0005] We have devised a way to overcome the above problem, rendering wafers that are bowed by up to 20μm each suitable for use with small pitch and/or height contacts and suitable for stacking despite their bowed nature.

[0006] One aspect of the invention involves a planarizing method performed on a non-planar wafer. The method involves forming electrically conductive posts extending through a removable material, each of the posts having a length such that a top of each post is located above a plane defining a point of maximum deviation for the wafer, concurrently smoothing the material and posts so as to form a substantially planar surface, and removing the material.

[0007] Another aspect of the invention involves an apparatus. The apparatus includes a non planar wafer having contacts thereon. The wafer has a deviation from planar by an amount that is greater than a height of at least one contact on the wafer. A set of electrically conductive

posts extends away from a surface of the wafer. The distal ends of the posts collectively define a substantially flat plane.

[0008] Through use of the approaches described herein, bowed wafers can be used with various techniques that allow for via densities, pitch and placement and involve forming small, deep vias in, and electrical contacts for, the wafers – on a chip, die or wafer scale, even though the heights or densities of the contacts thereon are small relative to wafer bow.

[0009] The advantages and features described herein are a few of the many advantages and features available from representative embodiments and are presented only to assist in understanding the invention. It should be understood that they are not to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages are mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 illustrates, in simplified form, a conventional non-flat wafer;

[0011] FIGS. 2 through 6 illustrate, in simplified from, use of our approach on a bowed wafer that is considered "dished;"

[0012] FIG. 7 illustrates, in simplified form, the wafer of FIG. 6 after a set of chips have been connected to it;

[0013] FIG. 8 through FIG. 15 illustrate, in simplified from, use of our approach on a bowed wafer 100 that is considered "bowed;"

[0014] FIG. 16 illustrates, in simplified form, the wafer of FIG. 15 after a set of chips have been connected to it using the planarizing posts formed using the process;

[0015] FIG. 17 illustrates, in simplified form, a pair of dished wafers that have been planarized according to the approach described herein and joined to each other; and

[0016] FIG. 18 illustrates, in simplified form, a pair of bowed wafers that have been planarized according to the approach described herein and joined to each other.

[0017] Note that all of the FIGS. are grossly distorted and out of scale for simplicity of presentation.

DETAILED DESCRIPTION

[0018] U.S. Patent Applications, Serial Nos. 11/329,481, 11/329,506, 11/329,539, 11/329,540, 11/329,556, 11/329,557, 11/329,558, 11/329,574, 11/329,575, 11/329,576, 11/329,873, 11/329,874, 11/329,875, 11/329,883, 11/329,885, 11/329,886, 11/329,887, 11/329,952, 11/329,953, 11/329,955, 11/330,011 and 11/422,551, incorporated herein by reference, describe various techniques for forming small, deep vias in, and electrical contacts for, semiconductor wafers. The techniques allow for via densities, pitch and placement that was previously unachievable and can be performed on a chip, die or wafer scale. In some cases, it is desirable to perform the techniques described therein on a wafer but the contact heights or densities are small relative to wafer bow. Advantageously, we have developed a way to do so. FIGS. 2 through 6 illustrate, in simplified from, use of our approach on a bowed wafer 100 that is considered "dished." The process is as follows:

[0019] First, as shown in FIG. 2, a material 200 is applied to the dished side 202 of the wafer 100 to a thickness that is at least equal to, and typically more than, the maximum deflection δ on that side (as indicated by the dashed line 204).

[0020] Depending upon the particular implementation, the material 200 could be a flowable material or fairly solid material. In general, to reduce the number of processing steps, the material will be a photoresist or photosensitive dielectric, so that it can be patterned. Alternatively, a machine-able or moldable material could be used. In the case of a substantially solid material, example suitable materials include photoresists from the Riston® dry film line of photoresist, commercially available from E. I. du Pont de Nemours & Co. Specifically, The Riston® PlateMaster, EtchMaster and TentMaster lines of photoresist are suitable and at, respectively, about 38μm, 33μm and 30μm in thickness, are all more than sufficient o handle the deviations at issue.

[0021] In the case of a device bearing wafer, using a material 200 that can be patterned makes it easier to match and create openings over the locations of the contacts or device pads on the wafer 100. In addition, if a substantially solid material 200 is used, the wafer can also contain unfilled vias or features extending into the wafer and there is little to no risk of those vias becoming filled by the material 200 – indeed it can protect them from becoming filled by subsequent steps if desired.

[0022] FIG. 3 illustrates, in simplified form, the wafer 100 after the material has been patterned to form openings 300-1, 300-2, 300-3, 300-4, 300-5, 300-6, 300-7, 300-8, 300-9, 300-10 in the wafer over pre-formed connection points.

[0023] Thereafter, the openings are filled with electrically conductive material, typically a metal, using any suitable process including, for example in the case of metal, deposition or plating (electro- or electroless) or some combination thereof.

[0024] FIG. 4 illustrates, in simplified form, the wafer 100 of FIG. 3 after the openings 300-1, 300-2, 300-3, 300-4, 300-5, 300-6, 300-7, 300-8, 300-9, 300-10 have each been filled with the electrically conductive material 402.

[0025] Next, the surface 400 of the wafer 100 is polished smooth using a conventional polishing or other smooth finishing method that will result in as small a deviation as possible, with maximum deviation of less than the contact height, typically from ±0μm to about 10μm. However, in some implementations where a post and penetration connection will be used, that approach can allow for greater deviations due to the inherent flexibility that such connections provide.

[0026] FIG. 5 illustrates, in simplified form, the wafer 100 after the polishing operation has been completed.

[0027] Next, as shown in FIG. 6, after the material 200 has been removed, using a process appropriate to the selected material 200, a series of elevated, conductive "posts" 600, 602, 604 606, 608, 610, 612, 614, 616, 618 will remain and, although the posts 600, 602, 604 606, 608, 610, 612, 614, 616, 618 may be of differing heights, their upper surfaces will be substantially flat (i.e. within the maximum deviation of the polishing or smooth finishing method). As a result, the connection points on the wafer 100 can now be connected to, or another chip, die or wafer can be stacked without encountering the problems of the prior art noted above.

[0028] FIG. 7 illustrates, in simplified form, the wafer 100 of FIG. 6 after a set of chips 702, 704, 706, 708 have been connected to it using the planarizing posts 600, 602, 604 606, 608, 610, 612, 614, 616, 618 formed using the process.

[0029] FIG. 8 illustrates, in simplified form, a wafer 800 that is considered "bowed."

[0030] FIG. 9 through FIG. 15 illustrate, in simplified from, use of our approach on the bowed wafer 800 of FIG. 8 "bowed." The process is as follows:

[0031] First, as shown in FIG. 9, as with FIG. 2, a material 200 such as described in connection with FIG. 2, is applied to the wafer 800, although, in this case, it is applied to the bowed side 802 of the wafer 100.

[0032] As illustrated in FIG. 10, the material 200 is again applied to a thickness that is at least equal to, and typically more than, the maximum deflection δ on that side (as indicated by the dashed line 1002).

[0033] FIG. 11 illustrates, in simplified form, the wafer 800 after the material has been patterned to form openings 1100-1, 1100-2, 1100-3, 1100-4, 1100-5, 1100-6, 1100-7, 1100-8, 1100-9, 1100-10 in the wafer over pre-formed connection points.

[0034] Thereafter, as above, the openings are filled with an electrically conductive material, typically metal, using any suitable process including, for example, deposition or plating (electro- or electroless) or some combination thereof.

[0035] FIG. 12 illustrates, in simplified form, the wafer 800 of FIG. 11 after the openings have been filled.

[0036] Next, as shown in FIG. 13, the wafer 800 will be polished smooth, in this case down to a level indicated by the dashed line 1300, using a conventional polishing or other

smooth finishing method that will result in it being substantially flat (i.e. having a deviation from a commercially creatable "perfectly flat" of between 0μm and no more than about 10μm).

[0037] FIG. 14 illustrates, in simplified form, the wafer 800 after the polishing operation has been completed.

[0038] Next, as shown in FIG. 15, after the material 200 has been removed, using a process appropriate to the selected material 200, a series of elevated, electrically conductive "posts" 1500, 1502, 1504 1506, 1508, 1510, 1512, 1514, 1516, 1518 will remain and, although the posts 1500, 1502, 1504 1506, 1508, 1510, 1512, 1514, 1516, 1518 may be of differing heights, their upper surfaces will be substantially planar (within the maximum deviation of the polishing or smooth finishing method). As a result, the connection points on the wafer 800 can now be connected to, or another chip, die or wafer can be stacked without encountering the problems of the prior art noted above.

[0039] FIG. 16 illustrates, in simplified form, the wafer 800 of FIG. 15 after a set of chips 1602, 1604, 1606 have been connected to it using the planarizing posts 1500, 1502, 1504 1506, 1508, 1510, 1512, 1514, 1516, 1518 formed using the process.

[0040] Thus, should now be appreciated that the approaches described above will allow one to readily connect, on a wafer basis, a pair of wafers that are at a maximum bowed deviation irrespective of whether they are dished or bowed in configuration.

[0041] FIG. 17 illustrates, in simplified form, a pair of dished wafers 1700, 1702 that have been planarized according to the approach described herein and joined to each other.

[0042] FIG. 18 illustrates, in simplified form, a pair of bowed wafers 1700, 1702 that have been planarized according to the approach described herein and joined to each other.

[0043] Of course, the same approach could be used to connect a dished to a bowed or a bowed to a dished wafer in the same manner.

[0044] It should thus be understood that this description (including the figures) is only representative of some illustrative embodiments. For the convenience of the reader, the above description has focused on a representative sample of all possible embodiments, a sample that teaches the principles of the invention. The description has not attempted to exhaustively enumerate all possible variations. That alternate embodiments may not have been presented for a specific portion of the invention, or that further undescribed alternate embodiments may be available for a portion, is not to be considered a disclaimer of those alternate embodiments. One of ordinary skill will appreciate that many of those undescribed embodiments incorporate the same principles of the invention and others are equivalent.

What is claimed is:

1. A planarizing method performed on a non-planar wafer having, on a side, contacts of a height, the wafer having a deviation from planar by an amount that is greater than the height, the method comprising:

applying a material to the side of the wafer, the material being of a thickness that is greater than the deviation from planar;

forming openings in the material, extending through the material, down to connection points on the side;

filling the openings with an electrically conductive material;

smoothing the material and electrically conductive material until they are substantially planar; and

removing the material.

2. The method of claim 1, further comprising:

joining a chip to the wafer using posts exposed by the removing the material so as to form an electrical connection between the wafer and the chip.

3. The method of claim 2, wherein the joining comprises forming a post and penetration connection.

4. The method of claim 1, further comprising:

joining another wafer to the wafer using posts exposed by the removing the material so as to form an electrical connection between the wafer.

5. The method of claim 1, wherein the applying the material to the side of the wafer comprises applying a flowable material to the side.

6. The method of claim 1, wherein the applying the material to the side of the wafer comprises applying a substantially solid material to the side.

7. A planarizing method performed on a non-planar wafer having, on a side, contacts of a height, the wafer having a deviation from planar by an amount that is greater than the height, the method comprising:

forming electrically conductive posts extending from the side through a removable material located on the side, each of the posts having a length such that a top of each post is located above a plane defining a point of maximum deviation for the wafer;

concurrently smoothing the material and posts so as to form a substantially planar surface above the side; and

removing the material.

8. The method of claim 7, further comprising:

stacking another wafer onto the wafer using the posts so as to form electrical connections between the wafers.

9. The method of claim 7, further comprising:

stacking a chip onto the wafer using the posts so as to form electrical connections between the wafer and the chip.

10. An apparatus comprising:

a non planar wafer having contacts thereon, the wafer having a deviation from planar by an amount that is greater than a height of at least one contact on the wafer; and

a set of electrically conductive posts extending away from a surface of the wafer, the posts each having a distal end, the distal ends of the posts collectively defining a substantially flat plane.

11. The apparatus of claim 10, wherein the posts comprise an electrically conductive material.

12. The apparatus of claim 11, wherein the posts comprise a metal.

13. The apparatus of claim 10, wherein the wafer comprises a semiconductor material.

14. The apparatus of claim 10, wherein the wafer comprises a ceramic.

15. The apparatus of claim 10 wherein at least one of the posts has a length from the distal end to a surface of the wafer that is greater than the deviation.

16. The apparatus of claim 10 wherein at least one of the posts has a length from the distal end to a surface of the wafer that is equal to the deviation.

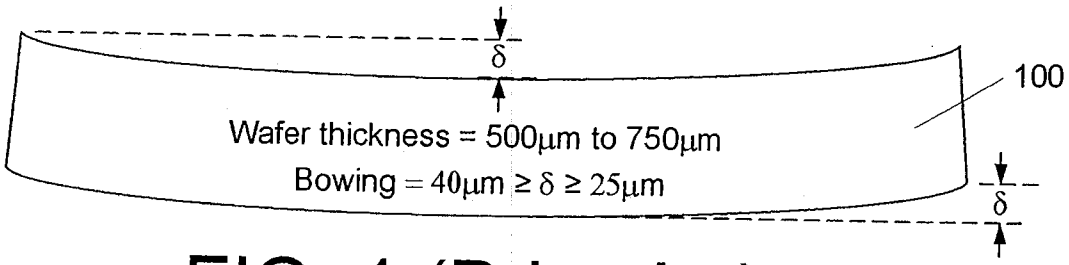

FIG. 1 (Prior Art)

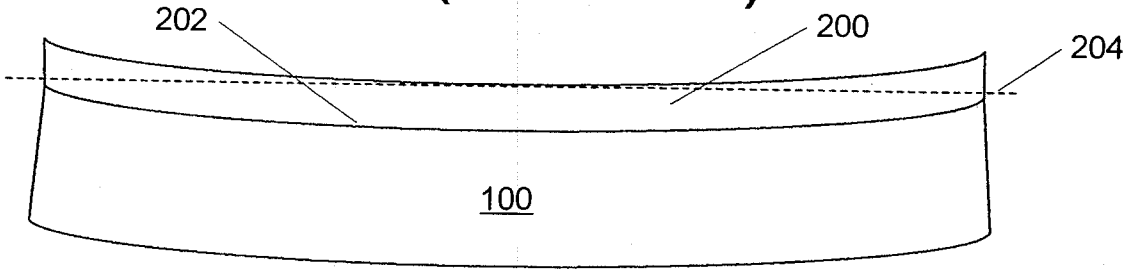

FIG. 2

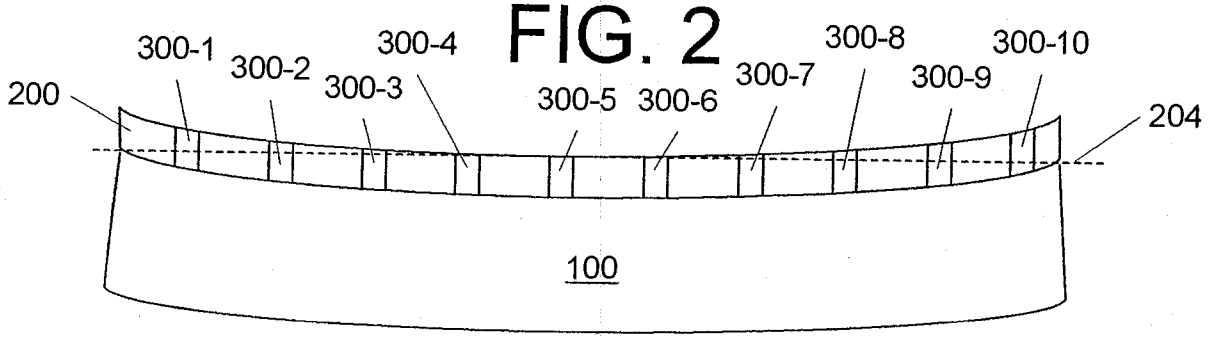

FIG. 3

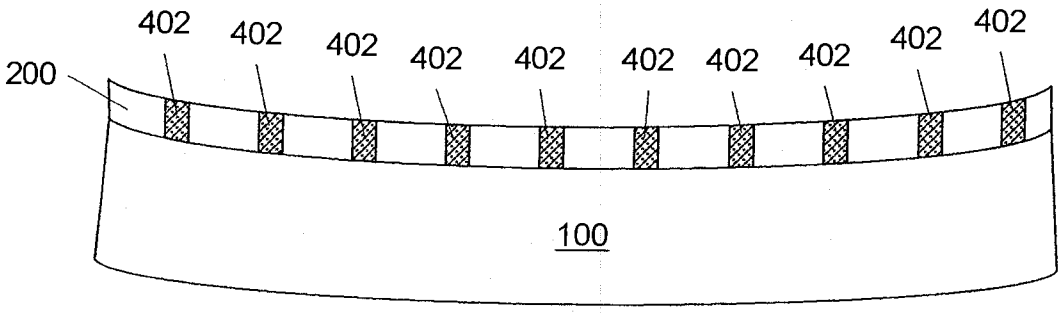

FIG. 4

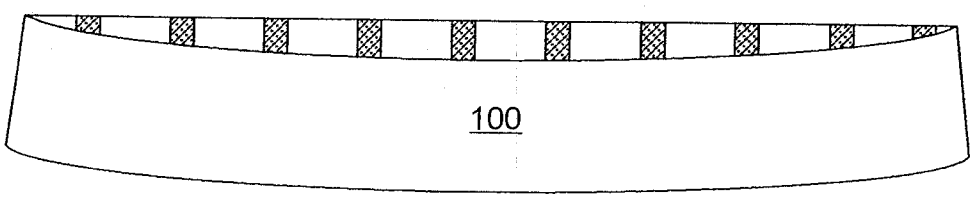

FIG. 5

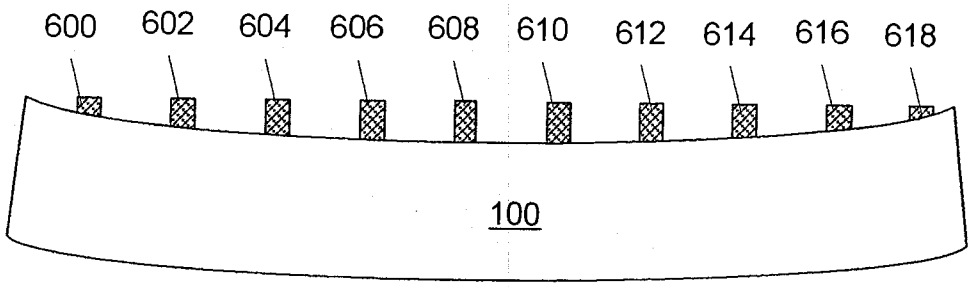

FIG. 6

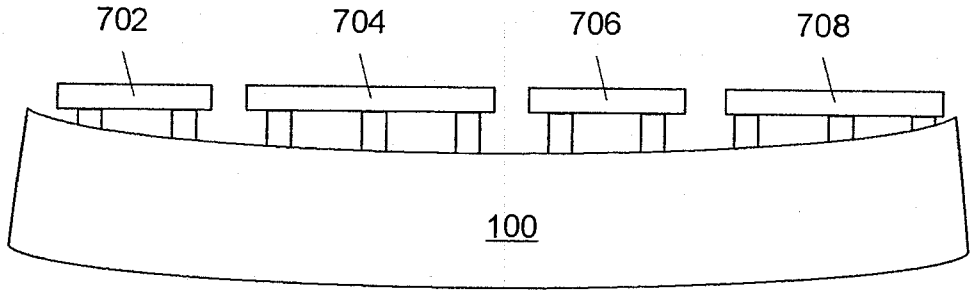

FIG. 7

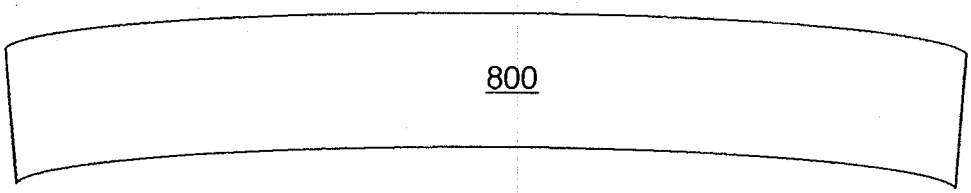

FIG. 8

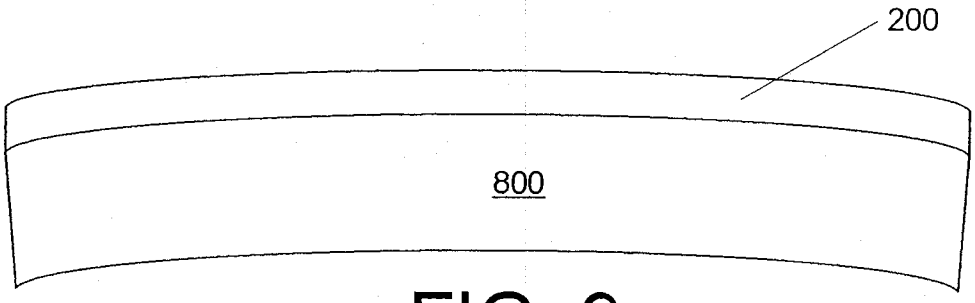

FIG. 9

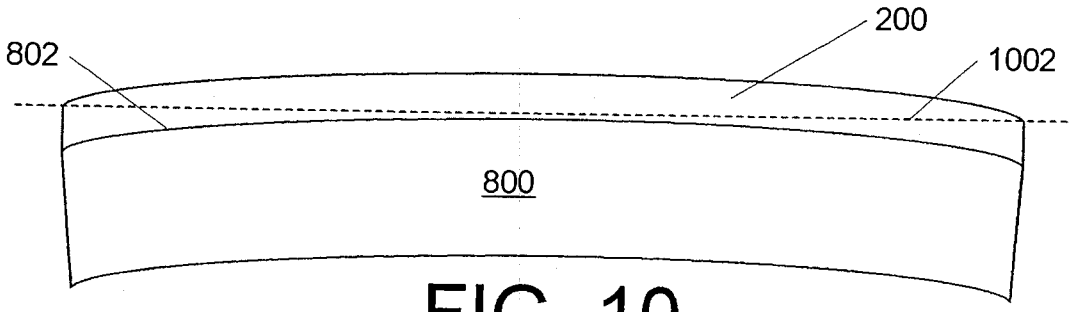

FIG. 10

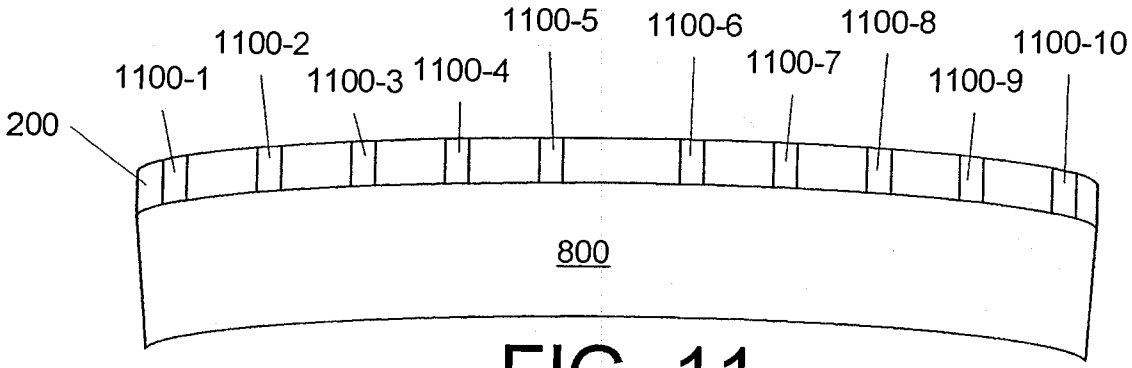

FIG. 11

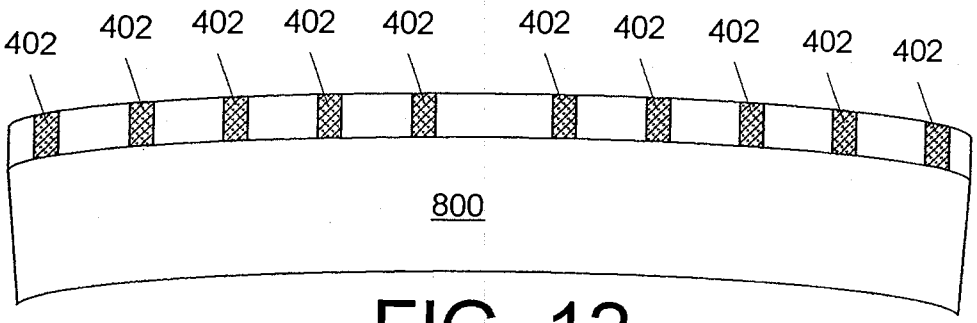

FIG. 12

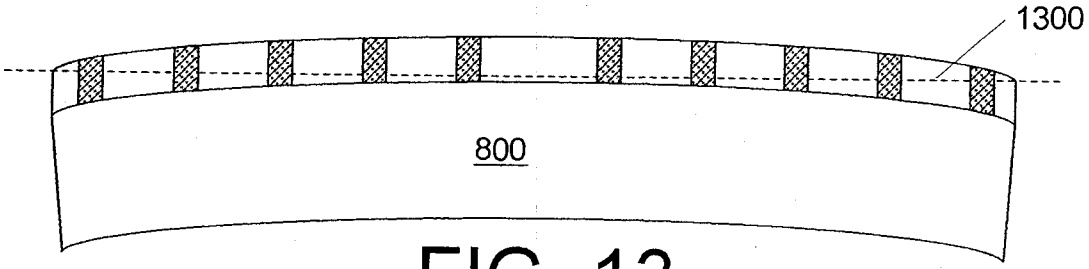

FIG. 13

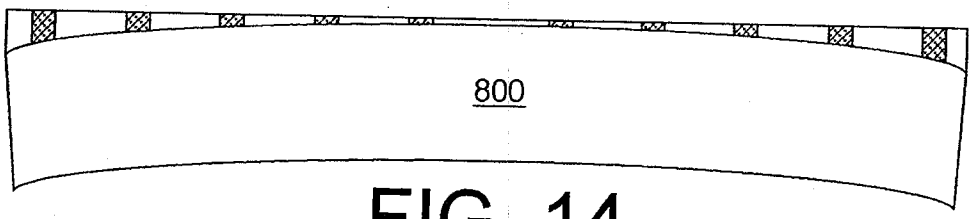

FIG. 14

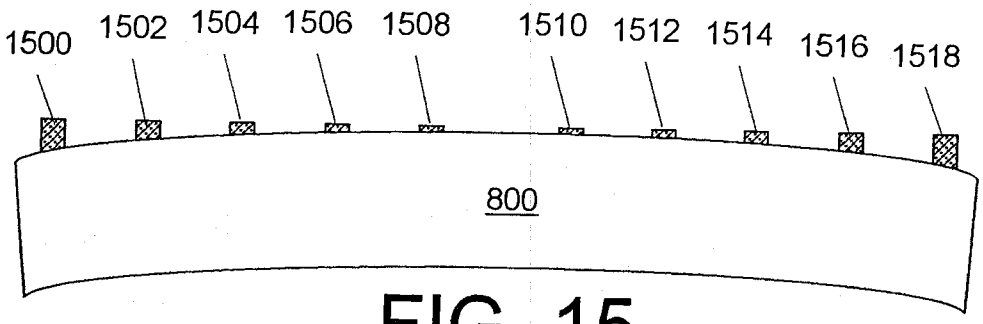

FIG. 15

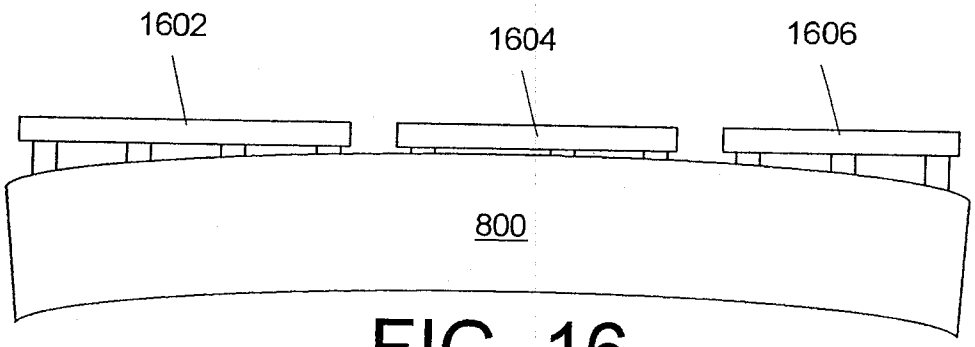

FIG. 16

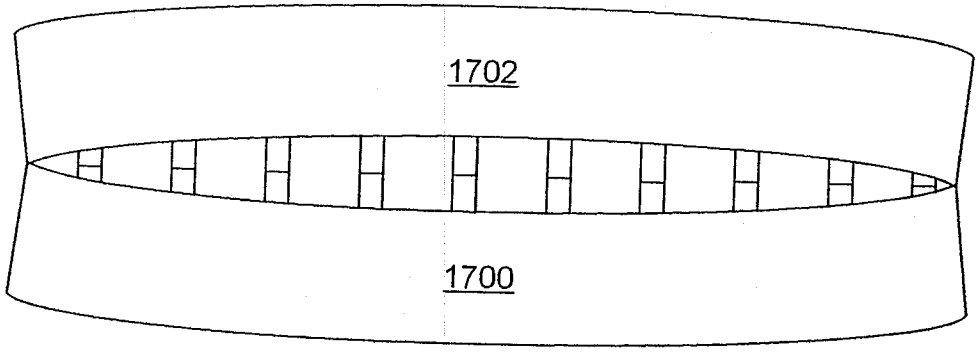

FIG. 17

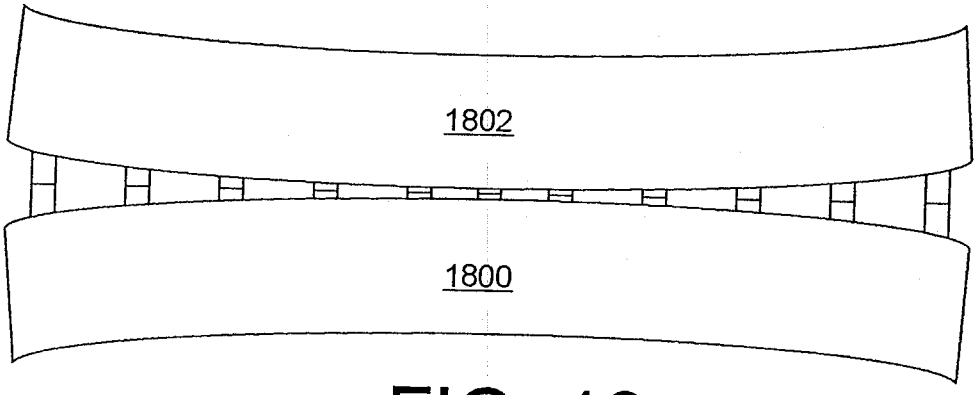

FIG. 18

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/053991

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60
ADD. H01L21/321 H01L21/461

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y X	US 6 220 499 B1 (BROFMAN PETER J [US] ET AL) 24 April 2001 (2001-04-24) the whole document	1-9 10-12, 14-16
Y	US 2005/026413 A1 (LEE JIN-YUAN [TW] ET AL) 3 February 2005 (2005-02-03) paragraphs [0001] - [0039]; figures 2A,2E	1-9
X	JP 09 246324 A (HITACHI LTD) 19 September 1997 (1997-09-19) the whole document	10-13, 15,16
X A	US 6 181 569 B1 (CHAKRAVORTY KISHORE K [US]) 30 January 2001 (2001-01-30) the whole document	10-13, 15,16 1-9

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Corchia, Alessandra

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