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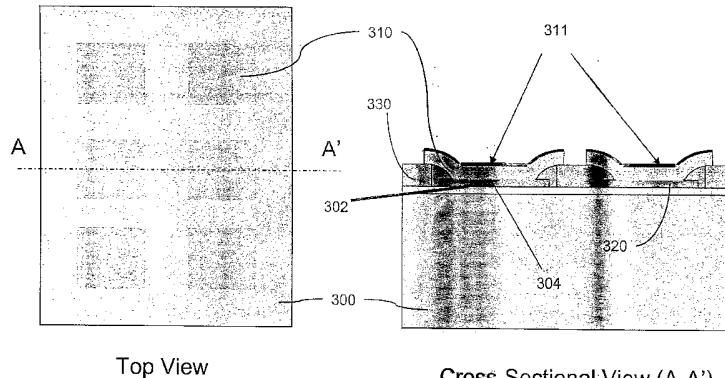
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(54) Title: METAL INTERCONNECT SYSTEM AND METHOD FOR DIRECT DIE ATTACHMENT

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards



Die with Solderable Metal Contacts for Direct Printed Circuit Board Mounting

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(57) Abstract: Provided herein is an exemplary embodiment of a semiconductor chip for directly connecting to a carrier. The chip includes a metal layer applied to a top surface of the chip; a passivation layer applied over the metal layer such that portions of the passivation layer is selectively removed to create one or more openings ("bond pads") exposing portions of the metal layer and one or more solderable metal contact regions formed on each of the one or more openings. The solderable metal contact regions electrically connect to the carrier when the chip is positioned face down on the carrier, supplied with a thin layer of solder and heated.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TITLE

[0001] Metal Interconnect System and Method For Direct Die Attachment

CROSS-REFERENCE TO RELATED APPLICATIONS

5 [0002] This application claims the benefit of priority to U.S. Application Numbers 60/529,166 and 60/544,702, filed December 12, 2003 and February 12, 2004, respectively, the entire disclosures of which are hereby incorporated by reference as if set forth at length herein.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR

10 **DEVELOPMENT**

[0003] Not applicable

REFERENCE OF A "MICROFICHE APPENDIX"

[0004] Not applicable

BACKGROUND OF THE INVENTION

15 **1. Field of Invention**

[0005] The present invention relates generally to semiconductor technology and more particularly, to a system and method for directly mounting semiconductor chips to a substrate such as a printed circuit board.

2. Brief Description of the Prior Art

20 [0006] A typical surface mountable semiconductor component consists of a semiconductor chip attached to a lead frame, wire bonded, and encapsulated into a plastic package with exposed leads. Soldering the leads to e.g., a printed circuit board provides mechanical, thermal, and electrical connections to the semiconductor chip.

[0007] FIGURE 1 – PRIOR ART

[0008] FIG. 1 shows an exemplary embodiment of a typical prior art wire bond chip or chip having a lead frame. Wire bonds add parasitic inductance and series resistance to electronic devices. The added inductance and resistance is undesirable for many devices, including high frequency devices, high speed devices, and low on-resistance power 5 semiconductor devices. The lead frame provides the primary thermal conduction path for the chip. However, the thermal performance of the wire bond chip is limited by the length of the thermal path to the substrate, circuit board or carriers and the lead frame design and composition.

[0009] FIGURE 2 – PRIOR ART

10 [0010] Flip chip bump processing was developed to address the above shortcomings of wire bond chips. Flip chip bump assembly also called Direct Chip Attach assembly, is the process of directly attaching the chip face-down to a substrate, board or carrier, by means of conductive bumps on the chip.

15 [0011] Several varieties of flip chip processing exist today, including solder bump, copper pillar bump; plated bump, gold stud bump and adhesive bump.

[0012] FIG. 2A illustrates a prior art chip 210 having a solder ball bump 220 formed on the chip's under bump metallization ("UBM") layer 260 using conventional techniques. The solder ball bump 220 electrically contacts to the silicon chip 210 enabling the chip to be directly attached face-down to the printed circuit board. A disadvantage of the solder 20 ball approach is the limited contact area of the ball to the chip surface and to the substrate. This reduces the thermal and electrical conduction areas thereby increasing the thermal and electrical resistance. The thermal and electrical paths are long, approximately the diameter of the solder ball. The limited contact area of the ball also

results in limited mechanical strength of the bond between the chip and the circuit substrate.

[0013] As shown in FIG. 2B, instead of a solder ball bump, the chip 210 may include a raised conductive region of a metallic material such as copper, nickel or other metal or alloy, with a top coating of solder. FIG. 2B illustrates the chip 210 having a copper pillar bump 230 formed on the chip's UBM layer 260 using conventional techniques. As shown, the copper pillar bump also includes a top coating of solder 240. Because copper is significantly more thermally and electrically conductive than solder the copper pillar bump 230 offers some improvement over the solder ball 220. However, the standard height of the pillar bump 230 (approx. 100 μm) adds to both the thermal and electrical resistance.

[0014] A further disadvantage is that the above flip chip processes involve multiple steps and require specialized equipment which increases the costs of the product.

SUMMARY OF THE INVENTION

[0015] The present invention addresses the aforementioned limitations of the prior art by providing, in accordance with one aspect of the present invention, a semiconductor chip for directly connecting to a carrier, having a metal layer applied to a top surface of the chip; a passivation layer applied over the metal layer such that portions of the passivation layer is selectively removed to create one or more openings ("bond pads") exposing portions of the metal layer and one or more solderable metal contact regions formed on each of the one or more openings. The solderable metal contact regions electrically connect to the carrier when the chip is positioned face down on the carrier, supplied with a thin layer of solder and heated.

[0016] In accordance with additional aspects of the present invention the solderable metal contact regions are approximately 1 μm thick and comprise either TiCu, TiNiAg or AlNiVCu metal layer combinations.

[0017] These and other aspects, features and advantages of the present invention will 5 become better understood with regard to the following description, appended claims, and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Exemplary embodiments of the present invention are now briefly described with reference to the following drawings:

10 [0019] FIG. 1 depicts aspects of the prior art in accordance with the teachings presented herein.

[0020] FIG. 2 depicts additional aspects of the prior art in accordance with the teachings presented herein.

[0021] FIG. 3 depicts a third aspect of the present invention in accordance with the 15 teachings presented herein.

[0022] FIG. 4 depicts a fourth aspect of the present invention in accordance with the teachings presented herein.

[0023] FIG. 5 depicts a fifth aspect of the present invention in accordance with the teachings presented herein.

20 [0024] FIG. 6 depicts a sixth aspect of the present invention in accordance with the teachings presented herein.

[0025] FIG. 7 depicts a seventh aspect of the present invention in accordance with the teachings presented herein.

[0026] Fig 8 depicts an eight aspect of the present invention in accordance with the teachings presented herein.

DESCRIPTION OF THE INVENTION

[0027] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto.

[0028] FIGURE 3

[0029] FIG. 3 depicts an exemplary embodiment of a semiconductor chip 300 constructed in accordance with the present invention. As shown, the semiconductor chip 300 includes an aluminum metal layer 302, a passivation layer 330, a plurality of "bond pads" or openings 304 in the passivation layer 330 to expose portions of the underlying metal layer 302 and a plurality of solderable electrical metal contact regions 310. The solderable electrical metal contact regions 310 are formed on the bond pads 304 and are made of materials similar to those of the UBM layer 260 in FIGS. 1 & 2. The solderable metal contact regions 310 allow the chip 300 to be directly soldered to a substrate such as a printed circuit board. Preferably, the solderable metal contact regions 310 are approximately 1 μm thick and are made of two or three layers of conductive metals, such

as TiCu, TiNiAg or AlNiVCu metal layer combinations. Optionally, the solderable metal contact regions 310 may include an additional film layer of solder 311 to prevent oxidation of exposed metal and to facilitate the chip's attachment to the substrate.

[0030] FIGURE 4

5 [0031] FIG. 4 depicts an exemplary embodiment of a chip 300 mounted onto a printed circuit board in accordance with the present invention's teachings herein. As shown, the chip 300 is flipped and mounted to a circuit board 430 using conventional surface mount techniques. A thin layer of solder paste 410 can be deposited with a stencil onto the printed circuit board 430. The chip 300 is then placed into the proper location and 10 lowered until it is in contact with paste 410. The printed circuit board 430 assembly is then heated to approximately 200°C until the solder reflows. The solderable metal contact regions 310 on the chip are then directly soldered to the copper printed circuit board traces 420 thereby forming a mechanical, electrical, and thermal connection.

15 [0032] If the solderable metal contact regions 310 include the optional solder layer, it is not necessary to apply the solder paste 410. The solder layer, once reflowed, will be sufficient to attach the chip to the printed circuit board, further simplifying the assembly process.

20 [0033] A semiconductor chip 300 of the present invention may be fabricated as follows: using conventional techniques, first, a semiconductor chip is prepared having at least one aluminum layer on the surface of the chip. Next, a passivation layer is applied over the surface of the chip, portions of which is selectively removed to create one or more openings or bond pads to expose a top aluminum layer. Next, solderable metal contact regions 310 are formed on each of the bond pads using conventional sputtering, plating,

and patterning processes. Optionally, a thin film of solder may be applied over the solderable metal contact regions to facilitate direct chip attachment to a substrate.

[0034] The present invention is applicable to all types of semiconductor chips, including integrated circuits, discrete semiconductor devices, sensors, micro-machined structures, 5 etc. The present invention has several advantages over existing techniques including the following: 1) simplicity of semiconductor packaging; 2) ease of manufacturing; 3) simplicity of mounting device to the printed circuit board; 4) enhanced thermal performance of the package; 5) very short thermal path from the semiconductor chip to the printed circuit board; 6) contact areas can be maximized to increase area of thermal 10 path; thereby reducing the thermal resistance; 7) very low electrical resistance from chip surface to the printed circuit board; 8) short current path from chip to printed circuit board; 9) contact areas can be increase to further minimize the series resistance; and 10) no wire bond or lead frame inductance and resistance.

[0035] Figure 5

15 [0036] FIGS. 5A-C depict exemplary alternative embodiments of a chip 100 in accordance with the present invention's teachings herein. Specifically, FIG 5A illustrates a portion of the device having a substrate 105, two sources 110 and a drain 120. In addition, device 100 is shown as a P substrate 105. In another embodiment, the P substrate is deposited on top of a P- substrate.

20 [0037] Sources 110 and drain 120 are preferably n-type dopants implants into P substrate 105. It will be appreciated that the variations of the design of the sources and drains are known to one skilled in the art and within the scope of the present invention. For

example, sources 110 and drain 120 could be p-type dopant implants into an N substrate

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[0038] As another example FIG. 5B shows a preferred embodiment where sources 110B is comprised of a region 112 which is doped as N+ region 114, which is doped as P+ and the region 116 is doped N. In an alternate embodiment, source 110B is comprised of region 114 doped P+, and regions 112 and 116 are N+ implants adjacent to either side of the P+ region 114. In yet another embodiment, regions, 112 and 114 also have a region 118. Region 118 may be a lightly doped N- Implant while the rest of region 112 and 114 are N+. Region 118's lightly doped N-Implant functions as a lightly doped drain.

10 [0039] Drain 120B, in this example , is comprised of region 124 doped as N+ and regions 124 and 126 doped as N. As with source 110B, it is within the scope of this invention and the skill of one skilled in the art to vary the doping.

[0040] Referring back to FIG. 5A gate 130 is comprised of a polysilicon gate over a SiO₂ or Si₃N₄ insulating layer and is placed between source 110 and drain 120. Adjacent are spacers 132 and 134 preferably comprised SiO₂ or Si₃N₄,and partially extending over source 110 and drain 120 respectively. (FIG 1B also shows spacers 132 and 134 extending over regions 118 and 122. Spacers also extend over regions 126.)

[0041] Source runners 140 and drain runners 170 formed on second interconnect layer and is preferably comprised of metal, although other conductive materials may be used. 20 Source runner 160 interconnects source runners 140 using Vias 162. Preferably, source runners 160 are in substantially parallel orientation with respect to source 110, although other orientations that are not parallel may be used.

[0042] Drain runners 150 are interconnected by drain runners 170 using vias 172. Preferably, drain runner 170 is substantially parallel orientation with respect to drain 120, although other orientations that are not parallel may be used.

[0043] Like the first interconnect layer, only one source and drain runners 160 and 170, 5 respectively are shown, but in the preferred embodiment multiple sources and drain runners 160 and 170 would be used and are, preferably, interleaved with each other.

[0044] Although the runners shown in FIG. 5A are substantially of equal widths and rectangular, runners can be of any shape. For instance, runners may be of unequal widths and runners may have varying narrow and wider portions or rounded corners.

10 [0045] FIG. 5A shows source pad-solderable metal contact region 180 formed on a third interconnect layer, which is preferably comprised of metal, although other conductive materials may be used. Source pad 180 is connected to source runners 160 using vias 182. Although not shown in Fig 5a for the sake of clarity, similar drain pads-solderable metal contact regions connect drain runners 170 and like wise for gate pads-solderable 15 metal contact regions.

[0046] In the preferred embodiment the vias from conductive interconnects and are comprised preferably out of tungsten, although other conductive material may be used.

These are formed in a manner that are well-known to those skilled in the art.

20 [0047] In another embodiment, no second interconnect layer is used for runners. As an example, Fig 5c shows an embodiment similar to Fig 5a except there is no second interconnect layer forming source 160 and drains 170. Instead, drain pad-solderable metal contact regions 190 is formed on the second interconnect layer and is connected to drain

runners 150 by vias 172. Although not shown in Fig 5c for the sake of clarity, similar source pads-solderable metal contact regions connect source runners 140.

[0048] Referring now to Fig 6 there is no top plan view of the embodiment shown in Fig 1a and showing additional sources 110, drains 120 and first layer interconnect source 5 runners 140 and drains runners 150. Sources 110 and drains 120 are shown having substantially vertical orientation while source runners 140 and drain runners 150 are shown in substantially horizontal orientation. Also, shown are vias 142 and 152 interconnecting the source runners 140 and drain runners 150 to sources 110 and drains 10 120, respectively. It should be noted that although Fig 6, for instance, shows at a point of connection the use of two vias, one via could be used as shown in Fig 7a, or more than two, as shown in Fig 5a for vias 182.

[0049] Referring to Fig 7a there is a top plan view showing the first interconnect layer (forming source runner 140 and drain runners 150), second interconnect layer (forming source runner 160 and drain runners 170) and third interconnect layer forming source 15 pad-solderable metal contact regions 180.

[0050] Source runners 140 and drain runners 150 are laid out in substantially horizontal orientation. Source runners 160 overlay source runners 140 and are interconnected using vias 172. Source pad-solderable metal contact regions 180 is shown in Fig 7a overlaying source runners 160 and drain runners 170, but is only connected to source 20 runners 160 by vias

[0051] Fig 7b shows the top plan view of the embodiment of Fig 5a showing the first interconnect (forming source runners 140 and drain runners 150), second interconnect

layer (forming source runners 160 and drain runners 170) and a third interconnect layer forming a drain pad-solderable metal contact regions 190 (in outline form)

[0052] Source runners 140 and drain runners 150 are laid out substantially horizontal orientation. Source runners 160 overlay source runners 140 and interconnect source 5 runners 140 using vias 162. Drain runners 170 overlay drain runners 150 and interconnect drain runners 170 using vias 172. Drain pad-solderable metal contact regions 190 is shown overlaying source runners 160 and drain runners 170, but is only connected to drain runners 170 by vias 192.

[0053] Fig 8 shows the top of the device 100 with source pads--solderable metal contact 10 region 180, analogous drain pad-solderable metal contact region 300 and gate pad-solderable metal contact regions 400. In the embodiment shown in Fig 8, the source and drain pads-solderable metal contact regions are arranged in a checker board layout.

[0054] Fig 8 b shows an alternative layout where each source pad-solderable metal contact regions 410 and drain pad-solderable metal contact regions 420 are shaped 15 stripes and are interleaved with each other. In the preferred embodiment gate pad-solderable metal contact regions 430 would be placed with a shortened source pad 410 or shortened drain pad-solderable metal contact regions 420 as needed.

CONCLUSION

[0055] Having now described preferred embodiments of the invention, it should be 20 apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar

purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor chip for direct attachment to a carrier, comprising:

5 providing a partially manufactured chip having a top surface;

applying a metal layer over said top surface of said chip;

applying a passivation layer over said metal layer;

selectively removing portions of said passivation layer to create one or more openings exposing portions of said metal layer;

10 forming solderable metal contact regions on said one or more openings;

wherein said solderable metal contact regions electrically connect to said carrier when said chip is positioned face down on said carrier, supplied with a thin layer of solder and heated.

15 2. The method as in claim 1 wherein said one or more solderable metal contact regions is made of materials selected from the group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination and an AlNiVCu metal layer combination.

3. The method as in claim 1 wherein said metal layer is aluminum.

4. The method as in claim 1 wherein said one or more solderable metal contact regions are approximately 1 μm thick.
5. A semiconductor chip for directly connecting to a carrier, comprising:
 - a metal layer applied to a top surface of said chip;
 - 5 a passivation layer applied over said metal layer such that portions of said passivation layer is selectively removed to create one or more openings exposing portions of said metal layer;
 - one or more solderable metal contact regions formed on each of said one or more openings; wherein said solderable metal contact regions electrically connect to said carrier when said chip is positioned face down on said carrier, supplied with a thin layer of solder and heated.
- 10 6. The chip as in claim 5 wherein said one or more solderable metal contact regions is made of materials selected from the group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination and an AlNiVCu metal layer combination.
- 15 7. The chip as in claim 5 wherein said metal layer is aluminum.
8. The chip as in claim 5 wherein said one or more solderable metal contact regions are approximately 1 μm thick.
- 20 9. A Lateral Discrete Power Semiconductor MosFET Comprising:

- (a) a semiconductor substrate;
- (b) at least one first doped region in said semiconductor substrate forming at least one source;
- (c) at least one second doped region in said semiconductor substrate forming at least one drain;
- 5 (d) a first connectivity layer at least one first runner and at least one second runner, wherein said at least one first runner is operatively connected to said at least one first doped region and said at least one second runner is operatively connected to said at least one second doped region.
- 10 (e) A second connectivity layer operatively connected to said first connectivity layer and having at least one third runner and at least one forth runner, wherein said at least one third runner is operatively connected to said at least one fourth runner is operatively connected to said at least one second runner.
- 15 (f) A third connectivity layer having at least one first pad operatively connected to said at least one third runner and at least one second pad operatively connected to said at least one fourth runner.

10. A semiconductor device of claim 9 wherein said at least one pad has at least one first copper pillar or one metal layer and said at least one first pad said at least one second pad arranged in a substantially checker board pattern.
11. A semiconductor device of claim 10 wherein said at least one first pad is interleaved with said at least one second pad.
12. A semiconductor device of claim 9 wherein said at least one first doped region is a source for transistor and said at least one second doped region is a drain for a transistor
13. A semiconductor device of claim 12 wherein said at least one source and at least one drain are laid out substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.
14. A semiconductor device of Claim 12 wherein said at least one source and at least one drain are laid out in substantially checkerboard pattern.
15. A Lateral discrete Power MosFET device comprising:
 - (a) semiconductor substrate
 - (b) at least one first doped region in said semiconductor substrate forming at least one source:
 - (c) at least one second doped region in said semiconductor substrate forming at least one drain:

(d) a first connectivity layer operatively connected to said first connectivity layer and operatively connected to said at least one second doped region.

16 A Lateral discrete power semiconductor device of claim 15 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer

5 17 A lateral discrete power semiconductor device of claim 16 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer and using a portion of said first conductivity layer for such connection.

10 18 A lateral discrete power semiconductor device of claim 15 having a third conductivity layer with at least one first pad and at least one second pad of such layer wherein said at least one first pad is operatively connected to said first connectivity and said at least one second pad is operatively connected to said second connectivity layer.

15 19 A Lateral discrete power semiconductor of claim 18 wherein said at least one first pad has at least one first copper pillar bump or copper direct attach or solder bump and at least one second pad has at least one second copper pillar bump or copper direct attach or solder bump.

20 A lateral discrete Power semiconductor of claim 19 wherein at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

21 A lateral discrete Power semiconductor of claim 19 wherein at least one first pad
5 is interleaved with said at least one second pad.

22 A lateral discrete Power Semiconductor of Claim 15 wherein said at least one source at least one drain are laid out in substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

23 lateral discrete Power Semiconductor of Claim 15 wherein said at least one source at least one drain are laid out in substantially checkerboard pattern
10

24 A Lateral discrete Power MosFET device comprising:

(a) semiconductor substrate

(b) at least one first doped region in said semiconductor substrate forming at least one source:

15 (c) at least one second doped region in said semiconductor substrate forming at least one drain:

(d) a first connectivity having at least one first runner operatively connected to said at least one first doped region and at least one second runner operatively connected to at least one second runner operatively connected to said at least one second doped region:

20

(e) a second connectivity layer having at least one first pad operatively connected to said at least one first runner and at least one second pad operatively connected to said at least one second runner.

25 A Lateral discrete Power MosFET of Claim 24 wherein said at least one copper

5 pillar bump or one copper direct die attach or one solder bump and said at least one second pad has at least one second copper pillar bump or copper direct die attach or one solder bump

26 A Lateral discrete Power MosFET of Claim 25 wherein said at least one first pad

and said at least one second pad are arranged in a substantially checkerboard pattern.

10

27 A Lateral discrete Power MosFET of Claim 25 wherein said at least one first pad is interleaved with said at least one second pad.

28 A Lateral discrete Power MosFET of Claim 24 wherein said at least one source

and at least one drain are laid out in substantially elongated shape and wherein

15

said at least one source are interleaved with said at least one drain.

29 A Lateral discrete Power MosFET of Claim 24 wherein said at least one source

and at least one drain are laid out in substantially checkerboard pattern

30 The combination of a Lateral discrete Power MosFET using source and drain

regions arranged in three metal system with the first metal that is in contact with

20

the silicon surface arranged in a checker board pattern, followed by two

additional striped metal structures to bring the source, drain and gates to the

corresponding copper pillar bumps. The Source and Drain Regions of the planar Mosfet are parallel stripes both with 90 degree angle between Metal 1 and Metal 2 and the third layer is 500um square pads.

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

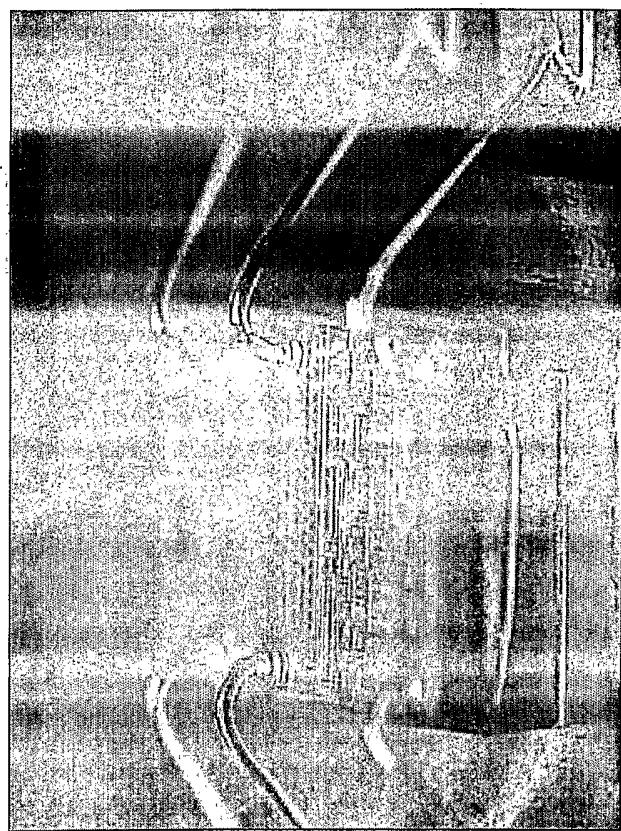


Figure 1. Example of Wire Bonding Used to Form the Electrical Connections to the Semiconductor Die

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

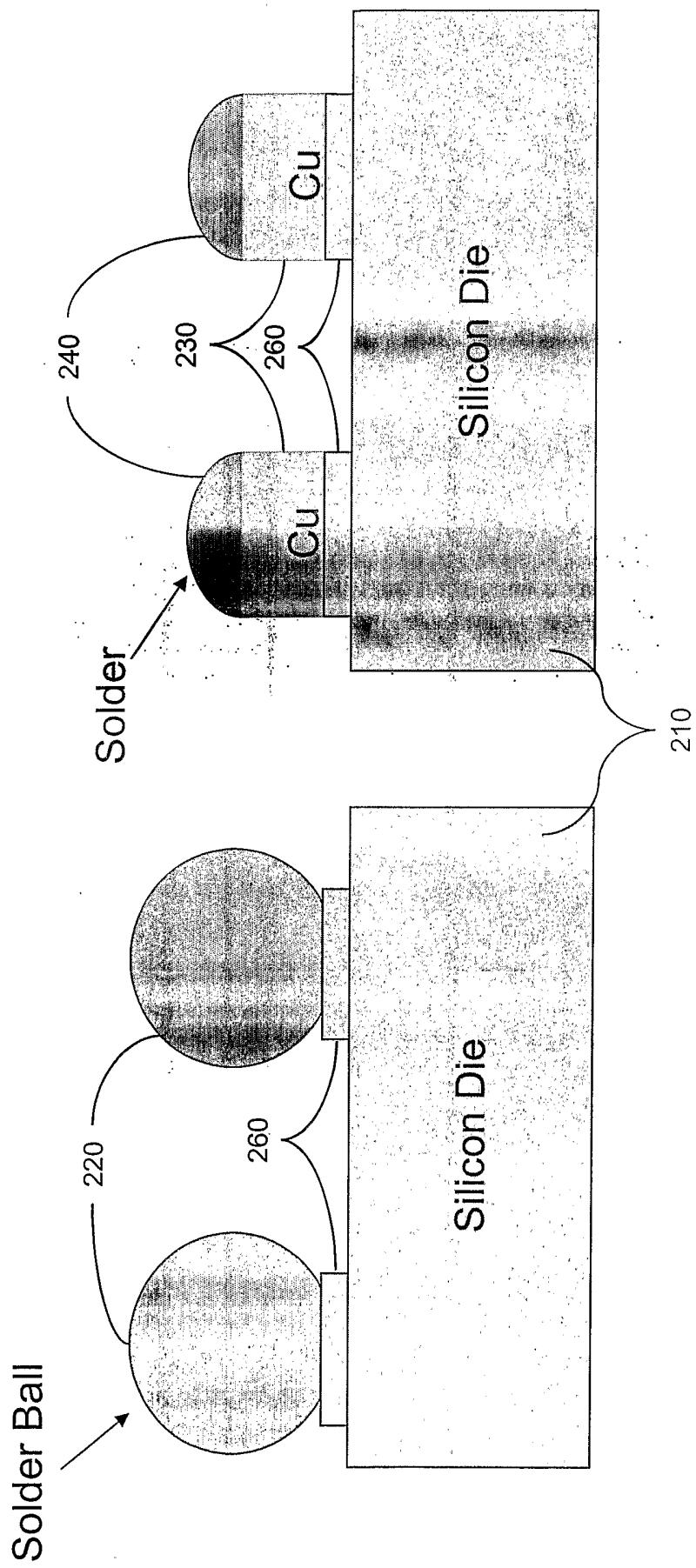
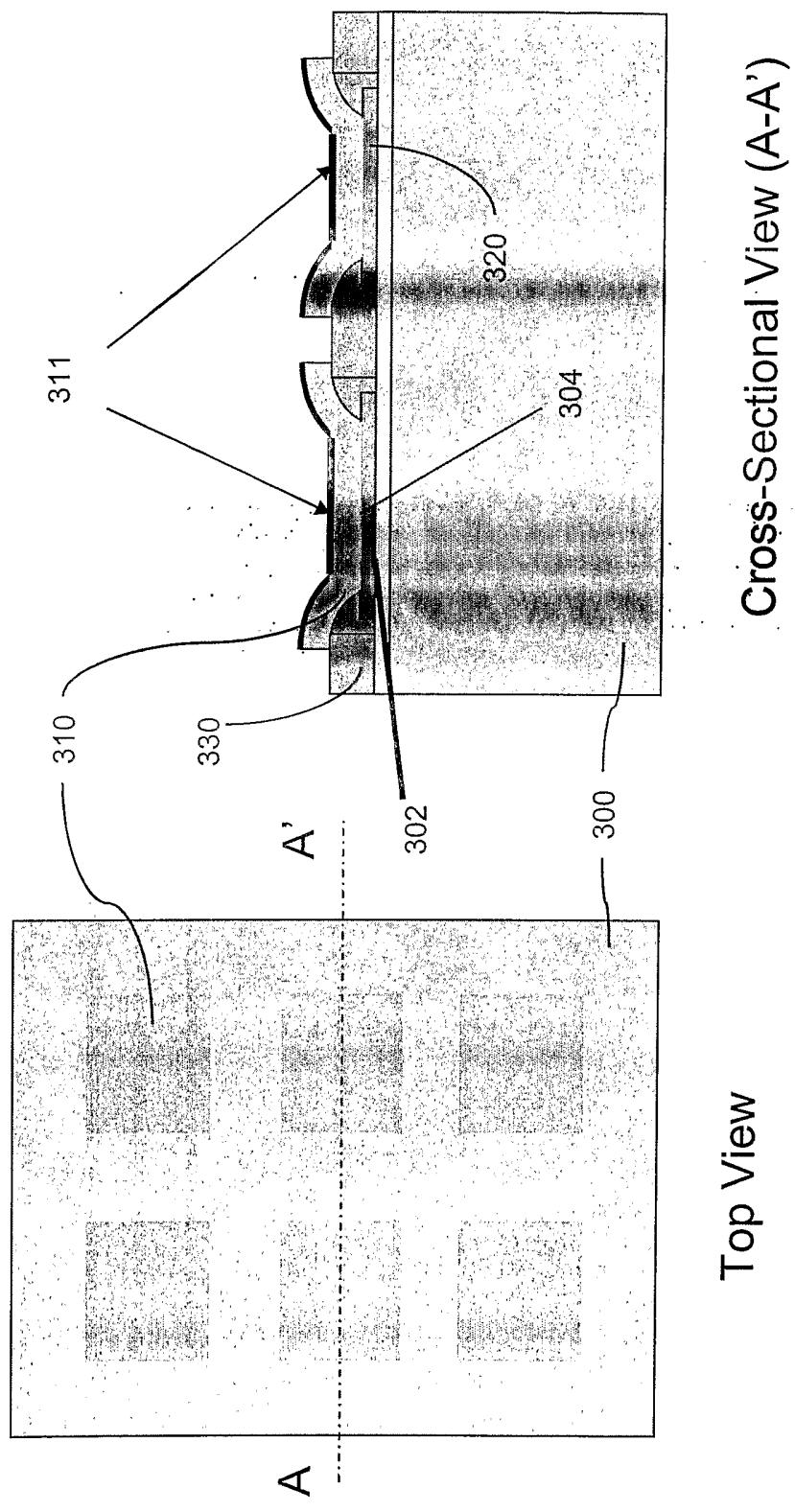


Figure 2. Typical Flip Chip Wafer Bumping Packages

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards



Top View

Cross-Sectional View (A-A')

Figure 3. Die with Solderable Metal Contacts for Direct Printed Circuit Board Mounting

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

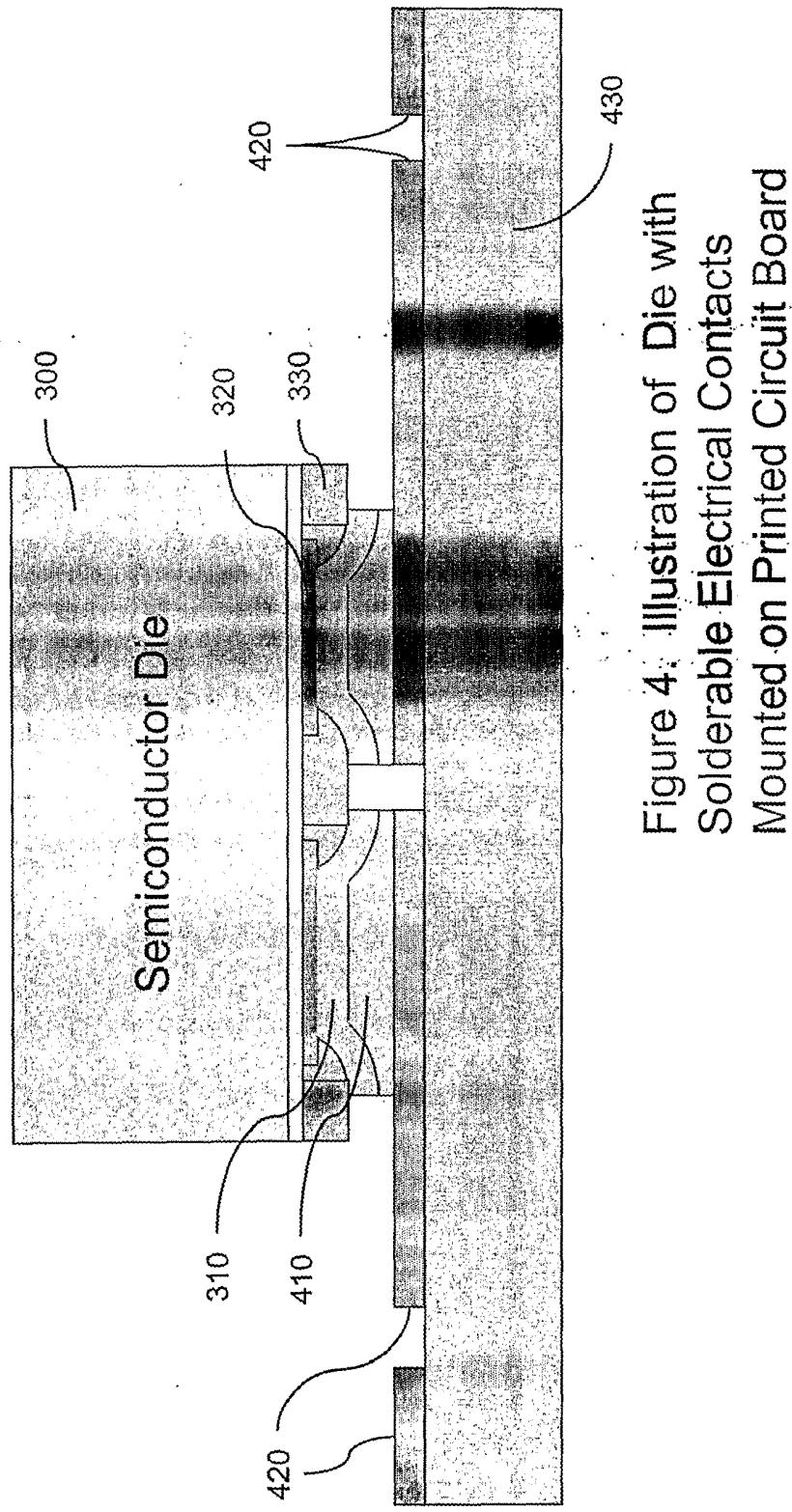


Figure 4: Illustration of Die with Solderable Electrical Contacts Mounted on Printed Circuit Board