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(54) **Title**: SILICON-OZONE CVD WITH REDUCED PATTERN LOADING USING INCUBATION PERIOD DEPOSITION

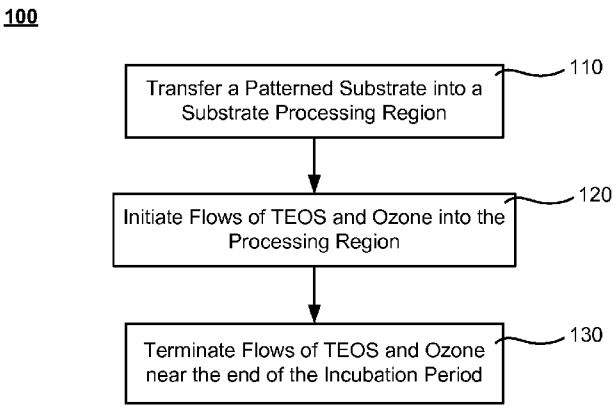


FIG. 1A

(57) **Abstract**: Aspects of the disclosure pertain to methods of depositing conformal silicon oxide layers on patterned substrates. In embodiments, dielectric layers are deposited by flowing a silicon-containing precursor and ozone into a processing chamber such that a relatively uniform dielectric growth rate is achieved across the patterned substrate surface having heterogeneous materials and/or a heterogeneous pattern density distribution. The deposition of dielectric layers grown according to embodiments may have a reduced dependence on underlying material and pattern density while still being suitable for non-sacrificial applications. Reduction in dependence on pattern density is achieved by terminating deposition near the end of an incubation period. Multiple deposition cycles may be conducted in series since the beneficial nature of the incubation period may repeat after a pause in deposition.

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SILICON-OZONE CVD WITH REDUCED PATTERN LOADING USING INCUBATION PERIOD DEPOSITION

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a PCT application of U.S. Patent Application No. 12/891,149 filed September 27, 2010, titled "SILICON-OZONE CVD WITH REDUCED PATTERN LOADING USING INCUBATION PERIOD DEPOSITION," and claims the benefit of U.S. Provisional Application No. 61/319,970 by Kweskin et al., filed April 1, 2010 and titled "SILICON-OZONE CVD WITH REDUCED PATTERN LOADING USING INCUBATION PERIOD DEPOSITION," which are incorporated herein in their entirety for all purposes.

FIELD

This application relates to manufacturing technology solutions involving equipment, processes, and materials used in the deposition, patterning, and treatment of thin-films and coatings, with representative examples including (but not limited to) applications involving: semiconductor and dielectric materials and devices, silicon-based wafers and flat panel displays (such as TFTs).

BACKGROUND OF THE INVENTION

Forming dielectric layers on a substrate by chemical reaction of gases is one of the primary steps in the fabrication of modern semiconductor devices. These deposition processes include chemical vapor deposition (CVD) as well as plasma enhanced chemical vapor deposition (PECVD), which uses plasma in combination with traditional CVD techniques.

CVD and PECVD dielectric layers can be used as different layers in semiconductor devices. For example, the dielectric layers may be used as intermetal dielectric layers between conductive lines or interconnects in a device. Alternatively, the dielectric layers may be used as barrier layers, etch stops, or spacers, as well as other layers.

Dielectric layers that are used for applications such as barrier layers and spacers are typically deposited over features, e.g., horizontal interconnects for subsequently formed lines, vertical interconnects (vias), gate stacks, etc., in a patterned substrate. Preferably, the

deposition provides a conformal layer. However, it is often difficult to achieve conformal deposition.

For example, it is difficult to deposit a barrier layer over a feature with few or no resulting surface defects or feature deformation. During deposition, the barrier layer material may overloaf, that is, deposit excess material on the shoulders of a via and deposit too little material in the base of the via, forming a shape that looks like the side of a loaf of bread. The phenomena is also known as footing because the base of the via has a profile that looks like a foot. In extreme cases, the shoulders of a via may merge to form a joined, sealed surface across the top of the via. The film thickness non-uniformity across the wafer can negatively impact the drive current improvement from one device to another. Modulating the process parameters alone does not significantly improve the step coverage and pattern loading problems.

Deposition of conformal layers over gate stacks to provide layers that are subsequently etched to form spacers is also challenging. While methods of depositing silicon nitride and silicon oxide layers for spacers using high temperature, low pressure conventional CVD have been developed, the thermal budget for such techniques is becoming too high as semiconductor device geometry continues to shrink. PECVD processes of silicon nitride and silicon oxide deposition can be performed at lower temperatures, but the step coverage and pattern loading results are not as desirable as those obtained with high temperature, low pressure CVD.

Therefore, a need exists for method of depositing conformal films over formed features in a patterned substrate.

BRIEF SUMMARY OF THE INVENTION

Aspects of the disclosure pertain to methods of depositing conformal silicon oxide layers on patterned substrates. In embodiments, dielectric layers are deposited by flowing a silicon-containing precursor and ozone into a processing chamber such that a relatively uniform dielectric growth rate is achieved across the patterned substrate surface having heterogeneous materials and/or a heterogeneous pattern density distribution. The deposition of dielectric layers grown according to embodiments may have a reduced dependence on underlying material and pattern density while still being suitable for non-sacrificial applications. Reduction in dependence on pattern density is achieved by terminating deposition near the end of an incubation period. Multiple deposition cycles may be

conducted in series since the beneficial nature of the incubation period may repeat after a pause in deposition.

Embodiments of the invention include methods for forming a conformal silicon oxide layer on a patterned substrate in a substrate processing region in a processing chamber. The methods include a step of depositing a layer of silicon oxide during an incubation period. The step includes initiating flows of a silicon-containing precursor and ozone (O_3) into the substrate processing region, and terminating the flows of the silicon-containing precursor and ozone near the end of the incubation period to avoid the formation of a nonconformal layer of silicon oxide.

Additional embodiments and features are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the disclosed embodiments. The features and advantages of the disclosed embodiments may be realized and attained by means of the instrumentalities, combinations, and methods described in the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

A further understanding of the nature and advantages of the disclosed embodiments may be realized by reference to the remaining portions of the specification and the drawings.

FIG. 1A-1B are flow charts of a conformal silicon oxide deposition process according to disclosed embodiments.

FIG. 2A is a graph of silicon oxide growth rates according to embodiments of the invention.

FIG. 2B is a graph of silicon oxide growth rate selectivity according to embodiments of the invention.

FIG. 3 shows a substrate processing system according to embodiments of the invention.

FIG. 4A shows is a cross-sectional view of a semiconductor processing chamber according to embodiments of the present invention;

FIG. 4B shows a cross-sectional view of a gas panel and supply lines in relation to a processing chamber.

DETAILED DESCRIPTION OF THE INVENTION

Aspects of the disclosure pertain to methods of depositing conformal silicon oxide layers on patterned substrates. In embodiments, dielectric layers are deposited by flowing a silicon-containing precursor and ozone into a processing chamber such that a relatively uniform dielectric growth rate is achieved across the patterned substrate surface having heterogeneous materials and/or a heterogeneous pattern density distribution. The deposition of dielectric layers grown according to embodiments may have a reduced dependence on underlying material and pattern density while still being suitable for non-sacrificial applications. Reduction in dependence on pattern density is achieved by terminating deposition near the end of an incubation period. Multiple deposition cycles may be conducted in series since the beneficial nature of the incubation period may repeat after a pause in deposition.

Embodiments of the invention are directed to methods of forming silicon oxide on a patterned surface of a substrate. Sub-atmospheric CVD (SACVD) and related processes involve flowing a silicon-containing precursor and an oxidizing precursor into a processing chamber to form silicon oxide on the substrate. The silicon-containing precursor may include TEOS and the oxidizing precursor may include ozone (O_3), oxygen (O_2) and/or oxygen radicals. The inventors have discovered that growing thin films within the incubation period of the process reduces the pattern-loading effect (PLE) of the deposited silicon oxide.

Without binding the claim coverage to hypothetical mechanisms, it is believed that a non-conformal film may initially be created early during the incubation period. Later in the incubation period, the thin portions of the film are thought to experience more rapid growth rates while the thicker portions of the film support less rapid growth rates. The effect is to even out the film thickness across the wafer and between different patterned structures. The inventors have also found that the growth rates during the incubation period are less selective, meaning the film growth rate is more similar from one material to another during the period. The non-selectivity helps to further improve conformality across the wafer and between different patterned structures.

In order to better understand and appreciate the invention, reference is now made to FIGS. 1A-1B which are flow charts of a conformal silicon oxide deposition process according to disclosed embodiments. Properties of silicon oxide growth rates under various

circumstances are shown in FIGS. 2A-2B to enhance the understanding of the silicon oxide deposition process. The process 100 in FIG 1A begins when a patterned substrate is transferred into a substrate processing region (operation 110). TEOS and ozone flows are initiated into the region in operation 120 and a conformal layer of silicon oxide is formed between operation 120 and operation 130. The flows of both ozone and TEOS and ozone are terminated in operation 130. FIG 2A shows how the growth rate remains comparable during the period of deposition represented in FIG. 1A. The silicon oxide deposition growth rate accelerates after the incubation period on exposed regions of silicon compared to exposed regions of silicon oxide. The vertical dashed line roughly indicates the point when the conformal deposition ends and the selective deposition begins in this exemplary embodiment.

Generally speaking, the flows of ozone and TEOS do not need to be initiated simultaneously nor do they have to be terminated simultaneously. The flow of TEOS is generally effected by flowing a carrier gas (e.g. N_2) through liquid TEOS such that the delivery rate of TEOS into the substrate processing region is above one of 1 g/min, 2 g/min or 3 g/min, in different embodiments. Both the carrier gas and the TEOS enter the substrate processing region. The flow of ozone is delivered along with more stable molecular oxygen. The flow rate of the ozone portion of that flow is above one of 1 slm, 2 slm, 3 slm, 5 slm or 10 slm, in different embodiments.

Typically, the initiation of the TEOS and ozone flows (operation 120) is followed by a period of slow growth and then a period of more rapid growth as represented in FIG. 2A. The process sequence shown in FIG. 1A interrupts (operation 130) the typical growth pattern near the transition from slow growth to rapid growth. If the typical growth pattern were interrupted earlier in the incubation period or too long after the transition to rapid growth, the conformality of the silicon oxide film would be reduced. An average deposition rate for each region may be defined by using the slope of a line drawn between the start and finish points on a plot of the deposited thickness vs. the time since initial deposition. In the case of the rapid growth, the line must be drawn between the transition start point and an extrapolated finish point to avoid underreporting the deposition rate. The location of operation 130 along the time axis is somewhat flexible while still offering the benefits of conformality. The period of slow growth before operation 130 will be referred to as the incubation period herein. One may wish to adjust the location of operation 130 in order to tune a total deposition thickness. The deposition rate during the incubation period may

exceed the deposition rate after the incubation period by a multiplicative factor of one of 1.3, 1.5, 1.7, 2.0, 2.5 or 3.0, in different embodiments. The deposition rate of silicon oxide between operation 120 and operation 130 may be greater than 50Å, 70Å, 80Å, 90Å, 100Å or 110Å, in different embodiments. The thickness of the conformal silicon oxide layer grown over one material (e.g. thermal silicon oxide) may be within one of 30%, 25%, 20%, 15%, 10% and 5% of the thickness of the conformal silicon oxide layer grown over another material (e.g. silicon), in embodiments of the invention.

Flow rates, as used herein, are not necessarily constant during the process. Flow rates of the different precursors may be initiated and terminated in different orders and their magnitudes may be varied. Unless otherwise indicated, mass flow rate magnitudes indicated herein are given for the approximate peak flow rate used during the process. Flow rate magnitudes indicated herein are for deposition on one side of a pair of 300 mm diameter wafers (area approximately 1400 cm^2). Appropriate correction based on deposition area is needed for a different number of wafers, larger or smaller wafers, double sided deposition or deposition on alternative geometry substrates (e.g. rectangular substrates).

The pressure in the substrate processing region are typical of many SACVD and HARP processes (e.g. 600 Torr). The pressure during the formation of the conformal silicon oxide film may be greater than one of 350 Torr, 400 Torr, 450 Torr, 500 Torr or 550 Torr, in different embodiments, to ensure desirable growth rates during the incubation period. Despite the name and acronym for the related process, sub-atmospheric chemical vapor deposition (SACVD), it should be noted that the processes described herein may be performed at pressures higher than atmospheric pressure (typically 760 Torr).

The substrate temperature is below a threshold value, in embodiments, also to stay within tight thermal budgets and to ensure that the deposition process possesses an incubation period. The temperature of the substrate during the deposition of the conformal silicon oxide is below one of 540°C, 500°C, 450°C, 400°C and 350°C, in different embodiments. No plasma is present in the substrate processing region in embodiments. A small ac and/or dc voltage may be applied to the substrate processing region without detriment to the benefits of the deposition process, according to embodiments. Such an excitation should not be considered to deviate from the scope of "essentially" plasma-free or a process having "essentially" no plasma as may be recited in some claims.

FIG. 1B shows a repeated deposition of the process sequence described with reference to FIG. 1A. FIG. 2B shows the dependence of silicon oxide growth selectivity as a function of silicon oxide film thickness and incubation deposition cycle. The process 150 begins when a when a patterned substrate is transferred into a substrate processing region (operation 160). TEOS and ozone flows are initiated then terminated near the end of the incubation period as described previously. The initiation, film growth and termination of the flows occur within operation 170 in FIG. 1B. If the target thickness has been achieved, no additional cycles are performed and the patterned substrate may be removed from the substrate processing region (operation 180). However, if a larger film thickness is desired, the flows of TEOS and ozone may be started again which will result in another incubation period. The second incubation period may last for a shorter period of time than the first but will again segue into a period of more selective growth after an incubation period. The flows of TEOS and ozone are terminated near the transition from slow to rapid growth on exposed silicon surfaces. The process may even repeat more than two times if additional film thickness is required. FIG. 2B shows that the selectivity becomes even more conformal during subsequent cycles and stays more conformal for larger film thicknesses. This provides an additional benefit when conformal deposition is desired. Deposition sequences have been explored including six incubation cycles and resulted in conformal films nearly 600Å thick. The flexibility provided by choosing a number for the multiple cycles in combination with adjusting the timing of the termination of one or both of the TEOS and ozone flows allows flexibility for achieving a desired silicon oxide film thickness. The thickness of the secondary layers described with reference to FIG. 1B may be greater than the same lower limits described with reference to the layer grown and described with reference to FIG. 1A.

The pattern loading was quantified by comparing the horizontal growth of the conformal silicon oxide layer from a vertical feature in a sparsely patterned region and a densely patterned region. An exemplary densely patterned region may have greater number of features than a sparsely patterned region to create the greater exposed surface area within a same area viewed from above the patterned substrate. A densely patterned region may have an exposed vertical area greater than a sparsely patterned region by a factor greater than one of 2, 3, 5, 10 or 20, in different embodiments. The thickness of the conformal silicon oxide layer in a densely patterned region may be within one of 30%, 25%, 20%, 15%, 10% and 5% of the thickness of the conformal silicon oxide layer in a sparsely patterned region, in

different embodiments. The thickness in each region may be measured on vertical surfaces in which case the growth is in a horizontal direction. Alternatively, the thickness may be measured on a horizontal surface within each region and the growth may then be in the vertical direction. The terms "vertical" and "horizontal" are used throughout to include substantially vertical and substantially horizontal directions which may or may not deviate from the theoretical vertical and horizontal by up to about 10 degrees.

Exemplary Substrate Processing System

Deposition chambers that may implement embodiments of the present invention may include sub-atmospheric chemical vapor deposition (SACVD) chambers and more generally, deposition chambers which allow operation at relatively high pressures without necessarily applying plasma excitation. Specific examples of CVD systems that may implement embodiments of the invention include the CENTURA ULTIMA® SACVD chambers/systems, and PRODUCER® HARP, eHARP and SACVD chambers/systems, available from Applied Materials, Inc. of Santa Clara, Calif.

Embodiments of the deposition systems may be incorporated into larger fabrication systems for producing integrated circuit chips. FIG. 4 shows one such system 200 of deposition, baking and curing chambers according to disclosed embodiments. In the figure, a pair of FOUPs (front opening unified pods) 202 supply substrate substrates (e.g., 300 mm diameter wafers) that are received by robotic arms 204 and placed into a low pressure holding area 206 before being placed into one of the wafer processing chambers 208a-f. A second robotic arm 210 may be used to transport the substrate wafers from the holding area 206 to the processing chambers 208a-f and back.

The processing chambers 208a-f may include one or more system components for depositing, annealing, curing and/or etching a flowable dielectric film on the substrate wafer. In one configuration, two pairs of the processing chamber (e.g., 208c-d and 208e-f) may be used to deposit the flowable dielectric material on the substrate, and the third pair of processing chambers (e.g., 208a-b) may be used to anneal the deposited dielectic. In another configuration, the same two pairs of processing chambers (e.g., 208c-d and 208e-f) may be configured to both deposit and anneal a flowable dielectric film on the substrate, while the third pair of chambers (e.g., 208a-b) may be used for UV or E-beam curing of the deposited film. In still another configuration, all three pairs of chambers (e.g., 208a-f) may be configured to deposit and cure a flowable dielectric film on the substrate. In yet another

configuration, two pairs of processing chambers (e.g., 208c-d and 208e-f) may be used for both deposition and UV or E-beam curing of the flowable dielectric, while a third pair of processing chambers (e.g. 208a-b) may be used for annealing the dielectric film. Any one or more of the processes described may be carried out on chamber(s) separated from the fabrication system shown in different embodiments.

FIG. 4A shows a simplified representation of an exemplary semiconductor processing chamber within a semiconductor processing tool 200. This exemplary chamber 410 is suitable for performing a variety of semiconductor processing steps which may include CVD processes, as well as other processes, such as reflow, drive-in, cleaning, etching, and gettering processes. Multiple-step processes can also be performed on a single substrate without removing the substrate from the chamber. Representative major components of the system include a chamber interior 415 that receives process and other gases from a gas delivery system 489, pumping system 488, a remote plasma system (RPS) 455, and a control system 453. These and other components are described below in order to understand the present invention.

The semiconductor processing chamber 410 includes an enclosure assembly 412 housing a chamber interior 415 with a gas reaction area 416. A gas distribution plate 420 is provided above the gas reaction area 416 for dispersing reactive gases and other gases, such as purge gases, through perforated holes in the gas distribution plate 420 to a substrate (not shown) that rests on a vertically movable heater 425 (which may also be referred to as a substrate support pedestal). The heater 425 can be controllably moved between a lower position, where a substrate can be loaded or unloaded, for example, and a processing position closely adjacent to the gas distribution plate 420, indicated by a dashed line 413, or to other positions for other purposes, such as for an etch or cleaning process. A center board (not shown) includes sensors for providing information on the position of the substrate.

Gas distribution plate 420 may be of the variety described in U.S. Patent No. 6,793,733. These plates improve the uniformity of gas disbursement at the substrate and are particularly advantageous in deposition processes that vary gas concentration ratios. In some examples, the plates work in combination with the vertically movable heater 425 (or movable substrate support pedestal) such that deposition gases are released farther from the substrate when the ratio is heavily skewed in one direction (e.g., when the concentration of a silicon-containing gas is small compared to the concentration of an oxidizer-containing

gas) and are released closer to the substrate as the concentration changes (e.g., when the concentration of silicon-containing gas in the mixture is higher). In other examples, the orifices of the gas distribution plate are designed to provide more uniform mixing of the gases.

The heater 425 includes an electrically resistive heating element (not shown) enclosed in a ceramic. The ceramic protects the heating element from potentially corrosive chamber environments and allows the heater to attain temperatures up to about 800°C. In an exemplary embodiment, all surfaces of the heater 425 exposed within the chamber interior 415 are made of a ceramic material, such as aluminum oxide (Al_2O_3 or alumina) or aluminum nitride.

Reactive and carrier gases are supplied through inlet tube 443 into a gas mixing box (also called a gas mixing block) 427, where they are preferably mixed together and delivered to the gas distribution plate 420. The gas mixing block 427 is preferably a dual input mixing block coupled to inlet tube 443 and to a cleaning/etch gas conduit 447. A valve 428 operates to admit or seal gas or plasma from conduit 447 to the gas mixing block 427. Conduit 447 receives gases from an RPS 455, which has an inlet 457 for receiving input gases. During deposition processing, gas supplied to the plate 420 is vented toward the substrate surface (as indicated by arrows 421), where it may be uniformly distributed radially across the substrate surface, typically in a laminar flow.

Purging gas may be delivered into the chamber interior 415 through the plate 420 and/or an inlet port or tube (not shown) through a wall (preferably the bottom) of enclosure assembly 412. The purging gas flows upward from the inlet port past the heater 425 and to an annular pumping channel 440 and may be useful to purge the chamber, for example, of ozone and TEOS between incubation period depositions. An exhaust system then exhausts the gas (as indicated by arrow 422) into the annular pumping channel 440 and through an exhaust line 460 to a pumping system 488, which includes one or more vacuum pumps. Exhaust gases and entrained particles are drawn from the annular pumping channel 440 through the exhaust line 460 at a rate controlled by a throttle valve system 463.

The RPS 455 can produce a plasma for selected applications, such as chamber cleaning or etching native oxide or residue from a process substrate. Plasma species produced in the remote plasma system 455 from precursors supplied via the input line 457 are sent via conduit 447 for dispersion through the plate 420 to the gas reaction area 416. Precursor

gases for a cleaning application may include fluorine, chlorine, and other reactive elements. The RPS 455 also may be adapted to deposit plasma enhanced CVD films by selecting appropriate deposition precursor gases for use in the RPS 455.

The system controller 453 controls activities and operating parameters of the deposition system. The processor 451 executes system control software, such as a computer program stored in a memory 452 coupled to the processor 451. The memory 452 typically consists of a combination of static random access memories (cache), dynamic random access memories (DRAM) and hard disk drives but of course the memory 452 may also consist of other kinds of memory, such as solid-state memory devices. In addition to these memory means the semiconductor processing chamber 410 in a preferred embodiment includes a removable storage media drive, USB ports and a card rack (not shown).

The processor 451 operates according to system control software programmed to operate the device according to the methods disclosed herein. For example, sets of instructions may dictate the timing, mixture of gases, chamber pressure, chamber temperature, plasma power levels, susceptor position, and other parameters for carrying out one or more incubation period depositions in a sequence. The instructions are conveyed to the appropriate hardware preferably through direct cabling carrying analog or digital signals conveying signals originating from an input-output I/O module 450. Other computer programs such as those stored on other memory including, for example, a USB thumb drive, a floppy disk or another computer program product inserted in a disk drive or other appropriate drive, may also be used to operate the processor 451 to configure the semiconductor processing chamber 410 for varied uses.

The processor 451 may have a card rack (not shown) that contains a single-board computer, analog and digital input/output boards, interface boards and stepper motor controller boards. Various parts of the semiconductor processing system 200 conform to the Versa Modular European (VME) standard which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data bus and 24-bit address bus.

A process for depositing a conformal silicon oxide layer on a patterned substrate or a process for cleaning a chamber can be implemented using a computer program product that is executed by the system controller. The computer program code can be written in any conventional computer readable programming language: for example, 68000 assembly

language, C, C++, Pascal, Fortran or others. Suitable program code is entered into a single file, or multiple files, using a conventional text editor, and stored or embodied in a computer usable medium, such as a memory system of the computer. If the entered code text is in a high level language, the code is compiled, and the resultant compiler code is then linked with an object code of precompiled Microsoft Windows® library routines. To execute the linked, compiled object code the system user invokes the object code, causing the computer system to load the code in memory. The CPU then reads and executes the code to perform the tasks identified in the program.

The interface between a user and the controller is via a flat-panel touch-sensitive monitor. In the preferred embodiment two monitors are used, one mounted in the clean room wall for the operators and the other behind the wall for the service technicians. The two monitors may simultaneously display the same information, in which case only one accepts input at a time. To select a particular screen or function, the operator touches a designated area of the touch-sensitive monitor. The touched area changes its highlighted color, or a new menu or screen is displayed, confirming communication between the operator and the touch-sensitive monitor. Other devices, such as a keyboard, mouse, or other pointing or communication device, may be used instead of or in addition to the touch-sensitive monitor to allow the user to communicate with the system controller.

The embodiment disclosed herein relies on direct cabling and a single processor 451. Alternative embodiments comprising multi-core processors, multiple processors under distributed control and wireless communication between the system controller and controlled objects are also possible.

Fig. 4B shows a simplified representation of a gas supply panel 480 in relation to semiconductor processing chamber 410. As discussed above, the portion of semiconductor processing system 200 shown includes semiconductor processing chamber 410 with a heater 425, a gas mixing box 427 with inputs from inlet tube 443 and conduit 447, and RPS 455 with input line 457. As mentioned above, the gas mixing box 427 is configured for mixing and injecting deposition gas(es) and cleaning gas(es) or other gas(es) through inlet tube 443 and the input line 457 to the chamber interior 415.

The RPS 455 is integrally located and mounted below the processing chamber 410 with conduit 447 coming up alongside the chamber 410 to the gate valve 428 and the gas mixing box 427, located above the chamber 410. Plasma power generator 411 and ozonator 459 are

located remote from the clean room. Delivery lines 483 and 485 from the gas supply panel 480 provide reactive gases to inlet tube 443. The gas supply panel 480 includes lines from gas or liquid sources 490 that provide the process gases for the selected application. The gas supply panel 480 has mixing system 493 that mixes selected gases before flow to the gas mixing box 427. In some embodiments, mixing system 493 includes a liquid injection system for vaporizing one or more reactant liquids such as tetraethylorthosilicate ("TEOS"), triethylborate ("TEB"), and triethylphosphate ("TEPO"). Vapor from the liquids is usually combined with a carrier gas, such as helium. Supply lines for the process gases may include (i) shut-off valves 495 that can be used to automatically or manually shut off the flow of process gas into line 485 or line 457, and (ii) liquid flow meters (LFM) 401 or other types of controllers that measure the flow of gas or liquid through the supply lines.

As an example, a mixture including TEOS as a silicon source may be used with mixing system 493 in a deposition process for forming a silicon oxide film during an incubation period. Sources of dopants such as phosphorous and boron may include TEPO and TEB which may also be introduced to mixing system 493. Precursors delivered to mixing system 493 may be liquid at room temperature and pressure and may be vaporized by conventional boiler-type or bubbler-type hot boxes. Alternatively, a liquid injection system may be used and offers greater control of the volume of reactant liquid introduced into the gas mixing system. The liquid is typically injected as a fine spray or mist into the carrier gas flow before being delivered to a heated gas delivery line 485 to the gas mixing block and chamber. Oxygen (O_2) and ozone (O_3) flow to the chamber through another gas delivery line 483, to be combined with the reactant gases from heated gas delivery line 485 near or in the chamber. Of course, it is recognized that other sources of dopants, silicon, oxygen and additive precursors may also be used. Though shown as an individual gas distribution line, line 485 may actually comprise multiple lines separated to discourage inter-precursor reactions before the precursors are flowed into chamber interior 415.

As used herein "substrate" may be a support substrate with or without layers formed thereon. The support substrate may be an insulator or a semiconductor of a variety of doping concentrations and profiles and may, for example, be a semiconductor substrate of the type used in the manufacture of integrated circuits. A layer of "silicon oxide" may include minority concentrations of other elemental constituents such as nitrogen, hydrogen, carbon and the like. A gas may be a combination of two or more gases. The terms trench and gap are used throughout with no implication that the etched geometry necessarily has a

large horizontal aspect ratio. Viewed from above the surface, gaps may appear circular, oval, polygonal, rectangular, or a variety of other shapes. Gaps may also be a region between two pillars in which case the gaps are not physical separate from other gaps. As used herein, a conformal layer refers to a generally uniform layer of material on a surface in the same shape as the surface, i.e., the surface of the layer and the surface being covered are generally parallel. A person having ordinary skill in the art will recognize that the deposited material likely cannot be 100% conformal and thus the term "generally" allows for acceptable tolerances.

Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the disclosed embodiments. Additionally, a number of well known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention.

Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Each smaller range between any stated value or intervening value in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of these smaller ranges may independently be included or excluded in the range, and each range where either, neither or both limits are included in the smaller ranges is also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

As used herein and in the appended claims, the singular forms "a", "an", and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a process" includes a plurality of such processes and reference to "the dielectric material" includes reference to one or more dielectric materials and equivalents thereof known to those skilled in the art, and so forth.

Also, the words "comprise," "comprising," "include," "including," and "includes" when used in this specification and in the following claims are intended to specify the presence of

stated features, integers, components, or steps, but they do not preclude the presence or addition of one or more other features, integers, components, steps, acts, or groups.

WHAT IS CLAIMED IS:

1. A method for forming a conformal silicon oxide layer on a patterned substrate in a substrate processing region in a processing chamber, the method comprising:

a step of depositing a layer of silicon oxide during an incubation period comprising:

initiating flows of a silicon-containing precursor and ozone (O_3) into the substrate processing region, and

terminating the flows of the silicon-containing precursor and ozone near the end of the incubation period to avoid the formation of a nonconformal layer of silicon oxide.

2. The method of claim 1 wherein the patterned substrate has a densely patterned region and a sparsely patterned region and the flows of the silicon-containing precursor and the ozone are terminated such that a thickness of the conformal silicon oxide layer in the densely patterned region is within a conformality percentage of a thickness in the sparsely patterned region.

3. The method of claims 2 wherein the conformality percentage is 30%.

4. The method of claim 1 wherein the patterned substrate has a first exposed material and a second exposed material and the flows of the silicon-containing precursor and the ozone are terminated such that a thickness of the conformal silicon oxide layer deposited on the first exposed material is within a conformality percentage of a thickness deposited on the second exposed material.

5. The method of claims 4 wherein the conformality percentage is 30%.

6. The method of claim 1 wherein the layer of silicon oxide is not conformal at an earlier time during the incubation period but becomes conformal near the end of the incubation period.

7. The method of claim 1 further comprising an additional step of depositing an additional layer of silicon oxide during an additional incubation period.

8. The method of claim 1 wherein a deposition rate during the incubation period is similar on any two of silicon, silicon oxide and silicon nitride.

9. The method of claim 1 wherein a deposition rate on silicon after the incubation period is greater than during the incubation period by a multiplicative factor of 1.3.

10. The method of claim 1 wherein the step of depositing a layer of silicon oxide during an incubation period further comprises flowing water vapor.

11. The method of claim 7 wherein a duration of the additional incubation period is less than a duration of the incubation period.

12. The method of claim 1 wherein terminating the flows of the silicon-containing precursor and ozone near the end of the incubation period comprising terminating the flows of the silicon-containing precursor and ozone at a time selected to achieve a predetermined thickness for the conformal silicon oxide layer.

13. The method of claim 2 wherein an average exposed substantially-vertical area in the densely patterned region exceeds that of the sparsely patterned region by a multiplicative factor of 2.

14. The method of claim 2 wherein the two thicknesses of the conformal silicon oxide layer in the densely and sparsely patterned regions are measured on a substantially-vertical surface of the patterned substrate.

15. The method of claim 2 wherein the two thicknesses of the conformal silicon oxide layer in the densely and sparsely patterned regions are measured on a substantially-horizontal surface of the patterned substrate.

16. The method of claim 1 wherein essentially no plasma is applied to the substrate processing region.

17. The method of claim 1 further comprising the operation of flowing a carrier gas which carries the silicon-containing precursor into the substrate processing region.

18. The method of claim 1 wherein the silicon-containing precursor comprises TEOS.

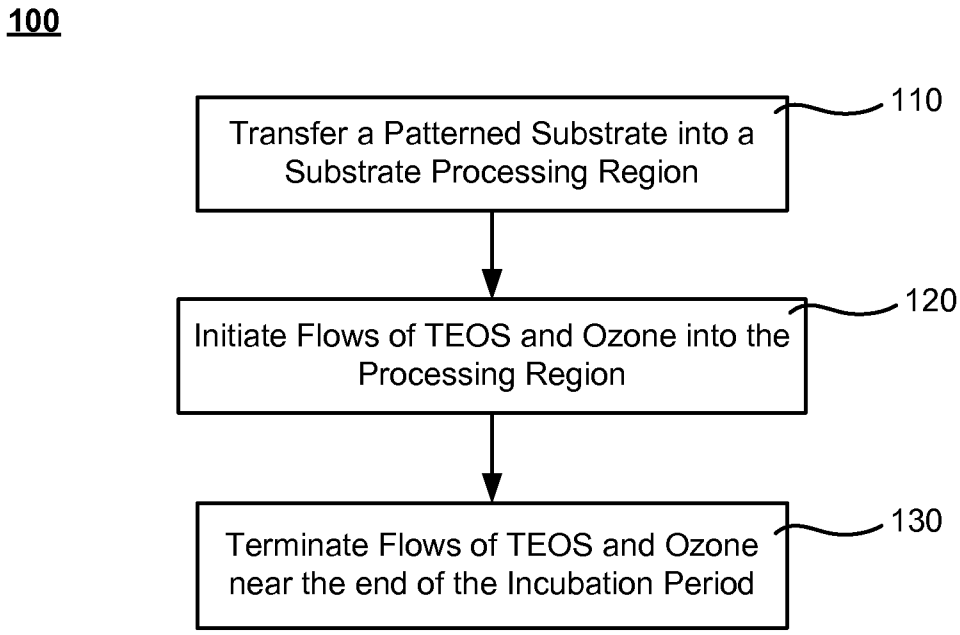

100
Transfer a Patterned Substrate into a Substrate Processing Region
110
Initiate Flows of TEOS and Ozone into the Processing Region
120
Terminate Flows of TEOS and Ozone near the end of the Incubation Period
130

FIG. 1A

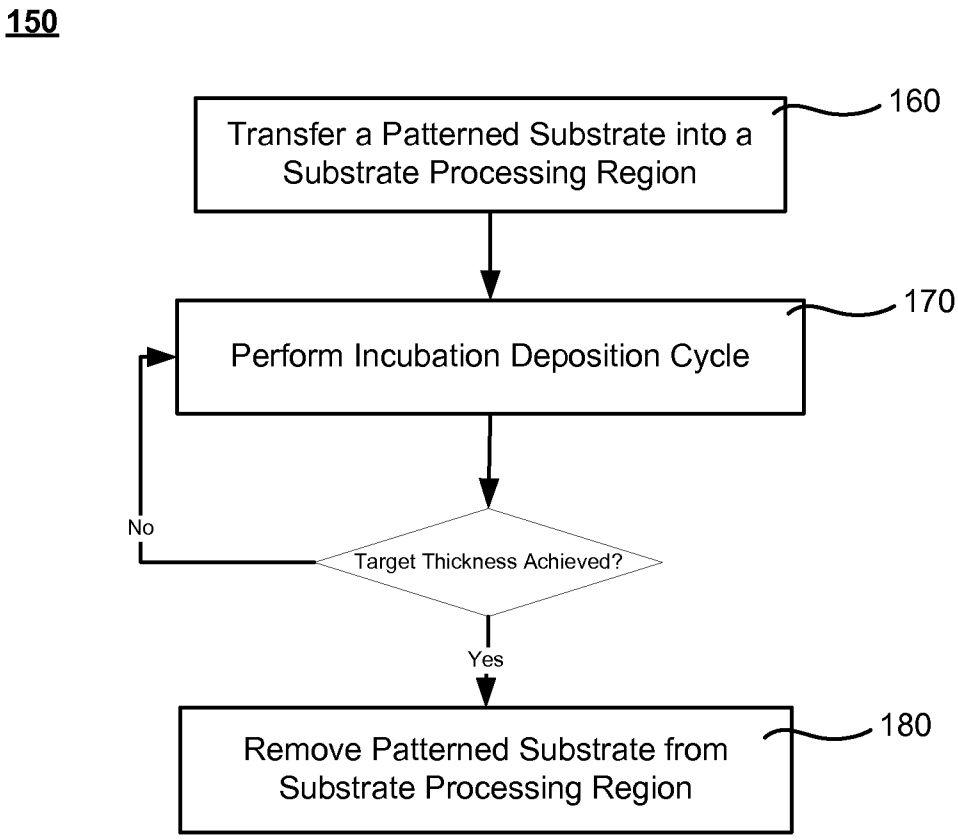

150
Transfer a Patterned Substrate into a Substrate Processing Region
160
Perform Incubation Deposition Cycle
170
No
Target Thickness Achieved?
Yes
Remove Patterned Substrate from Substrate Processing Region
180

FIG. 1B

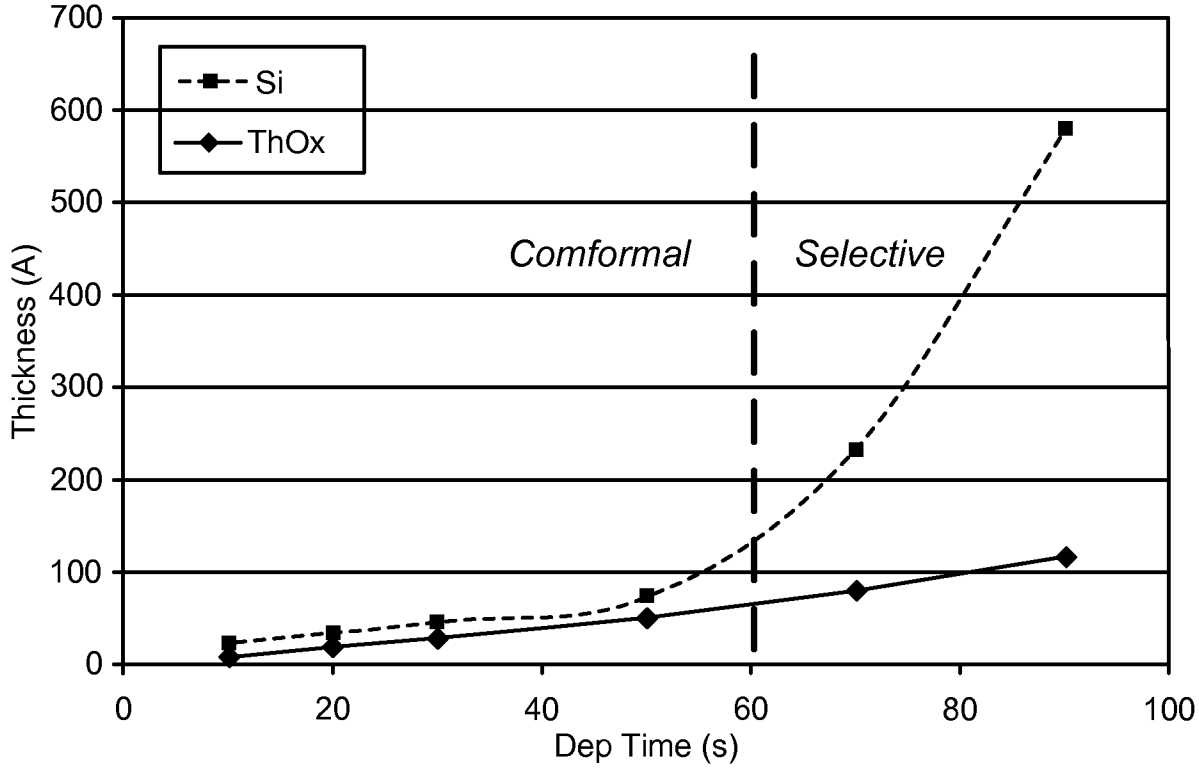

Si
ThOx
Comformal
Selective
Thickness (A)
Dep Time (s)
0
100
200
300
400
500
600
700
0
20
40
60
80
100

FIG. 2A

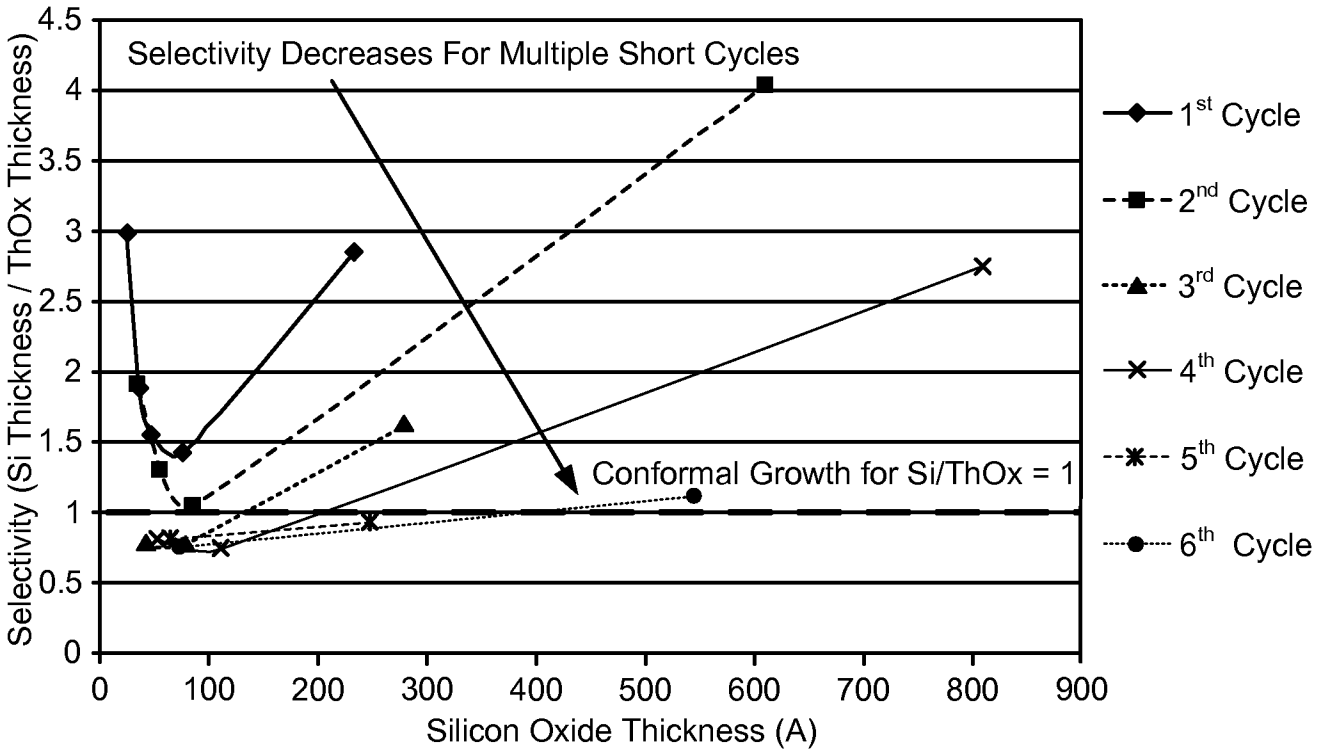

Selectivity Decreases For Multiple Short Cycles
Conformal Growth for Si/ThOx = 1
Selectivity (Si Thickness / ThOx Thickness)
Silicon Oxide Thickness (A)
1st Cycle
2nd Cycle
3rd Cycle
4th Cycle
5th Cycle
6th Cycle
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
0
100
200
300
400
500
600
700
800
900

FIG. 2B

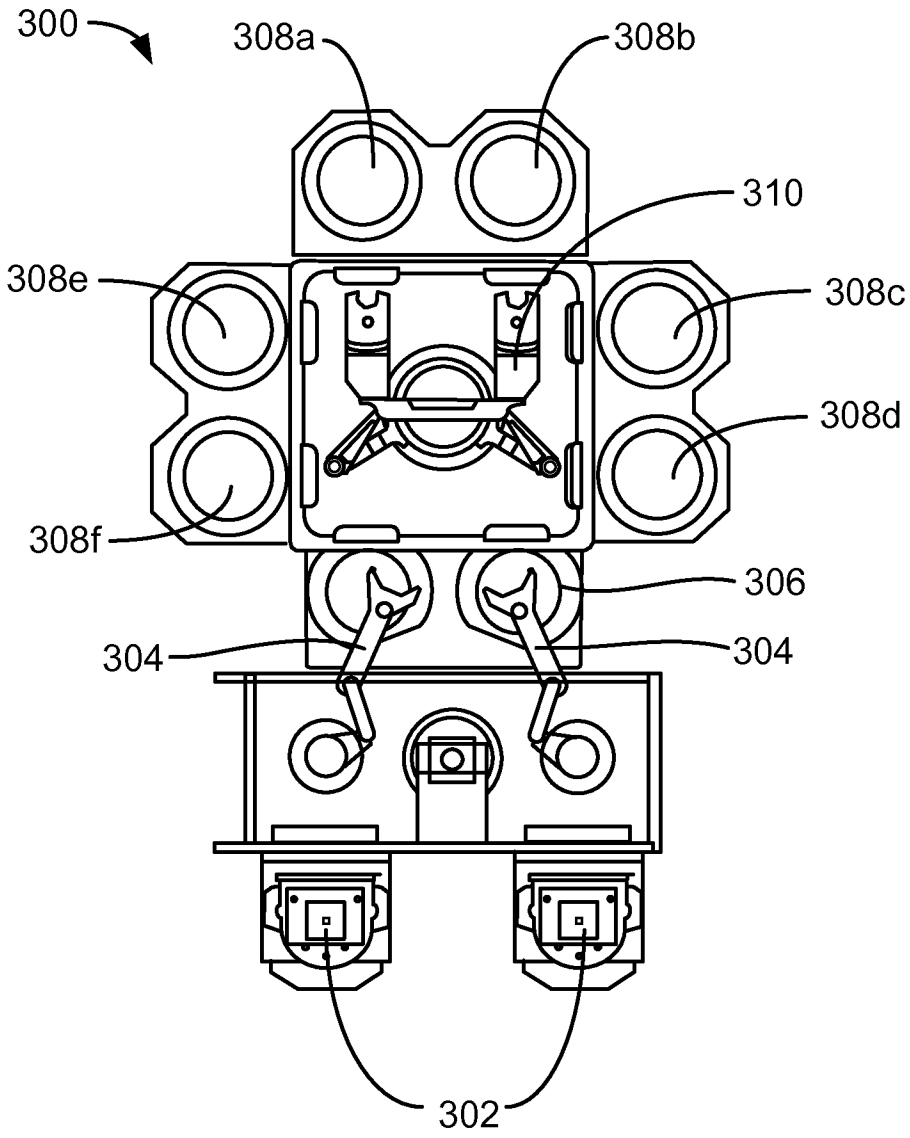


FIG. 3

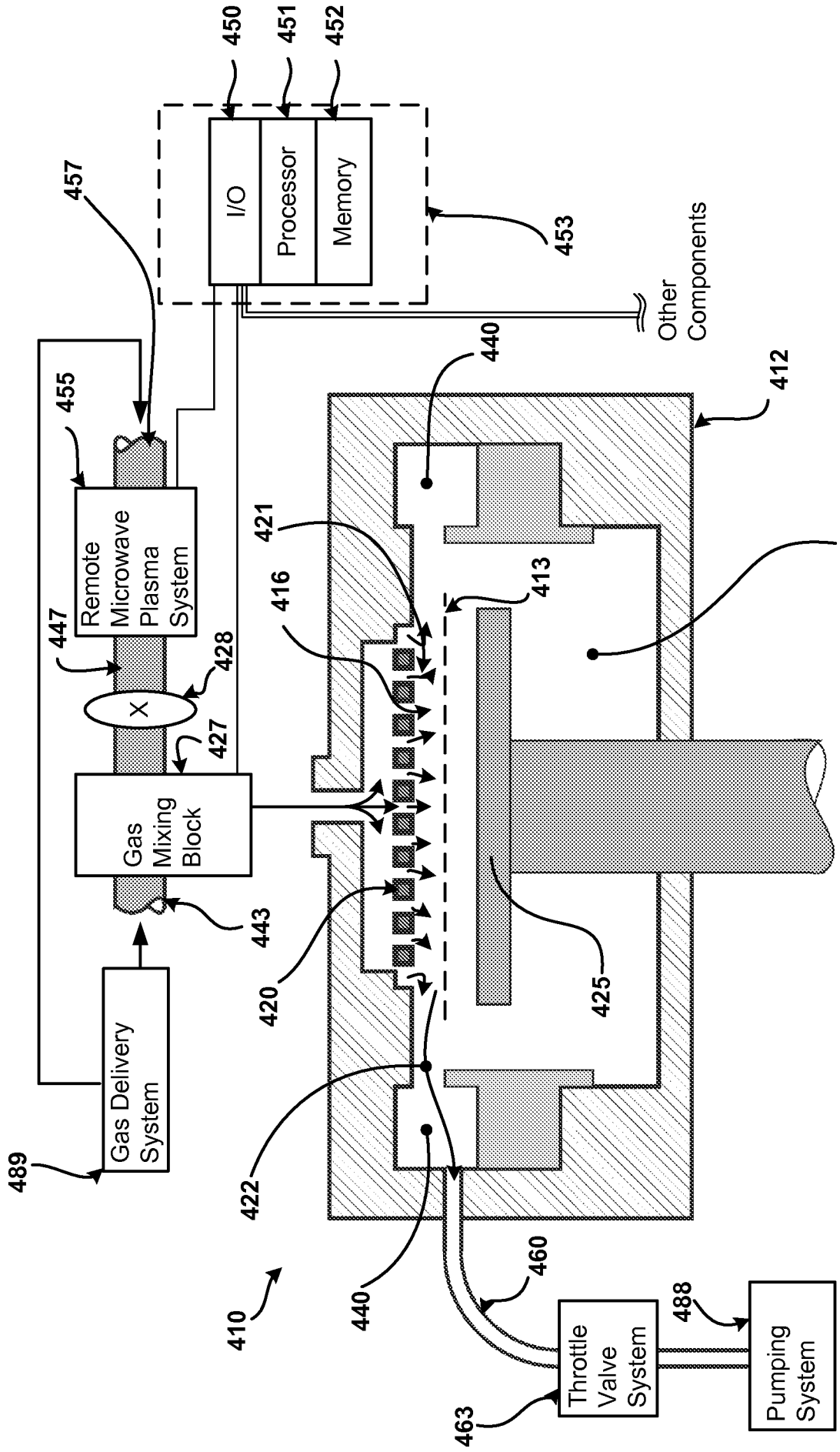

450
451
452
457
I/O
Processor
Memory
453
Other Components
455
Remote Microwave Plasma System
447
428
X
427
Gas Mixing Block
443
Gas Delivery System
489
440
412
421
416
413
415
420
425
422
410
440
460
488
Throttle Valve System
Pumping System
463

FIG. 4A

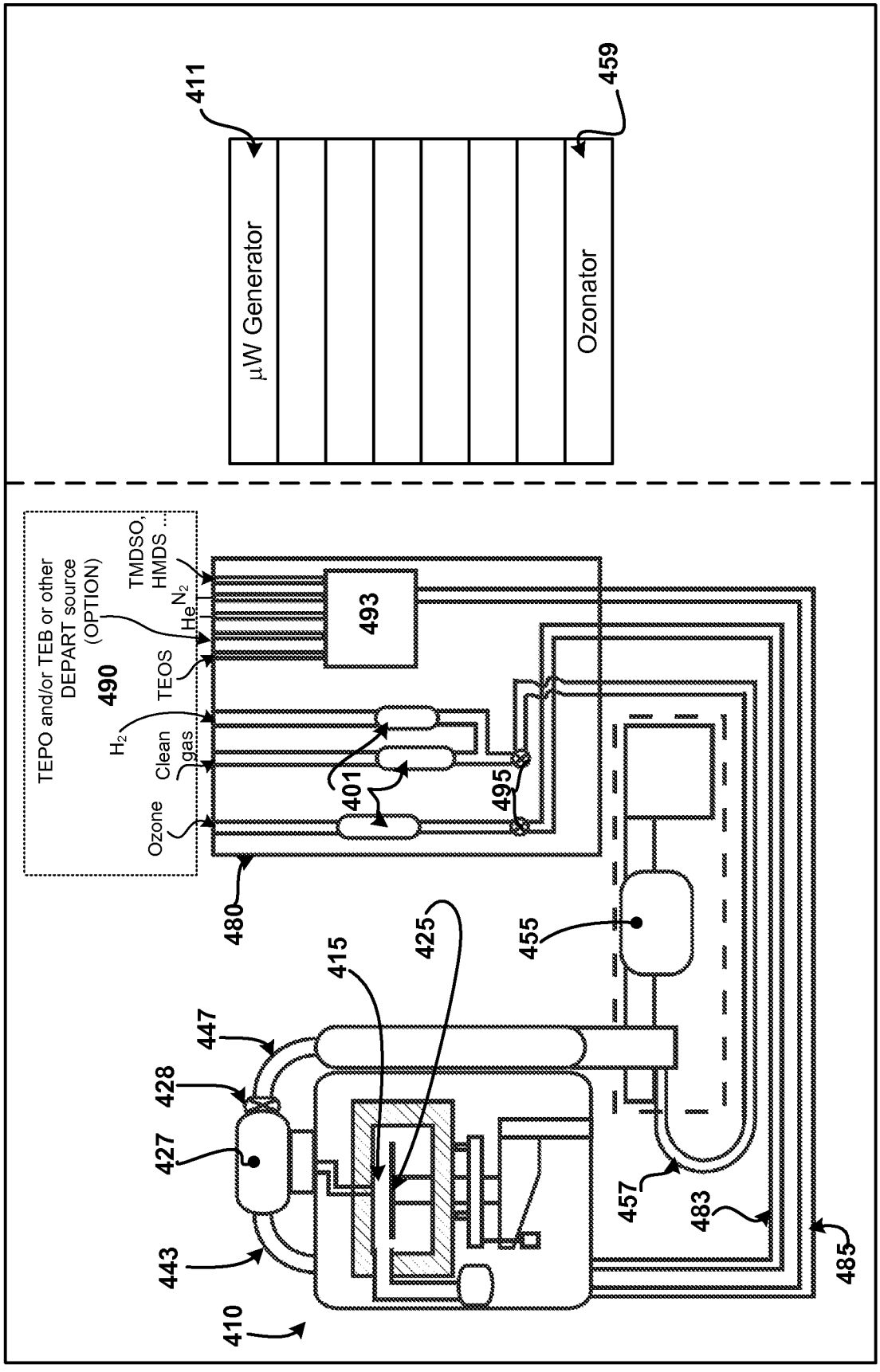

411
459
μW Generator
Ozonator
TEPO and/or TEB or other DEPART source (OPTION)
490
TMDSO, HMDS
N_2
He
TEOS
H_2
Clean gas
Ozone
493
401
495
480
425
455
415
447
428
427
443
410
457
483
485

FIG. 4B