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(54) **Title:** METHODS FOR FORMING METAL ELECTRODES ON SILICON SURFACES OF OPPOSITE POLARITY

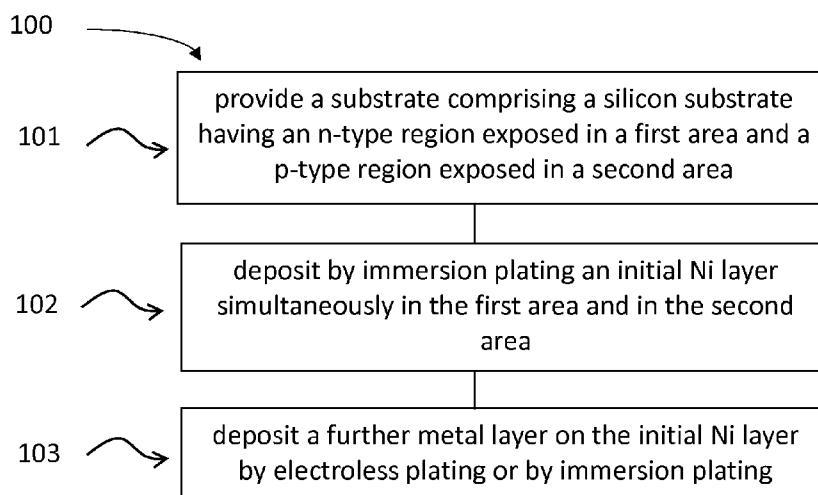


FIG 1

(57) **Abstract:** A method is provided for concurrently forming a first metal electrode on an n-type region of a silicon substrate and a second metal electrode on a p-type region of the silicon substrate. The method comprises providing a silicon substrate comprising an n-type region and a p-type region, wherein the n-type region is exposed at a first substrate surface in a first area and wherein the p-type region is exposed at a second substrate surface in a second area; depositing an initial Ni layer on the substrate simultaneously in the first area and in the second area by performing a Ni immersion plating process; and depositing a further metal layer on the initial Ni layer in the first area and in the second area by performing an electroless metal plating process or by performing an immersion metal plating process.



Methods for forming metal electrodes on silicon surfaces of opposite polarity**Field of the invention**

The invention relates to the field of semiconductor processing. More specifically it relates to plating-based methods for forming metal electrodes concurrently, or even simultaneously, on
5 n-type regions and on p-type regions of a silicon substrate. Furthermore, the present invention relates to methods for fabricating photovoltaic cells, such as bifacial photovoltaic cells, wherein metal electrodes are concurrently or simultaneously formed on n-type silicon regions and on p-type silicon regions by plating, and to photovoltaic cells thus obtained.

Background of the invention

10 Two important objectives of the photovoltaic industry are improving the photovoltaic cell and module efficiency, and reducing the cell and module manufacturing costs. A possible route towards improving the photovoltaic cell and module efficiency is the use of bifacial photovoltaic cells. A possible route towards reducing the cell and module manufacturing cost is the use of cheaper materials for the metallisation, as an alternative to traditional methods
15 of metallisations based on silver (Ag) paste .

A known alternative to Ag paste based metallisation for forming metal electrodes of silicon photovoltaic cells is Ni/Cu-based metallisation. In this approach, a thin nickel (Ni) layer is used for providing a low contact resistance to lowly doped silicon areas, as a diffusion barrier to the main conductor, copper (Cu), and as a seed layer for forming the Cu layer. The
20 Cu layer is used for providing a good conductivity and thus a low electrical resistance of the metal electrodes. A typical process flow comprises providing a dielectric layer, e.g. an anti-reflection coating, over the entire silicon surface, locally removing the dielectric layer, thereby exposing the underlying silicon surface at locations where metal contacts are to be provided, and providing the metal contacts at the exposed silicon regions by metal plating.

25 Common methods used for depositing such Ni/Cu stacks are light induced plating, electroplating and field induced plating. It is a disadvantage of these methods that they require electrical contacting of the silicon substrate and that they require an external current or voltage source and/or controlled illumination. For depositing the Ni layer, "electroless plating" may be used. For example, in electroless plating, auto-catalytic chemical plating
30 techniques may be used to deposit a layer of nickel or nickel alloy, e.g. by using chemical reactions in an aqueous solution that do not require the application of an external electrical power. However it is a disadvantage of an electroless plating process that it results in a

poor thickness uniformity due to non-uniform nucleation and the tendency for Ni to preferentially plate on the most conductive areas. Also for depositing the Cu layer on top of the Ni seed layer, electroless plating may be used. However, electroless Cu plating is very slow, e.g. more than a factor of ten slower than electroplating, and more bath renewals are required, leading to an increased generation of waste material.

In "Metallization improvement on fabrication of interdigitated backside and double sided buried contact solar cells", Solar Energy Materials & Solar Cells 86 (2005) 485-498, Jiun-Hua Guo et al. describe a process for nucleation of a nickel layer on both phosphorus and boron diffused contact areas based on immersion palladium chloride activation of the plating surfaces. However, this approach requires an additional step for the surface activation. Furthermore, the use of palladium results in an increased manufacturing cost. Using this approach, it may also be difficult to avoid spurious plating or ghost plating.

Summary of the invention

It is an object of embodiments of the present invention to provide good and efficient methods for forming metal electrodes concurrently on n-type regions and on p-type regions of a silicon substrate.

The above objective is accomplished by a method according to the present invention.

It is an advantage of embodiments of the present invention that a method is provided for forming metal electrodes concurrently, e.g. simultaneously, on n-type regions and on p-type regions of a silicon substrate by performing a plating process, such as to form metal electrodes having a good thickness uniformity.

It is an advantage of embodiments of the present invention that a method is provided for forming metal electrodes concurrently, e.g. simultaneously, on n-type regions and on a p-type regions of a silicon substrate by performing a plating process, in which the metal electrodes may be free of copper (Cu).

It is an advantage of embodiments of the present invention that a method is provided for forming metal electrodes concurrently, e.g. simultaneously, on n-type regions and on p-type regions of a silicon substrate by performing a plating process, in which the cost may be reduced as compared to known methods for forming metal electrodes.

It is an advantage of embodiments of the present invention that a method is provided for forming metal electrodes concurrently, e.g. simultaneously, on n-type regions and on p-type regions of a silicon substrate by performing a plating process, without the need for

providing an electrical contact or a physical contact to the substrate during the plating process, and/or without the need for providing controlled illumination during the plating process.

In a first aspect, embodiments of the present invention relate to a method for
5 concurrently, e.g. simultaneously, forming a first metal electrode on an n-type region of a silicon substrate and a second metal electrode on a p-type region of the silicon substrate. This method comprises providing a substrate that comprises a silicon substrate, the silicon substrate comprising an n-type region and a p-type region, wherein the n-type region is exposed at a substrate surface in a first area and wherein the p-type region is exposed at a
10 substrate surface in a second area. The method further comprises: depositing an initial nickel (Ni) layer on the substrate surface simultaneously in the first area and in the second area by performing a nickel (Ni) immersion plating process, and depositing a further metal layer on the initial nickel (Ni) layer in the first area and in the second area by performing an electroless metal plating process or by performing an immersion metal plating process or a combination
15 of both.

In a method in accordance with embodiments of the present invention, the step of depositing of the further metal layer may comprise depositing the further metal layer on the initial nickel (Ni) layer simultaneously in the first area and in the second area.

In a method in accordance with embodiments of the present invention, depositing the
20 further metal layer may comprise depositing a further nickel layer by performing an electroless nickel plating process.

In a method in accordance with embodiments of the present invention, the step of depositing of the further metal layer may comprise a sequence of, respectively, the steps of: depositing a further metal layer on the initial nickel layer in the first area, depositing a further
25 nickel layer in the second area by performing a nickel immersion plating process, and depositing the further metal layer on the further nickel layer in the first area and in the second area.

In a method in accordance with embodiments of the present invention, the step of depositing of the further metal layer may comprise the sequence of steps of: depositing a
30 first further nickel layer on the initial nickel layer in the first area by performing an electroless nickel plating process, depositing a second further nickel layer in the second area by performing a nickel immersion plating process, and depositing a third further nickel layer on the first further nickel layer in the first area and on the second further nickel layer in the

second area by performing an electroless nickel plating process. Furthermore, in such method, the step of depositing the initial nickel layer may have a process step duration in the range of 15s to 60s, e.g. 40s to 50s, e.g. 30s.

5 In a method in accordance with embodiments of the present invention, the initial Ni layer may, for example, have a thickness in the range between 4 nanometer and 2 micrometer, embodiments of the present invention not being limited thereto.

10 In a method in accordance with embodiments of the present invention, depositing the further metal layer on the initial Ni layer may, for example, comprise depositing a further Ni layer by performing an electroless Ni plating process or depositing a Ag layer by performing an electroless Ag plating process or an immersion Ag plating process.

15 In a method in accordance with embodiments of the present invention, the first area and the second area may be located at the same substrate side, e.g. at the same substrate surface. In a method in accordance with embodiments of the present invention, the first area and the second area may be located at opposite sides (e.g. opposite surfaces) of the substrate.

20 In a method in accordance with embodiments of the present invention, in which depositing the further metal layer on the initial Ni layer comprises depositing a further Ni layer, a solderable capping layer may be provided on the further Ni layer. The solderable capping layer may for example be a thin silver (Ag) layer, e.g. having a thickness in the range between 150 nm and 350 nm, embodiments of the present invention not being limited thereto. The thin Ag layer may, for example, be deposited on top of the further Ni layer by performing a Ag immersion plating process.

25 It is an advantage of such a thin Ag layer, provided on the Ni layer, that it may substantially increase the electrical conductivity of the first metal electrode and of the second metal electrode. As an alternative to a thin Ag layer, the solderable capping layer may for example be a thin Sn layer or an organic capping layer.

30 A method in accordance with embodiments of the present invention may further comprise performing an annealing or sintering step, such as for example at a temperature in the range of 250°C to 400°C, after having deposited the initial Ni layer or after having deposited the further metal layer, thereby reducing the metal-silicon contact resistance.

In a method in accordance with embodiments of the present invention, providing the substrate may comprise: providing a silicon substrate comprising an n-type region and a p-type region; providing a dielectric layer on at least one surface of the silicon substrate; and

removing the dielectric layer from the substrate in the first area and in the second area, thereby exposing a surface of the silicon substrate in the first area and in the second area.

A method for concurrently, e.g. simultaneously, forming a first metal electrode on an n-type region of a silicon substrate and a second metal electrode on a p-type region of the silicon substrate according to embodiments of the present invention may advantageously be used in a fabrication process of photovoltaic cells, such as for example bifacial photovoltaic cells or back contact photovoltaic cells. For example, embodiments of the present invention may also relate to a fabrication method for fabricating photovoltaic cells, such as for example bifacial photovoltaic cells or back contact photovoltaic cells, in which this fabrication method comprises a step of concurrently forming a first metal electrode on an n-type region of a silicon substrate and a second metal electrode on a p-type region of the silicon substrate according to embodiments of the first aspect of the present invention. For example, such fabrication method may comprise providing a silicon substrate of a photovoltaic cell to be fabricated, and applying this step of concurrently forming first and second metal electrodes on respectively an n-type and a p-type region of the silicon substrate.

It is an advantage of a method according to embodiments of the present invention that it allows forming metal electrodes with a good thickness uniformity concurrently on surfaces of opposite polarity, e.g. simultaneously on a surface of p-doped regions and on a surface of n-doped regions of a silicon substrate. For example, using other plating methods as known in the art, such as light induced plating or field induced plating, it may not be possible to concurrently or simultaneously deposit a metal directly on n-type silicon regions and on p-type silicon regions. For example, light-induced plating can only be used for metallizing n-type regions and not for metallizing p-type regions, while field-induced plating can only be used for metallizing p-type regions and not for n-type regions.

It is an advantage of a method in accordance with embodiments of the present invention that, by using an immersion plating process for forming the initial Ni layer, a full coverage of the first area and the second area with a good thickness uniformity can be obtained. The step of thickening the initial Ni layer by depositing a further metal layer by means of electroless plating or immersion plating is substantially independent of the polarity of the silicon substrate surface underlying the initial Ni layer.

A method according to embodiments of the present invention may advantageously be used for providing metal electrodes (e.g. metal fingers) to busbar-free photovoltaic cells. Such busbar-free photovoltaic cells may be further contacted and/or interconnected after

finishing the cell fabrication process by soldering a plurality of electrically conductive wires to the metal electrodes. These electrically conductive wires replace the busbars of a conventional photovoltaic cell and are provided for collecting an electrical current from the metal electrodes of the cell. The plurality of electrically conductive wires, such as for example
5 10 to 50 metal wires, are provided after cell processing, for example during a module fabrication process.

For example, embodiments of the present invention may also relate to a fabrication method for fabricating a busbar-free photovoltaic cell, in which this fabrication method comprises a step of concurrently forming a first metal electrode on an n-type region of a
10 silicon substrate and a second metal electrode on a p-type region of the silicon substrate according to embodiments of the first aspect of the present invention such as to form metal fingers of the busbar-free photovoltaic cell.

It is an advantage that for such busbar-free photovoltaic cells the electrical conductivity of the metal electrodes can be lower as compared to 'standard' or conventional
15 photovoltaic cells having typically three to five busbars. Therefore, metals having a lower electrical conductivity than Ag or Cu, such as Ni, can be used for forming the electrodes of the busbar-free cells without a risk of significantly increasing the electrical resistance of the metallisation pattern. It is an additional advantage that Ni is a cheaper material than Ag or Cu. In preferred embodiments a thin Ag layer is provided on top of the Ni layer, e.g. by
20 immersion Ag plating, to enable soldering of metal wires to the metal electrodes and to further improve the electrical conductivity of the metal electrodes. The thickness of such Ag layer may for example be in the range between 150 nm and 350 nm, such as in the order of about 250 nm.

Alternatively, for such busbar-free photovoltaic cells, a metal having a good electrical
25 conductivity such as Ag may be used for forming the electrodes, e.g. for forming the further metal layer on an initial Ni layer, with a reduced thickness as compared to a thickness required for 'standard' photovoltaic cells having typically three to five busbars. It is an advantage of such a reduced thickness that it results in a cost reduction.

It is an advantage of a method according to embodiments of the present invention
30 that the metal electrodes may be free of Cu. It is known that in photovoltaic cells having Ni/Cu electrodes, there is a risk of Cu penetration through the Ni layer into the underlying silicon, which can result in device degradation and a reduction of the cell efficiency. It is an advantage of Cu-free metal electrodes that the risk of cell degradation due to diffusion of Cu

into the underlying silicon is avoided, resulting in an improved long-term reliability of the photovoltaic cells. The use of Cu-free electrodes may also lead to a cost reduction.

It is an advantage of a method according to embodiments of the present invention that the metal electrodes can be provided without the need for providing an electrical
5 contact or a physical contact to the substrate during the plating process and without the need for providing controlled illumination during the plating process.

It is an advantage of a method according to embodiments of the present invention that the metal electrodes can be provided without ghost plating, e.g. without deposition of a metal at undesired locations on the silicon surface.

10 A method according to embodiments of the present invention can advantageously be used for providing metal electrodes to bifacial photovoltaic cells or to back contact photovoltaic cells, embodiments of the present invention not being limited thereto.

It is an advantage of a method according to embodiments of the present invention that shading or shadowing losses of the photovoltaic cells may be reduced as compared to
15 'standard' photovoltaic cells, because conventional busbars can be replaced by electrically conductive wires that may be substantially narrower than the busbars. Such reduction of shading losses results in an increase of the cell efficiency.

It is an advantage of a method according to embodiments of the present invention that it allows batch processing of large numbers of wafers in relatively cheap tools with small
20 footprints.

Certain objects and advantages of various inventive aspects have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the invention. Thus, for example, those skilled in the art will recognize that the invention may be embodied
25 or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other objects or advantages as may be taught or suggested herein. Further, it is understood that this summary is merely an example and is not intended to limit the scope of the invention. The invention, both as to organization and method of operation, together with features and advantages thereof, may best be
30 understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined

with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

5 **Brief description of the drawings**

FIG 1 schematically shows process steps of an exemplary method for forming metal electrodes concurrently on a surface of n-type regions and on a surface of p-type regions of a silicon substrate according to embodiments of the present invention.

FIG 2 schematically shows process steps of an exemplary fabrication process for fabricating a bifacial photovoltaic cell, wherein the metal electrodes at the front side of the cell and at the rear side of the cell are provided using a plating based metallisation method according to
10 embodiments of the present invention.

FIG 3 shows a first example of measured thickness of Ni layers provided by electroless plating on an initial immersion plated Ni layer as a function of the initial Ni layer thickness, on p-type silicon regions and on n-type silicon regions, for illustrating features and aspects of a method
15 in accordance with embodiments of the present invention.

FIG 4 shows a second example of measured thickness of Ni layers provided by electroless plating on an initial immersion plated Ni layer as a function of the initial Ni layer thickness, on p-type silicon regions and on n-type silicon regions, for illustrating features and aspects of a
20 method in accordance with embodiments of the present invention.

FIG 5 shows results of solder tab adhesion measurements for metal electrodes provided by a method in accordance with embodiments of the present invention on n-type regions, as a function of the NH_4F concentration in the immersion Ni plating bath.

FIG 6 shows results of solder tab adhesion measurements for metal electrodes provided by a
25 method in accordance with embodiments of the present invention on p-type regions, as a function of the NH_4F concentration in the immersion Ni plating bath.

FIG 7 schematically shows an example of a cross section of a substrate having an n-type region exposed at a first substrate surface in a first area and a p-type region exposed at a second substrate surface in a second area, the first area and the second area being located at
30 an opposite side of the substrate, to illustrate features and properties of embodiments of the present invention.

FIG 8 schematically shows an example of a cross section of a substrate having an n-type region exposed at a first substrate surface in a first area and a p-type region exposed at a second substrate surface in a second area, the first area and the second area being located at a same side of the substrate, to illustrate features and properties of embodiments of the present invention.

FIG 9 schematically shows the structure of FIG 7, after forming a first metal electrode and a second metal electrode by a method in accordance with embodiments of the present invention.

FIG 10 schematically shows the structure of FIG 8, after forming a first metal electrode and a second metal electrode by a method in accordance with embodiments of the present invention.

FIG 11 illustrates another exemplary method in accordance with embodiments of the present invention.

Any reference signs in the claims shall not be construed as limiting the scope of the present invention.

In the different drawings, the same reference signs refer to the same or analogous elements.

The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

Detailed description of illustrative embodiments

The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

Furthermore, the terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

Moreover, the terms top, bottom, over, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

It is to be noticed that the term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

Similarly it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments

are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

In the description provided herein, numerous specific details are set forth in order to provide a thorough understanding of the invention and how it may be practiced in particular embodiments. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

In the context of the detailed description provided hereinbelow, the front surface or front side of a photovoltaic cell or of a photovoltaic module is the surface or side adapted for being oriented towards a light source and thus for receiving illumination. In case of bifacial photovoltaic cells or modules, both surfaces are adapted to receive impinging light. In such case, the front surface or front side is the surface or side adapted for receiving the largest fraction of the light or illumination. The back surface, rear surface, back side or rear side of a photovoltaic cell or a photovoltaic module is the surface or side opposite to the front surface or side.

In the context of the detailed description provided hereinbelow, a busbar is an electrically conductive strip for collecting an electrical current, e.g. a current generated under illumination, from a plurality of metal contacts or metal electrodes provided on a surface of a photovoltaic cell. A busbar is provided for direct electrical connection with an external electrical lead. A busbar typically collects the electrical current from finer or narrower metal contacts, also called metal fingers, on the cell. These finer or narrower metal contacts collect an electrical current from the cell and deliver the current to the busbars; they are typically not provided for direct electrical connection to an external electrical lead.

In the context of the detailed description provided hereinbelow, a busbar-free photovoltaic cell is a photovoltaic cell not having busbars. A busbar-free photovoltaic cell typically comprises a plurality of metal contacts or metal electrodes on a surface of the cell but after cell fabrication it does not comprise an electrically conductive element for collecting current from the plurality of metal contacts. After finishing the cell processing, for example during module fabrication, electrically conductive elements such as for example electrically conductive wires are soldered to the plurality of metal contacts. These electrically conductive

elements are provided for collecting an electrical current from the plurality of metal electrodes and they replace the conventional busbars.

The present invention provides a method for concurrently, e.g. simultaneously, forming metal electrodes on a surface of an n-type region (or n-type regions) and on a surface of a p-type region (or p-type regions) of a silicon substrate with a good uniformity. In particularly advantageous embodiments of the present invention, these metal electrodes may be free of copper (Cu). The method furthermore may be based on a plating process wherein no electrical or physical contact to the silicon substrate is needed during plating and wherein no controlled illumination is needed during plating. The method is compatible with high volume batch processing.

In a first aspect, embodiments of the present invention provide a method for concurrently forming, such as for example simultaneously forming, a first metal electrode (or a plurality of first metal electrodes) in a first area (or in first areas) on a surface of an n-type silicon region (or n-type silicon regions) and forming a second metal electrode (or a plurality of second metal electrodes) in a second area (or second areas) on a surface of a p-type silicon region (or p-type silicon regions).

FIG 1 schematically illustrates process steps of a method 100 in accordance with embodiments of the present invention. The method comprises providing 101 a substrate that comprises a silicon substrate. This silicon substrate has an n-type region exposed at a first substrate surface in a first area and a p-type region exposed at a second substrate surface in a second area.

Examples of substrates 20 that may be used in embodiments of the present invention are schematically shown in FIG 7 and in FIG 8. FIG 7 shows an example of a cross section of a substrate 20 comprising a silicon substrate 10 having an n-type region 11 that is exposed at a substrate surface 21 in a first area 1, the silicon substrate 10 further comprising a p-type region 12 that is exposed at a substrate surface 22 in a second area 2. In the example shown in FIG 7, the first area 1 and the second area 2 are located at opposite sides or at opposite surfaces 21 and 22 of the silicon substrate 10. FIG 8 shows an example of a cross section of a substrate 20 comprising a silicon substrate 10 having an n-type region 11 that is exposed at a substrate surface 21 in a first area 1, the silicon substrate 10 further comprising a p-type region 12 that is exposed at a substrate surface 21 in a second area 2. In the example shown in FIG 8, the first area 1 and the second area 2 are located at a same side or same surface 21 of the silicon substrate 10.

In areas where the n-type region 11 and the p-type region 12 are not exposed, a layer 13, such as a dielectric layer, may be present on the substrate surface 21, 22. FIG 7 and FIG 8 show a single n-type region and a single p-type region. However, embodiments of the present invention are not limited thereto. In embodiments of the present invention the silicon substrate may comprise a plurality of p-type regions and/or a plurality of n-type regions on which metal electrodes are formed simultaneously or concurrently.

FIG 9 and FIG 10 show exemplary structures, corresponding to the exemplary substrates illustrated in FIG 7 and FIG 8 respectively, that may be obtained after forming a first metal electrode 31 in the first area 1 and a second metal electrode 32 in the second area 2, as provided by a method according to embodiments of the present invention. In the example shown, the first metal electrode 31 and the second metal electrode 32 comprise a stack of an initial Ni layer 33 formed by Ni immersion plating and a further metal layer 34 on top of the initial Ni layer 33, according to embodiments of the present invention.

In the method illustrated in FIG 1, an initial nickel (Ni) layer 33 is deposited on the substrate surface or surfaces, simultaneously in the first area 1 and in the second area 2, by means of an immersion plating process, which is also called a galvanic displacement plating process. Afterwards, the initial Ni layer 33 is thickened by depositing a further metal layer 34 on the initial Ni layer 33. Particularly, in a method in accordance with embodiments of the present invention, the step of depositing 103 of the further metal layer may comprise depositing the further metal layer on the initial Ni layer simultaneously in the first area and in the second area.

However, in another method in accordance with embodiments of the present invention, the step of depositing 103 of the further metal layer may be performed in a plurality of steps, in which at least a first such step is directed at depositing the further metal layer predominantly on the initial Ni layer in the first area, and at least a second such step is directed at depositing the further metal layer predominantly on the initial Ni layer in the second area. For example, depositing 103 of the further metal layer may comprise depositing the further metal layer on the initial nickel layer in the first area, e.g. without depositing any further metal in the second area, e.g. without depositing any significant or substantial amount of the further metal in the second area. This may then be followed, by, for example, depositing a further nickel layer in the second area by performing a nickel immersion plating process, e.g. by repeating a similar or the same nickel plating process as applied for

depositing 102 the initial nickel layer, and, then, depositing the further metal layer on the initial nickel layer and/or on the further nickel layer in the first area and in the second area.

Depositing 103 the further metal layer 34, e.g. a further Ni layer or a silver (Ag) layer, may be done by performing an electroless metal plating process, e.g. an electroless Ni plating process or an electroless Ag plating process.

In other embodiments, depositing 103 the further metal layer 34, e.g. Ag layer, may be done by performing an immersion metal plating process, e.g. an immersion Ag plating process.

In other embodiments, depositing 103 the further metal layer 34, e.g. nickel layer or silver layer, may be done by performing at least one electroless metal plating process and at least one immersion plating process.

In embodiments wherein the further metal layer 34 is a further Ni layer, the further Ni layer 34 may be covered with an additional layer such as a thin immersion plated Ag or Sn layer or an organic capping layer, e.g. to improve solderability. It is an advantage of covering the further Ni layer 34 with a thin immersion plated Ag layer, e.g. having a thickness in the range between 150 nm and 350 nm, that it results in an increased conductivity of the first and second metal electrodes. In embodiments wherein the further metal layer 34 is a Ag layer there is no need to provide an additional layer to improve solderability or to improve the conductivity of the first and second metal electrodes.

A method in accordance with embodiments of the present invention may advantageously be used for providing metal electrodes to busbar-free photovoltaic cells, wherein multiple electrically conductive wires are connected to, e.g. soldered to, the metal electrodes after cell fabrication.

Thus embodiments of the present invention may relate to a fabrication method for fabricating a busbar-free photovoltaic cell, in which this fabrication method comprises a step of forming a first metal electrode on an n-type region of a silicon substrate and a second metal electrode on a p-type region of the silicon substrate according to embodiments of the present invention, e.g. such as to form metal fingers of the busbar-free photovoltaic cell.

Using such approach, the required electrical conductivity of the metal electrodes, e.g. metal fingers, can be lower than in traditional photovoltaic cells having typically three to five busbars. Therefore, metals such as Ni, having a lower electrical conductivity than Ag or Cu, can be used for forming the metal electrodes without a risk of increasing the series resistance of the cells and without a risk of lowering the fill factor of the cells.

In a method according to embodiments of the present invention, first an initial Ni layer 33 may be deposited 102 by immersion Ni plating or galvanic displacement Ni plating, see e.g. step 102 in FIG 1. For example, this initial Ni layer 33 may be a thin and uniform initial Ni layer. Such non-contact plating method allows plating simultaneously on exposed n-type and p-type silicon surfaces. The plating process may proceed until all exposed silicon is plated, i.e. till all exposed silicon surfaces are covered with a Ni layer. The process may be self-limiting. Therefore, by plating for a sufficient time, e.g. enough for complete coverage on both surface polarities, such as for example 2 to 10 minutes;, a uniform initial Ni layer may be deposited on both n-type and p-type surfaces, wherein the layer fully covers the exposed surfaces.

However, in a method of the present disclosure partial coverage of the exposed surfaces by the initial Ni layer may be sufficient to allow good metal plating afterwards, with a good metal layer thickness uniformity. The thickness of the initial Ni layer, e.g. in at least one of the first area and the second area, may be typically in the range between 5 nanometer and 2 micrometer, embodiments of the present invention not being limited thereto. The initial Ni layer 33 is then thickened by depositing 103 a further metal layer 34 on the initial layer 33 by a metal plating process, e.g. an electroless plating process or an immersion plating process, see e.g. step 103 in FIG 1.

For example, a further Ni layer may be deposited on the initial Ni layer by electroless Ni plating, till a thickness in the range between for example 0.2 micrometer and 8 micrometer is obtained, the present disclosure not being limited thereto. The electroless plating rate may be typically in the order of 0.2 micrometer per minute. The initial Ni layer 33 has the function of a seed layer for the electroless Ni plating. The electroless plating rate is substantially independent of the polarity (n-type or p-type) of the silicon underlying the initial Ni layer. Therefore a good thickness uniformity can be obtained.

As mentioned hereinabove, in a method of the present disclosure partial coverage of the exposed surfaces by the initial Ni layer may be sufficient to allow good metal plating afterwards, with a good metal layer thickness uniformity. For example, in a method in accordance with embodiments of the present invention, the deposition 102 of the initial Ni layer may be concluded, e.g. terminated, when the initial Ni layer has reached a coverage, uniformity and/or thickness that is sufficient to allow good metal plating afterwards in depositing 103 the further metal layer, e.g. such as to obtain a good metal layer thickness uniformity after depositing 103 the further metal layer, on at least one of the first area and

the second area. For example, the deposition 102 of the initial Ni layer may be concluded when the initial Ni layer reaches such coverage, uniformity and/or thickness on at least one of the first area and the second area, yet before it exceeds this level of coverage, uniformity and/ or thickness to the extent that a disadvantageous increase of contact resistance is obtained due to a further increasing thickness of the initial Ni layer.

Thus, the skilled person may perform a deposition 102 of the initial Ni layer such that the initial Ni layer is not too thick, as would disadvantageously increase the contact resistance, and not too thin, as would provide an initial Ni layer that is insufficient to adequately carry out the following step of depositing 103 the further metal layer, e.g. insufficient such that no or only poor electroless Ni plating would occur in an embodiment where the further metal layer deposition relates to an electroless Ni plating process. Tuning the deposition 102 of the initial Ni layer to obtain a thickness that is both sufficient in view of further metal layer deposition and not excessive in view of a possible disadvantageous increase in contact resistance lies well within the capabilities of the skilled person, e.g. can be achieved by simple experimental optimization of a process duration of the deposition 102 of the initial Ni layer.

Furthermore, the step of depositing 102 the initial Ni layer may be concluded, e.g. terminated, when the initial Ni layer has reached a coverage, uniformity and/or thickness that is sufficient to allow good metal plating afterwards, yet not excessive in view of the implied contact resistance, on only the first area, e.g. on the first area while not necessarily being sufficient to allow good metal plating on the second area. For example, the rate of deposition 102 of the initial Ni layer may be higher in the first area 1, where the n-type region 11 is exposed, than in the second area 2, where the p-type region is exposed, such that a particular selection of a sufficient yet not excessive initial layer thickness may be reached on the first area 1 before the same sufficient yet not excessive initial layer thickness is reached on the second area 2.

For example, the step of depositing 102 the initial Ni layer may be carried out for a process step duration in the range of 10 seconds to 1.5 minutes, preferably in the range of 15 seconds to 45 seconds, such as about 30 seconds, e.g. for a process step duration of 30 seconds. While the initial nickel layer 33 is deposited 102 on the substrate surface simultaneously in the first area 1 and the second area 2, mainly the first area 1, i.e. the exposed n-type area, may be plated during this step. For example, only a relatively small

amount of nickel may be deposited during this depositing 102 on the second area 2, i.e. the exposed p-type area.

Then, a further metal layer 34 may be deposited 401 on the initial Ni layer 33 in the first area 1, as illustrated in FIG 11. For example, this deposition 401 of a further metal layer on the initial Ni layer in the first area 1 may comprise an electroless or immersion plating process, such as an electroless Ni plating step. For example, an electroless Ni plating may be applied for a process step duration in the range of 1 minute to 3 minutes, e.g. 2 minutes. After the deposition 401 of the further metal layer on the initial Ni layer in the first area, e.g. a first electroless Ni plating process, for example a first electroless Ni plating process of about 2 minutes, the first area may be fully covered with nickel, e.g. the exposed n-type area may be fully covered due to the initial Ni layer forming a good seed layer on the n-type material, but the second area may be only partially covered with nickel, or may not be covered to any substantial extent with nickel, due to the initial Ni layer forming an insufficient seed layer on the p-type material.

Then, a further Ni layer may be deposited 402 in the second area 2 by immersion plating, e.g. by applying the same or a similar process step as used for depositing 102 the initial Ni layer. For example, the step of depositing 402 the further Ni layer may be carried out for a process step duration in the range of 45 seconds to 3 minutes, preferably in the range of 60 seconds to 120 seconds, such as about 90 seconds, e.g. having a process step duration of 90 seconds. While, in this step, the further nickel layer is deposited 402 on the substrate surface in the second area 2, no further Ni may be deposited 402 in the first area 1. For example, no substantial or significant amount of nickel may be deposited 402 in the first area 1, because, after deposition 401 of the further metal layer on the initial Ni layer in the first area, no or only a negligible amount of silicon would remain exposed in the first area.

Then, a further metal layer may be deposited 403 on the further Ni layer in the second area, e.g. by the same or a similar process step as used for depositing 401 the further metal layer on the initial Ni layer in the first area, e.g. an electroless Ni plating process step. This deposition 403 of the further metal layer on the further Ni layer in the second area may for example have a process step duration in the range of 4 minutes to 15 minutes, e.g. in the range of 5 minutes to 12 minutes. It shall be understood by the person skilled in the art that, even though the further metal layer is deposited 403 on the further Ni layer in the second area, this does not preclude that by the same process step more metal is deposited in the first area as well, thus further growing the further metal layer in the first area as well. It shall

be understood by the person skilled in the art that, even though the further metal layer is deposited 403 on the further Ni layer in the second area, this does not preclude that the further metal layer is also deposited by the same process step on the initial Ni layer in the second area as well.

5 It is an advantage of such approach in accordance with embodiments of the present invention that the amount of nickel deposited by respectively the initial plating step of depositing 102 the initial Ni layer on the n-type material in the first area and the later plating step of depositing 402 a further Ni layer on the p-type material in the second area is decoupled. Due to this decoupling, an additional degree of freedom is obtained for
10 optimization of the process, e.g. the process duration of each step can be used as a separate optimization parameter. Thus, particular constraints posed by design considerations, e.g. an upper limit imposed on the contact resistance, can be more easily satisfied by routine optimization.

 In embodiments of the present invention, instead of electroless plating of Ni to
15 thicken the initial Ni layer, another metal such as for example silver (Ag) may be provided on the initial Ni layer 33. The Ag layer may for example be provided by electroless plating or by immersion plating. It is an advantage of providing an Ag layer as the further metal layer 34 that it results in a lower resistance of the metal electrodes as compared to a process wherein a further Ni layer is provided. As compared to Ni, the use of Ag may have the disadvantage of
20 a higher cost. However, when the method is used for providing metal electrodes of busbar-free photovoltaic cells, the Ag layer thickness and thus the amount of Ag material (and thus the cost) may be reduced as compared to 'classical' photovoltaic cells having e.g. three to five busbars.

 In embodiments of the present invention, e.g. wherein the further metal layer 34 is a
25 Ni layer, e.g. provided in a single process step on the initial Ni layer in both the first area and the area simultaneously or provided in multiple steps in the first area and the second area as described hereinabove, the method may further comprise, after having performed the electroless Ni plating process, depositing a copper (Cu) layer on the further metal layer, e.g. on a further Ni layer. Depositing the copper layer may for example be done by means of an
30 electroless copper plating process. This can result in a further increase of the thickness of the metal electrodes and an increase of their electrical conductivity. Such embodiments may advantageously be used for providing metal electrodes including busbars, e.g. for cells having

a limited number of busbars such as for example three to five busbars, embodiments of the present invention not being limited thereto.

In embodiments of the present invention, for example in the context of fabricating busbar-free photovoltaic cells, the first metal electrode and/or the second electrode may consist of a plurality of continuous, parallel metal lines or metal fingers, extending from one edge of the substrate or cell to an opposite edge of the substrate or cell. However, embodiments of the present invention are not limited thereto. In embodiments of the present invention, the first metal electrode and/or the second metal electrode may for example also be composed of interrupted lines. In embodiments of the present invention, the first metal electrode and/or the second metal electrode may have a configuration different from a finger configuration, i.e. different from a configuration consisting of a plurality of substantially parallel metal lines. For example, the first metal electrode and/or the second metal electrode may be composed of a plurality of metal features extending in different non-parallel directions.

FIG 2 schematically shows process steps of an example of a fabrication process 200 for a bifacial photovoltaic cell, wherein the metal electrodes at the front side of the cell and at the rear side of the cell are provided using a plating-based metallisation method 100 in accordance with embodiments of the present invention, as described hereinabove. For bifacial cells, typically n-type silicon wafers may be used as a silicon substrate 10, for example with a resistivity in the range between 3 Ohm.cm and 5 Ohm.cm. However, embodiments of the present invention are not limited thereto, and wafers with another resistivity and/or p-type wafers may be used as a silicon substrate. After saw damage removal, the front and rear surface of the substrates may be textured using known techniques, as shown in FIG 2, step 201. At a surface of the substrate an emitter region may be formed 202, for example by boron diffusion when an n-type substrate is used, or by phosphorus diffusion when a p-type substrate is used. At the opposite surface of the substrate a high/low junction may optionally be provided 203, for example by phosphorus diffusion when an n-type substrate is used, or by boron diffusion when a p-type substrate is used. However, embodiments of the present invention are not limited thereto and other methods may be used for forming the doped regions, such as, for example, ion implantation, APCVD or PECVD. The emitter region may be formed at the rear surface and the high/low junction may be formed at the front surface of the substrate, or vice versa, the emitter region may be formed at the front surface and the high/low junction may be formed at the rear surface.

Both the front and rear surface may be passivated by providing 204 a dielectric layer, such as for example a PECVD SiN_x layer, or by providing a dielectric stack. The dielectric stack may for example comprise a SiO_2 layer, e.g. a thermally grown SiO_2 layer, and a SiN_x layer, e.g. deposited by PECVD (Plasma Enhanced Chemical Vapour Deposition), embodiments of the present invention not being limited thereto. For example, instead of a SiO_2 layer an AlO_x layer 5 may be used, such as e.g. an AlO_x layer deposited by ALD (Atomic Layer Deposition), PECVD, APCVD (Atmospheric Pressure Chemical Vapour Deposition), printing or sputtering. For example, instead of a SiN_x layer another dielectric layer or a layer stack e.g. comprising a deposited SiO_x layer or a SiO_xN_y layer deposited by PECVD may be used. A same stack or a 10 different stack may be used at the front and rear surfaces. The dielectric stacks may also function as an antireflection coating. After providing the dielectric layers or dielectric layer stacks, both the dielectric layer or dielectric layer stack at the front side and at the rear side of the silicon substrate may be patterned 205, for example by laser ablation or by photolithography, embodiments of the present invention not being limited thereto. 15 Patterning of the dielectric layers or dielectric layer stacks may comprise locally removing the dielectric layers or stacks, e.g. in the first area 1 and second area 2, i.e. making openings in the dielectric layers or stacks to expose the underlying silicon, using a pattern corresponding to the desired metallisation pattern. In embodiments of the present invention, the metallisation pattern may preferably be a busbar-free pattern.

20 In embodiments of the present invention, a selective doping process may be used, wherein the doping concentration at locations corresponding to the metallisation pattern is higher than the doping concentration at other locations, e.g. higher than the doping concentration of the previously provided emitter region and high/low junction. Selective doping at the n-type side may for example comprise providing a dopant source, for example a 25 spin-on dopant or a spray-on dopant, followed by laser doping and annealing for damage removal and dopant drive-in. The laser doping step results in openings being formed in the dielectric stack according to the metallisation pattern and in a selective doping at the location of the openings. Selective doping at the p-type side may for example comprise providing an AlO_x layer (which may be part of the passivating dielectric layer stack as described above) as 30 the dopant source, followed by laser doping and annealing for damage removal and dopant drive-in. However, embodiments of the present invention are not limited thereto and other selective doping methods may be used. An annealing step for damage removal and dopant drive-in may be performed after the plating steps for providing the metal electrodes. It is an

advantage that the annealing step may then additionally be combined with metal annealing (sintering step) to reduce the metal-silicon contact resistance. However, embodiments of the present invention are not limited thereto, and the annealing step for damage removal and dopant drive-in may also be done before forming the metal electrodes.

5 At step 206, as shown in FIG 2, a plating based metallisation process in accordance with a method 100 of embodiments of the present invention is performed, e.g. steps 102 and 103 shown in FIG 1.

Examples are provided hereinbelow, which illustrate experiments in which a method according to embodiments of the present invention was used for providing metal contacts on
10 a bifacial photovoltaic cell. These examples are provided for illustrating features and advantages of embodiments of the present invention, and to aid the skilled person in reducing the invention to practice. However, these examples should not be construed as limiting the invention in any way. For these experiments, n-type wafers with a resistivity of 3 to 5 Ohm.cm were used. After saw damage removal the front and rear surface of the
15 substrates were textured. At the front side a 90 Ohm/square p-type region (emitter region) was formed by boron diffusion. At the rear side a phosphorus diffusion was done to create a 120 Ohm/square high/low junction. Both the front and rear surface were passivated by providing a dielectric stack consisting of a thermally grown SiO₂ layer and a SiN_x layer deposited by PECVD. Openings were made in the dielectric layer stack, i.e. the dielectric layer
20 stack was locally removed, according to a photovoltaic cell contact pattern comprising three busbars and a plurality of parallel fingers spaced by 1.5 mm, both at the front side and at the rear side. Local removal of the dielectric layer stack was done by ps UV laser ablation.

Afterwards a plating based metallisation process in accordance with a method of embodiments of the present invention was performed. Before plating, the samples were
25 cleaned in a 8:1 H₂SO₄:H₂O₂ solution at 80°C for 45 seconds, to remove any organics from the surfaces to be plated. This was followed by rinsing, removal of oxide from the surfaces to be plated in a 2% HF solution for 90 seconds, and rinsing.

An initial Ni layer was deposited on the exposed silicon substrate surfaces by performing an immersion plating process. The immersion Ni (i-Ni) bath contained DI water,
30 NH₄F and nickel sulphamate Ni(SO₃NH₂)₂. NH₄F concentrations in the range between 5w% and 15w% were used. For the Ni(SO₃NH₂)₂ different concentrations in the range between 0.1M and 0.3M were used. The pH of the plating bath was adjusted by adding NH₄OH, to different pH values in the range between 7 and 9.5. Immersion Ni plating was performed at

80°C, with different durations in the range between 2.5 minutes and 15 minutes. The i-Ni bath was provided in a glass beaker placed on a hotplate. The temperature of the plating solution was measured by a thermocouple and the solution temperature was controlled within +/- 2°C. Solution agitation was provided by a stirrer at 200 rpm. No controlled external illumination was applied, i.e. only the lab background light was present.

Afterwards the samples were rinsed in deionized (DI) water and the initial Ni layer was thickened by performing an electroless Ni plating process, to thereby deposit a further Ni layer. A commercially available plating solution was used for the electroless Ni (E-Ni) plating bath, at 82°C. The pH of the E-Ni bath was 4.8, and the E-Ni plating time was in the range between 10 minutes and 15 minutes.

After rinsing in DI water, a thin Ag layer was provided on top of the further Ni layer by immersion Ag plating, using a commercially available process. This process uses two baths: first a pre-clean bath (pre i-Ag bath) at 38°C, 30 s, and then a deposition bath (i-Ag bath) at 52°C, 60 s. After rinsing of the samples in DI water and drying with N₂, the contacts were sintered (annealed) in a belt furnace in a nitrogen atmosphere (O₂ concentration < 10ppm) for 4 minutes at a temperature in the range between 250°C and 400°C.

Deposited layer thicknesses were measured by XRF (X-Ray Fluorescence).

The table hereinbelow shows the measured thickness of the initial Ni layer 33 formed by immersion plating, for different i-Ni plating bath and process conditions. Thicknesses were measured both on n-type regions and on p-type regions. The results show that simultaneous plating is achieved on both n-type regions and p-type regions, for a wide range of process conditions. The process conditions affect the layer thickness and the ratio between the thickness on n-type regions and the thickness on p-type regions. The i-Ni layer thickness on n-type regions is larger than on p-type regions.

pH	NH ₄ F [w%]	Ni(SO ₃ NH ₂) ₂ [M]	Duration [min]	i-Ni thickness on p region [nm]	i-Ni thickness on n region [nm]
8	15	0.3	15	299	1390
7.5	15	0.1	15	658	1844
8	15	0.1	5	209	630
8	5	0.1	15	31	1560
7.75	10	0.2	10	216	734
7.5	15	0.3	5	176	890
7.75	10	0.2	10	216	924
8	5	0.3	5	8	86
7.5	5	0.3	15	126	238

7.5	5	0.1	5	18	500
7.75	10	0.2	10	201	748

The initial Ni layers provided on p-type regions and on n-type regions, as reported in the table hereinabove, were thickened by performing an electroless Ni (E-Ni) plating process as described hereinabove, thereby depositing a further Ni layer 34 on the initial Ni layer 33. The E-Ni plating time was 10 minutes. FIG 3 shows the measured thickness d_{E-Ni} (in micrometers) of the further Ni layers provided on top of the initial i-Ni layers, as reported in the table hereinabove, as a function of the initial i-Ni layer thickness d_{i-Ni} (in micrometers). In FIG 3, filled circles 31 correspond to Ni layers formed on n-type regions and filled triangles correspond to Ni layers formed on p-type regions. From these exemplary results, it can be seen that the thickness of the further Ni layer (i.e. the Ni layer provided on the initial Ni layer by electroless plating) can be substantially independent of the thickness of the underlying initial Ni layer, and that it can be substantially independent of the polarity of the doped silicon region underlying the initial Ni layer, even for very thin initial Ni layers.

However, due to a faster deposition rate when forming the initial Ni layer *i-Ni* on the n-type region, when compared to deposition on the p-type region, as demonstrated by the information presented in the table hereinabove, for particularly short process durations of the i-Ni deposition, e.g. less than or equal to 5 minutes, a large relative difference may arise between the deposited i-Ni layer thickness on the p-type region and on the n-type region. Thus, for such short process durations, the further Ni layer *E-Ni* may not form, or may not form well, in the p-type region, as shown by the data points 33 plotted in FIG 3, while the further Ni layer *E-Ni* does form adequately in the n-type region for the same processing steps. Nevertheless, as described hereinabove, short process duration times for formation of the initial Ni layer *i-Ni* may be preferable to obtain a particularly low contact resistance. As also described hereinabove, in a method according to embodiments of the present invention, the step of depositing the further metal layer may comprise a plurality of substeps to easily combine a good contact resistance due to a particularly thin initial Ni layer and a good plating of the further metal layer over the initial Ni layer, e.g. by first forming a further metal layer on the initial N layer in the n-type region, then extending the initial Ni layer on the p-type region by performing a second immersion Ni plating step, and then forming a further metal layer in the p-type region.

Another example relates to an experiment in which first an initial Ni layer was provided by immersion Ni plating using a plating solution with 10 w% NH_4F and 0.1 M

Ni(SO₃NH₂)₂ (with different pH values) for 10 minutes, and next an electroless Ni plating process was performed for 15 minutes, thereby depositing a further Ni layer on the initial Ni layer. FIG 4 shows the measured thickness d_{E-Ni} of the further Ni layer as a function of the underlying initial Ni layer thickness d_{i-Ni} , for Ni layers formed on n-type regions (filled circles 31) and on p-type regions (filled triangles 32). It can be seen that the thickness d_{E-Ni} of the further Ni layer is substantially independent of the thickness d_{i-Ni} of the underlying initial Ni layer and that it is substantially independent of the polarity of the doped silicon region underlying the initial Ni layer.

In another example, an experiment was performed wherein an initial Ni layer was deposited by immersion plating on n-type regions and on p-type regions in the absence of light. Before plating, the samples were cleaned in a 8:1 H₂SO₄:H₂O₂ solution at 80°C for 45 seconds, to remove any organics from the surfaces to be plated. This was followed by rinsing, removal of oxide from the surfaces to be plated in a 2% HF solution for 90 seconds, and rinsing. The immersion Ni (i-Ni) bath contained DI water, 7.5 w% NH₄F and 0.1M nickel sulphamate Ni(SO₃NH₂)₂. The pH of the plating bath was adjusted by adding NH₄OH, to a pH value of 8.0. Immersion Ni plating was performed at 80°C for 10 minutes. The i-Ni bath was provided in a glass beaker placed on a hotplate. The temperature of the plating solution was measured by a thermocouple and the solution temperature was controlled within +/- 2°C. Solution agitation was provided by a stirrer at 200 rpm. During immersion plating, the lab lights were off and the glass beaker was covered with a black cloth.

The following table, hereinbelow, shows the measured thickness of the Ni formed by immersion plating in the absence of light at different locations, both on p-type regions and on n-type regions. The results show that, also in the absence of light, simultaneous plating is achieved on both substrate polarities. The layer thickness on n-type regions is larger than on p-type regions.

i-Ni thickness on p region [nm]	i-Ni thickness on n region [nm]
195	838
176	797
171	777
148	823

Furthermore, the resistance between bus bars (R_{bb}) was used to evaluate line conductivity. A 4-point probe type resistance measurement was done between bus bars, the resistance measured being considered proportional to the average line conductivity (Ohm/cm) of the fingers between the two bus bars.

Based on calculations and experimental data, it has been observed that sufficient line conductivity can be obtained within a reasonable process time when using a metallisation process according to embodiments of the present invention. Calculations were done to estimate the finger conductivity needed to obtain a good Fill Factor for a photovoltaic cell comprising a busbar-free finger pattern, wherein the fingers are connected by thirty-eight wires soldered to the fingers and replacing the busbars ('smart wire' technology). It is known that current high Fill Factor standard n-PERT cells with three busbars have an R_{bb} of about 25 m. Ohm. The required finger conductivity of the Ni plated fingers to obtain the same I^2R ohmic power losses from the fingers connected by 38 wires as in such an n-PERT cell was calculated. For that finger conductivity it was calculated that the R_{bb} measured on a three-busbar cell would be about 4 Ohm. Photovoltaic cells were made as described above, the cells having a plurality of fingers being provided using a method in accordance with embodiments of the present invention and having three busbars to enable line conductivity measurements. The following process sequence was used: $H_2SO_4:H_2O_2$ cleaning for 45 s; oxide etching in 2% HF for 90 s; immersion Ni plating 10 min in a plating bath with 10w% NH_4F , 0.1M $Ni(SO_3NH_2)_2$ and a pH value of 8.5; 15 minutes electroless Ni plating; 30 s pre i-Ag; 60 s i-Ag plating. The measured R_{bb} values are shown in the following table, hereinbelow, for four cells. Cell 1 was sintered; cells 2, 3 and 4 were not sintered. On cell 1 the thickness of the metal electrodes was measured by X-Ray Fluorescence. On n-type regions, the Ni thickness was 2.9 micrometer and, on p-type regions, it was 2.3 micrometer. The Ni layers were covered by a 310 nm thick i-Ag layer on the n-type regions and a 294 nm thick i-Ag layer on the p-type regions.

	R_{bb} n-region [Ohm]		R_{bb} p-region [Ohm]	
	#1	#2	#1	#2
cell 1	0.94	0.95	1.0	1.1
cell 2	0.91	0.99	1.8	1.6
cell 3	0.95	0.90	1.2	1.2
cell 4	0.88	0.84	1.1	1.1

In this table presented hereinabove, #1 and #2 refer to two different measurements: a first measurement between a first and a second busbar, and a second measurement between the second and a third busbar. The results illustrate that R_{bb} values significantly less than 4 Ohm (estimated value, as described hereinabove) were obtained for all cells, both on n-type regions and on p-type regions. Therefore it can be concluded that sufficient line

conductivity can be achieved for integration with smart wire connection technology using short processing times. In these experiments, the good conductivity of the fingers may be closely related to the presence of the i-Ag layer (which is about 300 nm thick) on top of the Ni layer (having a thickness of 2.3 to 2.9 micrometer in these examples).

5 Based on optical microscope images and based on SEM images of the plated electrodes, no ghost plating was observed, neither on p-type regions nor on n-type regions.

Adhesion of the metal electrodes was measured by solder tab adhesion wherein a solder tab was soldered to the electrodes at 325°C and pulled off at an angle of 45 degrees, the maximum force N required to remove the tab being recorded. Solder tab adhesion results are illustrated in FIG 5 for n-type regions and in FIG 6 for p-type regions, for the samples reported in Table 1. FIG 5 and FIG 6 show the maximum force F_{max} (in Newton) required to remove the tab, e.g. the maximum force F_{max} representative of the solder adhesion, as a function of the NH_4F concentration $[NH_4F]$ in the i-Ni bath. These results suggest a correlation between NH_4F concentration and adhesion strength. A maximum force of 2.4 Newton would be considered as corresponding to a good adhesion, suitable for busbar and tab soldering. In the experiments done this was obtained for plating solutions with 5w% NH_4F but not for plating solutions having 10w% NH_4F or 15w% NH_4F . However, the adhesion required for a successful integration of smart wire technology may be less than for traditional busbars and tab soldering.

20 In another example, an experiment was performed wherein an initial Ni layer was deposited by a first immersion plating on predominantly n-type regions. Before plating, the samples were cleaned to remove any organics from the surfaces to be plated, followed by DI water rinsing, removal of oxide from the surfaces to be plated in a 2% HF solution for 90 seconds, and DI water rinsing. The immersion Ni (i-Ni) bath contained DI water, 30 w% NH_4F and 0.1M nickel sulphamate $Ni(SO_3NH_2)_2$. The pH of the plating bath was adjusted to a pH value of 8.5. This immersion Ni plating was performed at 60°C for 30 seconds, under solution agitation provided by a magnetic stirrer at 200 rpm. This immersion Ni plating was performed in darkness, as discussed hereinabove in relation to a previous example. Next, the samples were rinsed with DI water, and a process step of 2 minutes of electroless Ni plating was performed at 82°C, using a commercially available solution for electroless Ni plating (Macdermid Ultraplanar, pH 4.8). In a next step, after DI rinsing the samples again, a further immersion Ni plating was performed for 90 seconds, under similar conditions as in the previous immersion Ni plating step, e.g. again at 60°C, in darkness and under solution

agitation by a magnetic stirrer at 200 rpm. The immersion Ni bath used in this immersion Ni plating step also had the same composition as in the previous immersion Ni plating step. After again DI rinsing the samples, a further electroless Ni plating was performed at 82 °C for 12 minutes (Macdermid Ultraplanar, pH 4.8).

5 As described hereinabove, by such partition of the deposition of the further metal layer in a plurality of steps, e.g; in combination with a short step of depositing the initial Ni layer, such as the 30 second initial immersion plating step in this example, an initial Ni layer is obtained that is not too thick such as to substantially increase the contact resistance, yet sufficient to enable a good electroless Ni plating in the following step. Since the rate of Ni
10 deposition in the immersion Ni plating is higher on the n-type material than on the p-type material, the first steps of immersion plating and electroless Ni plating are specifically achieving a good plating on the n-type material surfaces, while the following steps of immersion plating and electroless Ni plating complete the process to achieve a good plating on the p-type material, as already discussed hereinabove.

15 This multistep approach of alternating immersion plating and electroless plating was further extended, in this example, by a next step of, after again DI rinsing the samples, a pre-iAg deposition step using a commercially available solution (MacDermid Helios Silver IM 448) for 60 seconds, and an iAg deposition step of 90 seconds (MacDermid Helios silver IM 448).

 The foregoing description details certain embodiments of the invention. It will be
20 appreciated, however, that no matter how detailed the foregoing appears in text, the invention may be practiced in many ways. It should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to including any specific characteristics of the features or aspects of the invention with which that
25 terminology is associated.

 Whereas the above detailed description as well as the summary of the invention has been focused on a method for forming contact electrodes, the present invention also relates to a device, e.g. a photovoltaic cell, comprising metal electrodes obtained using a method according to any of the embodiments as described above.

30 While the above detailed description has shown, described, and pointed out novel features of the disclosure as applied to various embodiments, it will be understood that various omissions, substitutions, and changes in the form and details of the device or process

illustrated may be made by those skilled in the technology without departing from the disclosure.

Claims

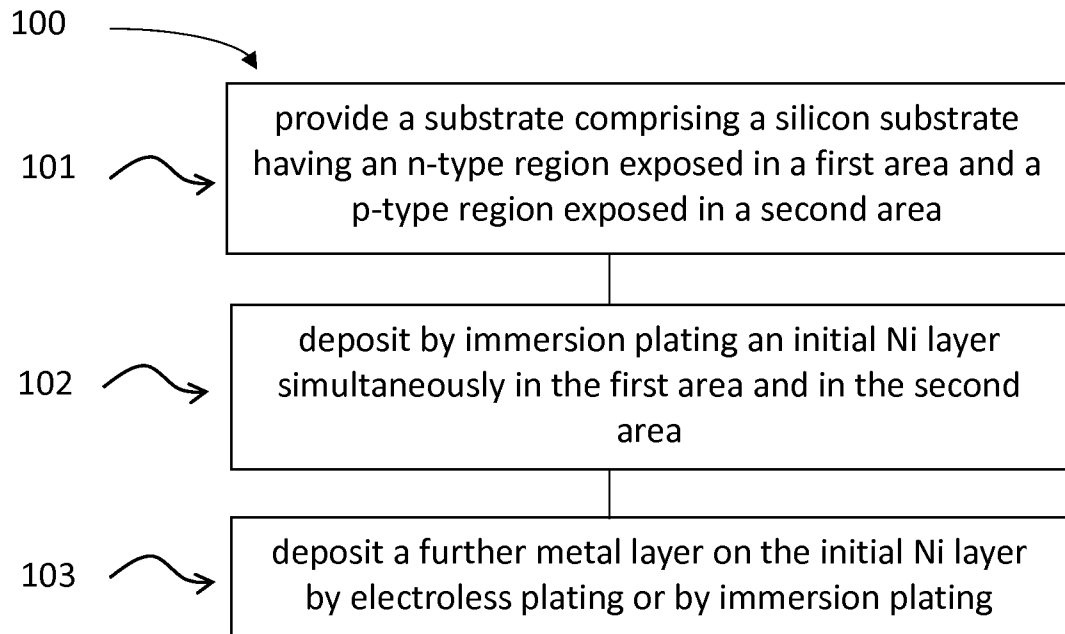
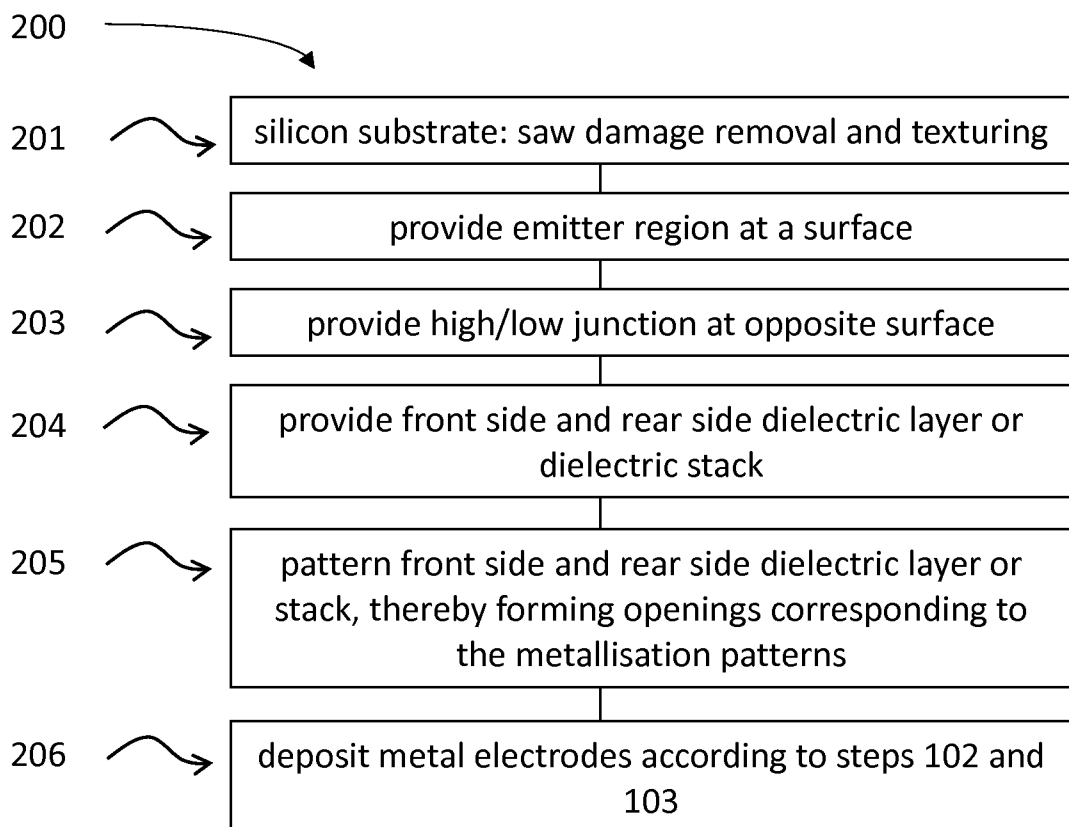
- 1.- A method (100) for concurrently forming a first metal electrode (31) on an n-type region (11) of a silicon substrate (10) and a second metal electrode (32) on a p-type region (12) of the silicon substrate (10), the method comprising:
- 5 - providing (101) a substrate (20) comprising a silicon substrate (10), the silicon substrate (10) comprising an n-type region (11) and a p-type region (12), wherein the n-type region (11) is exposed at a surface (21, 22) of the silicon substrate (10) in a first area (1) and wherein the p-type region (12) is exposed at a surface (21, 22) of the silicon substrate in a second area (2);
- 10 - depositing (102) an initial nickel layer (33) on the substrate surface (21, 22) simultaneously in the first area (1) and in the second area (2) by performing a nickel immersion plating process; and
- depositing (103) a further metal layer (34) on the initial Ni layer (33) in the first area (1) and in the second area (2) by performing an electroless metal plating process or
- 15 by performing an immersion metal plating process.
- 2.- The method (100) according to claim 1, wherein said depositing (103) of the further metal layer (34) comprises depositing said further metal layer (34) on the initial nickel layer (33) simultaneously in the first area (1) and in the second area (2).
- 3.- The method (100) according to any of the previous claims, wherein depositing (103) the
- 20 further metal layer (34) comprises depositing a further nickel layer by performing an electroless nickel plating process.
- 4.- The method (100) according to claim 1, wherein said depositing (103) of the further metal layer (34) comprises the sequence of steps of: depositing (401) a further metal layer on the initial nickel layer (33) in the first area (1), depositing (402) a further nickel
- 25 layer in the second area (2) by performing a nickel immersion plating process, and depositing the further metal layer on the further nickel layer in the first area (1) and in the second area (2).
- 5.- The method (100) according to claim 4, wherein said depositing (103) of the further metal layer (34) comprises the sequence of steps of: depositing (401) a first further nickel
- 30 layer on the initial nickel layer (33) in the first area (1) by performing an electroless nickel plating process, depositing (402) a second further nickel layer in the second area (2) by performing a nickel immersion plating process, and depositing a third further nickel layer

- on the first further nickel layer in the first area (10) and on the second further nickel layer in the second area (2) by performing an electroless nickel plating process.
- 6.- The method (100) according to claim 3 or claim 5, further comprising providing a solderable capping layer on the further nickel layer.
- 5 7.- The method (100) according to claim 6, wherein providing the solderable capping layer comprises:
- providing a silver layer by performing a silver immersion plating process,
 - or providing a tin layer by performing a tin plating process,
 - or providing an organic capping layer.
- 10 8.- The method (100) according to claim 7, wherein providing the solderable capping layer comprises providing a silver layer by performing a silver immersion plating process and wherein the silver layer has a thickness in the range between 150 nm and 350 nm.
- 9.- The method (100) according to claim 1 or claim 2, wherein depositing (103) the further metal layer (34) comprises depositing a silver layer by performing an electroless silver
- 15 plating process or by performing an immersion silver plating process.
- 10.- The method (100) according to any of the previous claims, wherein the initial nickel layer (33) has a thickness in the range between 5 nanometer and 2 micrometer.
- 11.- The method (100) according to any of the previous claims, wherein providing (101) the substrate (20) comprises:
- 20
- providing a silicon substrate (10) comprising the n-type region (11) and the p-type region (12);
 - providing a dielectric layer (13) on at least one surface (21, 22) of the silicon substrate (1); and
 - removing the dielectric layer from the substrate in the first area (1) and in the second
- 25 area (2).
- 12.- The method (100) according to any of the previous claims, further comprising performing a sintering step at a temperature in the range between 250°C and 400°C.
- 13.- The method (100) according to any of the previous claims, wherein the first area (1) and the second area (2) are at a same surface (21, 22) of the silicon substrate (10).
- 30 14.- The method (100) according to any of claims 1 to 12, wherein the first area (1) and the second area (2) are at opposite surfaces (21, 22) of the silicon substrate (10).
- 15.- A method (200) for fabricating a bifacial photovoltaic cell, the method comprising concurrently forming a first metal electrode (31) on an n-type region (11) of a silicon

substrate (10) and a second metal electrode (32) on a p-type region (12) of the silicon substrate (10) according to any of claims 1 to 12 or 14.

- 16.- A method for fabricating a back-contact photovoltaic cell, the method comprising concurrently or simultaneously forming a first metal electrode (31) on an n-type region
5 (11) of a silicon substrate (10) and a second metal electrode (32) on a p-type region (12) of the silicon substrate (10) according to any of claims 1 to 13.

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**FIG 1****FIG 2**

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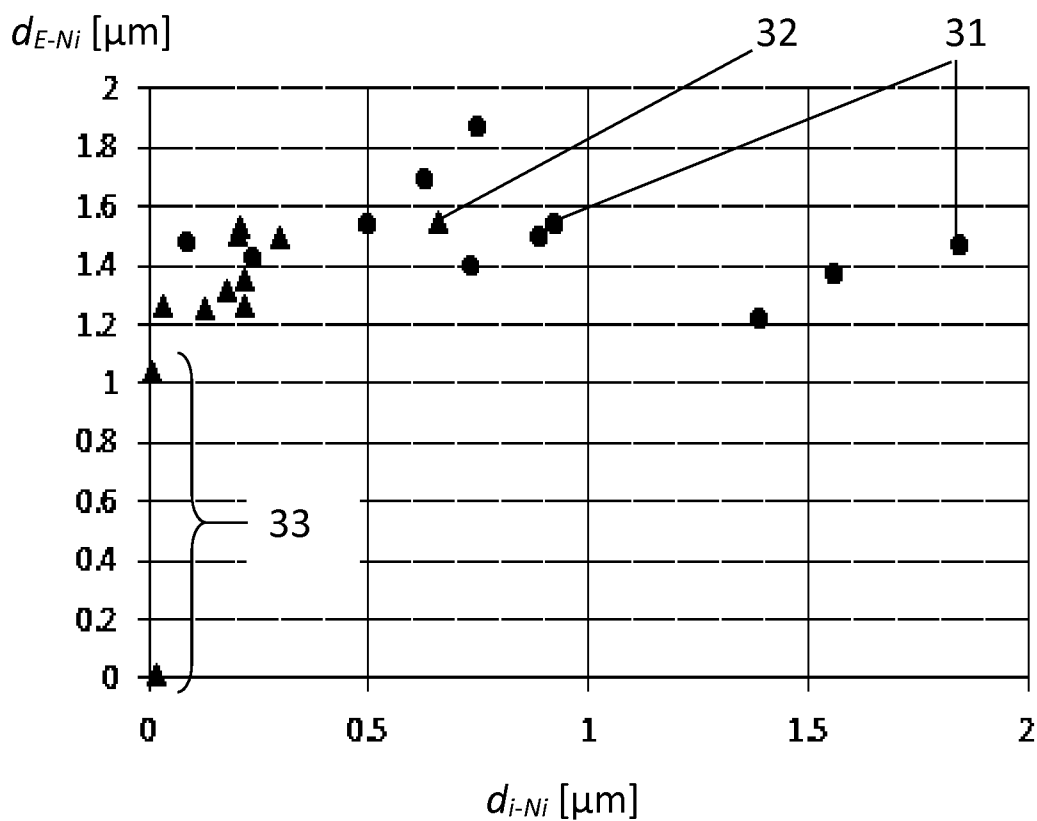


FIG 3

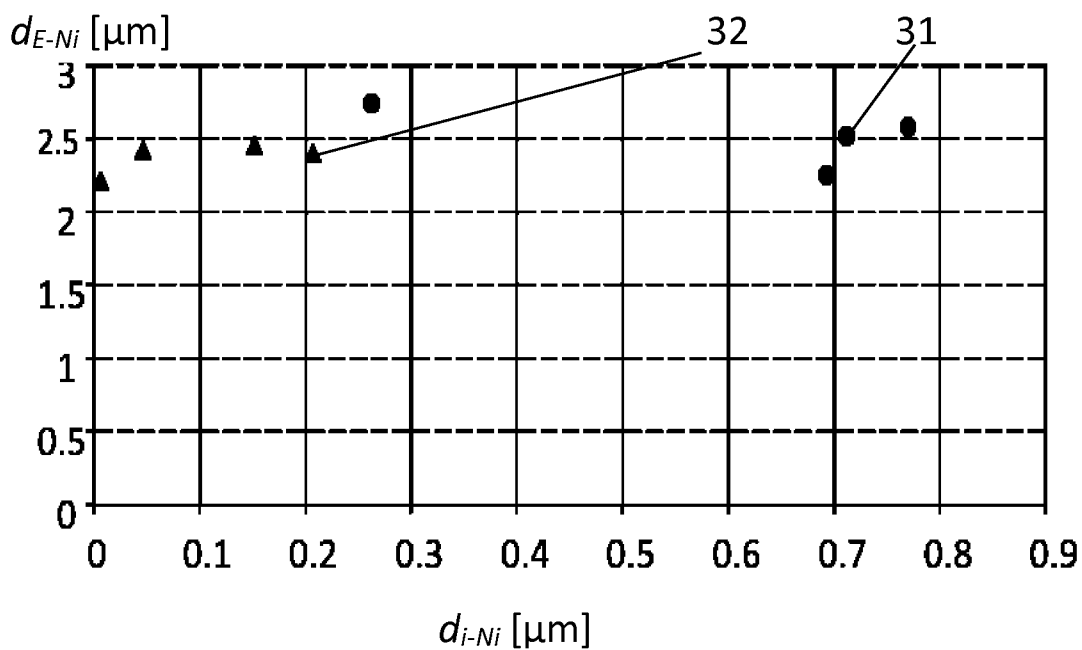


FIG 4

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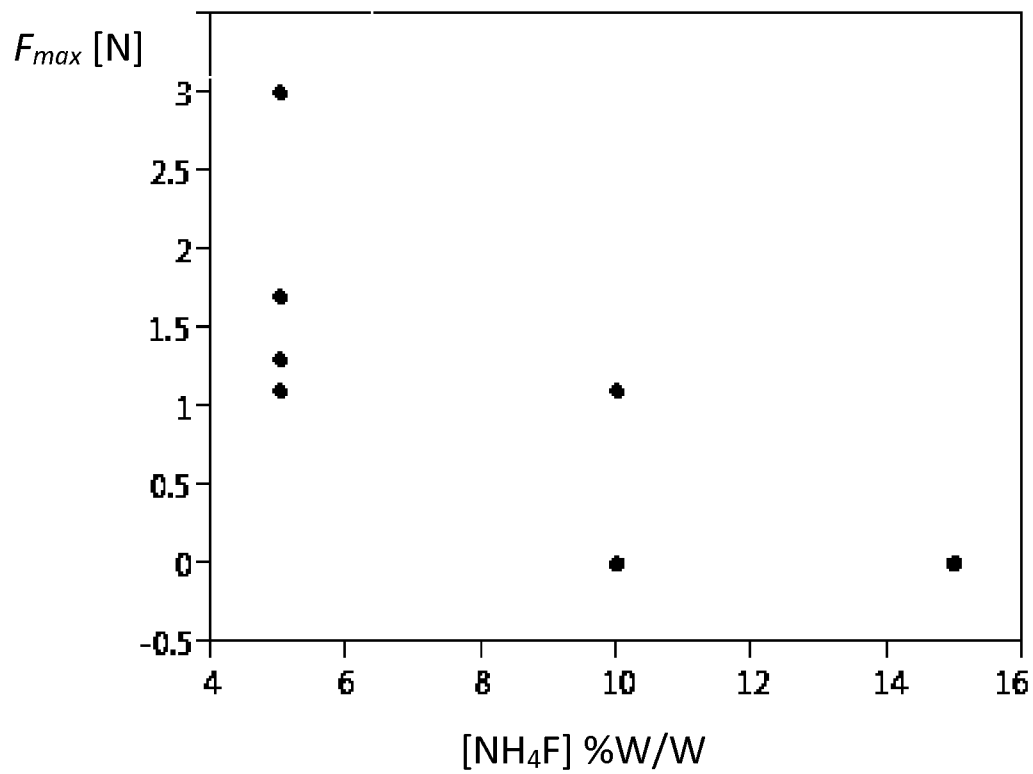


FIG 5

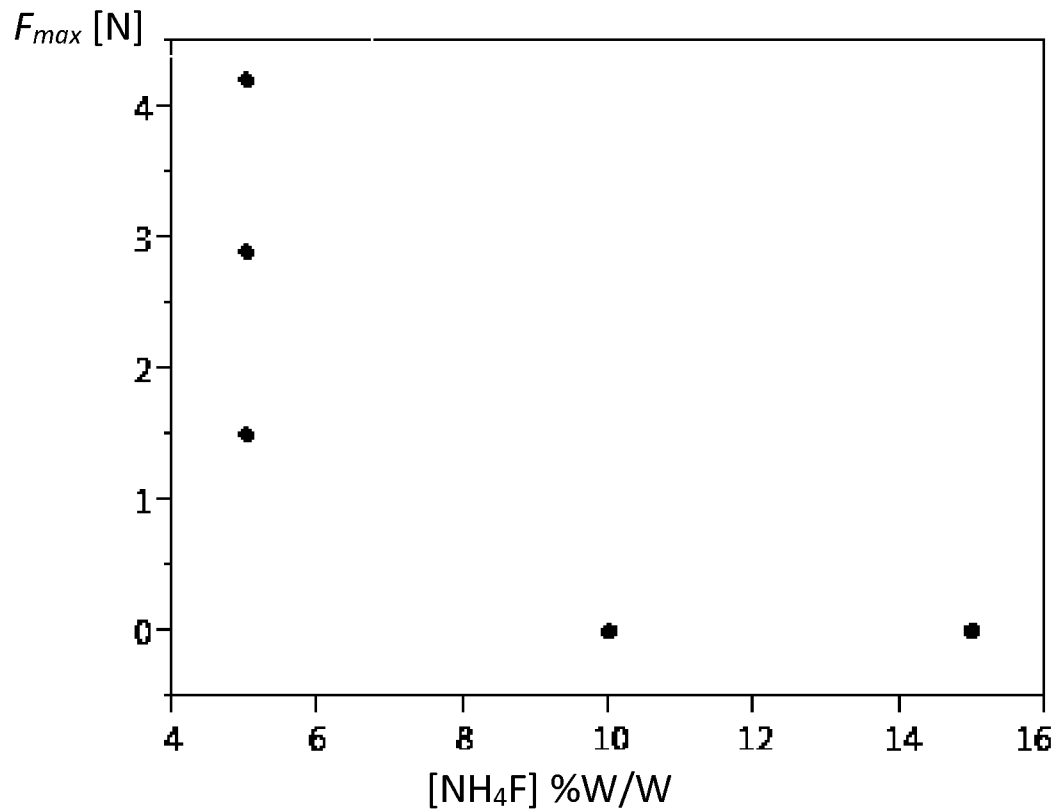


FIG 6

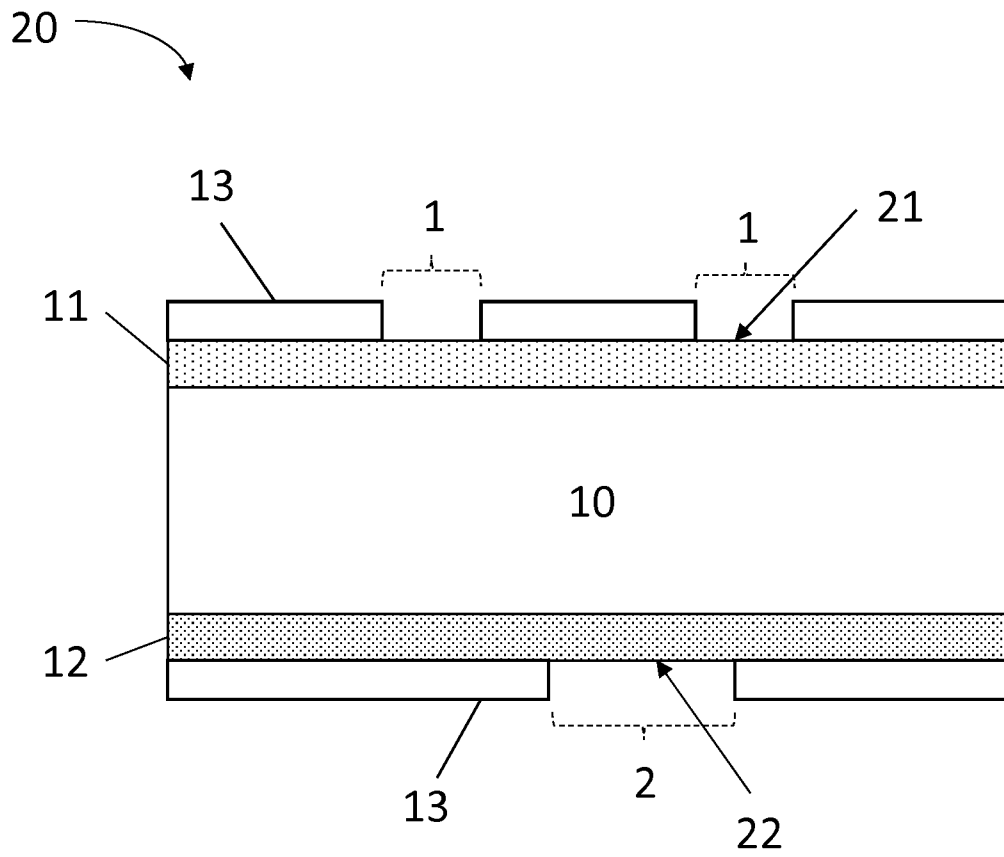


FIG 7

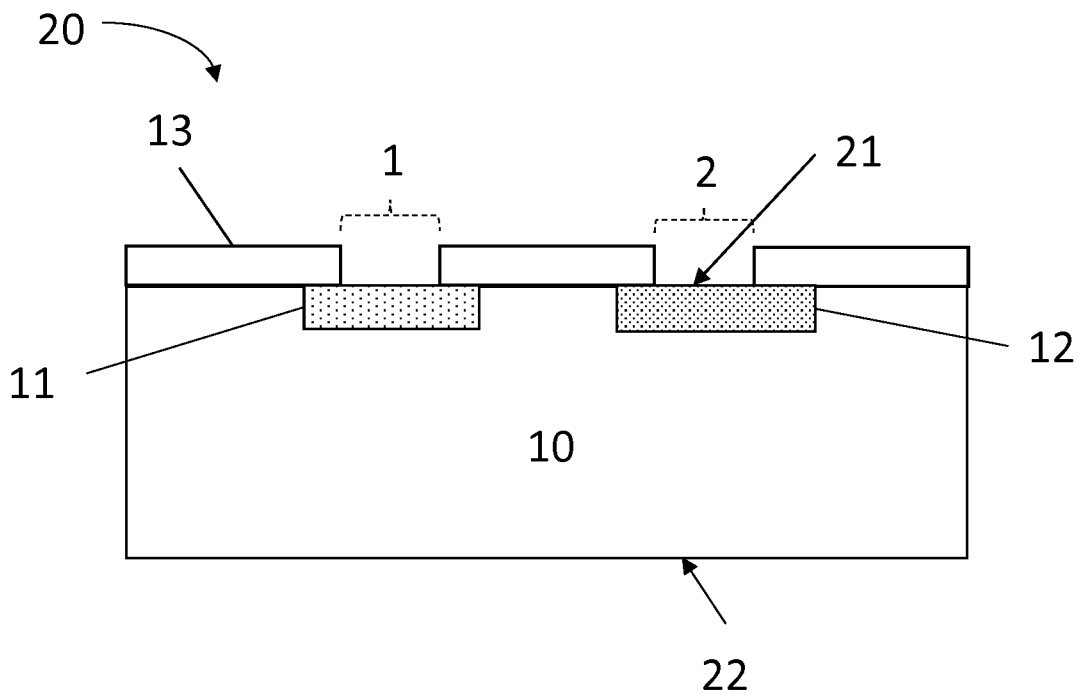


FIG 8

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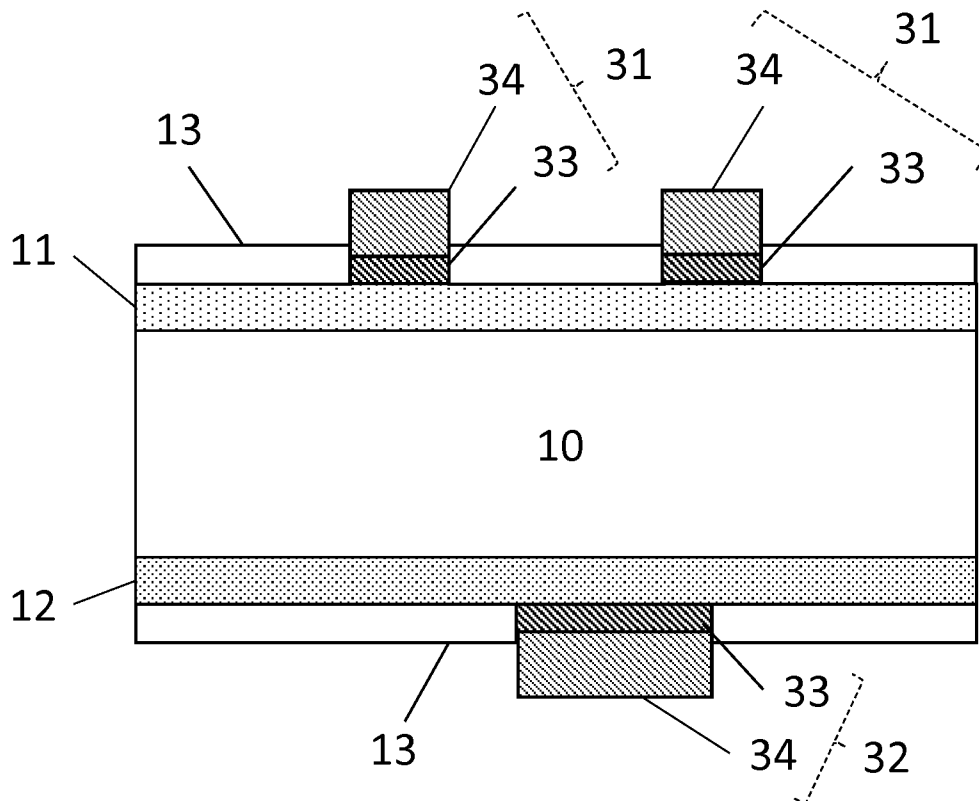


FIG 9

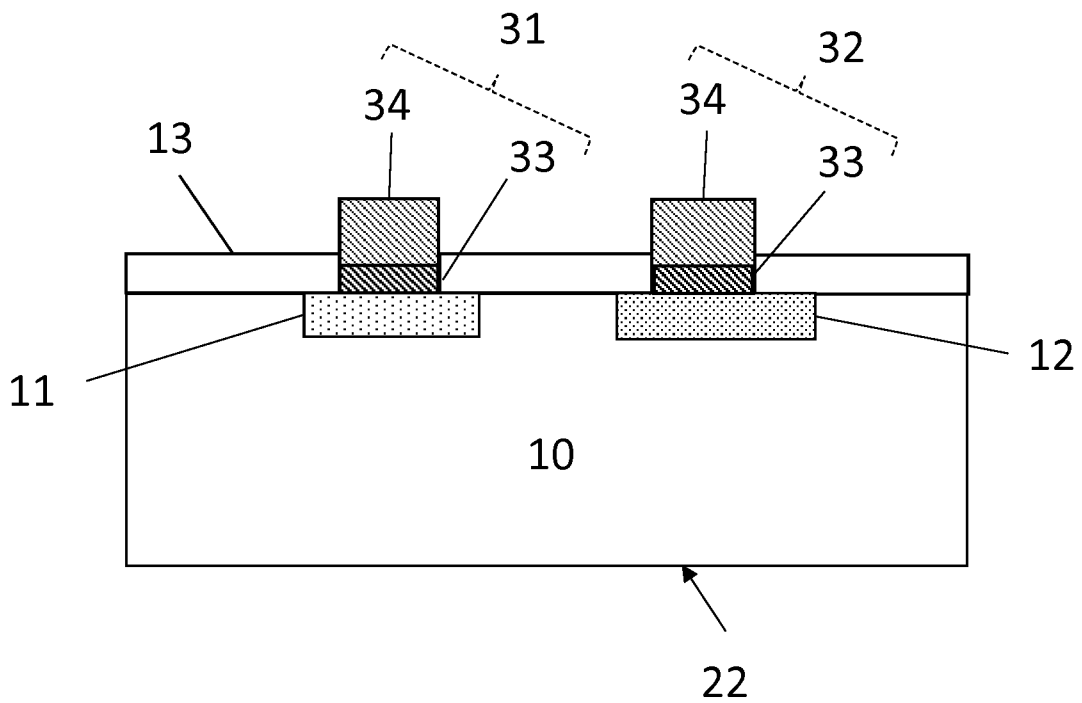
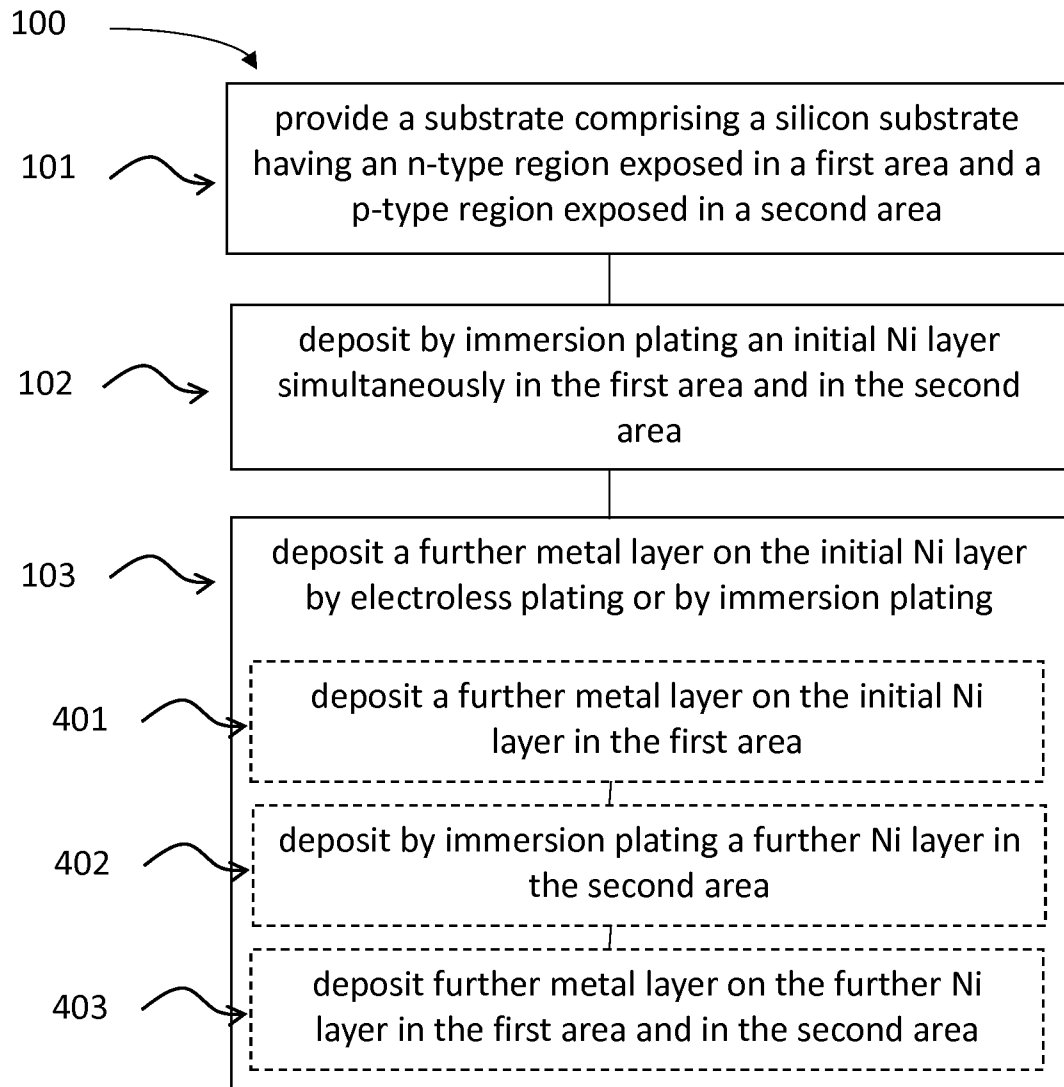


FIG 10

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**FIG 11**

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2016/062602

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/0224
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	abstract; figure 1 page 7, last paragraph - page 14, paragraph first	3,5, 7-11,13, 15,16
Y	----- EP 2 626 891 A2 (ROHM & HAAS ELECT MATERIALS [US]) 14 August 2013 (2013-08-14) abstract paragraphs [0010] - [0014], [0021] - [0034]	7-9
X	----- US 4 321 283 A (PATEL KIRIT B ET AL) 23 March 1982 (1982-03-23)	1-6, 10-16
Y	abstract; figures 4-7 column 2, line 52 - column 3, line 9 column 4, line 59 - column 6, line 27 ----- -/-	3,5,10, 11,13, 15,16



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

31 August 2016

Date of mailing of the international search report

06/09/2016

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Cichos, Anna

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2016/062602

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No

PCT/EP2016/062602

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