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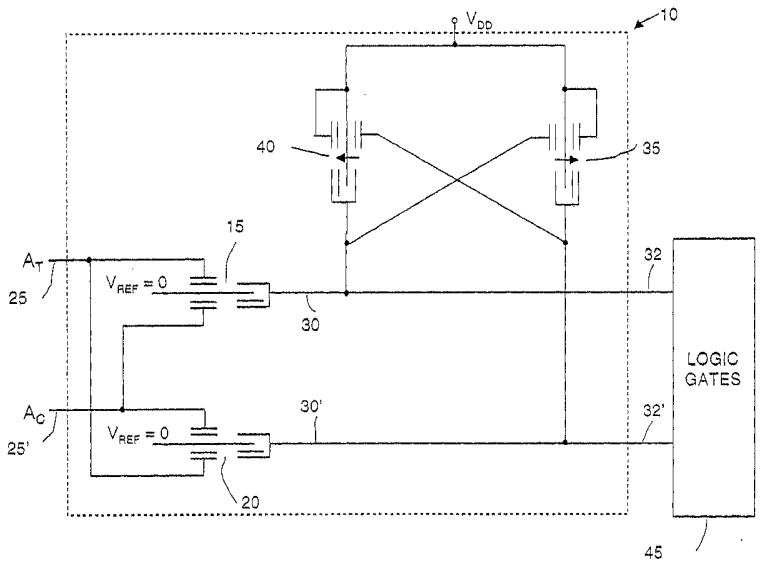
(54) Title: RECEIVER CIRCUIT USING NANOTUBE-BASED SWITCHES AND LOGIC



(57) Abstract: Receiver circuits using nanotube based switches and logic. Preferably, the circuits are dual-rail (differential). A receiver circuit(l0) includes a differential input having a first and second input link (25, 25'), and a differential output having a first and second output link (30, 30'). First, second, third and fourth switching elements (15, 20, 35, 40) each have an input node, an output node, a nanotube channel element, and a control structure disposed in relation to the nanotube channel element to controllably form and unform an electrically conductive channel between said input node and said output node. The receiver circuit can sense small voltage inputs and convert them to larger voltage swings.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC: **H04B 1/06**(2006.01),**1/16**(2006.01);**H03K 19/20**(2006.01);**H01L 21/00**(2006.01)

USPC: 455/254,334;326/115,125;438/48;977/938,940
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 455/254,334;326/115,125;438/48;977/938,940

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IEEE Journals

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPAT, JPO, EPO, DERWENT : nanotube, switches, transistor, sensitivity, detector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, E	US 2005/0282515 (BERTIN) 22 December 2005 (22.12.05), see Fig.1.	1-6
A	US 2004/0067602 A1 (JIN) 08 April 2004 (08.04.04), see entire document.	1-6
A	US 2004/0043527 A1 04 March 2004 (04.03.04), see entire document.	1-6
A	US 6,548,841 B2 (FRAZIER et al) 15 April 2003 (15.04.03), see entire document.	1-6
A	S. AMI and C. JOACHIM, Logic Gate and Memory Cells based on Single C60 Electromechanical Transistor, Institute of Physics Publishing, Nanotechnology 12, 2001, pages 44-52.	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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