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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) Title: SUBSTRATE CAVITY SEMICONDUCTOR PACKAGE

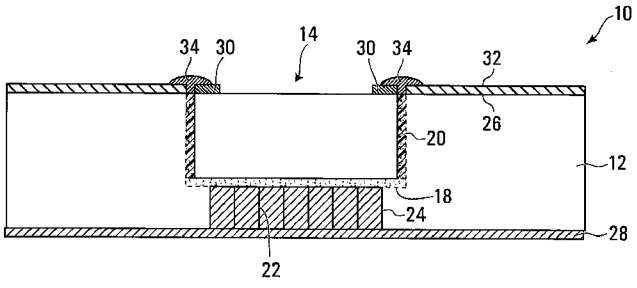


FIG. 1

(57) Abstract: A semiconductor package (10), said package comprising: a substrate (12); a cavity (14) formed within the substrate; a semiconductor chip (16) situated in the cavity. The semiconductor chip comprises a plurality of circuit contacts (30) extending from the semiconductor chip, proximate a periphery of the cavity. Conductive traces (32) are formed on the top surface of the substrate, and electrical interconnections (34) bridge the circuit contacts of the semiconductor chip to the conductive traces of the substrate. Conveniently, the semiconductor chip may be flush with the top surface of the substrate. The circuit contacts may extend from the top surface of the semiconductor chip.

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SUBSTRATE CAVITY SEMICONDUCTOR PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefits from U.S. Provisional Patent Application No. **61/064,316** filed February 27, 2008, the contents of which are hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to semiconductor packages, and more particularly to a semiconductor package with a semiconductor chip mounted within a cavity of a substrate.

BACKGROUND OF THE INVENTION

[0003] Numerous semiconductor packages are known. Typical packages include a semiconductor chip – typically an integrated circuit - attached to a substrate.

[0004] Example attachment techniques include wire bonding the semiconductor chip to the substrate; flip-chip attachment of the semiconductor chip to the substrate; or a building up the substrate to the semiconductor chip.

[0005] Each of these attachment techniques is imperfect. For example, wire bonding requires relatively lengthy interconnects between the semiconductor chip and the substrate. These introduce parasitic inductance interfering with the signal path.

[0006] Similarly, flip-chip attachment introduces capacitive interconnection

paths between the semiconductor chip and substrate.

[0007] Substrate build-up around the integrated circuit requires complex process steps and is not suitable for use with many types of integrative circuits such as sensors and organic electronic devices.

[0008] Accordingly, there is a need for a new semiconductor package.

SUMMARY OF THE INVENTION

[0009] In an exemplary embodiment of the present invention, a semiconductor package, includes a substrate; a cavity formed within the substrate; a semiconductor chip situated in the cavity; the semiconductor chip comprising a plurality of circuit contacts extending from the semiconductor chip, proximate a periphery of the cavity; a conductive layer formed on a top surface of the semiconductor chip; and electrical interconnections bridging the circuit interconnects to the conductive layer. Conveniently, the semiconductor chip may be flush with the top surface of the substrate. The circuit contacts may extend from the top surface of the semiconductor chip.

[0010] Other aspects and features of the present invention will become apparent to those of ordinary skill in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] In the figures which illustrate by way of example only, embodiments of the present invention,

[0012] **FIG. 1** is cross-sectional view of a semiconductor package, exemplary

of an embodiment of the present invention;

[0013] **FIG. 2** is top view of a semiconductor package, exemplary of an embodiment of the present invention;

[0014] **FIG. 3** is cross-sectional view of another semiconductor package, exemplary of an embodiment of the present invention; and

[0015] **FIG. 4** is cross-sectional view of another semiconductor package, exemplary of an embodiment of the present invention.

DETAILED DESCRIPTION

[0016] **FIG.1** illustrates, in cross-section, a semiconductor package **10** exemplary of an embodiment of the present invention. Semiconductor package **10** includes a substrate **12** in which a cavity **14**, extending from a top surface **26** is formed. An integrated circuit in the form of a semiconductor chip **16** is inserted into cavity **14**. A thin adhesive layer **18** may be used to physically bond the integrated circuit **16** into cavity **14**.

[0017] Filler **20**, formed of the same or different material as adhesive layer **18** may fill any gap between the side walls of cavity **14** and semiconductor chip **16**. Filler **20** may be formed of an epoxy.

[0018] A metal layer **24** including thermal vias **22** is formed at the bottom of cavity **14**, and extends to an opposite outer surface **28** of package **10**. Surface **28** may be covered with a metal layer.

[0019] Integrated circuit contacts **30**, located at the periphery of semiconductor chip **16**, proximate the interface between chip **16** and substrate **12**, provide electrical connection to any circuit formed on semiconductor chip **16**. The number of contacts **30** may depend on the nature of any circuit on chip **16**, and may be limited by space available proximate the periphery of the top surface

of chip **16**. Circuit contacts **30** may be formed in number of ways. For example, they may be formed on the top surface of semiconductor chip **16**, as conductive (e.g. metal) pads on semiconductor chip **16**.

[0020] Conductive traces **32** may be printed on top surface **26** of substrate **12** to route electrical signals from and to semiconductor chip **16**. Traces **32** on substrate **12** may interconnect a circuit on chip **16** to other circuits (also on semiconductor chips) provide input/outputs, electric power, or the like. Traces **32** may be formed of metal, such as silver, gold or the like. They may, for example, be ink, that is screen printed, deposited, or jet printed on surface **26**.

[0021] An interconnecting material **34**, such as silver may bridge the connection between contacts **30** on the top surface of integrated circuit chip **16** and traces **32** on top surface **26**.

[0022] Optionally, an encapsulant (not shown) may be formed atop interconnecting material **34** to electrically insulate the interconnecting material, and optionally the entire top surface **26** (including conductive traces **32**) of substrate **12**. Alternatively, interconnecting material **34**, and the remainder of top surface **26** may be separately coated. The encapsulant may be silicon, epoxy or another molding compound.

[0023] Substrate **12** may be formed as a low-temperature co-fired ceramic (LTCC) substrate. As will be appreciated, LTCC techniques allow multiple layers to be processed in parallel and aligned stack immediately prior to firing. Each layer may include conductive material arranged to interconnect chip **16** to an external circuit. Passive components, such as resistors and capacitors, may also be included in one or more of the layers. Conductive vias may interconnect multiple layers.

[0024] As will be appreciated, cavity **14** may be formed with a depth equal to the height (or thickness) of semiconductor chip **16**, and a cross-sectional area equal to larger the size of chip **16**. Cavity **14** may be formed by drilling, laser

cutting or the like in one or more of the multiple layers used to form substrate **12.** As such, chip **16** may in some embodiments be received to be substantially flush with the top surface **26** of substrate **12**, and also generally flush with the interior wall(s) of cavity **14**.

[0025] Conveniently, as the top surface of semiconductor chip **16** may be generally flush with the top surface **26** of substrate **12**, the top surface of chip **16** may be exposed, allowing chip **16** to act as a light source (such as a light emitting diode, laser, or the like), a micro-electrical mechanical system (a MEMS device), a sensor or the like. Conveniently, heat generated by chip **16** may be dissipated through thermal vias **22**, and metal layer **24** to surface **28.**

[0026] As required, top surface **26** of substrate **12** may be encapsulated and thus hermetically sealed or waterproofed. Conveniently, inexpensive ink jetting/dispensing or screen printing may provide traces to interconnect the integrated circuit on the substrate.

[0027] As will be appreciated, substrate **12** may contain several integrated circuit chips, interconnected to each other by traces **32**. To this end, **FIG. 2** depicts a semiconductor package **110** (like package **10** – **FIG. 1**), exemplary of an embodiment of the present invention. Semiconductor package **110** includes a substrate **112** (like substrate **12**), having a plurality of cavities **114**. Each cavity **114** receives a semiconductor chip **116**, and may be interconnected with the cavity **114** in the same way semiconductor chip **16** is interconnected with cavity **14** – **FIG. 1**. Each semiconductor chip **116** includes at least one contact point **130**, bridged to traces **132** (like traces **32**) formed atop the surface of substrate **112**. The multiple semiconductor chips **116** are electrically interconnected by these traces **114**. In the depicted embodiment, each semiconductor chip **116** contains one or more individual light emitting diodes (LED). In the depicted embodment, the multiple semiconductor chips **116** – and LEDs are interconnected in series, with the anode of one LED interconnected with the cathode of an adjacent LED. As will be readily appreciated, the nature or semi-

conductor chips **116** and the number and types of interconnects may vary from application to application.

[0028] Conveniently, a metal layer and metal vias (like metal layer **24** and vias **22 – FIG. 1**) may be formed beneath each cavity **114** to guide heat from semiconductor chips **116** to the bottom surface of substrate **112**.

[0029] In yet another alternate embodiment, depicted in **FIG. 3**, a semiconductor package **210** includes a substrate **212** in which a cavity **214** is formed. Again, an integrated circuit in the form of a semiconductor chip **216** is inserted into cavity **214** and a thin adhesive layer **218** may be used to bond the semiconductor chip **216** into cavity **214**. Again, filler **220** (like filler **20**), formed of the same or different material as adhesive layer **218** may fill any gap between the side walls of cavity **214** and semiconductor chip **216**. Filler **220** may be formed of an epoxy.

[0030] Integrated circuit contacts **230** located at the periphery of chip **216**, proximate the interface between chip **216** and substrate **212** provide electrical connection to any circuit formed on chip **216**.

[0031] Conductive traces **232** may be printed on the top surface of substrate **212** to route electrical signals from and to chip **216**. Traces **232**, however, lead to metal vias **242** extending into substrate **212**. Formed within substrate **212** is an inner conductive layer **240** that may interconnect integrated chip **216** to other integrated circuits, provide input/outputs, electric power, or the like.

[0032] An interconnecting material **234**, such as silver, gold or other suitable conductive material may bridge the connection between contacts **230** on the top surface of integrated circuit chip **216** and traces **232** on the top surface of substrate **212**. An encapsulant **250** may be formed atop interconnecting material **234** to electrically insulate the interconnecting material **234**.

[0033] Further metal vias **248** may extend from layer **240** to interconnection points on the top or bottom surface of substrate **212**, at a location distant from

chip **216**. These may allow for interconnection of semiconductor package to an external circuit. In the depicted embodiment, vias **248** extend to connectors **252** proximate an edge of semiconductor package **210**.

[0034] Substrate **212** may again be formed as an LTCC substrate. As will be appreciated, cavity **214** may again be formed with a size equal to chip **216** – and in particular having a depth equal to the height (or thickness) of chip **216**. As such, chip **216** may be received to be flush with the top surface of substrate **212**. In the depicted embodiment, semiconductor chip **216** may take the form of a sensor, having a sensing area exposed on the top surface of semiconductor package **200**. The sensor may be an optical, chemical, or other sensor.

[0035] Again, semiconductor package **200** may be generally waterproof – heremetically sealed by encapsulant **250**, while layer **240** is sealed by the remainder of substrate **212.**

[0036] In yet a further embodiment depicted in **FIG. 4**, a semiconductor package **200'** like semiconductor package **200** (**FIG. 3**) may include a semiconductor chip **216'** in a cavity **214'** retained by adhesive layer **218'** and filler **220'**. A conducting layer **240'** (like conducting layer **240**) is formed within substrate **212'**. Vias **242'** extend from the top surface **226'** of substrate **210'** to layer **240'**. A further set of vias **260** extend from layer **240'** to the opposite (bottom) surface **228'** to a connector **262**. Connector **262** may be a surface mount (SMT) connector.

[0037] Of course, the above described embodiments, are intended to be illustrative only and in no way limiting. The described embodiments of carrying out the invention, are susceptible to many modifications of form, arrangement of parts, details and order of operation. The invention, rather, is intended to encompass all such modification within its scope, as defined by the claims.

WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

   a substrate;

   a cavity formed within said substrate;

   a semiconductor chip situated in said cavity; said semiconductor chip comprising a plurality of circuit contacts extending from said semiconductor chip, proximate a periphery of said cavity;

   a conductive layer formed on a top surface of said semiconductor chip; and

   electrical interconnections bridging said circuit interconnects to said conductive layer.

2. The semiconductor package of claim 1, wherein said circuit contacts extend from a top surface of said semiconductor chip.

3. The semiconductor package of claim 1 or 2, wherein said cavity has a depth equal to the height of said semiconductor chip.

4. The semiconductor package of any one of claims 1 to 3, wherein said top surface of said semiconductor chip is generally flush with said top surface of said substrate.

5. The semiconductor package of any one of claims 1 to 4, wherein said circuit contacts are formed near a periphery of said semiconductor chip.

6. The semiconductor package of any one of claims 1 to 4, wherein said conductive layer is printed on said top surface of said substrate.

7. The semiconductor package of any one of claims 1 to 4, wherein said conductive layer is jet-printed on said top surface of said substrate.

8. The semiconductor package any one of claims 1 to 7, further comprising a metal layer extending from a bottom of said cavity to a bottom of said semiconductor package.

9. The semiconductor package of claim 8, wherein said bottom of said semiconductor package is covered with metal.

10. The semiconductor package of claim 8, wherein said metal layer comprises thermal vias.

11. The semiconductor package of any one of claims 1 to 10, comprising an encapsulant formed atop of said top surface of said substrate to insulate said electrical interconnections.

12. The semiconductor package of any one of claims 1 to 11, wherein said semiconductor chip comprises an optical light source, a sensor, or a MEMs device.

13. The semiconductor package of any one of claims 1 to 12, wherein said substrate is formed as low temperature co-fired ceramic.

14. The semiconductor package of any one of claims 1 to 13, further comprising at least one additional cavity, and at least one additional semiconductor chip in said additional cavity, said additional semiconductor chip comprising a plurality of circuit interconnects extending from a top surface of said additional semiconductor chip, interconnected with said conductive layer.

15. The semiconductor package of claim 14, wherein said conductive layer electrically interconnects said semiconductor chip and said additional semiconductor chip.

16. The semiconductor package of any one of claims 1 to 15, further comprising a conductive layer formed within said substrate, and at least one conductive via extending from a said conductive layer formed on said top surface to said conductive layer formed within said substrate.

17. The semiconductor package of claim 16, further comprising at least one connector mounted on a top or bottom surface of said substrate, and interconnected with said conductive layer formed within said substrate.

18. The semiconductor package of any one of claims 1 to 17, further comprising an adhesive to glue said semiconductor chip to said substrate.

19. The semiconductor package of any one of claims 1 to 18, further comprising a filler to fill any volume between an outer wall of said cavity and said semiconductor chip.

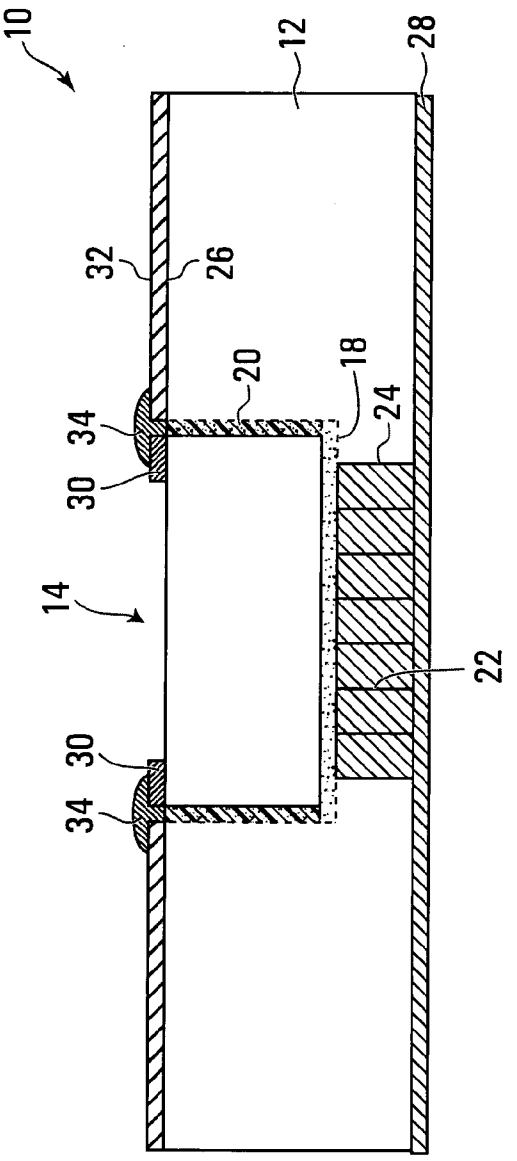


FIG. 1

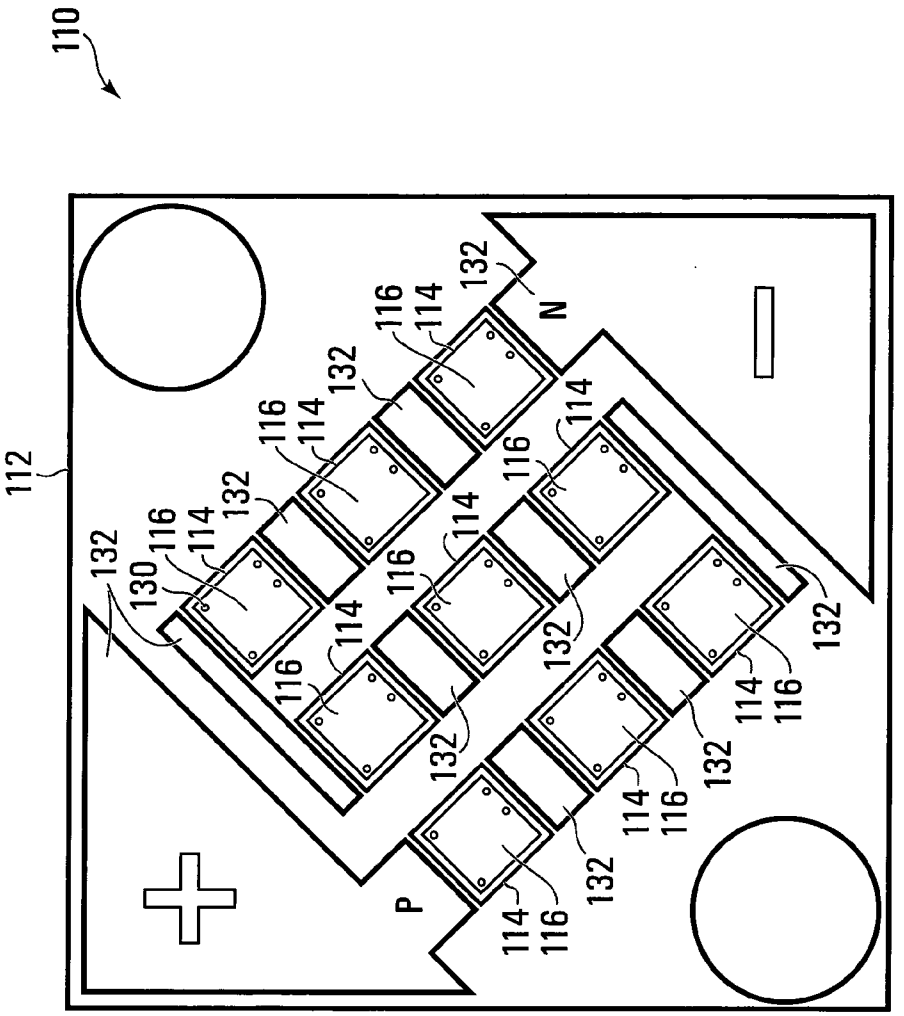


FIG. 2

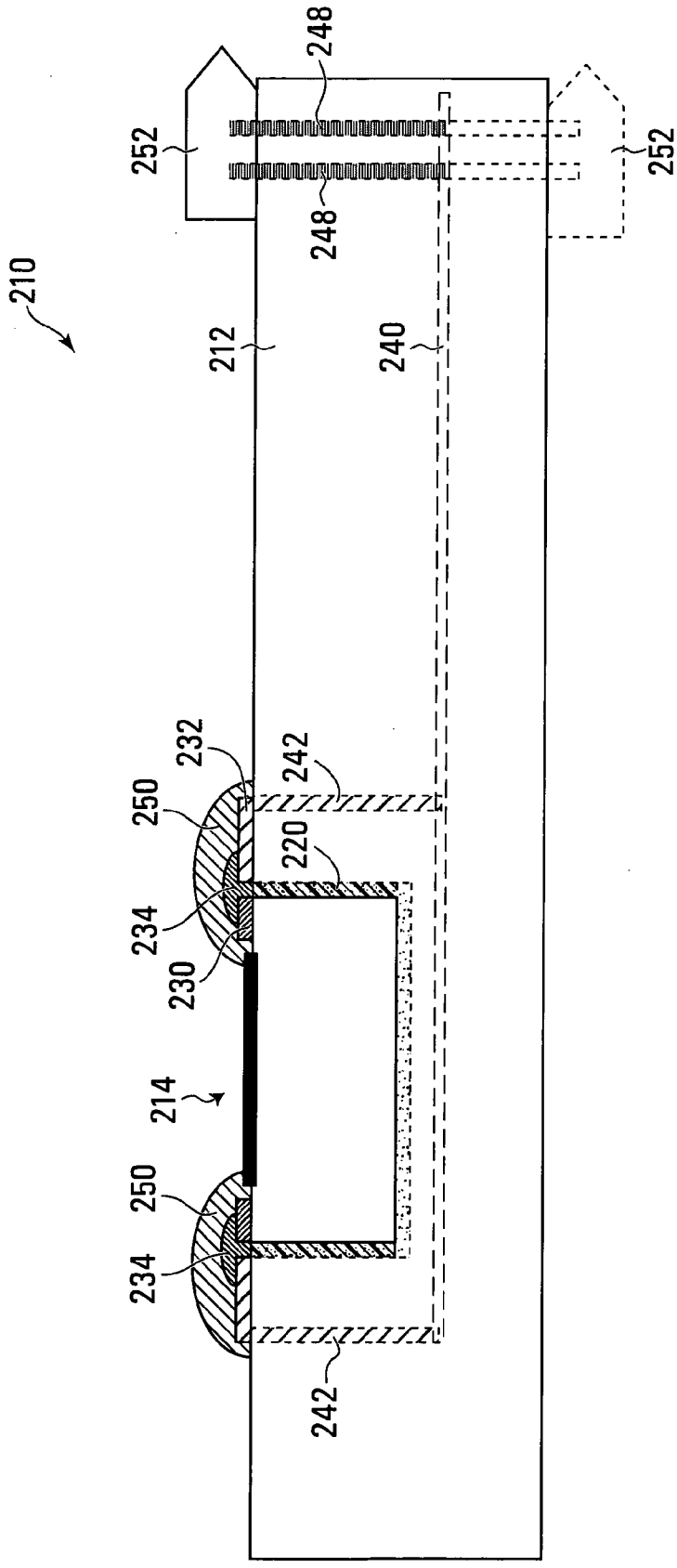

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FIG. 3

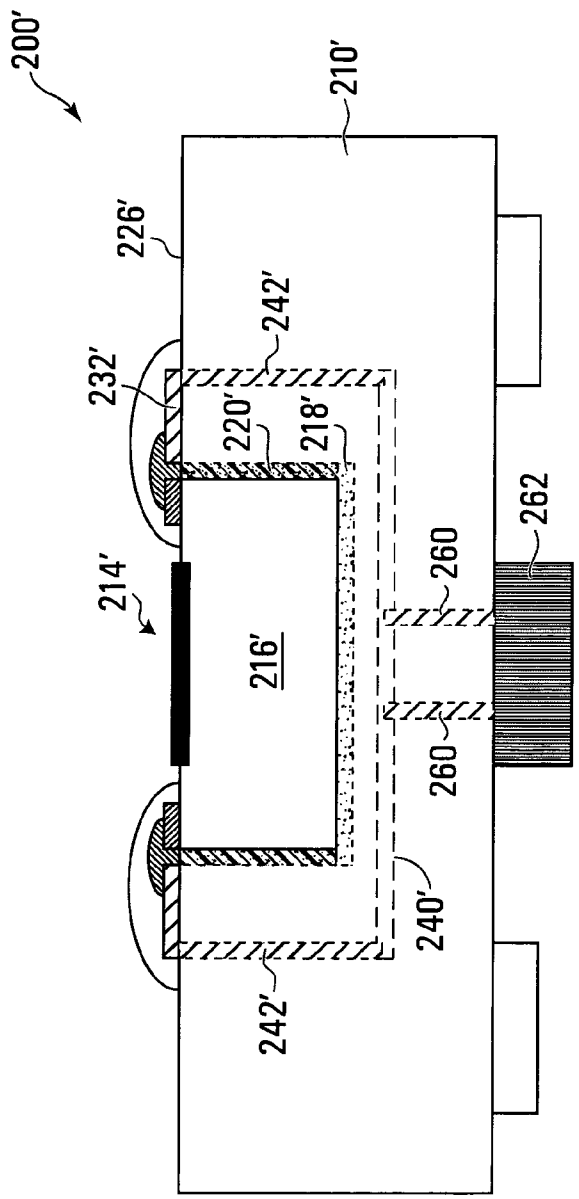


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2009/000076

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 23/02(2009.01) ***H01L 23/34***(2009.01) ***H01L 23/48***(2009.01) ***H01L 23/52***(2009.01) ***H01L 25/00***(2009.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPODOC (H01L/ec, packag+ or assembl+, substrate or csp, cavit+ or recess+ or hollow+ or well+, heat+ or metal+ or thermal+, sink+ or via+ or bridg+ or hole+), WPI (H01L/ic, packag+, substrate+ or csp+, cavit+ or recess+ or hollow+ or well+, heat+ or metal+ or thermal+, sink+ or via+ or bridg+ or hole+).

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages. In some instances, only the references to relevant figures are indicated.	Relevant to claim No.
X	US4999740 A (ILARDI et al) 12 March 1991 Figures 1 to 5. Columns 1, 2, 4 and 5.	1-5, 8, 9, 11, 14-16, 19.
Y		6, 7, 10, 12, 13, 17, 18.
X	US5397917 A (OMMEN et al) 14 March 1995 Figure 1. Columns 1 and 3 to 5.	1-6, 18.
Y		6, 18.
X	EP1727192 A1 (ITO et al) 29 November 2006 Figures 3A to 3E. Paragraphs [0002], [0039], [0057] to [0061] and [0069].	1-3, 5-7.
Y		7

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 April 2009	09 JUN 2009

Name and mailing address of the ISA/AU	Authorized officer
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INTERNATIONAL SEARCH REPORT	International application No. PCT/SG2009/000076

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US5991162 A (SASO) 23 November 1999 Figures 1(a) and 1(b). Columns 3 to 5.	1, 5, 8, 10.
Y		10.
X	EP1487019 A1 (Koninklijke Philips Electronics N.V.) 15 December 2004 Figures 1, 2, 7 and 23. Paragraphs [0011], [0022], [0058], [0061], [0067] and [0078] to [0081].	1, 2, 3, 5, 12.
Y		12.
X	EP0786806 A1 (COOPPENS et al) 30 July 1997 Figures 1 to 3 and 4A to 4D. Columns 1 and 5 to 7.	1-5, 13.
Y		13.
X	US6175497 B1 (TSENG et al) 16 January 2001 Figures 2 and 3. Column 3.	1, 2, 5, 16, 17.
Y		17.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2009/000076

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	4999740	WO	1990/010951	CA	2011164		
US	5397917		NONE				
EP	1727192	US	2006263930	JP	2006332094	CN	1870860
		KR	20060121100				
US	5991162	JP	11017349	JP	2950290	CN	1208959
		CN	1146990				
EP	1487019	WO	2004/112134	US	2006131736	US	7098530
		EP	1636843	JP	2006527499	CN	1802746
		CN	100456468				
EP	0786806		NONE				
US	6175497	JP	2000114436	JP	3895880	TW	399309

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX