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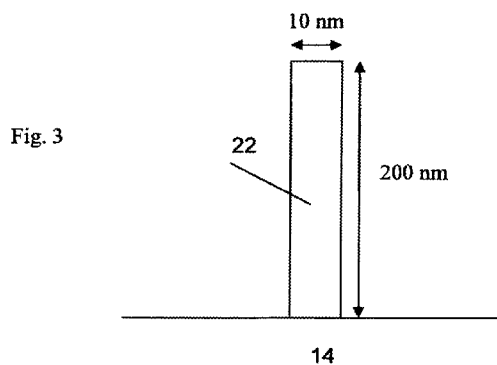
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(54) Title: METHOD OF FABRICATING NANO-RESISTORS



(57) Abstract: The present invention describes a novel method of fabricating nano-resistors (22) which allows full integration with standard CMOS fabrication process. The resistor comprises long and thin nano-structures as resistive element. It is formed by conductive nano-spacers (18B) on insulating layer. An embodiment of such structure is polysilicon nano-structures doped or implanted with n-type or p-type ions (20) to improve material conductance. The electrical properties of the device will change with respect to the dimension of these nano-structures. Resistors with polysilicon nano-structures down to 10 nm can be produced with resulting measured resistance in the MOhm scale.

Description

Title of Invention: **METHOD OF FABRICATING NANO-RESISTORS**

Technical Field

- [1] The present invention relates generally to resistors, more particularly to resistors within the nano-scale range.

Background Art

- [2] It is a trend for semiconductor devices to be getting smaller, so that it can be packed along as high density devices. The availability of nanotechnology allows further miniaturization of device such as sensors to improve sensitivity, robustness and performance. The miniaturized device has potential applications in integrated circuits and semiconductor based sensors for precision agriculture, aquaculture, environmental and biomedical applications. Integrated as a sensor, the nano-resistors can act as a resistive heating element to activate sensor membrane to detect selective ions. The performance of sensing membranes can improve significantly with temperature activation.
- [3] In some semiconductor devices, resistors are lithographically patterned in the plane of the semiconductor substrate to create a circuit element. Circuits made of such elements are usually low density application.
- [4] US 2003062590 describe a vertically oriented nano-circuit element which includes resistors for significant densities to be achieved. The vertically oriented nano-circuit can be fabricated using standard known process such as Damascene, wet etching, reactive etching, etc. In one aspect of the invention, the nano-circuit may include a top conductor extending in a first direction and a bottom conductor extending in a second direction. The top and bottom conductors may define an overlap, and the two conductors may be electrically connected. The vertically oriented nano-circuit may include a vertically oriented conductive spacer formed between the top and bottom conductors in an overlap region. The conductive spacer may be electrically connected with both top and bottom conductors.
- [5] An improved method of fabricating nano-resistors is desired to be achieved without high resolution lithographic equipment. The method should be part of standard CMOS process to minimize the cost of fabrication.

Summary of Invention

- [6] The present invention describes a novel method of fabricating nano-resistors which allows full integration with standard CMOS fabrication process. The resistor comprises long and thin nano-structures as resistive element. It is formed by conductive nano-spacers on insulating layer. An embodiment of such structure is polysilicon nano-

structures doped or implanted with n-type or p-type ions to improve material conductance. The electrical properties of the device will change with respect to the dimension of these nano-structures. Resistors with polysilicon nano-structures down to 10 nm can be produced with resulting measured resistance in the MOhm scale. The resistance of the device will also change linearly with respect to the length of the nano-structures.

- [7] The main feature of the method is the utilization of spacer technique to form the nano-resistor structure. Resistance property is dependant on dimension and ratio aspect of the structure. The nano-resistor can be fabricated directly onto an insulating layer or onto a non-conductive type substrate. The resistor material is not limited to doped silicon and metals.

Description of Drawings

- [8] The invention will now be described in greater detail, by way of an example, with reference to the accompanying drawings, in which:
- [9] Fig. 1(a) to 1(g) show sectional views of nano-resistor fabrication according to the invention;
- [10] Fig. 2 shows a graph showing a relationship between resistance and length of wire for 50 nm polysilicon device and 100 nm polysilicon device;
- [11] Fig. 3 shows a sectional view of a nano-resistor with ratio aspect of 20:1; and
- [12] Fig. 4 shows a diagram of an array of sensors with nanoresistive hotplate.

Description of Embodiments

- [13] Miniaturization of semiconductor device is a challenge. This device must not only be smaller in size, but also needs to have improved robustness and performance. Nano-resistors have potential applications in integrated circuit devices, especially in nano-electromechanical systems. In nano-electromechanical systems, the resistive device can be used as a platform to active metallic or metallic oxide nano-wires for sensing applications, in particular gas sensors for environmental monitoring.
- [14] A method of fabricating nano-resistors using conventional CMOS fabrication process is described in this disclosure. A main component of the resistive device constitutes of long nano-wires. The resolution of the wires is defined by the deposition process and not by high end lithographic tools such as deep ultraviolet, extreme ultraviolet, electron beam lithography, x-ray lithography or nano-imprint lithography.
- [15] A typical fabrication process of nano-resistors is shown in Fig. 1A to 1G. Only two lithographic masks are required to perform this process. First a nitride layer 12 is deposited onto the substrate 14 which acts as an insulating layer between resistive device and the underlying substrate. This is followed by deposition of an oxide layer 16. The oxide layer is then lithographically patterned and etched so that it is selectively

placed on top of insulator layer as a mould for nano-resistors. A layer of conductor 18 which is preferably polysilicon is then deposited onto the layered surface of insulating oxide and nitride layer. The polysilicon layer will be used to form the final resistor structure. Thickness of the deposited oxide will depend on the final dimension of the required resistive structures. For example, to produce 10 nm nano-resistors, a polysilicon thickness of 10 nm will be required. The deposited polysilicon layer is then doped or implanted with n-type or p-type ions 20 to produce an improved conductive layer 18A. Then the polysilicon layer is etched to form conductor spacer of resistor structures 18B and contact pads 16A. Finally the oxide layer between conductive spacer is removed to form the final resistor device 22. This oxide layer can be removed by plasma etching of hydrofluoric acid.

- [16] The fabrication process of the nano-resistors is CMOS compatible so that it can be easily integrated with other semiconductor circuit and devices. The main features of this process are cost effective fabrication without the use of state-of-the-art equipments. There is no lithography imposed limitation involved. The resistive nano-wires produced have high resolution with good alignment. The proposed set of process allows rapid prototyping, hence the resistor device can be mass manufactured at typical semiconductor foundry.
- [17] The fabricated nano-resistors of 50 nm and 100 nm are tested and compared for resistance properties. Different lengths of resistive wires produce resistance in the range of tenths to hundredths of kOhm, as shown in Fig. 2. For resistors with nano-wires as thin as 10 nm or 20 nm, the device resistance was found to increase significantly, typically in the region of MOhm. The resistance of the device was found to be typically linearly dependent on the length to nano-wires.
- [18] The nano-resistors formed can be of parallel wires or coil type. The nano-resistor is three-dimensional with aspect ratio of at least 20:1, as shown in Fig. 3. The aspect ratio usually refers to the ratio of height over width of a nano-structure. The resistance value of the device is tuned by varying the structural thickness.
- [19] For sensor applications, the nano-resistors heats up to very high temperatures when current are applied. The nano-resistors can also be operated as a temperature sensor where the electrical resistance of the nano-structured device changes with temperature. Typically the resistance changes linearly with increasing or decreasing temperature. These sensors can be used in environmental, device, or body temperature monitoring.
- [20] The device can be adapted to act as a nano-hotplate to activate ion sensitive membrane. By miniaturizing micro-hotplate to nano-hotplate, an array of sensors can be integrated in a micro area to increase device sensitivity or used to sense multiple ions. Typically for these type of sensors, ion sensitive membrane or structures (not shown) are formed on top of the nano-hotplate 24. During device operation, current I_h

is applied to the nano-hotplate to provide point heating to the membrane or structures on the upper layer. The sensitivity of these structures to selective ions are dependent on temperature which can be in the region between room temperature to hundredths of degree Celsius. By connecting multiple nano-hotplates with different individual types of membrane on the upper surface, a sensor system which can detect various types of ions is formed.

- [21] Accordingly, the invention disclosed a method to fabricate nano-resistors. It is the combination of the above features and its technical advantages give rise to the uniqueness of such invention. Although the descriptions above contain much specificity, these should not be construed as limiting the scope of the embodiment but as merely providing illustrations of some of the presently preferred embodiments.

Claims

- [Claim 1] A method of fabricating nano-resistors (22), comprising:
depositing a layer of conductor (18) on top of layered surface, said conductor thickness having measured in the range of nanometers;
forming conductor spacer (18B) by selectively etching part of the conductor; and
etching the space between conductor spacer;
characterized in that;
the conductor is polysilicon material.
- [Claim 2] A method of claim 1, wherein the layered surface is formed by a layer of insulator (12) on top of a substrate (14) and a layer of oxide (16) selectively placed on top of insulator layer as a mould for nano-resistors.
- [Claim 3] A method of claim 2, wherein the insulator layer (12) is preferably a nitride layer.
- [Claim 4] A method of claim 1, wherein the conductive layer (18) is doped with n-type or p-type ions (20).
- [Claim 5] A method of claim 1, wherein the nano-resistors (22) is three-dimensional with aspect ratio of at least 20:1.
- [Claim 6] A method of claim 1, wherein the nano-resistor (22) is adapted as temperature sensor.
- [Claim 7] A method of claim 1, wherein the nano-resistor (22) is adapted as nano-hotplate (24) to activate ion sensitive membrane.

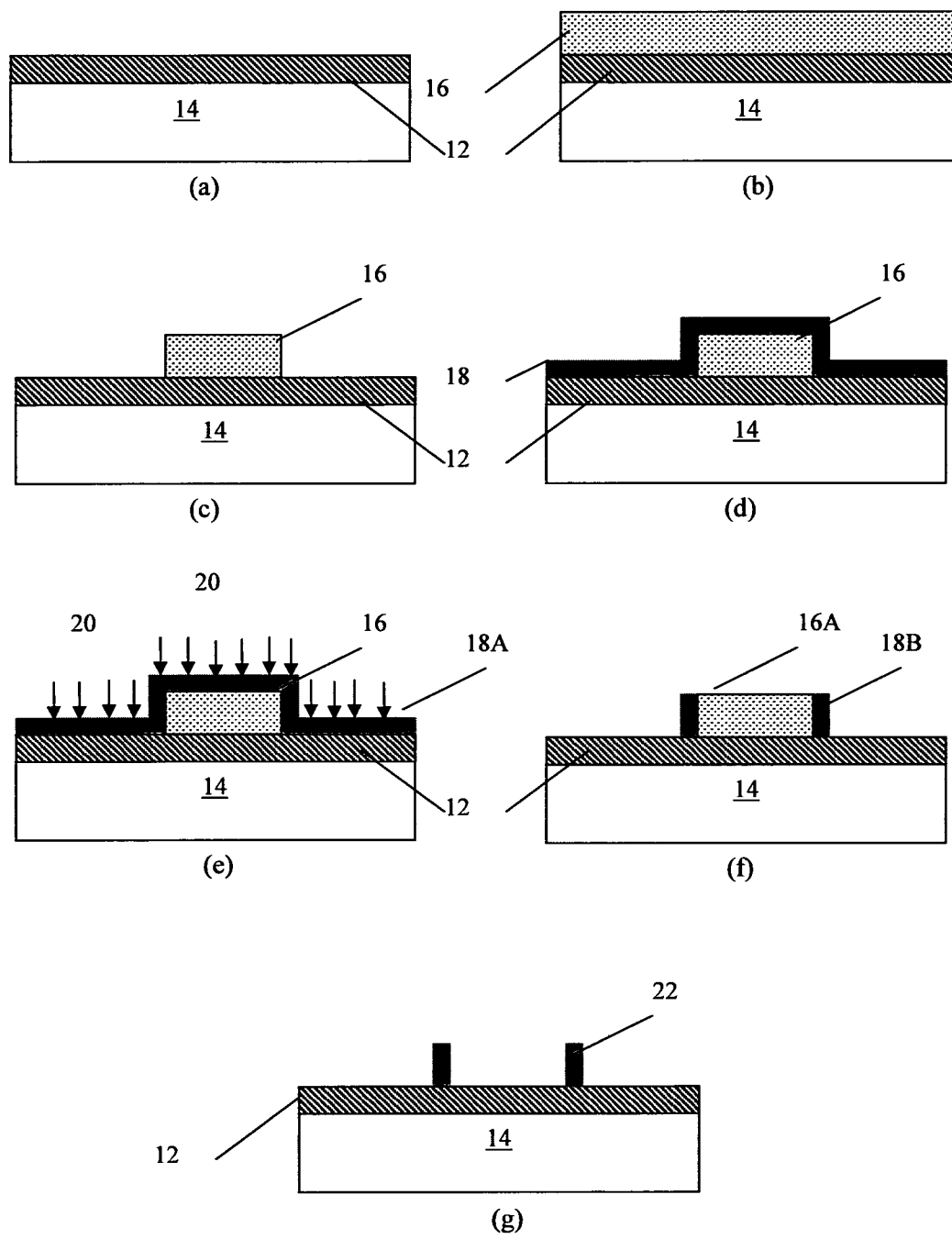


Fig. 1

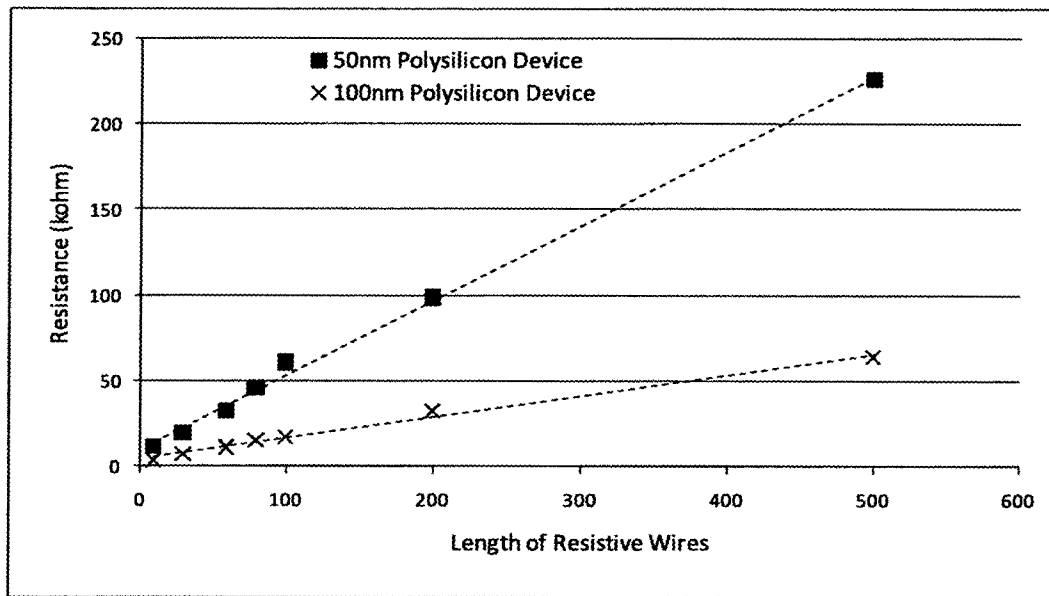


Fig. 2

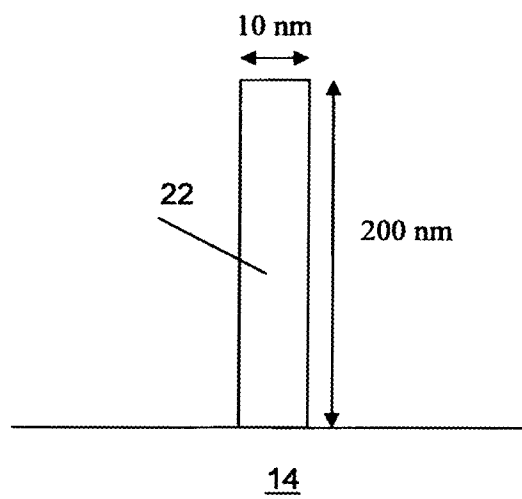


Fig. 3

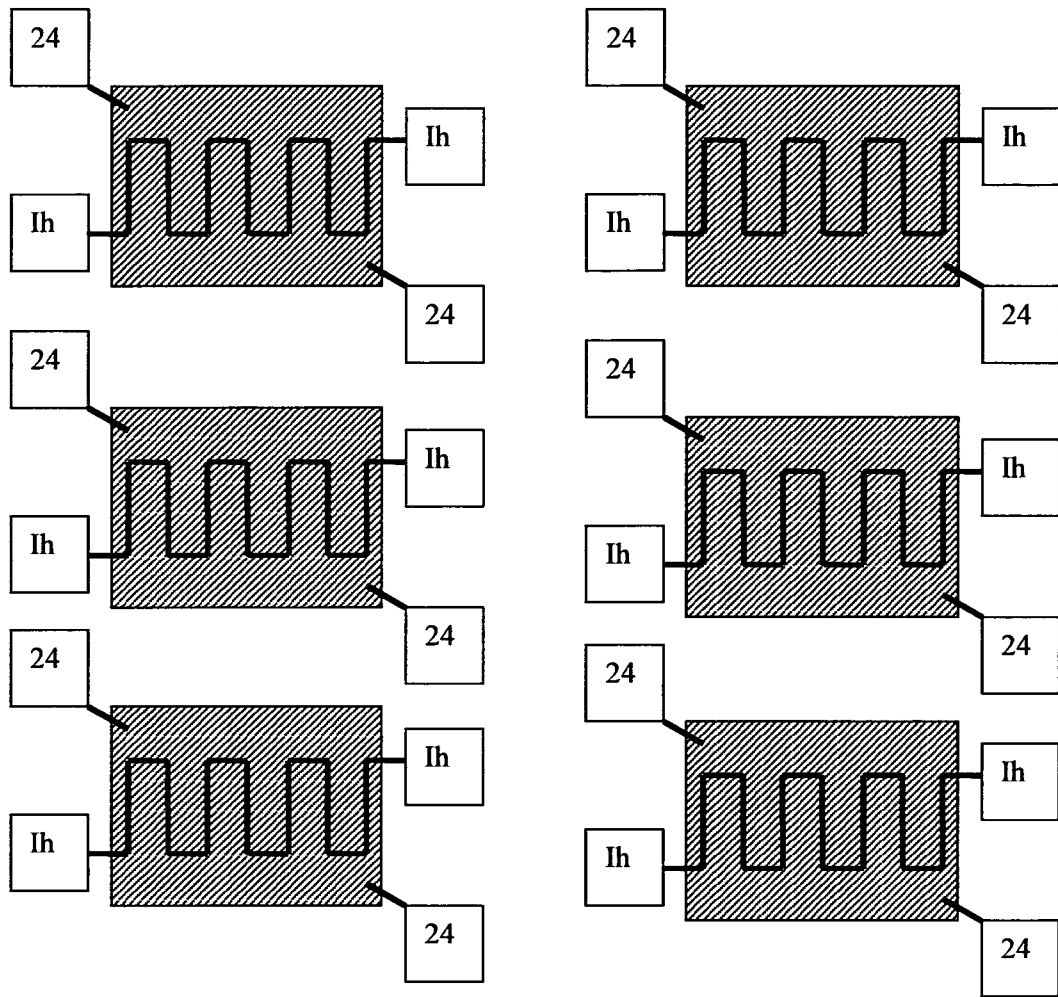


Fig. 4