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(54) **Title**: FEC FRAME HEADER DESIGN FOR CABLE TELEVISION SIGNALS

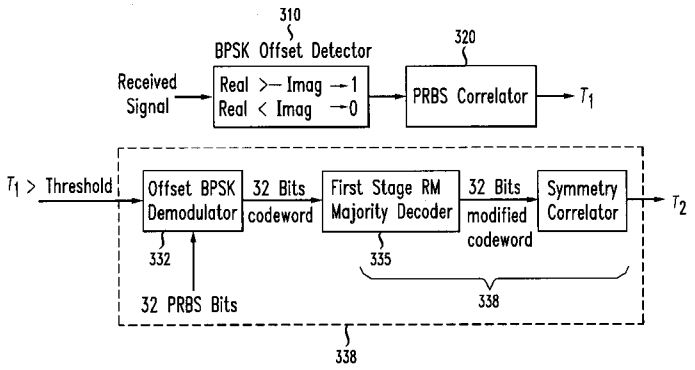


FIG. 3

(57) **Abstract**: An efficient and reliable encoding method suitable for header information in a digital cable television transmission system is provided. An embodiment is shown for FEC frame headers in a DVB-C2 standard, along with the detection algorithm for the FEC header. In the DVB-C2 Standard, Adaptive Coding and Modulation (ACM) or Variable Coding and Modulation (VCM) is applied to each FEC block to provide as much flexibility as possible. As a result, a frame header is attached in front of each FEC frame to inform the coding rate, modulation type and physical layer pipe identifier. Besides the signaling of physical layer related information, the FEC frame header has to provide a structure so that it can be easily and reliably detected in the receiver. Motivated by the need in DVB-C2 Standard, an efficient and reliable method and apparatus to encode the FEC header for DVB-C2 Standard is provided in at least one implementation in this disclosure. In addition, the detection algorithm of the FEC header is described.

WO 2010/056363 A1

FEC FRAME HEADER DESIGN FOR CABLE TELEVISION SIGNALS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application Serial No. 61/115123, filed November 17, 2008, which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

The present principles relate to cable transmission systems and techniques. More particularly, it relates to an FEC header design for cable television transmissions.

BACKGROUND OF THE INVENTION

Cable, satellite and terrestrial networks are three major mediums to deliver digital broadcasting services to end customers. Unlike satellite and terrestrial transmission, cable channels do not exhibit significant time and frequency selectivity. Consequently, spectrally efficient modulations (i.e., 256-QAM and 1024-QAM), are employed in cable networks to meet the capacity demand of bandwidth-consuming services such as HDTV and VoD, and to boost the penetration of digital video broadcasting. Recently, low-density parity-check (LDPC) codes have been introduced in DVB-S2 and DVB-T2 standards because of their design flexibility, decoding simplicity and the universally excellent error correction performance over various channel types.

LDPC codes are a class of Forward Error Correction (FEC) block codes, often used in transmission environments to protect audio and/or video data. These Forward Error Correction codes increase the possibility of receivers recovering from and correcting errors in a received multimedia stream, without the need to retransmit data that is received with errors. The FEC error control system requires the transmitter add redundant data to a data stream. The maximum fraction of errors that can be corrected by the FEC is determined by the way the error correction code is calculated. Examples of FEC are block codes such as LDPC codes, that work on fixed-sized blocks, packets

of bits, or symbols of a predetermined size, and convolutional codes that work on bit or symbol streams of arbitrary length. Many types of block error correction codes exist, among which are Reed-Solomon or, as already mentioned, the LDPC (Low-Density Parity Check). Other types of error correction codes have been developed for specific use in transmission of digital video streams over IP networks, such as SMPTE 2022 (Society of Motion Picture and Television Engineers), which unlike other typical FEC schemes such as Reed-Solomon, relies on very simple algorithms, and is useful in environments where limited resources are available, such as a Set Top Box receiver for Digital Television.

The Forward Error Correction codes are calculated during transmission time, so as to protect the multimedia stream as it is transmitted over a network, including any supplementary data added for the transmission. However, calculating error correction codes is demanding in terms of calculation resources. Therefore, in practice, error correction codes are generated for multimedia data to be transmitted in a broadcast-like manner, that is, when the same multimedia data can serve many receivers simultaneously. Examples of broadcast networks besides cable networks are TV/radio satellite or terrestrial broadcasting or IP multicast over wired or wireless transport media.

As a result of LDPC codes, frameworks such as, for example, density evolution, differential evolution and extrinsic information transfer (EXIT) charts, have been invoked to design and analyze the degree profile of a code ensemble. In terms of the threshold Signal-to-Noise Ratio (SNR) for decoding convergence, codes constructed following these frameworks can approach the Shannon limit closely, assuming the block length is infinite, the code structure is random and the number of decoding iterations is unbounded. However, from the perspective of practical implementation, the random structure usually leads to prohibitive encoding/decoding complexity and memory requirements. For this reason, structured LDPC codes that can achieve a better tradeoff between power efficiency and implementation simplicity have become a more appealing

option for system designers. For instance, the error control codes adopted by ETSI Second Generation Digital Video Broadcasting Standard for Satellite Channels (DVB-S2), IEEE 802.11n and IEEE 802.16 standards all belong to the category of structured LDPC codes.

On the other hand, the DVB-S2 LDPC codes family, which were originally designed for forward error control in satellite communications, have also been used by DVB-T2 (Second Generation DVB Standard for Terrestrial Channels), and are strongly recommended for DVB-C2 (Second Generation DVB Standard for Cable Channels). In addition to the consideration for system compatibility, the main reason behind the use of DVB-S2 codes can be attributed to their universal superior performance under various channel conditions. However, to meet the demand by cable operators for higher spectral efficiency and flexible throughputs, a technical challenge for using the DVB-S2 codes in DVB-C2 lies in the mapping of the given codes to constellations of very high order, which range from 256-QAM to 4096-QAM.

The DVB-C2 project has attempted to use the contents of the DVB-T2 Standard as much as possible. OFDM modulation will be adopted as well as the coding technique (BCH+LDPC) specified in DVB-T2 Standard. However, DVB-T2 Standard is designed for use in the terrestrial wireless channel while the DVB-C2 Standard is designed for use in the cable channel. A cable channel differs from a terrestrial channel in that a cable channel is a high quality (high SNR) channel with only a few weak echoes. Also, cable television operators have fewer spectrum restrictions than terrestrial broadcasters. Therefore, the signal frame structure and preambles used in DVB-T2 may not be suitable to be reused in DVB-C2 Standard.

A frame header of Forward Error Correction (FEC) is designed for use in the DVB-C2 Standard. In the DVB-C2 Standard, Adaptive Coding and Modulation (ACM) or Variable Coding and Modulation (VCM) is applied to each FEC block to provide as much flexibility as possible. The FEC block is composed of a Bose-Chaudhuri-

Hocquenghem (BCH) outer code and a Low-Density-Parity-Check (LDPC) inner code. Two dimensional interleaving is also performed. Interleaving is a procedure for rearranging the order of a sequence to fulfill different objectives. For channels subject to selective fading over time and frequency domains, bit and/or symbol interleaving have been used in conjunction with channel coding to distribute the error bursts. In addition, bit interleaving is employed by concatenated codes, particularly Turbo codes, to scramble the information bits to the second constituent encoder so that a long random code can be generated. A frame header is attached in front of each FEC frame to indicate the coding rate, modulation type and physical layer pipe identifier. Besides the signaling of physical layer related information, the FEC frame header has to provide a structure so that it can be easily and reliably detected in the receiver.

SUMMARY OF THE INVENTION

An efficient and reliable FEC frame header for digital cable television transmission is provided in at least one implementation in this disclosure. In addition, the detection algorithm of the FEC header is described. One possible implementation is shown, using the DVB-C2 standard as an example.

A frame header of Forward Error Correction (FEC) is designed for use in the DVB-C2 Standard. In the DVB-C2 Standard, Adaptive Coding and Modulation (ACM) or Variable Coding and Modulation (VCM) is applied to each FEC block to provide as much flexibility as possible. As a result, a frame header is attached in front of each FEC frame to inform the coding rate, modulation type and physical layer pipe identifier. Besides the signaling of physical layer related information, the FEC frame header has to provide a structure so that it can be easily and reliably detected in the receiver. Motivated by the need in DVB-C2 Standard, an efficient and reliable method and apparatus to encode the FEC header for DVB-C2 Standard is provided in at least one implementation in this disclosure. In addition, the detection algorithm of the FEC header is described.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the structure of the LDPC signaling part of the Data Slice Packet along with the position of the FEC Header and optional Next FEC Header.

Figure 2 shows one embodiment of some of the principles of the present invention.

Figure 3 shows one embodiment of a detector for the FEC Header under some of the principles of the present invention.

Figure 4 shows a flowchart depicting the method of encoding under the principles of the present invention.

Figure 5 shows an apparatus according to the principles of the present invention.

Figure 6 shows a flowchart depicting the method of decoding under the principles of the present invention.

Figure 7 shows an apparatus for decoding under the present principles.

DETAILED DESCRIPTION OF THE INVENTION

The DVB-C2 Standard is the next generation digital cable transmission system being developed by the DVB Project. The DVB-C2 Standard uses the contents of the DVB-T2 terrestrial transmission standard as much as possible. As a result, OFDM modulation will be adopted as well as the coding technique (BCH+LDPC) specified in DVB-T2 Standard. However, it must be noted that DVB-T2 Standard is designed for use in the terrestrial wireless channel while the DVB-C2 Standard is designed for use in the cable channel. Cable channels differ from wireless channels because the cable channel is a high quality (high SNR) channel with only a few weak echoes and because the wireless spectrum assigned for TV broadcasting is defined by the FCC while the spectrum of the cable networks can be used with somewhat fewer limitations. Consequently, the signal frame structure and preambles used in DVB-T2 may not be

suitable to be used in DVB-C2 Standard. The principles described herein allow an FEC frame header to be detected under noisy channel conditions with minimal complexity.

The data transmitted according to the DVB-C2 standard is contained in Data Slice Packets. Data Slice Packets are formed from one or two FEC Frame cells. These Data Slice Packets can either be Data Slice Type 1 or Data Slice Type 2. Data Slice Type 1 packets only transmit the FEC Frame data and use a pointer within the Level 1 Signaling Part 2 to detect their start. Data Slice Type 2 packets carry a 16-bit FEC Frame header that allows for synchronization to the Data Slice Packets without further information being transmitted. This header carries information regarding the modulation, coding parameters, PLP identifiers, and number of FEC Frames (one or two) following the header. Encoding of the header information must ensure that it can be properly synchronized and decoded.

The placement of the FEC Header is shown in Figure 1 and the present principles of encoding the header information are accomplished, in part, according to Figure 2. Figure 1 shows the FEC Header placement of the current FECFrame, labeled as QAM Modulated LDPC Packet in Figure 1, along with an optional Next FEC Header, which is the header that is used for the next FECFrame. The modulation order of the FEC Header can also be adapted so that it is based on the modulation order of the FEC Frame data portion. As an example, if the FEC Frame is modulated with either 16-QAM or 64-QAM, then BPSK can be used for the modulation of the FEC Header. If the FEC Frame is modulated with either 256-QAM, 1K-QAM, or 4K-QAM, then QPSK can be used as the modulation for the FEC Header.

Figure 2 shows how the 16 signaling bits of the FEC Header can be further encoded using the present principles for either a 16-QAM or 64-QAM modulated FEC Frame. The sixteen signaling bits of the FEC Header are first FEC encoded, for example, by Reed-Muller(32,16) coding. The 32 codeword bits that are an output of the Reed-Muller (32,16) coding are then modulated by offset BPSK according to 32 bits of a

pseudo-random binary sequence. This process results in 32 offset BPSK symbols. In a higher signal-to-noise environment, offset QPSK modulation can be used for the FEC Header coding, resulting in only 16 symbols.

Figure 3 illustrates detection of the FEC Header for the offset BPSK case. The received signal is demodulated with a BPSK offset detector 310 whose output is correlated with a pseudo-random binary sequence by means of the PRBS correlator 320. If the correlation is greater than a threshold value, the Reed-Muller symmetry detection 330 is performed. Threshold values can be chosen based on empirical evidence of values which show good correlation performance of the BPSK demodulated signal. The Reed-Muller(32,16) code is a second order Reed-Muller code and its codewords do not have a symmetrical structure, unlike a first order Reed-Muller code. Decoding of the Reed-Muller(32,16) code consists of three stages of majority decoding and after the first stage 335, the modified codeword has a symmetrical structure like a first order Reed-Muller code. This symmetry structure can be used to assist in the detection of the FEC Header. The results of the pseudo-random binary sequence correlation 332 and Reed-Muller symmetry correlation 338 are combined to make the decoding decision.

Simulation results have shown that use of Reed-Muller(32,16) code with BPSK modulation can achieve error free results for FEC Header signaling at 10 dB SNR in additive white Gaussian noise (AWGN) channels. Majority decoding has very low complexity leading to simple decoders as well.

The present description illustrates the present principles as applied to the 16-bit header of DVB-C2 as an example. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the present principles and are included within its spirit and scope. The present principles are equally applicable to header information of different

lengths with appropriate modification of the methods and apparatus of the present invention.

Figure 4 illustrates the method of encoding the FEC frame header. Encoding is performed by FEC encoding step 410. This encoding can be, for example, Reed-Muller(32,16) encoding. Following this step, modulation step 420 performs a modulation of the encoded header output, using a pseudo-random binary sequence. The modulation performed by step 420 can be, for example, BPSK or QPSK.

Figure 5 illustrates the apparatus for encoding the FEC Frame header. FEC Encoder 510 is used to perform encoding of the input FEC Frame header, such as Reed-Muller(32,16) encoding. The output of encoding block 510 is fed to a modulator block 520. Modulator block 520 is used to perform a modulation of the FEC encoded frame header value using a pseudo-random binary sequence. The modulation can be, for example, BPSK or QPSK.

Figure 6 illustrates the method of detecting the FEC frame header. Step 610 receives the header information. The header is then demodulated in step 620 by, for example, a BPSK offset detector. In step 630, the demodulated header output is correlated with a pseudo-random binary sequence. The result of this correlation is then compared with a threshold in step 640. If the correlation result is greater than a threshold, symmetry detection is performed in step 650. If the result of the correlation is not greater than the threshold, the process is reinitialized by receiving header information.

Figure 7 illustrates the apparatus for decoding header information using the present principles. Receiver block 710 receives header information. The received headers are input to demodulator block 720 which demodulates the received header information. Correlator block 730 is used to correlate the demodulated received header information with a pseudo-random binary sequence to produce a correlation result. Comparator block 740 compares the correlation output with a chosen threshold.

Symmetry detector block 750 perfoms a detection on the demodulated received header information if the correlation result is greater than a threshold.

All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the present principles and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions.

Moreover, all statements herein reciting principles, aspects, and embodiments of the present principles, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

Thus, for example, it will be appreciated by those skilled in the art that the block diagrams presented herein represent conceptual views of illustrative circuitry embodying the present principles. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable media and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

The functions of the various elements shown in the figures may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include,

without limitation, digital signal processor ("DSP") hardware, read-only memory ("ROM") for storing software, random access memory ("RAM"), and non-volatile storage.

Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

In the claims hereof, any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements that performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The present principles as defined by such claims reside in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. It is thus regarded that any means that can provide those functionalities are equivalent to those shown herein.

Reference in the specification to "one embodiment" or "an embodiment" of the present principles, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present principles. Thus, the appearances of the phrase "in one embodiment" or "in an embodiment", as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

CLAIMS:

1. A method of encoding header information, the method comprising:

encoding the header bits for data packets in a digital cable television environment using Reed-Muller coding;

modulating the output of the Reed-Muller coding with a pseudo-random binary sequence.

2. The method of Claim 1, wherein the Reed-Muller encoding step uses a second order Reed-Muller code.

3. The method of Claim 1, wherein the modulating step uses offset binary phase shift keying.

4. The method of Claim 1, wherein the modulating step uses quadrature phase shift keying.

5. The method of Claim 1, wherein the modulating step uses a modulation method that is dependent upon which modulation method is used for a data portion of said data packets.

6. The method of Claim 5, wherein binary phase shift keying is used to modulate said header information when 16-QAM or 64-QAM is used for said data portion of said data packets, and wherein quadrature phase shift keying is used to modulate said header information when 256-QAM, 1K-QAM, or 4K-QAM is used for said data portion of said data packets.

7. An apparatus for encoding header information, comprising:

a Reed-Muller encoder for encoding data packets in a digital cable television environment; and

a modulator for processing the output of the Reed-Muller encoder with a pseudo-random binary sequence.

8. The apparatus of Claim 7, wherein the Reed-Muller encoder uses a second order Reed-Muller code.

9. The apparatus of Claim 7, wherein the modulator uses offset binary phase shift keying.

10. The apparatus of Claim 7, wherein the modulator uses quadrature phase shift keying.

11. The apparatus of Claim 7, wherein the modulator uses a modulation method that is dependent upon which modulation method is used for a data portion of said data packets.

12. The apparatus of Claim 11, wherein binary phase shift keying is used to modulate said header information when 16-QAM or 64-QAM is used for said data portion of said data packets, and wherein quadrature phase shift keying is used to modulate said header information when 256-QAM, 1K-QAM, or 4K-QAM is used for said data portion of said data packets.

13. A method of decoding header information, the method comprising:

receiving header information for data packets in a digital cable television environment;

demodulating said received header information;

correlating said demodulated received header information with a pseudo-random binary sequence to produce a correlation result; and

conditionally performing a Reed-Muller symmetry detection on said demodulated received header information.

14. The method of Claim 13, wherein said condition for performing symmetry detection is when said correlation result is greater than a threshold.

15. The method of Claim 13, wherein the Reed-Muller detection step uses a second order Reed-Muller code.

16. The method of Claim 13, wherein the demodulating step uses offset binary phase shift keying.

17. The method of Claim 13, wherein the demodulating step uses quadrature phase shift keying.

18. The method of Claim 13, wherein the demodulating step uses a demodulation method that is dependent upon which modulation method is used for a data portion of said data packets.

19. The method of Claim 17, wherein binary phase shift keying is used to demodulate said header information when 16-QAM or 64-QAM is used for said data portion of said data packets, and wherein quadrature phase shift keying is used to demodulate said header information when 256-QAM, 1K-QAM, or 4K-QAM is used for said data portion of said data packets.

20. An apparatus for decoding header information, comprising:

a receiver for receiving header information for data packets in a digital cable television environment;

a demodulator for demodulating said received header information;

a correlator for correlating said demodulated received header information with a pseudo-random binary sequence to produce a correlation result; and

a Reed-Muller symmetry detector for conditionally processing said demodulated received header information.

21. The apparatus of Claim 16, wherein said condition causing said symmetry detector to process said demodulated received header information is that said correlation result is greater than a threshold.

22. The apparatus of Claim 19, wherein the Reed-Muller detector uses a second order Reed-Muller code.

23. The apparatus of Claim 19, wherein said demodulator uses offset binary phase shift keying.

24. The apparatus of Claim 19, wherein said demodulator uses quadrature phase shift keying.

25. The apparatus of Claim 19, wherein said demodulator uses a demodulation method that is dependent upon which modulation method is used for a data portion of said data packets.

26. The apparatus of Claim 23, wherein said demodulator uses binary phase shift keying to demodulate said header information when 16-QAM or 64-QAM is used for said data portion of said data packets, and wherein said demodulator uses quadrature phase shift keying to demodulate said header information when 256-QAM, 1K-QAM, or 4K-QAM is used for said data portion of said data packets.

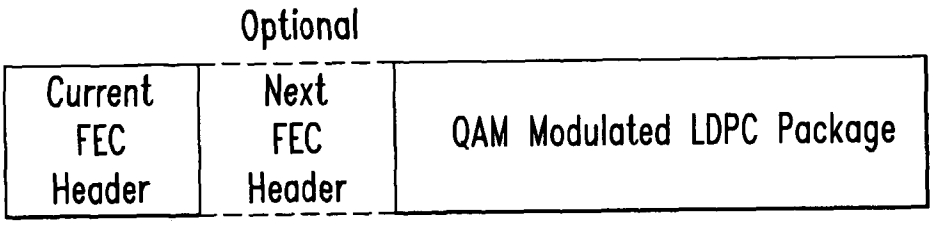

Optional
Current FEC Header
Next FEC Header
QAM Modulated LDPC Package

FIG. 1

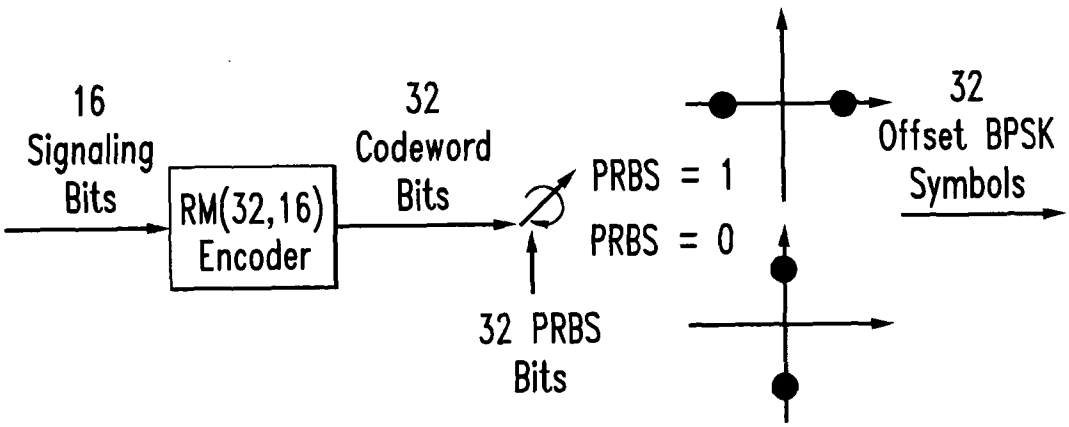

16 Signaling Bits
RM(32,16) Encoder
32 Codeword Bits
32 PRBS Bits
PRBS = 1
PRBS = 0
32 Offset BPSK Symbols

FIG. 2

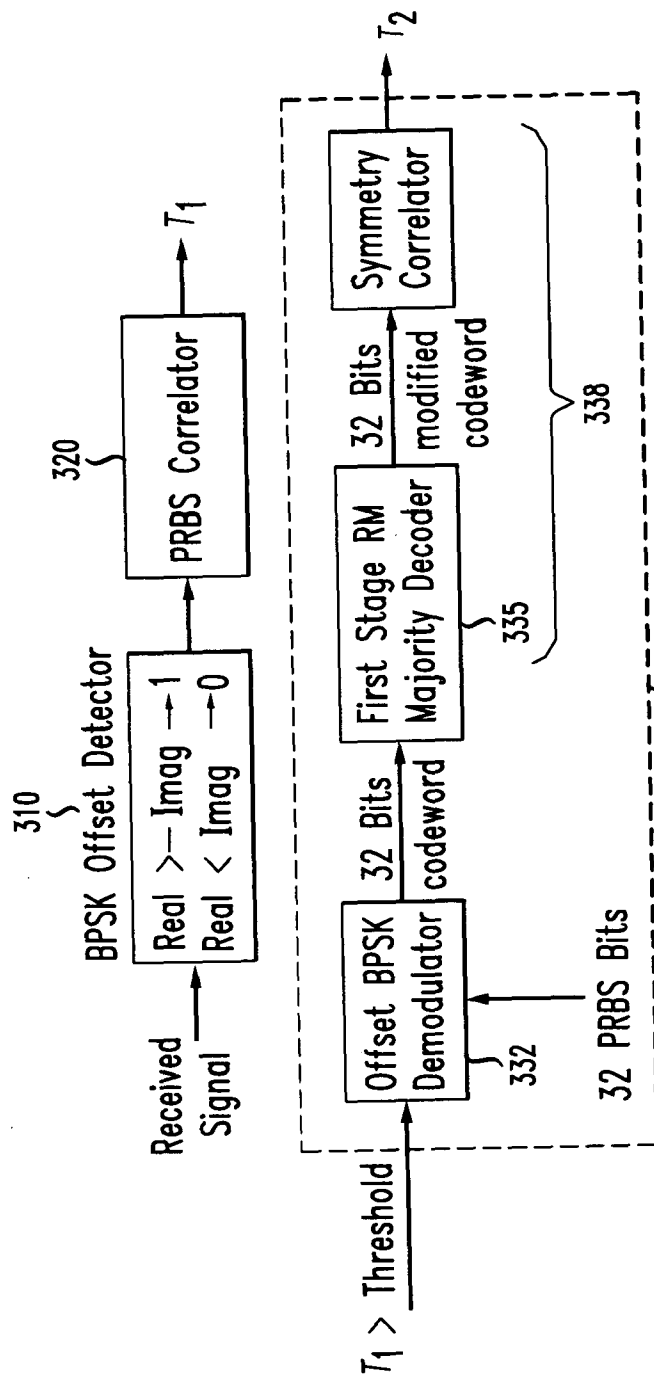

310
BPSK Offset Detector
Real >— Imag —1
Real < Imag —0
Received Signal
320
PRBS Correlator
T1
T1 > Threshold
Offset BPSK Demodulator
32 Bits codeword
332
First Stage RM Majority Decoder
335
32 Bits modified codeword
Symmetry Correlator
T2
32 PRBS Bits
338
338

FIG. 3

FIG. 4

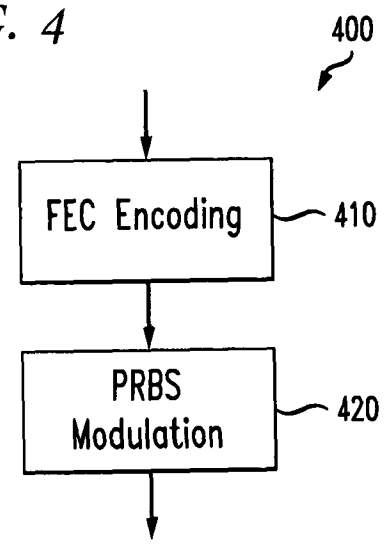

400
FEC Encoding
410
PRBS
Modulation
420

FIG. 5

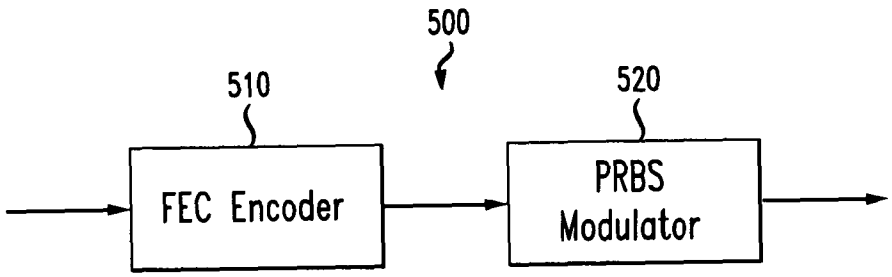

500
510
520
FEC Encoder
PRBS
Modulator

FIG. 6

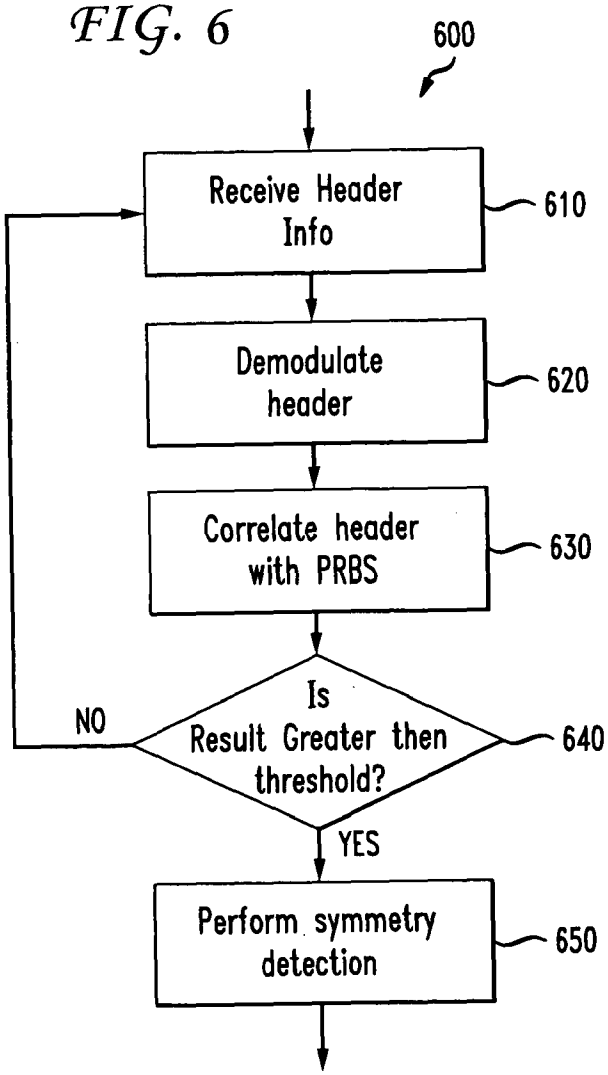
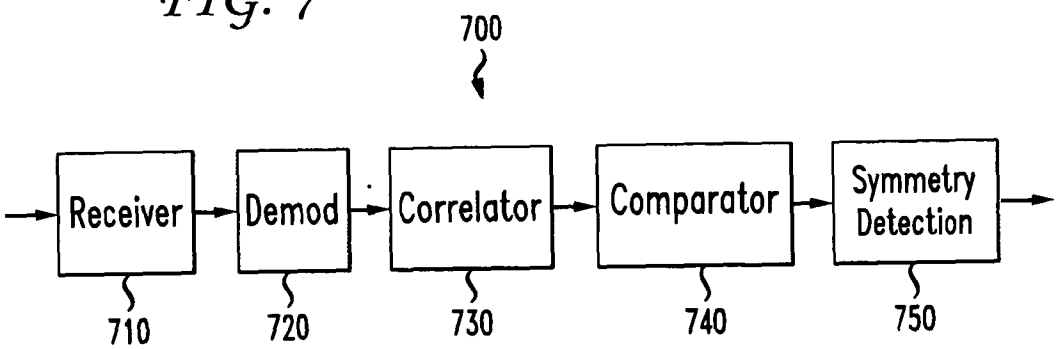

600
Receive Header Info
610
Demodulate header
620
Correlate header with PRBS
630
Is Result Greater then threshold?
640
NO
YES
Perform symmetry detection
650

FIG. 7


700
Receiver
Demod
Correlator
Comparator
Symmetry Detection
710
720
730
740
750

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/006138

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L27/20 H04L27/22 H04L1/00 H03M13/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CCSDS, The Consultative Committee for Space Data Systems: "DVB-S2 coding & modulation standard use for high data rate TM links. Experimental specification" Research and Development for Space Data System Standards June 2007 (2007-06), XP002571391 Retrieved from the Internet: URL:http://cwe.ccsds.org/sls/docs/SLS-CandS/Meeting%20Materials/2007/Spring+Summer_Material/DVB-S2_orange_book_withoutmark(July2007).pdf> [retrieved on 2010-03-02] 2. Overview 3.1 Architecture 3.2.5 Base-band scrambling 3.4 Physical Layer framing -/--	1-26

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 March 2010	17/03/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Palacián Lisa, Marta

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/006138

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/042685 A1 (CENTRE NAT ETD SPATIALES [FR]; GIRAUD XAVIER [FR]; DUVERDIER ALBAN [FR]) 19 April 2007 (2007-04-19) abstract page 1, line 4 - line 28 page 6, line 14 - line 20 page 9, line 15 - page 10, line 17 page 14, line 5 - page 16, line 16	1-26
X	MEHDI NOURI ET AL: "TEDS: a High Speed Digital Mobile Communication Air Interface for Professional Users Part I: Overview of Physical Layer" VEHICULAR TECHNOLOGY CONFERENCE, 2007. VTC2007-SPRING. IEEE 65TH, IEEE, PI, 1 April 2007 (2007-04-01), pages 959-963, XP031092772 ISBN: 978-1-4244-0266-3 abstract II. System overview III.B Channel coding and interleaving	1-26
A	WO 2005/006693 A1 (CONEXANT SYSTEMS INC [US]; EIDSON DONALD B [US]) 20 January 2005 (2005-01-20) abstract page 6, line 21 - page 7, line 2	1-26
A	US 6 865 236 B1 (TERRY JOHN [US]) 8 March 2005 (2005-03-08) abstract column 1, line 11 - line 16 column 2, line 14 - line 47 column 5, line 17 - column 6, line 65	1-26
A	PATERSON K G ET AL: "EFFICIENT DECODING ALGORITHMS FOR GENERALISED REED-MULLER CODES" EFFICIENT DECODING ALGORITHMS FOR GENERALISED REED-MULLER CODES, XX, XX, 1 November 1998 (1998-11-01), pages 1-26, XP000669487 the whole document	1-26

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/006138

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2007042685 A1	19-04-2007	CA 2625710 A1	19-04-2007
		EP 1946557 A1	23-07-2008
		FR 2892245 A1	20-04-2007
		US 2009161788 A1	25-06-2009
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US 6865236 B1	08-03-2005	NONE	