POWER SUPPLY DEVICE AND ELECTRIC APPLIANCE THEREWITH

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Abstract

A power supply device has a DC/DC converter producing an intermediary voltage from an input voltage, a series regulator producing a desired output voltage from the intermediary voltage, an output current monitoring circuit monitoring the output current flowing through the series regulator, and an intermediary voltage adjustment circuit adjusting the feedback control of the DC/DC converter such that, as the monitored output current increases, the intermediary voltage increases and that, as the monitored output current decreases, the intermediary voltage decreases. This configuration offers high efficiency over the entire load range.
FIG. 1

DC VOLTAGE SOURCE

POWER SUPPLY DEVICE

LOAD
FIG. 3
FIG. 4

VOLTAGE

L3(Vp)

Vdiff

L1(Vmo ≈ Vmi)

Vdiff

L2(Vo)

Io
FIG. 5
FIG. 7
Related Art
FIG. 8
Related Art

![Diagram of DC/DC Converter and Series Regulator]
POWER SUPPLY DEVICE AND ELECTRIC APPLIANCE THEREWITH

0001. This application is based on Japanese Patent Application No. 2006-153047 filed on Jun. 1, 2006, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

0002. Field of the Invention

0003. The present invention relates to a power supply device that produces a desired output voltage from an input voltage, and to an electric appliance incorporating such a power supply device.

0004. Description of Related Art

0005. FIG. 7 is a circuit diagram showing an example of a conventional series regulator.

0006. As shown in the figure, the conventional series regulator includes: an output transistor Tr connected in series between the node to which an input voltage Vi is applied and the node from which an output voltage Vo is derived; resistors Rx and Ry connected in series between the node from which the output voltage Vo is derived and the grounded node; and an amplifier ERR that produces the gate voltage of the output transistor Tr by amplifying the differential voltage between a feedback voltage Vfb derived from the node between the resistors Rx and Ry with a predetermined reference voltage Vref. Here, the desired output voltage Vo is produced from the input voltage Vi by controlling the conductance of the output transistor Tr in such a way as to keep the feedback voltage Vfb, which is commensurate with the output voltage Vo, equal to the reference voltage Vref.

0007. The series regulator configured as described above, when compared with switching regulators, produces less source-attributable ripples and noise and has a small circuit area, and is therefore widely used as means of power supply in portable appliances and the like that are susceptible to noise.

0008. Inconveniently, however, with the series regulator configured as described above, the input-output potential difference (Vi-Vo) multiplied by the output current Io is completely lost. Thus, assuming that the output current Io remains constant, the higher the input-output voltage difference (Vi-Vo), the lower the efficiency η.

0009. More specifically, when the input voltage Vi=3 V, the output voltage Vo=1 V, and the output current Io=100 mA, the loss in the output transistor Tr is (3-1) × 100 mA × 200 mW; by contrast, when the input voltage Vi=5 V, the output voltage Vo=1 V, and the output current Io=100 mA, the loss in the output transistor Tr is (5-1) × 100 mA × 400 mW. Thus, in this example, a small increase in the input voltage Vi from 3 V to 5 V results in doubling the loss in the output transistor Tr.

0010. As a conventional technology related to what has been described above, JP-A-H06-245492 (hereinafter “Patent Document 1”) discloses and proposes a direct-current stabilized power supply circuit as shown in a simplified fashion in FIG. 8. Here, in the stage precede a series regulator 200, a DC/DC converter 100 that produces from an input voltage Vi an intermediary voltage (as the input voltage to the series regulator 200) is inserted as means for keeping constant the input-output potential difference (Vp-Vo) across the series regulator 200.

[0011] As another conventional technology related to what has been described above, JP-A-H10-039937 (hereinafter “Patent Document 2”) discloses and proposes a power supply device that supplies drive electric power to a load device that includes a pulse load circuit that operates from direct-current power and produces a load current in the form of direct-current pulses. This power supply device includes: direct-current power generating means (a DC/DC converter circuit) for generating the direct-current power required by the load device; power delivering means for supplying the direct-current power generated by the just mentioned means to the load device; and voltage compensating means (a series regulator circuit), incorporated in the load device, for supplying the direct-current power from the direct-current power generating means to the pulse load circuit to compensate for variations in the drive voltage ascribable to the load current in the form of direct-current pulses generated in the pulse load circuit.

[0012] Certainly, with the direct-current stabilized power supply circuit of Patent Document 1, it is possible to keep constant the input-output potential difference across the series regulator 200 irrespective of variations in the input voltage Vi and the output voltage Vo. This helps achieve higher efficiency η than when the series regulator shown in FIG. 7 is used singly.

[0013] Inconveniently, however, in the direct-current stabilized power supply circuit of Patent Document 1, no consideration is given to the fact that the forward voltage drop Vdrop across the output transistor (= the on-state resistance Ron of the output transistor multiplied by the output current Io) included in the series regulator 200 varies with how heavy the load is (and hence how large the output current Io is).

[0014] More specifically, in the direct-current stabilized power supply circuit of Patent Document 1, the smaller the output current Io that flows through the output transistor in the series regulator 200, the smaller the forward voltage drop Vdrop across the output transistor; the larger the output current Io that flows through the output transistor, the higher the forward voltage drop Vdrop across it. Despite this, the input-output potential difference across the series regulator 200 is kept constant (e.g., 0.7 V).

[0015] Thus, so long as the output current Io is large, the direct-current stabilized power supply circuit of Patent Document 1 operates quite satisfactorily; in contrast, when the output current Io is small, the series regulator 200 is fed with an unnecessarily high voltage, hence the disadvantage of low efficiency η in a light-load condition.

[0016] On the other hand, according to the conventional technology of Patent Document 2, the purpose of arranging the series regulator near the load circuit is basically to eliminate the effect of variations in the direct-current voltage resulting from transient variations in the load current. Certainly this, compared with power supply devices including a DC/DC converter alone, helps improve the resistance to variations in the load current and helps increase the flexibility in the layout of the DC/DC converter. Like Patent Document 1, however, Patent Document 2 does not disclose or suggest anything about the lowering of efficiency η in a light-load condition or how to cope with it.

SUMMARY OF THE INVENTION

0017. An object of the present invention is to provide a power supply device that offers high efficiency over the
entire load range, and to provide an electric appliance incorporating such a power supply device.

[0018] To achieve the above object, according to one aspect of the invention, a power supply device is provided with: a DC/DC converter that produces an intermediary voltage from an input voltage; a series regulator that produces a desired output voltage from the intermediary voltage; an output current monitoring circuit that monitors the output current that flows through the series regulator; and an intermediary voltage adjustment circuit that adjusts the feedback control of the DC/DC converter such that, as the monitored output current increases, the intermediary voltage increases and that, as the monitored output current decreases, the intermediary voltage decreases.

[0019] Other features, elements, steps, advantages and characteristics of the present invention will become more apparent from the following detailed description of preferred embodiments thereof with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a block diagram showing an outline of the configuration of a cellular phone unit according to the invention;
[0021] FIG. 2 is a circuit diagram showing a power supply device 20 according to a first embodiment of the invention;
[0022] FIG. 3 is a circuit diagram showing an example of the intermediary voltage adjustment circuit 4;
[0023] FIG. 4 is a diagram showing the correlation between the output current Io and an intermediary voltage Vmo (=Vmi);
[0024] FIG. 5 is a diagram showing the correlation between the output current Io and the efficiency η;
[0025] FIG. 6 is a circuit diagram showing a power supply device 20 according to a second embodiment of the invention;
[0026] FIG. 7 is a circuit diagram showing an example of a conventional series regulator; and
[0027] FIG. 8 is a block diagram showing an example of a conventional power supply device having a DC/DC converter inserted in the stage preceding a series regulator.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0028] Hereinafter, the present invention will be described by way of examples in which it is applied to a power supply device incorporated in a cellular phone unit to produce a voltage for driving a load.
[0029] FIG. 1 is a block diagram showing an outline of the configuration of a cellular phone unit according to the invention (showing, in particular, the part concerned with the supply of electric power to a load).
[0030] As shown in the figure, the cellular phone unit of this embodiment includes: a direct-current voltage source 10 that produces an input voltage Vi; a power supply device 20 that produces from the input voltage Vi a desired output voltage Vo; and a load 30 that is driven with the output voltage Vo. Needless to say, the cellular phone unit of this embodiment further includes, though not illustrated in the figure, means for realizing its essential functions (such as communication functions), including a transmitter/receiver circuit, a loudspeaker, a microphone, a display, an operation panel, and a memory.

[0031] The direct-current voltage source 10 serves as means for producing a direct-current input voltage Vi, and is, in this embodiment, realized with a battery (e.g., a rechargeable battery such as a lithium-ion battery). The direct-current voltage source 10 may be realized with, instead of a battery, an AC/DC converter that converts a commercially distributed alternating-current voltage into a direct-current voltage.
[0032] The power supply device 20 serves as means for producing a desired output voltage Vo from the input voltage Vi led from the direct-current voltage source 10 and then feeding the output voltage Vo to the load 30.
[0033] FIG. 2 is a circuit diagram (partly a block diagram) showing a power supply device 20 according to a first embodiment of the invention.
[0034] As shown in the figure, the power supply device 20 of this embodiment includes a DC/DC converter 1, a series regulator 2, an output current monitoring circuit 3, and an intermediary voltage adjustment circuit 4.
[0035] First, the configuration and operation of the DC/DC converter 1 will be described.
[0036] The DC/DC converter 1 includes a semiconductor integrated circuit device IC1, resistors R1 to R2, capacitors C1 and C2, and an inductor L1, and is configured as a step-down switching regulator (chopper regulator) that produces from the input voltage Vi an intermediary voltage Vmo.
[0037] The input terminal (IN) of the DC/DC converter 1 is connected to the node to which the input voltage Vi is applied, and is also connected via the capacitor C1, which is for input smoothing, to the grounded node. The switching terminal (SW) is connected to one end of the inductor L1. The other end of the inductor L1 serves as the node from which the intermediary voltage Vmo is derived; this end of the inductor L1 is connected via the output current monitoring circuit 3 to the series regulator 2, and is also connected to the grounded node via the capacitor C2, which is for output smoothing, and then the resistor division circuit composed of the resistors R1 to R2. The node between the resistors R1 to R2 serves as the node from which a feedback voltage Vfb1 (a division voltage obtained by dividing the intermediary voltage Vmo in a predetermined division ratio) whose voltage level varies according to the intermediary voltage Vmo is derived, and is connected to the feedback terminal (FB) of the semiconductor integrated circuit device IC1.
[0038] The semiconductor integrated circuit device IC1 is realized with a common semiconductor integrated circuit device for switching, and therefore its internal configuration is not specifically illustrated. For example, the semiconductor integrated circuit device IC1 may include an error amplifier that amplifies the differential voltage between the feedback voltage Vfb1 and a predetermined reference voltage and be so configured as to turn a switching transistor on and off in such a way as to decrease the output signal (error voltage) of the error amplifier. More specifically, the semiconductor integrated circuit device IC1 may be so configured as to produce a PWM (pulse width modulation) signal according to the result of comparison between the error voltage and a predetermined slope voltage (a triangular or ramp-shaped voltage) and turn a switching transistor on and off by use of the PWM signal.
[0039] As described above, in the stage preceding the series regulator 2, the DC/DC converter 1 is inserted that produces a stable intermediary voltage Vmo that is not
affected by variations in the input voltage \( V_i \). This helps obtain higher efficiency \( \eta \) than with the configuration in which the series regulator 2 is used singly.

0040] Next, the configuration and operation of the series regulator 2 will be described.

0041] The series regulator 2 includes an output transistor \( N_1 \), resistors \( R_3 \) and \( R_4 \), a capacitor \( C_3 \), an amplifier \( A_1 \), and a direct-current voltage source \( E_1 \), and serves as means for converting into a desired output voltage \( V_o \) an intermediary voltage \( V_{mi} (\approx V_{mo}) \) fed via the output current monitoring circuit 3 from the DC/DC converter 1.

0042] The series regulator 2 of this embodiment employs, as the output transistor \( N_1 \), an N-channel field-effect transistor with a low forward voltage drop \( V_{pd} \), and is thus designed as a low-drop-out regulator (called LDO regulator) that operates properly even when the intermediary voltage \( V_{mi} \) is only slightly higher than the desired output voltage \( V_o \).

0043] The drain of the output transistor \( N_1 \) is connected to the node to which the intermediary voltage \( V_{mi} \) is applied. The source of the output transistor \( N_1 \) serves as the node from which the output voltage \( V_o \) is derived; the source of the output transistor \( N_1 \) is connected to the load \( 30 \) (unillustrated), and is also connected to the grounded node via the capacitor \( C_3 \), for output smoothing, and then the resistor division circuit composed of the resistors \( R_3 \) and \( R_4 \). The node between the resistors \( R_3 \) and \( R_4 \) serves as the node from which a feedback voltage \( V_{fb} \) (a division voltage obtained by dividing the output voltage \( V_o \) in a predetermined division ratio) whose voltage level varies according to the output voltage \( V_o \) is derived, and is connected to the inverting input terminal (−) of the amplifier \( A_1 \). The non-inverting input terminal (+) of the amplifier \( A_1 \) is connected to the positive terminal (at which a reference voltage \( V_{ref} \) is present) of the direct-current voltage source \( E_1 \). The negative terminal of the direct-current voltage source \( E_1 \) is connected to the grounded node. The output terminal of the amplifier \( A_1 \) is connected to the gate of the output transistor \( N_1 \).

0044] In the series regulator 2 configured as described above, the amplifier \( A_1 \) produces the gate voltage of the output transistor \( N_1 \) in such a way as to keep the feedback voltage \( V_{fb} \) applied to its inverting input terminal (−) equal to the reference voltage \( V_{ref} \) applied to its non-inverting input terminal (+).

0045] Specifically, while the feedback voltage \( V_{fb} \) is lower than the reference voltage \( V_{ref} \), the amplifier \( A_1 \) keeps the gate voltage of the output transistor \( N_1 \) high; by contrast, when the feedback voltage \( V_{fb} \) is equal to or higher than the reference voltage \( V_{ref} \), the amplifier \( A_1 \) controls the gate voltage of the output transistor \( N_1 \) such that, the larger the deviation of the feedback voltage \( V_{fb} \) from the reference voltage \( V_{ref} \) is, and thus the further the output voltage \( V_o \) is higher than its target level, the more the gate voltage of the output transistor \( N_1 \) is decreased.

0046] On the other hand, the conductance of the output transistor \( N_1 \) is controlled according to its gate voltage fed from the amplifier \( A_1 \). Thus, in the series regulator 2, the conductance of the output transistor \( N_1 \) is controlled in such a way as to keep the feedback voltage \( V_{fb} \) equal to the reference voltage \( V_{ref} \), and hence to keep the output voltage \( V_o \) equal to its target level.

0047] As described above, as means for ultimately producing the output voltage \( V_o \), the series regulator 2 configures as described above is used. This helps minimize source-attributable ripples and noise contained in the output voltage \( V_o \).

0048] Next, the configuration and operation of the output current monitoring circuit 3 will be described.

0049] The output current monitoring circuit 3 includes a sense resistor \( R_s \) and an amplifier \( A_2 \), and functions as means for monitoring the output current \( I_o \) that flows through the series regulator 2.

0050] The sense resistor \( R_s \) is connected in series between the DC/DC converter 1 and the series regulator 2. The non-inverting input terminal (+) of the amplifier \( A_2 \) is connected to one end (higher-potential end) of the sense resistor \( R_s \), and the inverting input terminal (−) of the amplifier \( A_2 \) is connected to the other end (lower-potential end) of the sense resistor \( R_s \). Thus, the monitoring voltage \( V_d \) outputted from the amplifier \( A_2 \) increases as the output current \( I_o \) increases, and decreases as the latter decreases.

0051] Next, the configuration and operation of the intermediary voltage adjustment circuit 4 will be described.

0052] The intermediary voltage adjustment circuit 4 of this embodiment serves as means for adjusting the voltage level of the feedback voltage \( V_{fb} \) by varying the resistance of the resistor \( R_2 \) (and hence the voltage division ratio of the resistor division circuit composed of the resistors \( R_1 \) to \( R_2 \)) according to the monitored output current \( I_o \) (i.e., the monitoring voltage \( V_d \)).

0053] FIG. 3 is a circuit diagram (partly a block diagram) showing an example of the intermediary voltage adjustment circuit 4.

0054] As shown in FIG. 3, in the intermediary voltage adjustment circuit 4 of this embodiment, the resistor \( R_2 \) shown in FIG. 2 is realized with a resistor \( RA \) (having a constant resistance) connected in series with an N-channel field-effect transistor \( NA \); in addition, a level shifter \( LS \) is provided as means for producing the gate voltage \( V_g \) of the transistor \( NA \) from the monitoring voltage \( V_d \).

0055] In the intermediary voltage adjustment circuit 4 configured as described above, as the monitoring voltage \( V_d \) fed from the output current monitoring circuit 3 increases, the gate voltage \( V_g \) of the transistor \( NA \) increases, and thus the impedance of the transistor \( NA \) (and hence the resistance of the resistor \( R_2 \)) decreases, causing the feedback voltage \( V_{fb} \) to decrease. Thus, the DC/DC converter 1 is feedback-controlled such that the intermediary voltage \( V_{mo} \) increases.

0056] By contrast, as the monitoring voltage \( V_d \) fed from the output current monitoring circuit 3 decreases, the gate voltage \( V_g \) of the transistor \( NA \) decreases, and thus the impedance of the transistor \( NA \) (and hence the resistance of the resistor \( R_2 \)) increases, causing the feedback voltage \( V_{fb} \) to increase. Thus, the DC/DC converter 1 is feedback-controlled such that the intermediary voltage \( V_{mo} \) decreases.

0057] In this way, the intermediary voltage adjustment circuit 4 configured as described above functions as means for adjusting the feedback control of the DC/DC converter 1 in such a way that, the larger the output current \( I_o \) monitored by the output current monitoring circuit 3 is, the intermediary voltage \( V_{mo} \) is increased and that, the smaller the output current \( I_o \) monitored is, the intermediary voltage \( V_{mo} \) is decreased.

0058] FIG. 4 is a diagram showing the correlation between the output current \( I_o \) and the intermediary voltage \( V_{mo} \). In the figure, solid line \( L1 \) represents the
behavior of the intermediary voltage $V_{m0}$, and solid line $L_2$ represents the behavior of the output voltage $V_o$; for comparison, broken line $L_3$ represents the intermediary voltage $V_p$ (see FIG. 8) in the conventional configuration.

As will be understood from FIG. 4, with the configuration (see solid line $L_1$) in which the intermediary voltage adjustment circuit 4 is provided to adjust the feedback control of the DC/DC converter 1 as described above, unlike the conventional configuration (see broken line $L_3$) in which the input-output potential difference $V_{diff}$ ($=V_{m0}-V_o$) of the series regulator 2 is kept constant, it is possible to avoid feeding an unnecessarily high intermediary voltage $V_{m0}$ to a series regulator 2, especially when the output current $I_o$ is small.

Put in more ideal terms, it is possible to feed the minimum necessary intermediary voltage $V_{m0}$ to the series regulator 2 by adjusting the feedback control of the DC/DC converter 1 by making the level shifter $LS$ produce the optimal gate voltage $V_g$ such that the intermediary voltage $V_{m0}$ ($=V_{m0}$) is so produced to be higher than the output voltage $V_o$ by the forward voltage drop $V_{drop}$ across the output transistor $N_1$, in other words, such that the input-output potential difference $V_{diff}$ of the series regulator 2 is kept equal to the forward voltage drop $V_{drop}$ across the output transistor $N_1$.

Incidentally, the forward voltage drop $V_{drop}$ across the output transistor $N_1$ included in the series regulator 2 can be calculated as the on-state resistance $R_{sn}$ (previously known) of the output transistor $N_1$ multiplied by the output current $I_o$. Thus, monitoring the output current $I_o$ with the sense resistor $R_s$ amounts to monitoring the forward voltage drop $V_{drop}$ across the output transistor $N_1$. Thus, the optimum level of the intermediary voltage $V_{m0}$ to be produced by the DC/DC converter 1 can be determined solely on the result of monitoring of the output current $I_o$.

As described above, unlike the conventional configuration in which the input-output potential difference $V_{diff}$ ($=V_{m0}-V_o$) across the series regulator 2 is kept constant, the power supply device $V_{m0}$ of this embodiment can produce an intermediary voltage $V_{m0}$ ($=V_{m0}$) that dynamically varies with variations in the output current $I_o$. Thus, with the power supply device $V_{m0}$ of this embodiment, it is possible to obtain improved efficiency $\eta$ in the device as a whole in a light-load condition, and hence to obtain high efficiency over the entire load range.

FIG. 5 is a diagram showing the correlation between the output current $I_o$ and the efficiency $\eta$. In the figure, solid line $L_4$ represents the efficiency $\eta$ as observed in the device as a whole when the invention is applied; for comparison, broken line $L_5$ represents the efficiency $\eta$ as conventionally observed.

Now, a power supply device $V_{m0}$ according to a second embodiment of the invention will be described in detail with reference to FIG. 6.

FIG. 6 is a circuit diagram (partly a block diagram) showing the power supply device $V_{m0}$ according to the second embodiment.

As shown in the figure, the power supply device $V_{m0}$ of this embodiment has a configuration similar to that of the first embodiment described previously. Accordingly, such parts as find their counterparts in the first embodiment will be identified with common reference numerals and symbols, and their detailed explanation will not be repeated; thus, the following description proceeds with emphasis placed on the features unique to this embodiment (another example of the configuration of the intermediary voltage adjustment circuit 4).

As shown in FIG. 6, the intermediary voltage adjustment circuit 4 of this embodiment includes a P-channel field-effect transistor $P_c$ and a resistor $R_a$.

The source of the transistor $P_c$ is connected to a supplied power line (e.g., the node to which the input voltage $V_i$ is applied). The drain of the transistor $P_c$ is connected to the node between the resistors $R_1$ to $R_2$ (i.e., the node from which the feedback voltage $V_{ref}$ is derived). The gate of the transistor $P_c$ is connected via the resistor $R_a$ to the supplied power line, and is also connected to the output terminal of the amplifier $AZ$.

The amplifier $AZ$ includes P-channel field-effect transistors $P_a$ and $P_b$, N-channel field-effect transistors $N_a$ and $N_b$, and a constant current source $I_a$.

The sources of the transistors $P_a$ and $P_b$ are both connected to the supplied power line. The gate of the transistors $P_a$ is connected to one end (higher-potential end) of the sense resistor $R_s$. The gate of the transistors $P_b$ is connected to the other end (lower-potential end) of the sense resistor $R_s$. The drains of the transistors $P_a$ and $N_b$ are connected together, and the node between them is connected to the drain of the transistor $N_b$. The sources of the transistors $N_a$ and $N_b$ are both connected via the constant current source $I_a$ to the grounded node.

In the intermediary voltage adjustment circuit 4 configured as described above, as the monitoring voltage $V_{d}$ fed from the output current monitoring circuit 3 increases, the impedance of the transistor $P_c$ increases, and thus the offset level (pull-up level) in the feedback voltage $V_{ref}$ decreases. Thus, feedback control is performed such that the intermediary voltage $V_{m0}$ increases.

By contrast, as the monitoring voltage $V_{d}$ fed from the output current monitoring circuit 3 decreases, the impedance of the transistor $P_c$ decreases, and thus the offset level (pull-up level) in the feedback voltage $V_{ref}$ increases. Thus, feedback control is performed such that the intermediary voltage $V_{m0}$ decreases.

In this way, as in the first embodiment, the intermediary voltage adjustment circuit 4 configured as described above functions as means for adjusting the feedback control of the DC/DC converter 1 in such a way that, the larger the output current $I_o$ monitored by the output current monitoring circuit 3 is, the intermediary voltage $V_{m0}$ is increased and that, the smaller the output current $I_o$ monitored is, the intermediary voltage $V_{m0}$ is decreased.
Configured as described above, the power supply device 20 of this embodiment can also produce an intermediary voltage \(V_{in} \approx (\approx V_{mi})\) that dynamically varies with variations in the output current \(I_o\). Thus, with the power supply device 20 of this embodiment, it is possible to obtain improved efficiency \(\eta\) in the device as a whole in a light-load condition, and hence to obtain high efficiency over the entire load range.

Although the embodiments described above deal with cases where the invention is applied to a power supply device in a cellular phone unit, this is in no way meant to limit the application of the invention; the invention finds wide application in power supply devices incorporated in electric appliances in general.

The invention may be practiced in any other manner than specifically described by way of embodiments above, and allows many modifications and variations within its spirit.

For example, although the embodiments described above deal with examples in which a step-down switching regulator is used as the DC/DC converter, this is in no way meant to limit how the invention is practiced; instead, a DC/DC converter of any other type may be used, such as a step-up switching regulator.

Although the embodiments described above deal with examples in which the intermediary voltage adjustment circuit 4 is so configured as to appropriately adjust the feedback voltage \(V_{fb1}\) of the DC/DC converter 1, this is in no way meant to limit how the invention is practiced; instead, the intermediary voltage adjustment circuit 4 may be so configured as to appropriately adjust the target voltage with which the feedback voltage \(V_{fb1}\) is compared in the DC/DC converter.

Although the embodiments described above deal with examples in which the sense resistor \(R_s\) is connected in series with the output transistor \(N_1\), this is in no way meant to limit how the invention is practiced; instead, for example, a current monitoring transistor may be connected in parallel with the output transistor \(N_1\) so that the current that flows through the current monitoring transistor is monitored with the sense resistor \(R_s\). With this configuration, since no sense resistor \(R_s\) is connected in series with the output transistor \(N_1\), it is possible to monitor the output current \(I_o\) without increasing the on-state resistance of the device.

In terms of advantages, the invention helps realize power supply devices and electric appliances incorporating them that offer high efficiency over the entire load range.

In terms of industrial applicability, the invention is useful in improving the efficiency of direct-current stabilized power supply devices that produce a desired output voltage from an input voltage.

While the present invention has been described with respect to preferred embodiments, it will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than those specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the present invention which fall within the true spirit and scope of the invention.

What is claimed is:

1. A power supply device comprising:
   a DC/DC converter producing an intermediary voltage from an input voltage;
   a series regulator producing a desired output voltage from the intermediary voltage;
   an output current monitoring circuit monitoring an output current flowing through the series regulator; and
   an intermediary voltage adjustment circuit adjusting feedback control of the DC/DC converter such that, as the monitored output current increases, the intermediary voltage increases and that, as the monitored output current decreases, the intermediary voltage decreases.

2. The power supply device according to claim 1, wherein the intermediary voltage adjustment circuit adjusts the feedback control of the DC/DC converter such that the intermediary voltage is so produced as to be higher than the desired output voltage by a forward voltage drop across an output transistor included in the series regulator.

3. The power supply device according to claim 2, wherein the DC/DC converter produces the intermediary voltage from the input voltage according to a feedback voltage whose voltage level varies with the intermediary voltage, and the intermediary voltage adjustment circuit adjusts the voltage level of the feedback voltage according to the monitored output current.

4. The power supply device according to claim 3, wherein the feedback voltage is a division voltage obtained by dividing the intermediary voltage in a predetermined division ratio, and the intermediary voltage adjustment circuit adjusts the voltage level of the feedback voltage by varying the division ratio according to the monitored output current.

5. An electric appliance comprising:
   a direct-current voltage source producing an input voltage;
   a power supply device producing a desired output from the input voltage; and
   a load driven with the output voltage,
   wherein the power supply device comprises
   a DC/DC converter producing an intermediary voltage from the input voltage;
   a series regulator producing the desired output voltage from the intermediary voltage;
   an output current monitoring circuit monitoring an output current flowing through the series regulator; and
   an intermediary voltage adjustment circuit adjusting feedback control of the DC/DC converter such that, as the monitored output current increases, the intermediary voltage increases and that, as the monitored output current decreases, the intermediary voltage decreases.

6. The electric appliance according to claim 5, wherein the intermediary voltage adjustment circuit adjusts the feedback control of the DC/DC converter such that the intermediary voltage is so produced as to be higher than the desired output voltage by a forward voltage drop across an output transistor included in the series regulator.

7. The electric appliance according to claim 6, wherein the DC/DC converter produces the intermediary voltage from the input voltage according to a feedback voltage whose voltage level varies with the intermediary voltage, and the intermediary voltage adjustment
circuit adjusts the voltage level of the feedback voltage according to the monitored output current.

8. The electric appliance according to claim 7, wherein the feedback voltage is a division voltage obtained by dividing the intermediary voltage in a predetermined division ratio, and the intermediary voltage adjustment circuit adjusts the voltage level of the feedback voltage by varying the division ratio according to the monitored output current.

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