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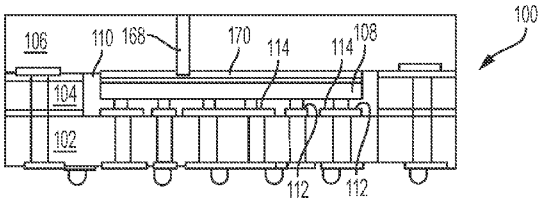

FIG. 2A

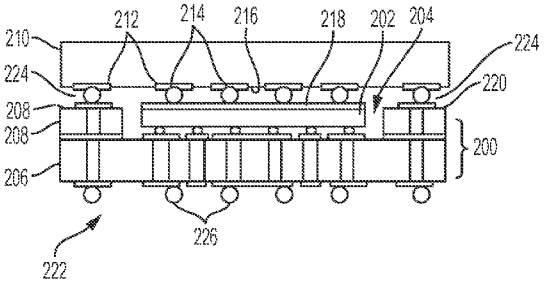

FIG. 3D

(57) Abstract: Structures and methods of fabricating semiconductor wafer assemblies (100) that encapsulate at least one die (108, 202, 402) in a cavity (110, 204, 404) etched into an oxide bonded semiconductor wafer stack (102+104, 206+208, 406+408). The methods generally include the steps of positioning the die (108, 202, 402) in the cavity (110, 204, 404), mechanically and electrically mounting the die (108, 202, 402) to the wafer stack (102+104, 206+208, 406+408), and encapsulating the die (108, 202, 402) within the cavity (110, 204, 404) by bonding a lid wafer (106, 210, 410) to the wafer stack (102+104, 206+208, 406+408) in one of multiple ways. Semiconductor processing steps are applied to construct the assemblies (e.g., deposition, annealing, chemical and mechanical polishing, etching, etc.) and connecting the die (e.g., bump bonding, wire interconnecting, ultrasonic bonding, oxide bonding, etc.) according to the embodiments described above. The cavity (110, 404) may be hermetically sealed to encapsulate the semiconductor die (108, 402). The wafer assembly (100) may be diced to produce one or more semiconductor chips, each semiconductor chip including one or more encapsulated semiconductor die (108, 202, 402). A thermal interface (164, 170, 412) may be comprised between the semiconductor die (108, 402) and one or more of the wafers (102, 104, 106, 406, 408, 410). The wafer stack (102+104, 406+408) and the lid wafer (106, 410) may be oxide bonded together. Alternatively, the wafer stack (206+208) and the lid wafer (210) may be bump (214) bonded so as to define an air gap (224) providing thermal isolation from the cavity (204). One of the wafers (102, 104, 106) may define a conduit (168) to the cavity (110) from the exterior of the wafer assembly (100),

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wherein the conduit (168) and the cavity (110) are at least partially filled with a thermally conductive material, are evacuated and sealed providing a vacuum package or are evacuated and backfilled with a liquid or gas before sealing.

DIE ENCAPSULATION IN OXIDE BONDED WAFER STACK

BACKGROUND

[0001] The present disclosure relates to fabrication of integrated circuits, semiconductor devices and other miniaturized devices, and more particularly, to fabrication of three-dimensional integrated circuits (3D-ICs) including semiconductor dies encapsulated in an oxide bonded wafer stack.

[0002] As semiconductor device sizes have decreased, 3D device integration has become a desired method for increasing the density of integrated circuits and/or semiconductor devices, offering much smaller form factor along with higher performance and lower power compared to 2D designs. 3D-IC assemblies are comprised of two or more stacked layers of active electronic components (e.g., sensors and readout circuits) using horizontal intra-tier and vertical (through-silicon vias, TSVs) inter-tier connectivity so that they behave as a single device. Package-to-package stacking and die-to-die (D2D) stacking allow selection of "known good dies" for stacking and can provide higher yield but limited performance improvement compared to 3D. 2D approaches sometimes use wire bonds that require a long connection which slows the speed and limits the number of possible connections. More elegant 2.5D solutions use bump bonds to an interposer that provides routing between circuits, but still result in higher power and lower performance than true 3D circuits. Also, due to the ultra-thin nature of the die, D2D stacks are difficult to handle and susceptible to breakage and contamination. Wafer-to-wafer (W2W) 3D stacking allows TSVs to be scaled down to smaller diameters with thinner wafers permitting higher 3D connection densities leading to higher bandwidth, performance, and power improvements and offering lower manufacturing costs. However, 3D stacking can suffer from reduced yields since, if any one of N chips in a 3D-IC is defective, the entire 3D-IC will be defective. In addition, the wafer stacking is optimal with wafers of the same size, and since non-silicon materials (e.g., III-V's) are typically manufactured on smaller wafers than silicon CMOS logic or DRAM, wafer level heterogeneous integration can pose manufacturing and yield challenges.

[0003] 3D integration using oxide bonding has been primarily used to bond full wafers as the processing is not as mature for bonding at the die level. Solder-seal wafer level packaging has been demonstrated, as has bonding of wafers with cavities. Known techniques are available for direct metal to metal bonding of an integrated circuit die onto a silicon wafer, but the techniques

have limitations for high layer count wafer stacking die to process stress, yield, interconnect density and thermal limitations. Other techniques have integrated multiple die onto an interposer, but have neither extended the stacking further in the z-axis to more than 2-3 layers, nor achieved heterogeneous or hermetically sealed devices.

[0004] The present disclosure contemplates a new and improved method for fabrication of 3D-ICs using die encapsulation that overcomes current limitations. Some embodiments also address the needed for on-chip thermal management permitting higher power dissipation and greater packaging densities.

SUMMARY

[0005] This disclosure is directed to oxide bonded semiconductor wafer assemblies encapsulating one or more device die, and processes for forming them. In one embodiment, the wafer assembly includes a first wafer having a first surface that includes an oxide layer, a second wafer having a first surface and a second surface, the first surface including an oxide layer that is bonded to the oxide layer of the first wafer, and wherein the first and second wafers define a cavity. A semiconductor die is mechanically and electrically connected to the first wafer in the cavity, and a third wafer having a first surface that is bonded to the second surface of the second wafer encapsulates the die. The die may be connected by a bump bond, a wire interconnection, an ultrasonic bond, and/or an oxide bond. The encapsulation may comprise a hermetic seal. Each of the wafers may include an integrated circuit (IC) and one or more through silicon vias (TSVs) for electrically connecting the ICs among the wafers and the die, and to external devices and wafers.

[0006] In another embodiment, a thermal interface may be formed between the semiconductor die and one or more of the wafers.

[0007] In another embodiment, the second (middle) wafer and the third (lid) wafer are bump bonded so as to define an air gap providing thermal isolation from the cavity.

[0008] In another embodiment, the second surface of the second (middle) wafer and the first surface of the third (lid) wafer each include an oxide layer. The second and third wafers may be oxide bonded together at their respective oxide layers.

[0009] In another embodiment, one or more of the first, second and third wafers may have a conduit to the cavity from the exterior of the wafer assembly. The conduit and the cavity may be

at least partially filled with a thermally conductive or other functional material. The conduit and cavity may be evacuated and sealed providing a vacuum package to enhance thermal isolation. The conduit and cavity may be evacuated and backfilled with a liquid or gas before the cavity is sealed.

[0010] In another aspect, methods of fabricating semiconductor wafer assemblies that encapsulate one or die in a cavity etched into an oxide bonded semiconductor wafer stack. The methods generally include the steps of positioning the die in the cavity, mechanically and electrically mounting the die to the wafer stack, and encapsulating the die within the cavity by bonding a lid wafer to the wafer stack in one of multiple ways. Semiconductor processing steps are applied to construct the assemblies (e.g., photolithography, deposition, annealing, chemical and mechanical polishing, etching, etc.) and connecting the die (e.g., bump bonding, wire interconnecting, ultrasonic bonding, oxide bonding, etc.) according to the embodiments described above.

[0011] Other objects and advantages of the disclosed embodiments will be better appreciated from the following detailed description.

BRIEF DESCRIPTION OF THE FIGURES

[0012] Various aspects of at least one embodiment of the present disclosure are discussed below with reference to the accompanying figures. It will be appreciated that for simplicity and clarity of illustration, elements shown in the drawings have not necessarily been drawn accurately or to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity or several physical components may be included in one functional block or element. Where considered appropriate, reference numerals may be repeated among the drawings to indicate corresponding or analogous elements. For purposes of clarity, not every component may be labeled in every drawing. The figures are provided for the purposes of illustration and explanation and are not intended as a definition of the limits of the invention. In the figures:

[0013] **FIG. 1** is a flowchart of three alternative methods for encapsulating one or more device die in an oxide bonded 3D-IC wafer stack, according to illustrative embodiments;

[0014] **FIGS. 2A-2F** are schematic cross-sectional illustrations of unassembled and partially assembled components of a 3D-IC wafer stack, and **FIGS. 2G** and **2H** are schematic cross-

section illustrations of 3D-IC semiconductor wafer assemblies according to certain embodiments;

[0015] **FIGS. 3A-3C** are schematic cross-sectional illustrations of partially assembled components of a 3D-IC wafer stack, and **FIG. 3D** is a schematic cross-section illustration of a 3D-IC wafer assembly, according to certain embodiments; and

[0016] **FIGS. 4A-4C** are schematic cross-sectional illustrations of partially assembled components of a 3D-IC wafer stack, and **FIG. 4D** is a schematic cross-section illustration of a 3D-IC wafer assembly, according to certain embodiments.

DETAILED DESCRIPTION

[0017] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the aspects of the present disclosure. It will be understood by those of ordinary skill in the art that these may be practiced without independently some of these specific details. In other instances, well-known methods, procedures, components and structures may not have been described in detail so as not to obscure the embodiments.

[0018] The following descriptions of preferred embodiments are merely exemplary in nature and are in no way intended to limit the disclosure, its application, or uses. Also, it is to be understood that the phraseology and terminology employed herein are for the purpose of description only and should not be regarded as limiting. It is appreciated that certain features, are, for clarity, described in the context of separate embodiments but may also be provided in combination in a single embodiment. Conversely, various features are, for brevity, described in the context of a single embodiment but may also be provided separately or in any suitable sub-combination.

[0019] No element, act, or instruction used herein should be construed as critical or essential unless explicitly described as such. As used herein, the articles “a” and “an” are intended to include one or more items, and may be used interchangeably with “one or more.” Further, the phrase “based on” is intended to mean “based, at least in part, on” unless explicitly stated otherwise. It will be further understood that the terms “comprise”, “have”, “include”, and “contain”, and any forms of these terms, are open-ended linking verbs. As a result, a method or device that “comprises,” “has,” “includes,” or “contains” one or more steps or elements possesses those one or more steps or elements, but is not limited to possessing only those one or

more steps or elements. Furthermore, a device or wafer structure that is described configured in a certain way is configured in at least that way, but may also be configured in ways that are not shown.

[0020] For purposes of the description hereinafter, the terms "upper", "lower", "top", "bottom", "vertical", "horizontal", "front side", "back side" and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. The terms "on top", "adjacent", "positioned on" or "positioned atop" mean that a first element, such as a first device structure or layer, is present on or in proximity to a second element, such as a second device structure or layer, wherein intervening elements, such as an interface structure or layer may be present, and does not necessarily mean, for example, that a first wafer layer and a second wafer layer are directly contacting one another without any intermediary conducting, insulating or semiconductor layers at the interface of the two layers.

[0021] Semiconductor elements, such as a ball grid array (BGA), can be used as part of aerospace sensor architectures and/or other semiconductor architectures. In the photonics domain, III-V materials based on indium phosphide (InP) and gallium arsenide (GaAs) have been a key enabler due to the excellent photonic properties associated with the direct band gap of these materials. In most instances, each of the semiconductor elements is soldered to a primary circuit board (e.g., motherboard, array, etc.) creating the semiconductor array. As used herein, the term "die" refers to a small piece of semiconductor material that has been fabricated with an IC, including but not limited to CMOS, optoelectronics, infrared detectors, MEMS, and the like, and the term "wafer" is used to refer to a thin slice of semiconductor material that may comprise substrate layers and/or be used in the fabrication of ICs. Wafers are typically configured round, but may be any size or shape that is compatible with oxide bond processing, including but not limited to rectangular panel sizes or diced shapes and sizes. The terms "bump" and "bumping" refer to a semiconductor packaging technique that attaches solder balls to bond pads of a wafer or die (e.g., at a TSV connector pad), forming a point of connection to other devices and/or wafers in a wafer stack or assembly. The bond pads may be oxide bonded to a supportive wafer, such as through DBH bonding, electroless nickel immersion gold under bump metallization, etc. For purposes of clarity only, the term "semiconductor wafer assembly" refers to a composite structure of multiple semiconductor wafers and at least one die encapsulated therein that results from fabrication according to any of the embodiments of the currently disclosed methods, while

the term "wafer stack" is used to refer to a wafer and die structure at any intermediate stage of the fabrication of the semiconductor wafer assembly.

[0022] In most D2W applications, electronic components are built on two semiconductor wafers. One wafer is diced, and the singulated die are aligned and connected (e.g., by bonding, wire interconnections, etc.) onto die sites of the second wafer. As in W2W methods, thinning and TSV interconnection creation are performed in D2W applications either before or after bonding.

[0023] Referring to **FIG. 1**, a flowchart illustrates a method **10** (having multiple alternative embodiments) for forming a semiconductor wafer assembly in which a device die is encapsulated within three semiconductor wafers, each of which may include an IC. The individual steps of embodiments of method **10** are described in detail with reference to **FIGS. 2A-2H**, **3A-3D** and **4A-4D** hereinafter. The embodiments include steps not shown for conventionally creating circuitry (e.g., traces, components, electrical vias) on one or more of semiconductor wafers to be used in manufacturing wafer assemblies. The embodiments of method **10** begin with common initial step **12** (forming corresponding TSV in opposed faces of two silicon wafers), step **14** (forming and direct bond hybridization (DBH) oxide bonding TSV bump pads onto the wafers and depositing an oxide layer on the opposed faces), step **16** (planarizing and bonding the wafers), and **18** (revealing the TSV, forming and DBH oxide bonding TSV pads, depositing and planarizing an oxide layer on a top surface of the wafer stack, and then a hard protect mask in preparation for etching the top surface). The embodiments of method **10** then diverge slightly to accommodate varying connection options between the wafers and the encapsulated die of the finished wafer assembly. Each embodiment includes a step (e.g., steps **20**, **30**, **40** respectively) for etching one or more cavities into the wafer stack, removing the hard protect mask, and preparing variants of a third wafer to be used as a cavity-sealing lid.

[0024] Distinct configurations of the finish semiconductor wafer assembly are achieved through the varying final steps of three exemplary embodiments of method **10**. In a first embodiment, step **22** (mounting and bonding die, lid wafer polishing), step **24** (lid wafer bonding) and optional step **26** (conduit etch, thermal filling; dicing) form the wafer assembly such that one or more die bump bonded to the bottom wafer are hermetically sealed in an etched cavity. In a second embodiment, step **32** (die and cavity preparation), step **34** (die attachment and lid wafer bumping) and step **36** (lid wafer attaching, bottom wafer TSV bumping, dicing)

form the wafer assembly such that a lid wafer encapsulates and is bump bonded to the mounted die, as well as the middle wafer. A third embodiment of method **10** is similar to the first embodiment, except that steps **42** (die mounting and bonding, thermal interface forming), **44** (cleaning, oxide bonding lid wafer) and **46** (bottom wafer TSV bumping, dicing) result in an oxide bond between the lid wafer and a thermal interface bonded to the encapsulated die. While the optional etching of a conduit (or vent) and underfilling with a thermal material is shown only in step **26**, it is understood that such operations could be employed in any of the embodiments.

[0025] **FIGS. 2A-2H**, **3A-3D** and **4A-4D** schematically show wafer structures corresponding to successive individual process steps of embodiments of method **10**. With reference to the schematic cross sectional illustration of a first embodiment of a semiconductor wafer assembly **100** shown in **FIG 2A**, disclosed herein are techniques that enable wafer (or substrate) bonded 3D-IC integration in a device package that uses oxide bonding of one or more semiconductor wafers (e.g., bottom wafer **102**, middle wafer **104** and lid wafer **106**) to enclose, hermetically if so desired, a die **108** within a sealed volume, such as cavity **110** that has been etched into one or more of the wafers **102**, **104**, **106**. The techniques allow incorporation of device die types in a format appropriate for wafer scale 3D-IC integration that may not be accommodated by conventional processing. The die **108** is typically formed of a semiconductor material such as silicon, though it is foreseeable that other materials could be used. Mechanical and electrical integration of the die **108** to bottom wafer **102** and optionally lid wafer **106** can be performed through DBH bonding or by using bump bonding at bumps **112** and pads **114**. In other embodiments, the die **108** may be mechanically and electrically connected by wire or similar interconnection and/or by an oxide or an ultrasonic bond.

[0026] **FIG. 2B** is a schematic cross-sectional illustration (that corresponds to step **12** of method **10**), of unassembled bottom wafer **102** and middle wafer **104** used in front end processing of wafer assembly **100**. Middle wafer **104** may be comprised of silicon or other etchable material, while the bottom wafer **102** and top wafer **106** may by comprised of silicon or a different material, such as silicon carbide, fused silica, glass, sapphire, gallium arsenide, indium phosphide, silicon on insulator (SOI), metals, ceramics and other dielectric, conductive, or semiconductor materials. In this embodiment, the wafers **102**, **104** may comprise semiconductor wafers, such as silicon semiconductor wafers, however other types of materials could be used. The wafers **102**, **104** are generally planar. Bottom wafer **102** includes a bottom

surface **116** and a cavity-facing top surface **118**, and middle wafer **104** includes a cavity-facing bottom surface **120** and a top surface **122**. Bottom wafer **102** may include an IC **124** disposed on or just below cavity-facing surface **118**. Middle wafer **104** may also have ICs **126**, **128** placed on or just below either or both of cavity-facing bottom surface **120** and top surface **122**.

[0027] A plurality of TSVs **130a**, **130b**, etc. (generally **130**) may be formed in each of wafers **102**, **104** and filled with electrically conductive materials (copper, aluminum, tungsten, doped polysilicon, etc.). TSVs **130** are selectively arranged to provide a plurality of electrical interconnections that allow the wafers **102, 104** to transmit electrical signals, e.g., to electrical components within a given wafer and/or between the device die **108** (of **FIG. 2A**). TSVs **130** can be formed using a variety of semiconductor processing methods. For example, in some embodiments, a series of photolithographic and chemical processes are performed to remove material from the wafers **102**, **104** to produce the vias **130**. In some embodiments, an additive process is used to add additional material to the wafers **102**, **104** to produce the TSVs **130**.

[0028] With reference to **FIG. 2C** (which corresponds to step **14** of method **10**), abutting surfaces **118**, **120** of bottom wafer **102** and middle wafer **104** are processed to prepare the wafers for bonding to create an intermediate wafer stack **132** (shown in FIG. 2D). In this embodiment, the surfaces **118**, **120** are processed to add one or more bump pads **134** for future interconnecting with the device die **102** (shown in **FIG. 1A**). Oxide layers **136**, **138** may then be formed on the opposing surfaces **118**, **120** of the wafers **102**, **104**. Silicon dioxide is formed on a silicon wafer surface when silicon is exposed to oxygen (or a fluid that includes oxygen, e.g., air). A thin layer (e.g., 10 Å) of oxide can be formed on the surfaces **118**, **120** when silicon is exposed to air under ambient conditions. Various semiconductor processing technologies are used to create silicon dioxide on silicon surfaces. These technologies typically involve processing the silicon wafer using higher temperatures and different environments (e.g., fluid) to controllably grow layers of silicon dioxide on silicon. For example, temperatures in excess of 600° C are often used in O2 or H2O environments. However, 350° C is often the limit for active silicon wafers, in order to avoid degrading performance of the wafer. The formed oxide layer on each surface **118**, **120** may then be polished to produce smooth oxide layer surfaces **136**, **138** that are co-planar with the bump pads **134**. Various techniques can be used to create the smooth surfaces. For example, chemical or mechanical planarization of wafer surfaces **118**, **120** can be accomplished to produce smooth surfaces by polishing, etching, or a combination of the two. In

some embodiments, the surfaces **118**, **120** of the wafers **102**, **104** may be smoothed by exposing the wafers to an abrasive and/or corrosive chemical in conjunction with a polishing pad that is in contact with the wafer surfaces **118**, **120** and is moved relative to the wafer surfaces. In some embodiments, the surfaces **118**, **120** are smoothed to a surface roughness of less than 10 Angstroms.

[0029] The wafers **102**, **104** may then be bonded together to form wafer stack **132** as shown in **FIG. 2D** (corresponding to step **16** of method **10**), which depicts a cross-sectional view of wafer stack **132**. The wafers **102**, **104** may be oxide bonded together by DBH and annealed by bringing their planarized oxide surfaces **118**, **120** into contact with each other to create a covalent bondline **139** between the wafers **112**, **114**. The covalent bondline **139** is generally thinner and has less thermal resistance than organic adhesive bonds currently used to join wafers together in a conventional wafer assembly. Because the covalent bondline **139** is relatively thin (e.g., thinner than solder bumps and underfill), interconnects can be placed on the wafers **102**, **104** with much higher spacing density.

[0030] With reference to **FIG. 2E** (which corresponds to step **18** of method **10**), the exposed bottom surface **116** of bottom wafer **102** and top surface **122** of top wafer **104** of wafer stack **132** may then be thinned and planarized to reveal ends **140** of TSVs **130**, and interconnect pads **142** may be oxide bonded onto surfaces **116**, **122** at the revealed TSVs ends **140**. An oxide layer (not shown) may then be selectively added and planarized, and a hard mask **144** formed over regions of wafer surface **122** to be protected from a subsequent etching process.

[0031] With reference to **FIG. 2F** (which corresponds to step **20** of method **10**), cavity **110** may then be formed in the wafer stack **132** through etching of region **146** of top surface **122** of middle wafer **104** unprotected by the hard protection mask **144** (each shown in **FIG. 2E**). Use of hard protection mask **144** (e.g., comprised of a TiW alloy) permits a much wider processing temperature range, enabling the device die (not shown) to be mounted in the cavity **110** using a wide range of techniques. Cavity **110** may be etched into the middle wafer **104** down to a buried oxide (BOX) layer **148** at oxide bondline **139** previously formed (step **16**) between bottom wafer **102** and middle wafer **104**. The BOX layer **148** serves as an etch stop for the cavity etch process, revealing the bump pads **134** for connecting to device die **108** (shown in **FIG. 2G**) that were previously formed (step **14**) on the surfaces of the wafers **102**, **104**. An outer perimeter of the cavity **110** may be defined by the intersection of the substantially planar BOX layer **148** with

substantially vertical sidewalls **150**, **152** of the cavity **110** (and to be further defined by bottom surface **154** of to-be-added lid wafer **106**). Cavity **110** may be etched with dimensions based upon the number and size of dies to be encapsulated and upon thermal management design requirements, utilizing a silicon etching method, preferably deep reactive ion etch (DRIE), producing nearly vertical sidewalls orthogonal to the BOX layer **148**. Alternatively, cavity **110** may be etched using a reactive ion etch (RIE) or an anisotropic chemical etch (which may result in inclined or sloped sidewalls.) The functions of cavity **110** include providing device die **108** environmental protection, high density circuit interconnections, physical packaging and thermal interfaces, as well as to obscure device functionality and provide device security from reverse engineering. Bottom surface **154** of lid wafer **106** (which may include a down-facing IC **156**) may contemporaneously be prepared for oxide bonding through oxide layer forming and planarization.

[0032] With reference to **FIG. 2G** (which corresponds to step **22** of method **10**), one or more homogeneous or heterogeneous device die **108** may then be mechanically and electrically connected to bump pads **134** exposed in cavity **110** via bumps **158**. The die mounting process may comprise a variety of techniques, including ultrasonic bonding, solder bumping (e.g., via bump bonds **134**), or oxide bonding, Wirebond, epoxy, and may include electrical, mechanical, or thermal interfaces in multiple configurations on any of the surfaces between the die and wafer **102**, **104** to which the diet is bonded. Table One presents example transient liquid phase solder bump technologies that could be utilized for mounting device die **108**.

Material System	Process Time and Temp.	Re-melt Temp
Cu-In	4 min at 180C	> 307C
Cu-Sn	4 min at 280C	> 415C
Ag-Sn	60 min at 250C	> 600C
Ag-In	120 min at 175C	> 880C
Au-Sn	15 min at 260C	> 278C
Au-In	0.5 min at 200C	> 495C
Ni-Sn	6 min at 300C	> 400C

Table One

[0033] With reference to **FIG. 2H** (which corresponds to step **24** of method **10**), after the die **108** is mounted to bump pads **134** in the cavity **110**, the hard mask layer **144** (shown in **FIG. 2G**) may be removed, allowing the lid wafer **106** to be mounted to the wafer stack **132**. In the embodiment shown, cavity **110** is thereby enclosing with extremely robust oxide bonds at wafer interfaces **160**, **162** between the remaining portion of top surface **118** of middle wafer **104** and bottom surface **154** of lid wafer **106**. Optionally, a thermal material layer **164** may be formed on the die **108**, providing a thermal interface between die **108** and lid wafer **106**. Additionally, or alternatively, similar thermal interfaces (not shown) may be formed between the die **108** and one or more of the other wafers **102**, **104** and/or other die in order to assist in thermally managing the 3D-IC wafer assembly **100**. Lid wafer **106** may be oxide bonded at interfaces **160**, **162** to form a complete semiconductor wafer assembly **100**. In some embodiments, the lid wafer **106** may comprise an external layer of a wafer-on-wafer stack resulting from a completely independent semiconductor fabrication process. The revealed ends **166** of TSVs **130** in, and the interconnect pads **142** formed on bottom surface **116** of bottom wafer **102** may provide electrical paths for connection(s) between the die **108** and wafers **102**, **104**, **106** to external devices and wafers (not shown). In other embodiments, the remaining portion of top surface **118** of middle wafer **104** and bottom surface **154** of lid wafer **106** may be bonded at the interfaces **162**, **164** using a solder or a thermocompressive bond. As noted, the bonding process may seal cavity **110** at the interfaces **160, 162** so as to form a hermetic seal encapsulating the device die **108**.

[0034] The top surface **118** and bottom surface **154** can be bonded at the interfaces **160**, **162** in the absence of any external pressure. However, in some embodiments such as thermocompressive bonding, additional pressure is applied to force the surfaces **118**, **154** into contact with each other. The die **108** may be interconnected through metal features (e.g., bump pads, vias, etc.) or circuity exposed within the cavity **110** to any or all of the wafers **102**, **104**, **106** in the 3D wafer assembly **100**, each of which may contain one or more electrically conductive ICs **124**, **126**, **166**, including active or passive ICs, which can be either planar on any surface, or vertically arranged through the wafer.

[0035] With reference again to **FIG. 2A** (some features of which correspond to processing step **26**), a hole or conduit **168** may be etched through any or all of the wafers **102**, **104**, **106**, for example, so as to allow ingress of a thermal or structural material to make contact with the encapsulated die **108**. Alternatively, this conduit **168** could be used to purge or backfill the

cavity **110** with a desired gas or liquid to enhance certain properties of the embedded ICs. A thermally conductive material **170** (e.g., a non-conductive cooling fluid, or any number of materials used for thermal, electrical, chemical, protective functions, or mechanical purposes) may fill a portion or all of the cavity **110** and then the conduit **168** may be plugged (e.g., with solder, etc.) or filled with the thermally conductive material **170**. Alternatively, the conduit **168** may serve as a thermal vent to and from cavity **110**. The completed first embodiment of the 3D-IC wafer assembly **100** may then be diced by conventional means.

[0036] Those of skill in the art will appreciate the advantages that the disclosed techniques provide, including the ability to manage D2W yield losses independently from W2W processes that form wafer stacks that may be bonded to the 3D-IC wafer assemblies **100** such as described above. The yield of devices resulting from the processes disclosed herein is improved by incorporating only "known-good die" into the devices and thereby avoiding stacking yield loss, which decreases the overall costs. Furthermore, the ability to bond thin dies allows for the stacking of multiple device layers, including those from different technologies, connected vertically utilizing TSVs while maintaining a low-profile package and short electrical path lengths. Different device dies often have distinct thicknesses (e.g., 100μm - 700μm). In order to accommodate dissimilar die thicknesses in multiple die encapsulation wafer assembly embodiments, middle wafer **104** can be fabricated to have a thickness (and thus, cavity depth) greater than that of the thickest interconnected die **108**, in order to eliminate the need to closely match III-V device thicknesses, and also to provides thermal isolation. In addition, blind frontside via processes may be employed for wafers connecting to the D2W assemblies **100** in order to contain costs, and permits back-off positions for solder bum processing for die mounting and external wafer connections. Conventional organic bonds used in underfilling attachment of individual dies together is performed after individual chips/dies have been excised from an array; whereas the technology described herein permits the bonding to be performed at the wafer level. In some embodiments, the covalent bondlines may be 10 times thinner than an organic bondline.

[0037] **FIGS. 3A-3D** are schematic cross-sectional illustrations of exploded and integrated views of a wafer stack **200** undergoing processing according to a second method embodiment (corresponding to steps **30-36** of method **10**) to fabricated an alternative embodiment of an oxide bonded wafer assembly encapsulating a device die **202** in a cavity **204** formed by a bottom wafer **206**, middle wafer **208** and lid wafer **210**. The front end semiconductor processes employed in

fabricating this alternative wafer assembly may be identical to those described in association with **FIGS. 2A-2D** of the first method embodiment. The wafer processing results depicted in **FIGS. 3A-3D** have some similarities (e.g., general semiconductor processing techniques, orientations and compositions of the wafer, etc.), but differ in several aspects from those shown in **FIGS. 2E-2H**. **FIG. 3A** illustrates wafer stack **200** comprised of bottom wafer **206** and middle wafer **208**, into which one or more cavity **204** has been etched. As shown in **FIGS. 3B-3D**, different back end processes may be utilized in this second embodiment to form bump pads **212** and bumps **214** (which may be thermal bumps where connected to die **202**) on a bottom surface **216** of lid wafer **210**. The lid wafer **210** is bump bonded to a back side **218** of mounted die **202** and to middle wafer **208** at connection points **220**. Bump bonding the lid wafer **210** to the middle wafer **208** (as opposed to the oxide bonding of the first method embodiment) results in a 3D-IC semiconductor wafer assembly **222** such as depicted in **FIG. 3D**, in which the middle wafer **208** and the lid wafer **210** define an air gap **224**, rather than encapsulating the device die **202** in a hermetically sealed cavity. Lid wafer **210** may be electrically and mechanically coupled to middle wafer **208** through solder ball bonds **224** which, for example, enables electrical signals to be passed among the wafers **206, 208, 210** and die **202** in the wafer assembly **222**. Once the lid wafer **210** is bonded, the completed, electrical connections **226** may be added to the wafer assembly **222** for connecting to external devices, wafers, etc., and the wafer assembly may be further processed and/or diced.

[0038] **FIGS. 4A-4D** are schematic cross-sectional illustrations of exploded and integrated views of a wafer stack **400** undergoing processing according to a third method embodiment (corresponding to steps **40-46** of method **10**) to fabricated an alternative embodiment of an oxide bonded wafer assembly encapsulating a device die **402** in an enclosed cavity **404** defined by a bottom wafer **406**, middle wafer **408** and lid wafer **410**. The front end semiconductor processes employed in fabricating this alternative wafer assembly may be identical to those described in association with **FIGS. 2A-2D** of the first method embodiment. The wafer processing results depicted in **FIGS. 4A-4D** have some similarities (e.g., general semiconductor processing techniques, orientations and compositions of the wafer, etc.), but differ in several aspects from those shown in **FIGS. 2E-2H**. One variation from the first embodiment is shown in **FIG. 4B**, wherein a thermal interface layer **412** (or other functional layer such as described above) may be formed on the device die **402** either before or after attaching the die **402** in the cavity **404**. The

thermal interface layer **412** may then be planarized, cleaned and oxide bonded in a manner similar to that described above, as may contemporaneously be an opposing bottom surface **418** of lid wafer **410**. Electrical bumps **420** for external connection to other wafers (not shown) may be added to surface **422** of bottom wafer **406**, as shown in **FIG. 4D**. Lid wafer **410** may be electrically and mechanically coupled to middle wafer 408 at top surface regions **414**, **416** and to thermal layer **412**. The bonding between middle layer 406 and lid layer **408** results in a composite 3D-IC wafer assembly **424** having a hermetically sealed cavity **404** encapsulating device die **402**. The surfaces **414, 416, 418**, may be prepared to be planarized oxide surfaces (similarly as described with respect to, for example, **FIGS. 2A-2H**) prior to bonding the wafers together.

[0039] As various modifications could be made to the exemplary embodiments, as described above with reference to the corresponding illustrations, without departing from the scope of the disclosure, it is intended that all matter contained in the foregoing description and shown in the accompanying drawings shall be interpreted as illustrative rather than limiting. Thus, the breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims appended hereto and their equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor wafer assembly, comprising:

a first wafer including an integrated circuit, and having a first surface that includes an oxide layer;

a second wafer having a first surface and a second surface, the first surface including an oxide layer that is bonded to the oxide layer of the first semiconductor wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit, and having a first surface that is bonded to the second surface of the second wafer, thereby encapsulating the semiconductor die within the cavity.

2. The semiconductor wafer assembly of claim 1, wherein the semiconductor die is mechanically and electrically connected to the first wafer by at least one of a bump bond, a wire interconnection, an ultrasonic bond, and an oxide bond.

3. The semiconductor wafer assembly of claim 1, wherein the cavity is hermetically sealed to encapsulate the semiconductor die.

4. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the third wafer is proximate the first surface of the third wafer and electrically connected to the first and second wafers.

5. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the first wafer is proximate the first surface of the first wafer that is electrically connected to the second and third wafers.

6. The semiconductor wafer assembly of claim 1, wherein the wafer assembly is configured to produce one or more stacked integrated circuits, each including one or more encapsulated semiconductor dies, when the wafer assembly is diced.

7. The semiconductor wafer assembly of claim 1, further comprising at least one electrical path to the semiconductor die through at least one of the first, second and third wafers to an exterior surface of the wafer assembly.

8. The semiconductor wafer assembly of claim 1, further comprising one or more thermal interfaces between the semiconductor die and one or more of the first, second, and third wafers.

9. The semiconductor wafer assembly of claim 1, wherein the second wafer and the third wafer are bump bonded so as to define an air gap providing thermal isolation from the cavity.

10. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the first wafer is proximate the first surface, and the first wafer includes electrical paths through the first wafer to the integrated circuit.

11. The semiconductor wafer assembly of claim 1, wherein:
the second surface of the second wafer and the first surface of the third wafer each include an oxide layer; and
the second wafer and the third wafer are oxide bonded together at their respective oxide layers.

12. The semiconductor wafer assembly of claim 1, wherein one or more of the first, second and third wafers defines a conduit to the cavity from the exterior of the wafer assembly.

13. The semiconductor wafer assembly of claim 12, wherein the conduit and the cavity are at least partially filled with a thermally conductive material.

14. The semiconductor wafer assembly of claim 12, wherein the conduit and the cavity are evacuated and sealed providing a vacuum package.

15. The semiconductor wafer assembly of claim 12, wherein the conduit and the cavity are evacuated and backfilled with a liquid or gas before sealing.

16. The semiconductor wafer assembly of claim 1, wherein the second wafer includes an active integrated circuit interconnected to the integrated circuits of the first wafer and third wafer.

17. The semiconductor wafer assembly of claim 1, wherein the semiconductor die further comprises at least one oxide layer oxide bonded to at least one of the first wafer and the third wafer.

18. A method of encapsulating a die into a semiconductor wafer assembly, the method comprising:

etching a cavity into an oxide bonded semiconductor wafer stack;

positioning a semiconductor die in the cavity;

mechanically and electrically mounting the semiconductor die to the wafer stack; and

encapsulating the semiconductor die within the cavity by bonding a lid wafer to the wafer stack.

19. The method of claim 18, wherein mechanically and electrically mounting the semiconductor die comprises a process selected from bump bonding, wire interconnecting, ultrasonic bonding, and oxide bonding.

20. The method of claim 18, wherein bonding the lid wafer to the wafer stack further comprises:

creating an oxide layer a first surface of the wafer stack;

creating an oxide layer on a first surface of the lid wafer; and

bonding the oxide layer of the first surface of the wafer stack to the oxide layer of the first surface of the lid wafer to create a wafer assembly and to form a hermetic seal around the cavity.

21. The method of claim 18, further comprising forming a conduit from the exterior of the wafer assembly through the lid wafer to the cavity.

22. The method of claim 21, further comprising delivering a sufficient amount of a thermal material to the conduit to fill the conduit or the conduit and at least a portion of the cavity.

23. The method of claim 18, further comprising forming a thermal material layer on the semiconductor die.

24. The method of claim 18, further comprising dicing the wafer assembly to produce one or more semiconductor chips, each semiconductor chip including one or more encapsulated semiconductor die.

25. The method of claim 18, further comprising evacuating and sealing the conduit and the cavity to provide a vacuum package.

26. The method of claim 18, further comprising evacuating and backfilling the conduit and the cavity with a liquid or gas before sealing.

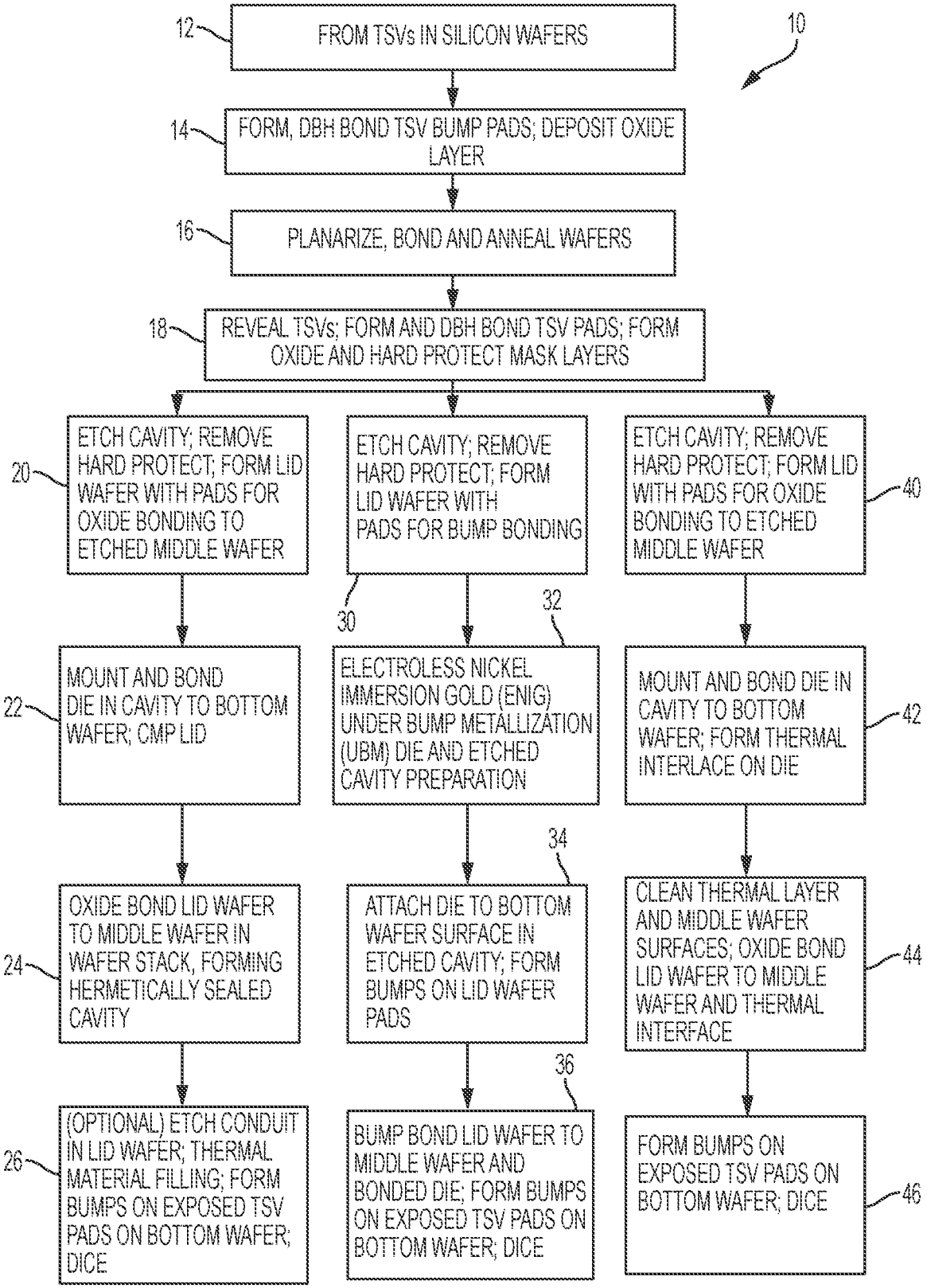
12
FROM TSVs IN SILICON WAFERS
10
14
FORM, DBH BOND TSV BUMP PADS; DEPOSIT OXIDE LAYER
16
PLANARIZE, BOND AND ANNEAL WAFERS
18
REVEAL TSVs; FORM AND DBH BOND TSV PADS; FORM OXIDE AND HARD PROTECT MASK LAYERS
20
ETCH CAVITY; REMOVE HARD PROTECT; FORM LID WAFER WITH PADS FOR OXIDE BONDING TO ETCHED MIDDLE WAFER
ETCH CAVITY; REMOVE HARD PROTECT; FORM LID WAFER WITH PADS FOR BUMP BONDING
ETCH CAVITY; REMOVE HARD PROTECT; FORM LID WITH PADS FOR OXIDE BONDING TO ETCHED MIDDLE WAFER
40
30
32
22
MOUNT AND BOND DIE IN CAVITY TO BOTTOM WAFER; CMP LID
ELECTROLESS NICKEL IMMERSION GOLD (ENIG) UNDER BUMP METALLIZATION (UBM) DIE AND ETCHED CAVITY PREPARATION
MOUNT AND BOND DIE IN CAVITY TO BOTTOM WAFER; FORM THERMAL INTERLACE ON DIE
42
34
24
OXIDE BOND LID WAFER TO MIDDLE WAFER IN WAFER STACK, FORMING HERMETICALLY SEALED CAVITY
ATTACH DIE TO BOTTOM WAFER SURFACE IN ETCHED CAVITY; FORM BUMPS ON LID WAFER PADS
CLEAN THERMAL LAYER AND MIDDLE WAFER SURFACES; OXIDE BOND LID WAFER TO MIDDLE WAFER AND THERMAL INTERFACE
44
36
26
(OPTIONAL) ETCH CONDUIT IN LID WAFER; THERMAL MATERIAL FILLING; FORM BUMPS ON EXPOSED TSV PADS ON BOTTOM WAFER; DICE
BUMP BOND LID WAFER TO MIDDLE WAFER AND BONDED DIE; FORM BUMPS ON EXPOSED TSV PADS ON BOTTOM WAFER; DICE
FORM BUMPS ON EXPOSED TSV PADS ON BOTTOM WAFER; DICE
46

FIG. 1

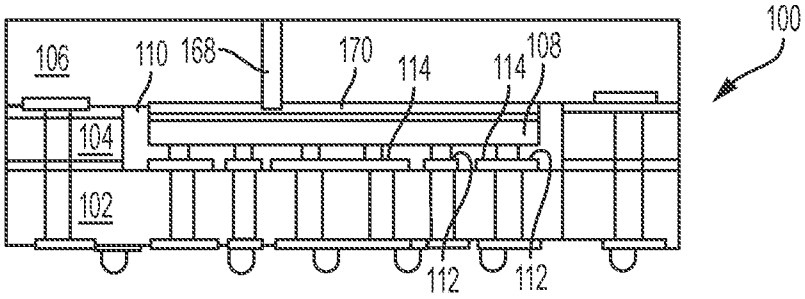

FIG. 2A

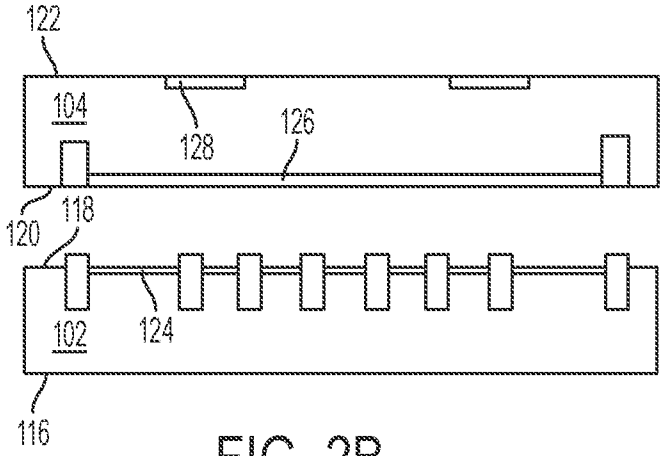

FIG. 2B

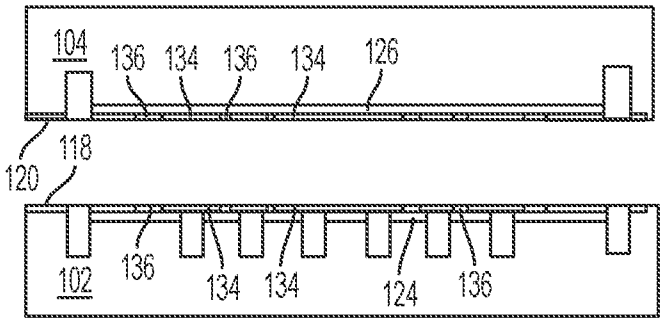

FIG. 2C

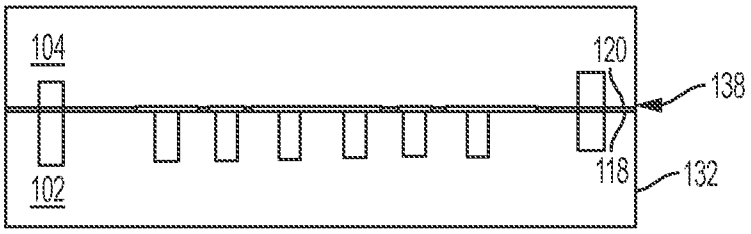

FIG. 2D

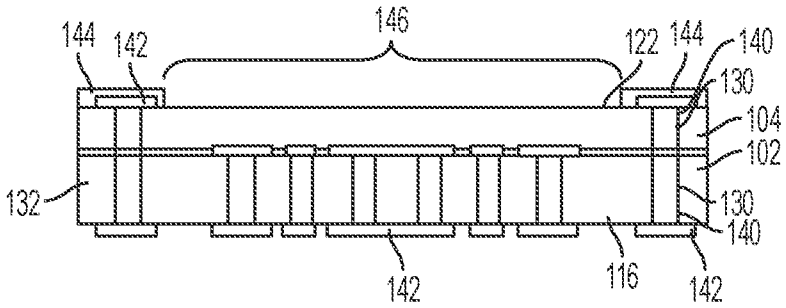

FIG. 2E

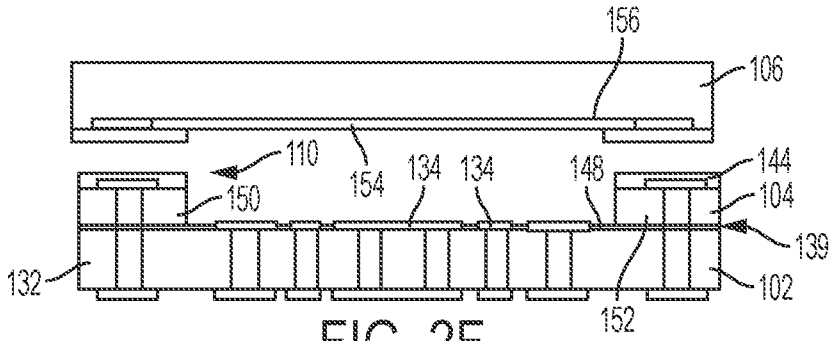

FIG. 2F

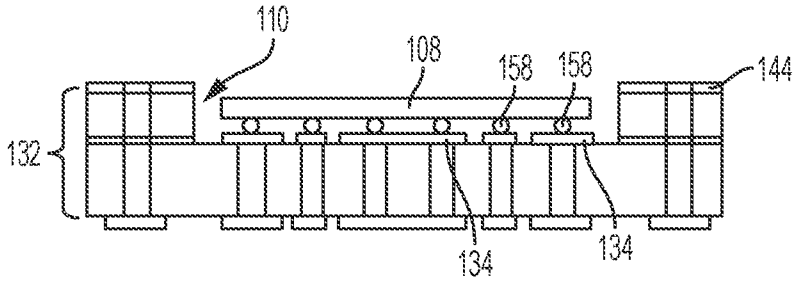

FIG. 2G

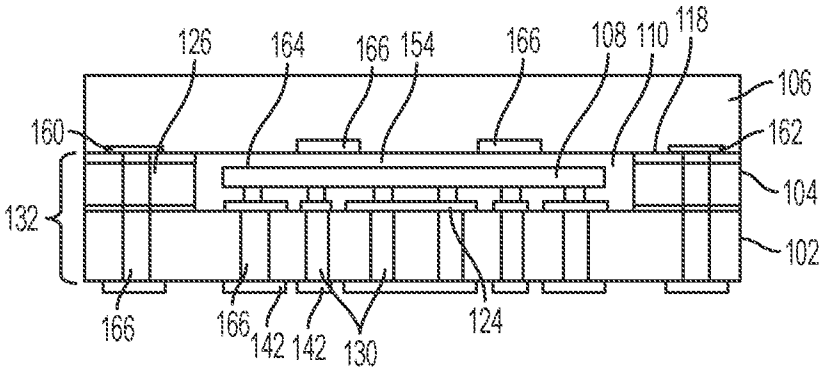

FIG. 2H

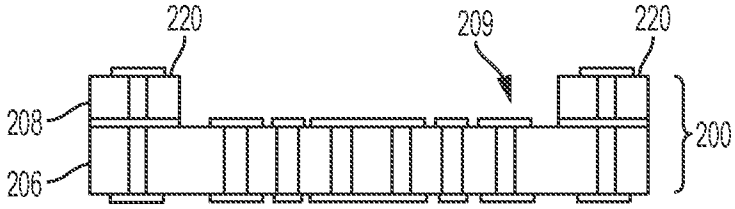

FIG. 3A

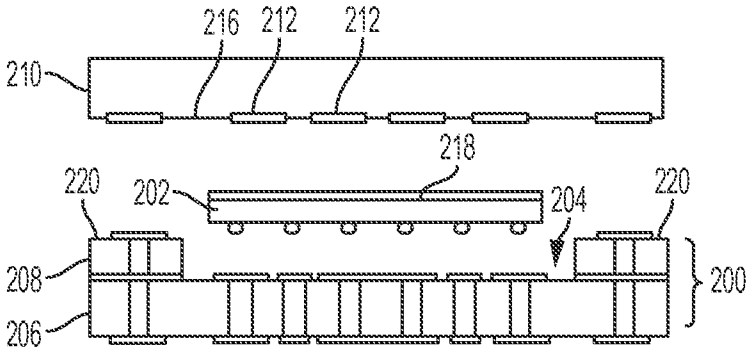

FIG. 3B

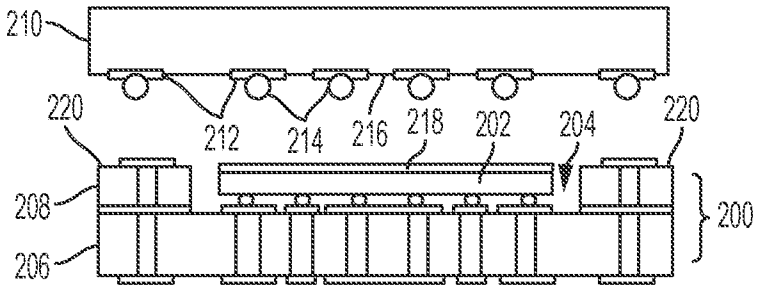

FIG. 3C

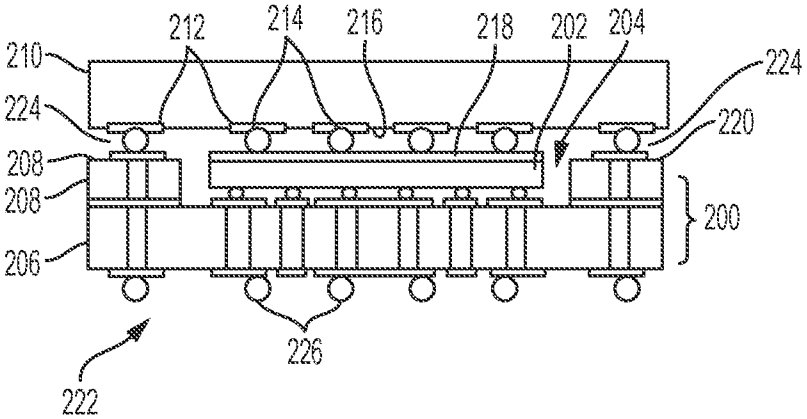

FIG. 3D

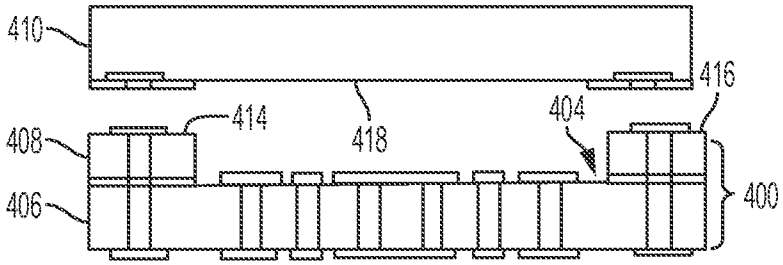

FIG. 4A

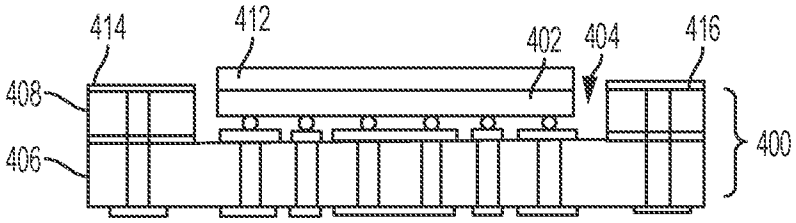

FIG. 4B

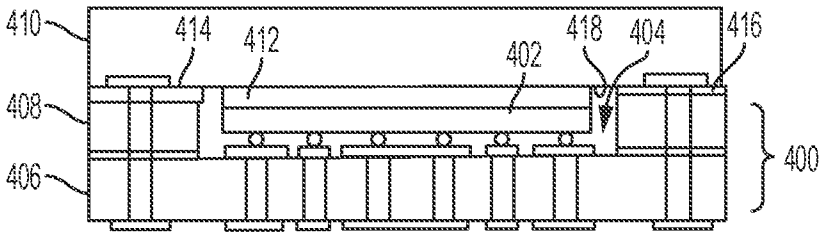

FIG. 4C

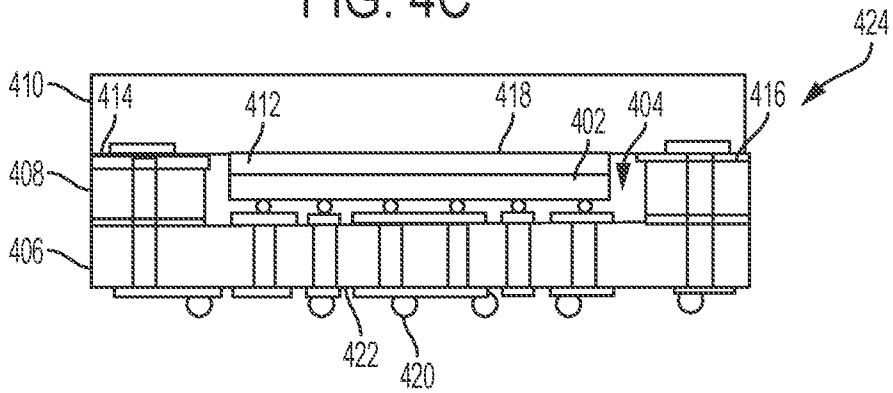

FIG. 4D

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/061922

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/065 H01L21/98 H01L23/10 H01L21/50 H01L21/54
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/216857 A1 (ZHAO YANG [US]) 28 September 2006 (2006-09-28) paragraph [0003] - paragraph [0008] paragraph [0022] - paragraph [0048] paragraph [0052] paragraph [0059] paragraph [0067] - paragraph [0069] figures 1-11, 17	1-7, 10-12, 14, 16-21, 24,25

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 February 2018	26/04/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Maslankiewicz, Pawel

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/061922

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 3 104 410 A1 (MITSUBISHI HEAVY IND LTD [JP]) 14 December 2016 (2016-12-14) paragraph [0020] paragraph [0031] - paragraph [0037] paragraph [0048] - paragraph [0049] figures 8-12, 20-21	1-7, 10-12, 14, 16-21, 24,25
Y	DRAB J: "Multilevel Wafer Stacking for 3D Circuit Integration", RAYTHEON TECHNOLOGY TODAY, no. 1, 2015, pages 30-31, XP055451119, the whole document	1-7, 10-12, 14, 16-21, 24,25
Y	WO 03/034490 A2 (HYMITE AS [DK]) 24 April 2003 (2003-04-24) page 5, line 8 - page 6, line 30 figures 1a-g	18-21, 24,25
A	US 2008/157330 A1 (KROEHNERT STEFFEN [DE] ET AL) 3 July 2008 (2008-07-03) paragraph [0038] - paragraph [0094] figures 2-14	1-7, 10-12, 14, 16-21, 24,25
A	US 2005/167795 A1 (HIGASHI MITSUTOSHI [JP]) 4 August 2005 (2005-08-04) paragraph [0137] - paragraph [0138] figures 9-10	2,19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/061922

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-7, 10, 11, 14, 16-20, 24, 25(completely); 12, 21(partially)

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7, 10, 11, 14, 16-20, 24, 25(completely); 12, 21(partially)

A semiconductor wafer assembly as in claim 1 and a method of encapsulating a die into a semiconductor wafer assembly as in claim 18,
with in addition the following special technical feature (cf. claims 2, 19): the semiconductor die is mechanically and electrically connected to the first wafer by at least one of a bump bond, a wire interconnection, an ultrasonic bond, and an oxide bond

The technical effect is associated with the manner of bonding the semiconductor die and the first wafer. The associated problem to be solved is how to provide a reliable mechanical and electrical connection between the semiconductor die and the first wafer.

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2. claims: 8, 13, 15, 22, 23, 26(completely); 12, 21(partially)

A semiconductor wafer assembly as in claim 1 and a method of encapsulating a die into a semiconductor wafer assembly as in claim 18,
with in addition the following special technical features: one or more thermal interfaces between the semiconductor die and one or more of the first, second and third wafers (claim 8),
forming a thermal material layer on the semiconductor die (claim 23)
or
filling the package with a selected material (thermally conductive material, gas or liquid) through a conduit (claims 13, 15, 22 and 26)

The technical effect of these special technical features is associated with ensuring desired thermal properties of the die neighbourhood, in particular of the interface between the semiconductor die and the wafers. The associated problem to be solved is how to reliably remove heat from the semiconductor die (see the description, pars. [0033], [0035]).

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3. claim: 9

A semiconductor wafer assembly as in claim 1,
with in addition the following special technical feature: bump bonding the second wafer and the third wafer so as to define an air gap

The technical effect is associated with thermal isolation

from the cavity. The associated problem to be solved is how to isolate the third wafer from the cavity and thus avoid the influence of heat generated by the components in the cavity on the third wafer.

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006216857 A1	28-09-2006	DE 102006046820 A1	03-05-2007
		US 2006216857 A1	28-09-2006
EP 3104410 A1	14-12-2016	EP 3104410 A1	14-12-2016
		JP WO2015136998 A1	06-04-2017
		US 2017025383 A1	26-01-2017
		WO 2015136998 A1	17-09-2015
WO 03034490 A2	24-04-2003	AT 464656 T	15-04-2010
		AU 2002351771 A1	28-04-2003
		CN 1605126 A	06-04-2005
		EP 1436837 A2	14-07-2004
		HK 1074913 A1	06-02-2009
		JP 4546087 B2	15-09-2010
		JP 2005506701 A	03-03-2005
		US 2003071283 A1	17-04-2003
		US 2004266038 A1	30-12-2004
		US 2005059204 A1	17-03-2005
		WO 03034490 A2	24-04-2003
US 2008157330 A1	03-07-2008	DE 102006062473 A1	03-07-2008
		US 2008157330 A1	03-07-2008
US 2005167795 A1	04-08-2005	EP 1433742 A2	30-06-2004
		JP 4342174 B2	14-10-2009
		JP 2004209585 A	29-07-2004
		KR 20040060733 A	06-07-2004
		US 2005167795 A1	04-08-2005
		US 2009068795 A1	12-03-2009