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(71) Applicant *(for all designated States except US)*: **XY-TRANS, INC.** [US/US]; 5422 Carrier Drive, Suite 201, Orlando, FL 32819 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **AMMAR, Danny F.** [—/—]; 7054 Horizon Circle, Windermere, FL 34786 (US). **GRAHAM, Ronald D.** [—/—]; 14139 Greater Pines Blvd., Clermont, FL 34711 (US).

(74) Agents: **WARTHER, Richard K.** et al.; Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A., 255 S. Orange Avenue, Suite 1401, P. O. Box 3791, Orlando, FL 32801 (US).

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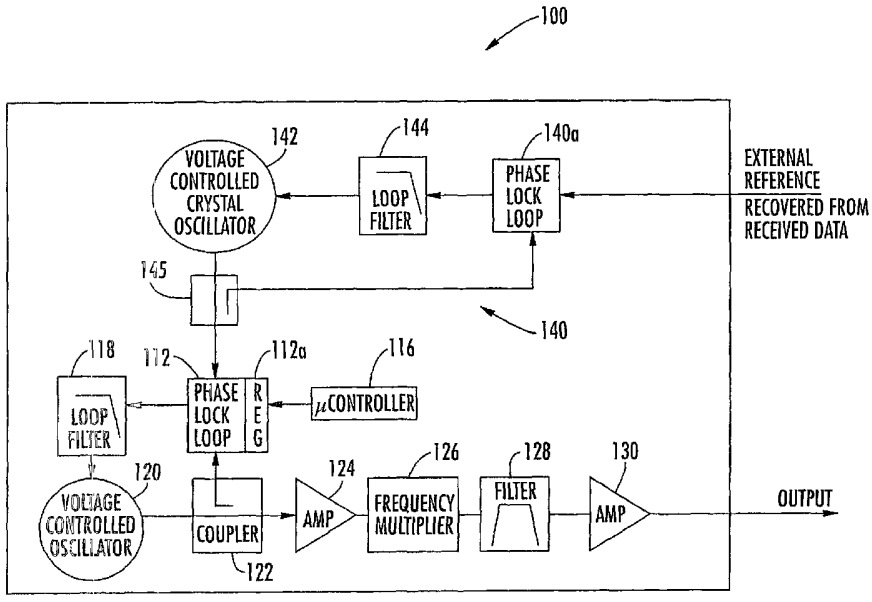
(54) Title: PHASE LOCKED LOOP (PLL) FREQUENCY SYNTHESIZER AND METHOD



(57) Abstract: A phase locked loop (PLL) frequency synthesizer generates a high frequency signal by generating an output signal from a voltage controlled oscillator of a primary phase locked loop (PLL) circuit. The voltage controlled oscillator output is programmably divided with a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency. An external reference signal used for the primary phase locked loop circuit is isolated by generating a voltage controlled, clean reference signal and filtering and synchronizing the clean reference signal with the external reference signal within a secondary phase locked loop circuit to produce the reference signal output to the primary phase locked loop circuit.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

PHASE LOCKED LOOP (PLL) FREQUENCY SYNTHESIZER AND METHOD

Related Application

This application is based upon prior filed copending provisional application Serial No. 60/383,866 filed May 29, 2002, the disclosure which is hereby incorporated by reference.

Field of the Invention

This invention relates to phase locked loop (PLL) frequency synthesizers, and more particularly, this invention relates to phase locked loop (PLL) frequency synthesizers that generate high frequency signals for microwave and millimeter wave radar and telecommunications equipment by using an external reference clock signal.

Background of the Invention

In many telecommunication systems and electronic testing instruments, a frequency synthesizer uses a phase locked loop (PLL) circuit to generate a continuous wave signal at a precise and stable frequency. These types of phase locked loop circuits are well known to those skilled in the art, and usually include a tunable voltage controlled oscillator (VCO) having an output signal that is locked to a known reference signal by a phase detector. Any output voltage is typically related to the phase difference between a reference signal and the voltage controlled oscillator output signal. The phase detector output is coupled back to the input of the voltage controlled

oscillator in a feedback loop to tune and lock the voltage controlled oscillator at a desired frequency. Thus, the phase and frequency of any final output signal from the voltage controlled oscillator has the same phase and frequency as the reference signal.

Programmable divider circuits are also used in the feedback loop between the voltage controlled oscillator and the phase detector to divide the voltage controlled output signal by a factor "N". Supplemental divider circuits can divide the reference frequency by a factor "M". By programming the value of the ratio "N" and "M", the voltage controlled oscillator output signal can be made equal to a desired multiple of the reference frequency.

In some prior art frequency synthesizer devices, digitally programmable continuous wave signals are generated by phase locked loop frequency synthesizers using a programmable divider operative with the reference signal. Other frequency synthesizers generate digitally programmable, continuous wave signals using digital rate multipliers and digital dividers. Rate multiplier circuits sometimes are used to program the reference frequency by suppressing pulses of a reference signal to various program values. Spur filters are sometimes operatively connected to phase detectors and a voltage controlled oscillator to reduce spurious FM side bands. Mixers can be interposed in the feedback path to shift and extend the set of frequencies that can be generated by the phase locked loop frequency synthesizer.

It is also well known that phase locked loop frequency synthesizers are commonly used to generate high frequency sources for microwave and millimeter wave radar and telecommunications equipment. The high frequency source, also known as the Local Oscillator

(LO), is used to up-convert low frequency transmitter signals to high frequency RF signals, or down-convert received RF signals to lower frequencies.

Traditionally, phase locked loop frequency synthesizers have used an accurate, relatively spur free, crystal oscillator reference typically found to be in the range of about 10 to about 100 MHz. The phase noise and spur levels of a reference clock signal are very critical, because at the output of a voltage controlled oscillator, any spurious signals are multiplied by the ratio of the voltage controlled oscillator to the phase comparison frequency. This directly impacts the performance of the closed phase locked loop circuit.

As is known to those skilled in the art, a typical phase locked loop circuit compares the phase of the divided reference clock, with that of the divided voltage controlled oscillator output signal. Any error detected in the phase between the signals is converted to a voltage that is used to correct the voltage controlled oscillator phase error. The correction voltage is applied through a filter to reduce spurious signals in the output signal, and improve the close-in, phase noise performance of the phase locked loop circuit. The loop bandwidth is typically established wide enough to reject the close-in noise of the voltage controlled oscillator, but narrow enough to reduce spurious signal levels in the signal output, thus, yielding an optimized noise spectrum that is better than that of the voltage controlled oscillator alone.

Summary of the Invention

It is an object of the present invention to provide a phased locked loop frequency synthesizer that can operate with a corrupted external reference clock and generate a spur-free output.

It is yet another object of the present invention to provide a phase locked loop frequency synthesizer that overcomes the drawbacks of the prior art as described above.

The present invention provides a novel and unobvious phase locked loop frequency synthesizer and method for generating microwave and millimeter wave signals by implementing a voltage controlled, oscillator-based, phase locked loop frequency synthesizer that can operate with a corrupted external reference clock, and yet generate a very accurate and relatively spur free output signal. The present invention is advantageous for wireless terrestrial and satellite communications where the transmission and reception sources are synchronized with a reference signal that has been recovered from received communications data, which may have been corrupted with noise and spurious signals. The circuit and method of the present invention provide faster lock times than a comparable and typical frequency locked loop circuit.

The present invention generates a relatively spur free, high frequency, local oscillator signal using a corrupted reference clock signal and isolates the corrupted reference clock signal from the frequency synthesizer circuits. The present invention prevents corruption of the frequency source. The voltage controlled oscillator output frequency can be multiplied to generate higher frequency local oscillator signals with very low spurious and harmonic signals. A secondary "reference signal" phased locked loop circuit with a narrow loop bandwidth reduces reference noise and spurious sidebands with faster lock times than a comparable frequency locked loop.

In accordance with the present invention, a phase locked loop (PLL) frequency synthesizer includes

a primary phase locked loop circuit having a voltage controlled oscillator (VCO) circuit and a programmable divider circuit for establishing a voltage controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency. A secondary "reference signal" phase locked loop circuit is operatively connected to the primary phase locked loop circuit and operative for receiving and isolating an external reference signal used for the phase locked loop circuit. An oscillator generates a voltage controlled, clean reference signal. The secondary phase locked loop circuit filters and synchronizes this clean reference signal with the external reference signal for producing the reference signal output to the primary phase locked loop circuit.

In yet another aspect of the present invention, the phase locked loop (PLL) frequency synthesizer includes a filter within the secondary phase locked loop circuit for filtering the external reference signal and attenuating spurs that are outside the bandwidth of the secondary phase locked loop circuit. The filter is operative at about 2.5 Hz. The programmable divider circuit comprises chip registers that are programmable for establishing a desired divide ratio between the voltage controlled oscillator and reference signal output. A microcontroller is operatively connected to the chip registers for establishing the desired divide ratios. A frequency multiplier circuit is operatively connected to the voltage controlled oscillator for multiplying the frequency of any output signal from the voltage controlled oscillator.

In yet another aspect of the present invention, a printed wiring board supports the primary

and secondary phase locked loop circuits. A plurality of isolation vias are formed preferably as through holes and isolate any circuit components of the primary and secondary phase locked loop circuits. A housing is matched as to its coefficient of thermal expansion with the printed wiring board and comprises a support member on which the printed wiring board is mounted. A housing cover has an interior surface. Channelization walls are formed by channelization on the interior surface and form isolated channels that receive individual circuit components when the housing cover is mounted on the support member. The channelization walls are juxtaposed against any isolation vias used for isolating individual circuit components when the housing cover is placed on the support plate.

A method aspect of the present invention is also disclosed and comprises the step of generating an output signal from the voltage controlled oscillator of a primary phase locked loop (PLL) circuit, which includes a programmably divided, voltage controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency. The reference signal used for the phase locked loop circuit is isolated by filtering and synchronizing a clean reference signal with the external reference signal and producing the reference signal output to the primary phase locked loop circuit.

Brief Description of the Drawings

Other objects, features and advantages of the present invention will become apparent from the detailed description of the invention which follows, when considered in light of the accompanying drawings in which:

FIG. 1 is a block diagram of a prior art phased locked loop frequency synthesizer using a voltage controlled oscillator.

FIG. 2 is a block diagram of a phased locked loop frequency synthesizer in accordance with the present invention using a noisy external reference signal that is filtered and synchronized with a clean reference signal in a secondary phase locked loop circuit.

FIG. 3 is an exploded isometric view of a housing for the frequency synthesizer such as shown in FIG. 2, and showing the mechanical layout of various parts and components in accordance with the present invention.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

The present invention provides a novel and unobvious phase locked loop frequency synthesizer and method for generating microwave and millimeter wave signals by implementing a voltage controlled oscillator-based, phase locked loop frequency synthesizer that can operate with a corrupted external reference clock, and yet generate a very accurate and relatively spur free signal output. The present invention is advantageous for wireless terrestrial and

satellite communications where the transmission and reception sources are synchronized with a reference signal recovered from received communications data that may have been corrupted with noise and spurious signals. The circuit and method of the present invention provides faster lock times than a comparable and typical frequency locked loop circuit.

The present invention generates a relatively spur free, high frequency, local oscillator signal using a corrupted reference clock signal. It isolates this corrupted reference clock signal from the frequency synthesizer circuits to prevent corruption of the frequency source. Because of the improved performance, the voltage controlled oscillator output frequency can be multiplied to generate higher frequency, local oscillator signals which have very low spurious and harmonic signals. A secondary "reference signal" phased locked loop circuit having a narrow loop bandwidth reduces the reference noise and spurious sidebands with faster lock times than a comparable frequency locked loop.

FIG. 1 illustrates a block diagram of a prior art voltage controlled oscillator-based phase locked loop frequency synthesizer **10**. This type of frequency synthesizer **10** is widely available in the industry and has traditionally been used to generate high frequency sources by multiplying a voltage controlled oscillator output. The phase locked loop circuit at **12** is typically formed as a single phase locked loop semiconductor chip, which may include other circuit components known to those skilled in the art. A crystal oscillator **14** produces a voltage controlled reference signal. The phase locked loop circuit **12** includes a phase detector, as known to those skilled in the art, formed as part of the chip, and can include a

frequency divider circuit that can be operative for dividing and/or multiplying as required, depending on signal output in some cases. A microcontroller **16** is operative with the phase locked loop circuit for controlling chip registers **12a** that establish a desired divide ratio. The phase locked loop circuit **12** outputs a signal from the phase detector into a loop filter **18**, which typically is a low-pass filter that passes signals only below the established cut-off frequency the loop circuit. The loop bandwidth is typically between 1.0 kHz and 2.5 kHz. This error signal becomes a varying DC level signal used to control the frequency of the voltage controlled oscillator.

The phase detector, as known to those skilled in the art, compares the two input signals. The signal output is taken from the voltage controlled oscillator **20** via a coupler **22** that loops back into the phase locked loop circuit **12** and the phase detector, typically formed as a single chip. The output from the voltage controlled oscillator **20** via coupler **22** is multiplied and passed into an amplifier **24** and frequency multiplier circuit **26** followed by a bandpass filter **28** to aid in filtering spurious signals. The signal then passes into a secondary amplifier circuit **30** and is output as the final, amplified and frequency multiplied signal.

The frequency synthesizer circuit **10** as shown in FIG. 1 provides a reliable method of generating low phase noise, local oscillator (LO) signals and uses a low noise, relative spur free crystal oscillator **14** source. A typical voltage controlled oscillator output frequency can be about 2.5 GHz, and may have a tunable bandwidth of up to approximately an octave. The phase locked loop circuit can be available as a single

semiconductor chip that divides the coupled voltage control oscillator output by a factor "N", and divides the reference signal output by a factor "M", thus making the divided output equal as a common phase comparison frequency. The microcontroller **16** is used to program the phase locked loop chip registers **12a** contained within the chip with the desired divide ratios (M and N). The crystal oscillator frequency is typically in the range of about 10 to about 100 MHz.

As known to those skilled in the art, the crystal oscillator is critical because the local oscillator output with phased noise and spur levels is a direct multiplication of the phase noise and spur levels of the reference signal inside the loop forming the circuit. The frequency multiplier is used to multiply the frequency of the voltage controlled oscillator output up to higher frequencies, and can be accomplished in single or multiple stages, depending on the actual frequency requirements.

In some prior art frequency synthesizers, the reference signal is generated as an external reference clock signal that is recovered from the received telecommunications date of wireless terrestrial or satellite communications. In these systems, the transmission and reception sources are required to be synchronized with the reference signal recovered from the received telecommunications data. Often, the external reference is corrupted with noise and spurious signals that have been part of the received data. Also, the use of a frequency locked circuit does not often provide adequate lock times.

The present invention isolates a corrupted reference clock signal from the frequency synthesizer circuits and prevents corruption of any frequency source. It generates a relatively spur free, high

frequency local oscillator signal using this corrupted reference signal. It can generate high frequency, local oscillator signals with very low spurious and harmonic signals. It also allows faster lock times as compared to comparable, frequency locked loop circuits.

The present invention isolates the external reference signal that is recovered from the received data of a communications system that may have been corrupted with the noise and spurious signals. It generates a clean reference signal from a voltage controlled, temperature compensated crystal oscillator. The circuit filters and synchronizes this clean reference signal with the external reference signal within a secondary "reference signal" phase locked loop circuit to produce the reference signal output to the primary phase locked loop circuit.

FIG. 2 shows a frequency synthesizer circuit of the present invention that can operate with a noisy external reference without degrading the in-band phase noise or spur levels. Those circuit components that are similar to the circuit components shown in FIG. 1 are given the same reference numeral with reference to FIG. 2, except in the 100 series, with the phase locked loop circuit **102** now termed a primary phase locked loop circuit.

As illustrated, the primary phase locked loop circuit **102** of the frequency synthesizer **100** shown in FIG. 2 is similar to the frequency synthesizer **10** shown in FIG. 1. What is improved is the addition to this frequency synthesizer **100** of a secondary "reference signal" phase locked loop circuit **140**. This circuit has a narrow bandwidth to filter and synchronize a clean reference signal that is generated from an internal, voltage controlled, temperature compensated

crystal oscillator **142** with the corrupted, external reference signal, which typically has been recovered from any received telecommunications data. Often, this data has been corrupted by noise and spurious signals.

The secondary phase locked loop circuit **140** may include various components necessary for practicing the invention, as suggested by those skilled in the art, including the major chip components of the phase locked loop chip circuit **140a**, including a phase detector and any divider circuits formed as chip registers as necessary and suggested by those skilled in the art. A low bandwidth loop filter **144**, such as approximately 2.5 Hz, attenuates all spurs outside the bandwidth of the phase locked loop. This secondary phase locked loop **140** has the ability to rapidly phase lock the internal crystal oscillator **142** to the external reference clock (less than 30 seconds has been measured), such that it is much faster than comparable, frequency locked loop circuits. A coupler **145** completes the loop circuit and forms the secondary phase locked loop circuit **140**.

It is possible to implement the circuit as shown in FIG. 2, using a housing **150** and printed wiring board (PWB) **152** as shown in FIG. 3, where the printed wiring board interfaces with the housing. The printed wiring board **152** can be formed as a synthesizer board and can be made from a soft board material, such as Rogers board from Rogers Corporation, as known to those skilled in the art. Each separate circuit section or chip, such as the chip components labeled **170**, for example, is secured at appropriate circuit positions on the printed wiring board **152**. These components could include the voltage controlled oscillators, phased locked loop circuits, filters and multipliers. The

various circuits, chips and other components are isolated on the board through the use of isolation vias preferably formed as "through holes" that prevent unwanted signal propagation from one area of the board to another area of the board. This is shown by the filter **156** positioned on the printed wiring board and isolated from other sections, chips and components by isolation vias **154**. Other components, including a DC connector **158** as known to those skilled in the art, are placed on the printed wiring board. The printed wiring board **152** is mounted on a support plate **160** forming a bottom cover of the housing **150**.

The isolation that occurs between various circuits, chips and other components is further improved by creating isolated areas as "channels" or cut-outs **161**, which are formed by channelization within the housing cover **162**. The channels **161** correspond to the position of various components, i.e., chips, filters and other circuit components that are positioned on the printed wiring board. The channels **161** are positioned on the interior surface **164** of the housing cover **162** and include channelization walls **161a** that are juxtaposed directly at the position where the isolation vias **154** are located on the soft, printed wiring board. This is critical to aid in achieving low phase noise and maintain frequency synthesizer output free of spurious and harmonic signals.

In one aspect of the present invention, the housing **150**, including the support plate **160** and the housing cover **162**, is made from a coefficient of thermal expansion (CTE) matched material having a similar coefficient of thermal expansion as the printed wiring board **152**. For example, aluminum silicon has a coefficient of thermal expansion of about 17 and will

be matched to a selected printed wiring board and housing material section. The use of a coefficient of thermal expansion matched housing reduces phase hits that are typically caused by having different rates of expansion in the housing and printed wiring board material versus the temperature. An EMI gasket **180** is positioned on the top cover and provides the additional seal between the top cover and support plate.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that the modifications and embodiments are intended to be included within the scope of the dependent claims.

THAT WHICH IS CLAIMED IS:

1. A phase locked loop (PLL) frequency synthesizer comprising:

a primary phase locked loop circuit having a voltage controlled oscillator (VCO) circuit and a programmable divider circuit for establishing a voltage controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency; and

a secondary phase locked loop circuit operatively connected to the primary phased lock loop circuit, and operative for receiving and isolating an external reference signal used for the primary phase locked loop circuit, and including an oscillator for generating a voltage controlled, clean reference signal wherein said secondary phase locked loop circuit filters and synchronizes the clean reference signal with the external reference signal for producing the reference signal output to the primary phase locked loop circuit.

2. A phase locked loop (PLL) frequency synthesizer according to Claim 1, and further comprising a filter within the secondary phase locked loop circuit for filtering the external reference signal and attenuating spurs that are outside the secondary phase locked loop circuit bandwidth.

3. A phase locked loop (PLL) frequency synthesizer according to Claim 2, wherein the filter is operative at about 2.5 Hz.

4. A phase locked loop (PLL) frequency synthesizer according to Claim 1, wherein said programmable divider circuit comprises chip registers that are programmable for establishing a desired divide

ratio between the voltage controlled oscillator output and reference signal output.

5. A phase locked loop (PLL) frequency synthesizer according to Claim 4, and further comprising a microcontroller operatively connected to said chip registers for establishing the desired divide ratios between the voltage controlled oscillator output and the reference signal output.

6. A phase locked loop (PLL) frequency synthesizer according to Claim 1, and further comprising a frequency multiplier circuit operatively connected to said voltage controlled oscillator output for multiplying the frequency of the output.

7. A phase locked loop circuit (PLL) according to Claim 1, and further comprising a printed wiring board on which the primary and secondary phase locked loop circuits are positioned, including a plurality of isolation vias that isolate any circuit components of the primary and secondary phase locked loop circuits, and a housing that is matched as to its coefficient of thermal expansion with the printed wiring board and comprising a support member on which the printed wiring board is mounted, and a housing cover having an interior surface and channelization walls on the interior surface that form channels that receive individual circuit components when the housing cover is mounted to the support member, wherein the channelization walls are juxtaposed against any isolation vias used for isolating individual circuit components.

8. A phase locked loop (PLL) frequency synthesizer comprising:

a primary phase locked loop circuit having a voltage controlled oscillator (VCO) circuit and a programmable divider circuit for establishing a voltage

controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency; and

a secondary phase locked loop circuit operatively connected to the primary phase locked loop circuit, and operative for receiving and isolating an external reference signal that has been recovered from received data of a telecommunications system and may have been corrupted from noise and spurious signals and used for the primary phase locked loop circuit, and including a frequency controlled, temperature compensated crystal oscillator for generating a voltage controlled, clean reference signal wherein said secondary phase locked loop circuit filters and synchronizes the clean reference signal with the external reference signal for producing the reference signal output to the phase locked loop circuit.

9. A phase locked loop (PLL) frequency synthesizer according to Claim 8, and further comprising a filter positioned within the secondary phase locked loop circuit for filtering the external reference signal and attenuating spurs that are outside the secondary phase locked loop circuit bandwidth.

10. A phase locked loop (PLL) frequency synthesizer according to Claim 9, wherein the filter is operative at about 2.5 Hz.

11. A phase locked loop (PLL) frequency synthesizer according to Claim 8, wherein said programmable divider circuit comprises chip registers that are programmable for establishing a desired divide ratio between the voltage controlled oscillator output and reference signal output.

12. A phase locked loop (PLL) frequency synthesizer according to Claim 11, and further comprising a microcontroller operatively connected to

said chip registers for establishing the desired divide ratios between the voltage controlled oscillator output and the reference signal output.

13. A phase locked loop (PLL) frequency synthesizer according to Claim 8, and further comprising a frequency multiplier circuit operatively connected to said voltage controlled oscillator output for multiplying the frequency of the output.

14. A phase locked loop circuit (PLL) according to Claim 7, and further comprising a printed wiring board on which the primary and secondary phase locked loop circuits are positioned, including a plurality of isolation vias that isolate any circuit components of the primary and secondary phase locked loop circuits, and a housing that is matched as to its coefficient of thermal expansion with the printed wiring board and comprising a support member on which the printed wiring board is mounted, and a housing cover having an interior surface and channelization walls on the interior surface that form channels that receive individual circuit components when the housing cover is mounted to the support member, wherein the channelization walls are juxtaposed against any isolation vias used for isolating individual circuit components.

15. A method of generating a high frequency signal comprising the steps of:

generating an output signal from a voltage controlled oscillator of a primary phase locked loop (PLL) circuit having a programmably divided, voltage controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency; and

isolating an external reference signal used for the phase locked loop circuit by generating a

voltage controlled, clean reference signal and filtering and synchronizing the clean reference signal with the external reference signal within a secondary phase locked loop circuit to produce the reference signal output to the primary phase locked loop circuit.

16. A method according to Claim 15, and further comprising the step of filtering the external reference signal to attenuate spurs that are outside the secondary phased lock loop bandwidth.

17. A method according to Claim 16, wherein the step of filtering further comprises the step of filtering at about 2.5 Hz.

18. A method according to Claim 15, wherein the phase locked loop circuit comprises a programmable divider circuit having chip registers and further comprising the step of programming the chip registers to establish any desired divide ratios between the voltage controlled oscillator output and reference signal output.

19. A method according to Claim 18, and further comprising the step of programming the chip registers using a microcontroller operatively connected to the chip registers to establish the desired divide ratios between the voltage controlled oscillator output and reference signal output.

20. A method according to Claim 15, and further comprising the step of frequency multiplying the output signal from the voltage controlled oscillator.

21. A method according to Claim 15, and further comprising the step of:

positioning any circuit components of the phased lock loop circuit and secondary phased lock loop circuit on a printed wiring board;

isolating the circuit components using isolation vias; and

mounting the printed wiring board on a support member of a housing that is matched as to its coefficient of thermal expansion with the printed wiring board.

22. A method according to Claim 21, and further comprising the step of covering the printed wiring board by a housing cover having an interior surface and channelization walls on the interior surface that form isolation channels that receive individual circuit components in positions such that the channelization walls are juxtaposed against any isolation vias used for isolating individual circuit components.

23. A method of generating a high frequency signal comprising the steps of:

generating an output signal from a voltage controlled oscillator of a primary phase locked loop (PLL) circuit having a programmably divided, voltage controlled oscillator output and a reference signal output at a divide ratio such that the outputs are equal to a common phase comparison frequency; and

isolating an external reference signal that had been recovered from received data of a communications system that may have been corrupted with noise and spurious signals and used for the phase locked loop circuit by generating a clean reference signal from a voltage controlled, temperature compensated crystal oscillator and filtering and synchronizing the clean reference signal with the external reference signal within a secondary phase locked loop circuit to produce the reference signal output to the primary phase locked loop circuit.

24. A method according to Claim 23, and further comprising the step of filtering the external reference signal to attenuate spurs that are outside the secondary phased lock loop bandwidth.

25. A method according to Claim 24, wherein the step of filtering further comprises the step of filtering within a filter of about 2.5 Hz.

26. A method according to Claim 23, wherein the phase locked loop circuit comprises a programmable circuit having chip registers and further comprising the step of programming the chip registers to establish any desired divide ratios between the voltage controlled oscillator output and reference signal output.

27. A method according to Claim 26, and further comprising the step of programming the chip registers using a microcontroller operatively connected to the chip registers to establish the desired divide ratios between the voltage controlled oscillator output and reference signal output.

28. A method according to Claim 23, and further comprising the step of frequency multiplying the output signal from the voltage controlled oscillator.

29. A method according to Claim 23, and further comprising the step of:

positioning any circuit components of the phased lock loop circuit and secondary phased lock loop circuit on a printed wiring board;

isolating any circuit components using isolation vias; and

mounting the printed wiring board on a support member of a housing that is matched as to its coefficient of thermal expansion with the printed wiring board.

30. A method according to Claim 29, and further comprising the step of covering the printed wiring board by a housing cover having an interior surface and channelization walls on the interior surface that form isolation channels that receive individual circuit components in positions such that the channelization walls are juxtaposed against any isolation vias used for isolating individual circuit components.

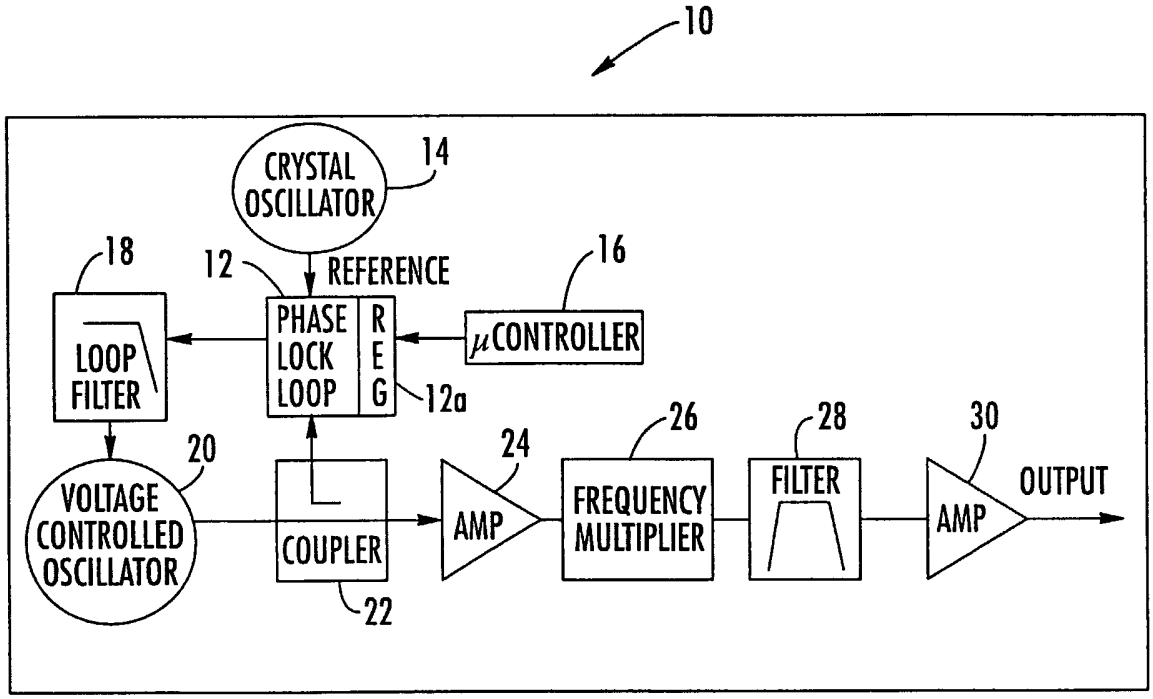
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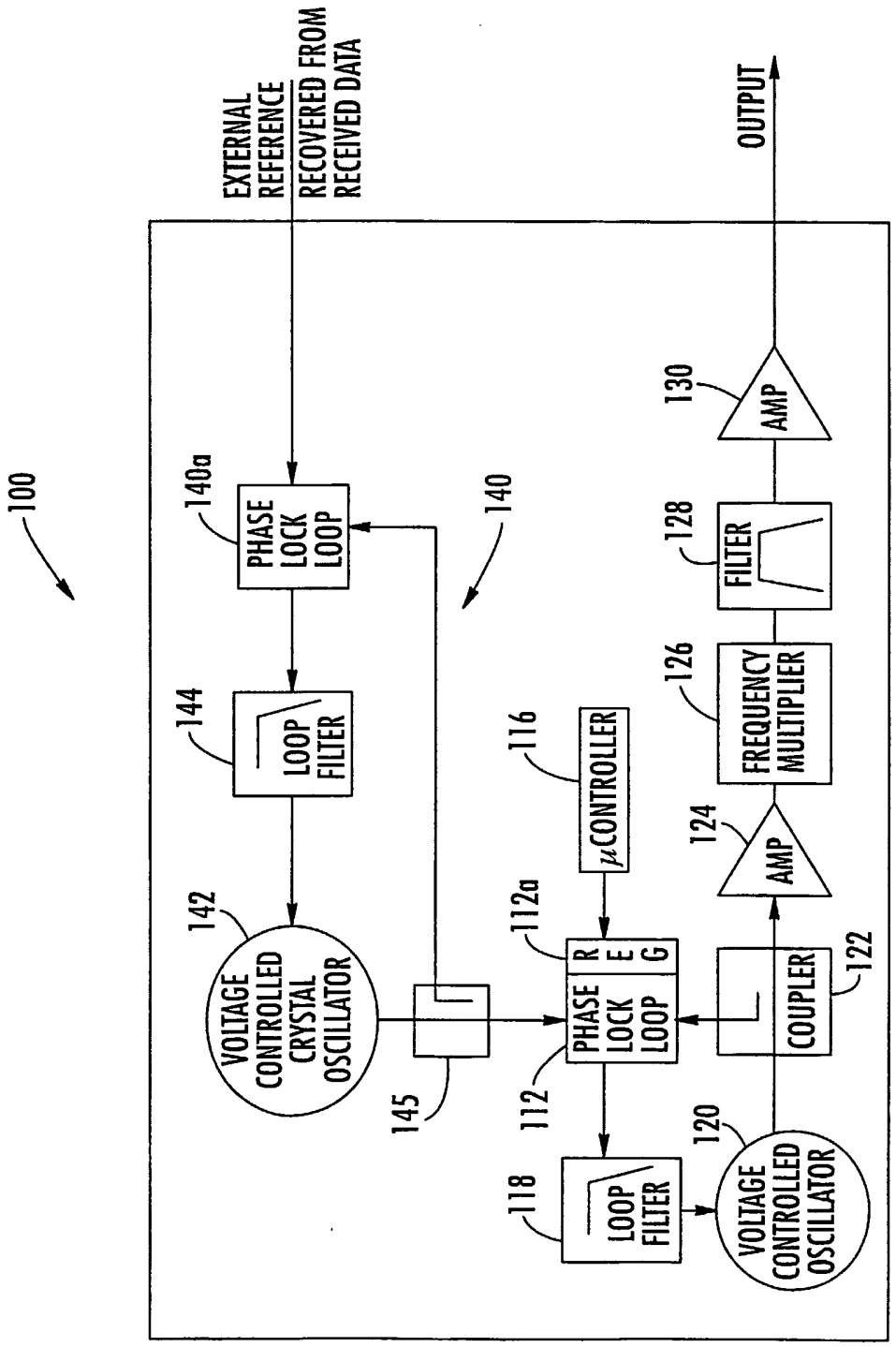
FIG. 1.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LOOP FILTER
120
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122
COUPLER
124
AMP
126
FREQUENCY MULTIPLIER
128
FILTER
130
AMP

FIG. 2.

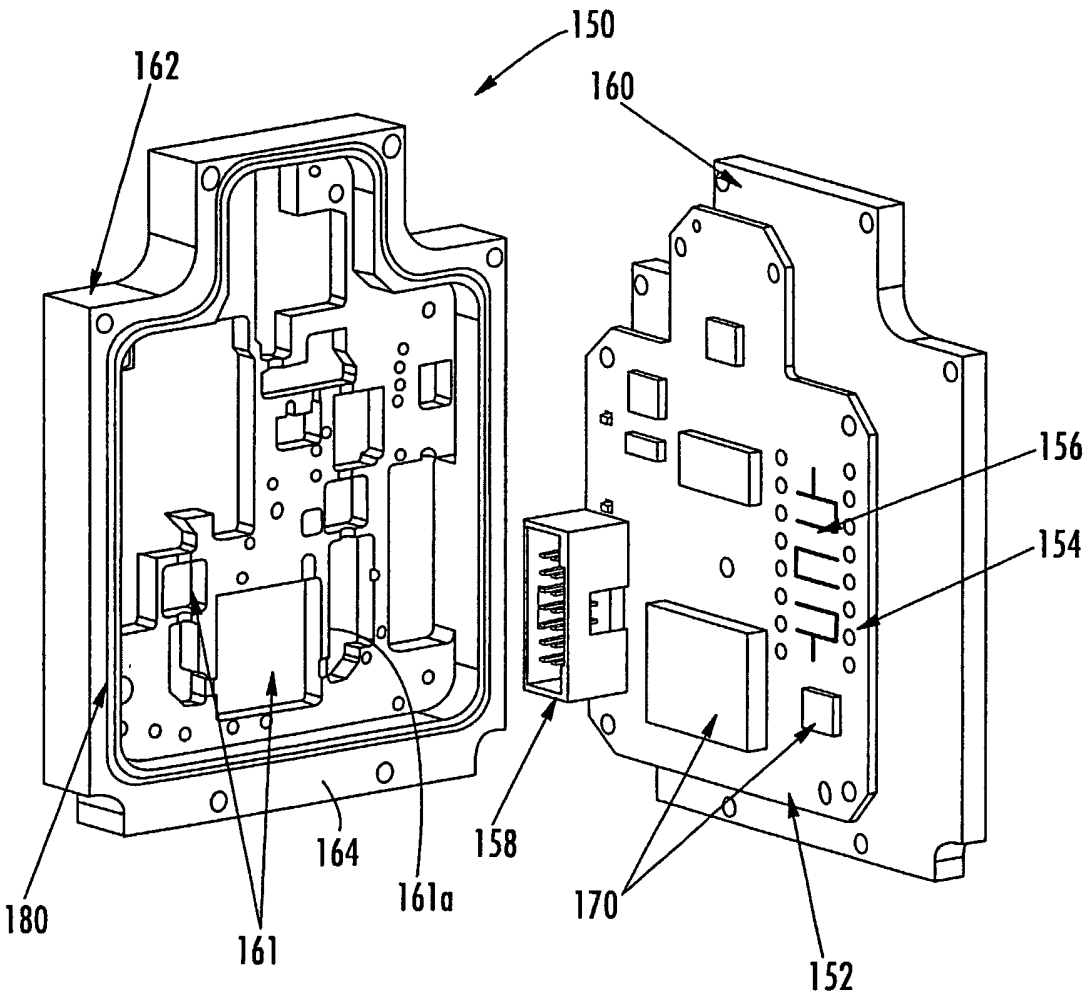

FIG. 3.

INTERNATIONAL SEARCH REPORT

PCT/US 03/11438

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/23

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 144 254 A (WILKE WILLIAM G) 1 September 1992 (1992-09-01) column 4, line 54 -column 6, line 6 column 12, line 20 - line 40 abstract	1,2,4-6, 8,9, 11-13, 15,16, 18-20, 23,24, 26-28
A		3,7,10, 14,17, 21,22, 25,29,30

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 2003	29. 08. 2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	ANNA FLODMAN/JA A

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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