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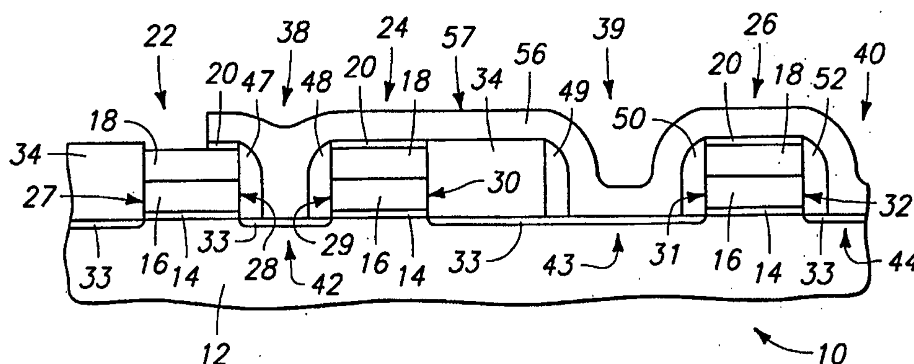

(57) Abstract

A method of fabricating integrated circuitry comprises forming a conductive line (22, 24, 26) having opposing sidewalls (27 and 28, 29 and 30, 31 and 32) over a semiconductor substrate. An insulating layer (34) is then deposited. The insulating layer (34) is etched along at least a portion of at least one sidewall of the line (22, 24, 26). An insulating spacer forming a layer (46) is then deposited over the substrate and the line. It is anisotropically etched to form an insulating sidewall spacer (47-50, 52). A method of forming a local interconnect comprises at least two transistor gates over a semiconductor substrate. A local interconnect layer (56) is deposited to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates. In one aspect, a conductivity enhancing impurity is implanted into the local interconnect layer (56) in at least two implanting steps, with one of the implantings providing a peak implant location which is deeper into the layer than the other. Conductivity enhancing impurity is diffused from the local interconnect layer into semiconductor substrate material therebeneath. In one aspect, conductivity enhancing impurity is implanted through the local interconnect layer into semiconductor substrate material therebeneath. Field isolation material regions and active area regions are formed on a semiconductor substrate. A trench is etched into the field isolation material into a desired line configuration. A conductive material is deposited to at least partially fill the trench and form a conductive line therein. Integrated circuitry is disclosed and claimed.

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DESCRIPTION

METHODS OF FORMING LOCAL INTERCONNECTS AND CONDUCTIVE LINES, AND RESULTING STRUCTURE

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Technical Field

This invention relates to integrated circuitry, to methods of fabricating integrated circuitry, to methods of forming local interconnects, and to methods of forming conductive lines.

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Background Art

The reduction in memory cell and other circuit size implemented in high density dynamic random access memories (DRAMs) and other circuitry is a continuing goal in semiconductor fabrication. Implementing electric circuits involves connecting isolated devices through specific electric paths. When 15 fabricating silicon and other semiconductive materials into integrated circuits, conductive devices built into semiconductive substrates need to be isolated from one another. Such isolation typically occurs in the form of either trench and refill field isolation regions or LOCOS grown field oxide.

Conductive lines, for example transistor gate lines, are formed over bulk 20 semiconductor substrates. Some lines run globally over large areas of the semiconductor substrate. Others are much shorter and associated with very small portions of the integrated circuitry. This invention was principally motivated in making processing and structure improvements involving local interconnects, although the invention is not so limited.

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Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

30 Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer at a processing step subsequent to 35 that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a diagrammatic sectional view of an alternate embodiment semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 11 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of Fig. 11 taken through line 12-12 in Fig. 11.

Fig. 13 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 11.

Fig. 14 is a view of Fig. 13 taken through line 14-14 in Fig. 13.

Fig. 15 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 13.

Fig. 16 is a view of Fig. 15 taken through line 16-16 in Fig. 15.

Fig. 17 is a diagrammatic sectional view of another alternate embodiment semiconductor wafer fragment at one processing step in accordance with the invention, and corresponds in sequence to that of Fig. 16.

Best Modes for Carrying Out the Invention and Disclosure of Invention

The invention includes integrated circuitry, methods of fabricating integrated circuitry, methods of forming local interconnects, and methods of forming conductive lines. In one implementation, a method of fabricating integrated circuitry comprises forming a conductive line having opposing sidewalls over a semiconductor substrate. An insulating layer is deposited over the substrate and the line. The insulating layer is etched proximate the line along at least a portion of at least one sidewall of the line. After the etching, an insulating spacer forming layer is deposited over the substrate and the line, and it is anisotropically etched to form an insulating sidewall spacer along said portion of the at least one sidewall.

In one implementation, a method of forming a local interconnect comprises forming at least two transistor gates over a semiconductor substrate. A local interconnect layer is deposited to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates. In one aspect, a conductivity enhancing impurity is implanted into the local interconnect layer in at least two implanting steps, with one of the two implantings providing a peak implant location which is deeper into the layer than the other. Conductivity enhancing impurity is diffused from the local interconnect layer into semiconductor substrate material therebeneath. In one aspect, a conductivity enhancing impurity is implanted through the local interconnect layer into semiconductor substrate material therebeneath.

In one implementation, field isolation material regions and active area regions are formed on a semiconductor substrate. A trench is etched into the field isolation material into a desired line configuration. A conductive material is deposited to at least partially fill the trench and form a conductive line therein.

In one implementation, integrated circuitry comprises a semiconductor substrate comprising field isolation material regions and active area regions. A conductive line is received within a trench formed within the field isolation material.

Other implementations are disclosed, contemplated and claimed in accordance with the invention.

Referring to Fig. 1, a semiconductor wafer in process is indicated generally with reference numeral 10. Such comprises a bulk monocrystalline silicon substrate 12. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above.

A gate dielectric layer 14, such as silicon dioxide, is formed over semiconductor substrate 12. A conductively doped semiconductive layer 16 is formed over gate dielectric layer 14. Conductively doped polysilicon is one

example. An insulative capping layer 18 is formed over semiconductive layer 16. An example material is again silicon dioxide. Intervening conductive layers, such as refractory metal silicides, might of course also be interposed between layers 16 and 18. An etch stop layer 20 is formed over insulative capping layer 18. An
5 example preferred material is polysilicon.

Referring to Fig. 2, the above-described layers over substrate 12 are patterned and etched into a plurality of exemplary transistor gate lines 22, 24 and 26. Lines 22, 24 and 26 have respective opposing sidewalls 27 and 28, 29 and 30, and 31 and 32. Lines 22, 24 and 26 are shown in the form of field
10 effect transistor gates, although other conductive lines are contemplated. LDD implant doping is preferably conducted to provide illustrated implant regions 33 for the transistors. One example implant dose for regions 33 would be 2 X 10^{13} ions/cm^2. Alternately, the LDD implant doping can implanted after source/drain regions have been formed (or a combination of both). Forming
15 LDD regions later in the process reduces the D_t seen by such implants.

Referring to Fig. 3, an insulating layer 34 is deposited over substrate 12 and lines 22, 24 and 26. The thickness of layer 34 is preferably chosen to be greater than that of the combined etch stop layer, capping layer and semiconductor layer, and to be received between the transistor gate lines to fill
20 the illustrated cross-sectional area extending between adjacent gate lines. Example and preferred materials include undoped silicon dioxide deposited by decomposition of tetraethylorthosilicate, and borophosphosilicate glass.

Referring to Fig. 4, insulative material layer 34 has been planarized. Such is preferably accomplished by chemical-mechanical polishing using etch stop
25 layer 20 of gates 22, 24 and 26 as an etch stop for such polishing.

Referring to Fig. 5, a layer of photoresist 36 has been deposited and patterned. Insulative material 34 is etched to effectively form contact openings 38, 39 and 40 therein to proximate substrate 12, and preferably effective to outwardly expose material of semiconductor substrate 12. For
30 purposes of the continuing discussion, the exposed portions of semiconductor substrate 12 are designated as locations 42, 43 and 44. The depicted etching constitutes but one example of etching insulating layer 34 proximate lines 22 and 24 along at least a portion of facing sidewalls 28 and 29. Such portion preferably comprises a majority of the depicted sidewalls, and as shown
35 constitutes the entirety of said sidewalls to semiconductor substrate 12.

With respect to line 26, the illustrated insulating layer 34 etching is conducted along at least a portion of each of opposing line sidewalls 31 and 32. Further with respect to lines 22 and 24, such etching of insulating layer 34 is conducted along portions of sidewalls 28 and 29, and not along the respective opposing sidewalls 27 and 30. Further, such insulating layer 34 etching exposes conductive material of at least one of the transistor gates, with such etching in the illustrated example exposing conductive material 16 of sidewalls 28, 29, 31 and 32 of the illustrated transistor gates. Further with respect to gate lines 22 and 24, the insulative material is etched to remain/be received over the one sidewalls 27 and 30, and not sidewalls 28 and 29.

After etching of layer 34, at least one of the exposed sidewalls is covered with insulating material. Such preferably comprises deposition of an insulating layer 46 over substrate 12; lines 22, 24 and 26; and planarized and etched insulative material 34 to a thickness which less than completely fills at least some of the contact openings. Such layer preferably comprises a spacer forming layer, with silicon dioxide and silicon nitride being but two examples.

Referring to Fig. 7, spacer forming layer 46 is anisotropically etched to form insulative sidewall spacers 47, 48, 49, 50 and 52. Such constitutes but one example of forming the illustrated insulative sidewall spacers. In one implementation, insulating layer 34 is received between at least one of the sidewalls and one of the sidewall spacers, for example as shown with respect to line 24 between sidewall 30 and spacer 49. Further with respect to this example line 24, insulative material 34 is received between the one sidewall 30 and the one insulative spacer 49 formed thereover, and is not received between the opposing sidewall 29 and the other spacer 48 formed thereover. Yet, in the depicted section, insulative sidewall spacers 48 and 49, and 50 and 52 are formed over each of the respective opposing line sidewalls of lines 24 and 26, wherein in the depicted section only one insulative spacer 47 is formed over one sidewall of line 22. Further, insulative material 34 received between sidewall 30 and insulative spacer 49 of line 24 has a maximum lateral thickness which is greater than or equal (greater as shown) to a maximum lateral thickness of sidewall spacer 49. Source/drain implanting may occur at this point in the process, if desired.

Referring to Fig. 8, a local interconnect layer 56 is deposited to overlie at least one of the transistor gates, and ultimately interconnect locations 42, 43 and 44 of substrate 12, and is thus provided in electrical connection therewith.

An example preferred material for layer 56 is polysilicon. Due to the spacing constraints between the insulative spacers of lines 22 and 24 versus that of lines 24 and 26, layer 56 completely fills contact opening area 38 and less than completely fills contact opening areas 39 and 40.

5 Depending on the circuitry being fabricated and the desires of the processor, layer 56 might be *in situ* conductively doped as deposited and/or separately implanted with conductivity enhancing impurity subsequent to deposition. Further, any such subsequent implantings might be masked to only be provided within portions of layer 56 where, for example, both n-type and p-type substrate 10 regions are being conductively connected by an ultimately conductive interconnect formed from layer 56. Most preferably, interconnect layer 56 will ultimately comprise suitably conductively doped semiconductive material. Where such will comprise both n-type and p-type doping material, another conductive strapping layer, such as a refractory metal silicide, will ideally be formed atop layer 56 to 15 avoid or overcome an inherent parasitic diode that forms where p-type and n-type materials join. Further with respect to combined n-type and p-type processing, multiple local interconnect layers might be provided and patterned, and perhaps utilize intervening insulative layers, spacers or etch stops. Further prior to deposition of layer 56, a conductive dopant diffusion barrier layer might 20 also be provided.

Example preferred implantings, whether p-type, n-type, or a combination of the same, is next described still with reference to Fig. 8. Such depicts two preferred implantings represented by peak implant locations or depths 58 and 60. Such are preferably accomplished by two discrete implantings which provide peak 25 implant location 60 deeper relative to layer 56 than implant 58. For example within layer 56 in contact openings 38 and 39, regions of layer 56 are shown where peak implant 60 is deeper within layer 56 than is peak implant 58. Yet, the peak implant location or depth for implant 60 is preferably not chosen to be so deep to be within conductively doped material 16 of lines 22, 24 and 26. 30 Further in contact opening locations 39 and 40, the implanting to produce depicted implant 60 is conducted through local interconnect layer 56 and into semiconductor substrate material 12 therebeneath. Diffusing of the conductivity enhancing impurity provided within layer 56 might ultimately occur from local interconnect layer 56 into semiconductor substrate material 12 therebeneath within 35 locations 42, 43 and 44 to provide the majority of the conductivity enhancing impurity doping for the source/drain regions of the illustrated transistor lines.

Depending on the processor's desire and the degree of diffusion, such source/drain regions might principally reside within semiconductor substrate material 12, or reside as elevated source/drain regions within layer 56.

Further and as shown, layer 56 in certain locations acts as a spacer for the deeper implant. Further, such may actually reduce junction capacitance by counter doping halo implants that are further away from gate polysilicon. This can provide flexibility in the settings of the halo implants.

Referring to Fig. 9, local interconnect layer 56 is formed (i.e., by photopatterning and etching) into a local interconnect line 57 which overlies at least portions of illustrated conductive lines 24, 26 and 28, and electrically interconnects substrate material locations 42, 43 and 44.

Further considered aspects of the invention are next described with reference to Figs. 10-16. Fig. 10 illustrates a semiconductor wafer fragment 10a comprising a bulk monocrystalline silicon substrate 12. Semiconductor substrate 12 has been patterned to form field isolation region 64 and active area region 62. In the illustrated example, material 66 of field isolation region 64 comprises silicon dioxide fabricated by LOCOS processing. Such might constitute other material and other isolation techniques, for example trench and refill resulting from etching trenches into substrate 12 and depositing oxide such as by CVD, including PECVD.

Fragment 10a in a preferred and exemplary embodiment comprises an extension of fragment 10 of the first described embodiment, such as an extension in Fig. 10 starting from the far right portion of Fig. 4 of the first described embodiment. Accordingly, insulating layer 34 is shown as having been deposited and planarized,

Referring to Figs. 11 and 12, a trench 68 is etched into field isolation material 66 and is received within insulating layer 34. Such includes opposing insulative sidewalls 77 and a base 79. Trench 68 in this illustrated example extends to an edge 70 of isolation material 66 proximate, and here extending to, active area substrate material 12 of region 62. An example preferred depth for trench opening 68 is 10% to 20% greater than the combined thickness of the conductive and insulating materials of gate stacks 22, 24 and 26.

Referring to Figs. 13 and 14, a conductive material 72 is deposited to at least partially fill trench 68, and electrically connects with substrate material 12 of active area region 62. As shown, material 72 is preferably deposited to overfill trench 68. The width of trench 68 is preferably chosen to be more

narrow than double the thickness of layer of material 72. Such preferred narrow nature of trench 68 facilitates complete filling thereof with conductive material 72 in spite of its depth potentially being greater than the globally deposited thickness of layer 72.

5 Referring to Figs. 15 and 16, conductive layer 72 has been etched to produce the illustrated local interconnect line 75 which includes a line segment 76 received within trench 68 over isolation material 66. A small degree of overetch preferably occurs as shown to assure complete removal material 72 from over the outer surface of insulating layer 34. Ideally, the shape of 10 trench 68 is chosen and utilized to define the entire outline and shape of the conductive line being formed relative to isolation material 66. Further, conductive material of line 75 preferably contacts material 66 of trench sidewalls 77 and base 79.

Fig. 17 illustrates an exemplary alternate wafer fragment 10b embodiment 15 corresponding to Fig. 16, but using a trench isolation oxide 66b as opposed to LOCOS oxide 66. An exemplary preferred trench filled line 68b is shown.

CLAIMS

1. A method of fabricating integrated circuitry comprising:

forming a conductive line having opposing sidewalls over a semiconductor substrate;

5 depositing an insulating layer over the substrate and the line;

etching the insulating layer proximate the line along at least a portion of at least one sidewall of the line; and

after the etching, depositing an insulating spacer forming layer over the substrate and the line, and anisotropically etching it to form an insulating
10 sidewall spacer along said portion of the at least one sidewall.

2. The method of claim 1 wherein the etching of the insulating layer is conducted along at least a portion of each of the opposing line sidewalls, the anisotropic etching forming an insulating sidewall spacer over each of the
15 opposing line sidewalls.

3. The method of claim 1 wherein the etching of the insulating layer is conducted along the portion of the one sidewall and not along the opposing sidewall.

20

4. The method of claim 1 wherein the portion comprises a majority of said one sidewall.

5. The method of claim 1 wherein the portion comprises the
25 substantial entirety of said at least one sidewall.

6. The method of claim 1 wherein the etching of the insulating layer outwardly exposes material of the semiconductor substrate.

30 7. The method of claim 1 wherein the conductive line is formed to comprise a transistor gate.

8. The method of claim 1 comprising planarizing the insulating layer prior to said etching of it.

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9. The method of claim 1 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with one of the active area regions.

10. A method of fabricating integrated circuitry comprising:

forming a pair of transistor gates having respective opposing sidewalls over a semiconductor substrate, one sidewall of one of the transistor gates facing one sidewall of the other transistor gate;

depositing an insulating layer over the substrate and between the pair of transistor gates to fill an area extending therebetween;

etching a contact opening into the insulating layer to proximate the substrate between the pair of transistor gates;

depositing an insulating spacer forming layer within the contact opening to less than completely fill the contact opening; and

anisotropically etching the spacer forming layer to form a pair of insulating sidewall spacers over the one sidewalls of the pair of transistor gates.

11. The method of claim 10 wherein the contact opening etching exposes material of the semiconductor substrate.

12. The method of claim 10 wherein the contact opening etching exposes conductive material of at least one of the pair of transistor gates.

13. The method of claim 10 wherein the contact opening etching exposes conductive material of each of the pair of transistor gates.

14. The method of claim 10 wherein the contact opening etching exposes conductive material of at least one of the sidewalls of at least one of the pair of transistor gates.

15. The method of claim 10 comprising planarizing the insulating layer prior to said etching of it.

16. The method of claim 10 comprising:

5 forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at 10 least partially fills the trench and which electrically connects with one of the active area regions.

17. A method of fabricating integrated circuitry comprising:

forming a pair of transistor gates having respective opposing sidewalls over 15 a semiconductor substrate, one sidewall of one of the transistor gates facing one sidewall of the other transistor gate;

depositing an insulating layer over the substrate and between the pair of transistor gates to fill an area extending therebetween;

etching a contact opening into the insulating layer to proximate the 20 substrate between the pair of transistor gates, the etching exposing conductive material of at least one of the one sidewalls of the pair of transistor gates;

after the etching, covering the at least one of the one sidewalls with insulating material; and

forming electrically conductive material within the opening in electrical 25 connection with material of the semiconductor substrate.

18. The method of claim 17 wherein the contact opening etching exposes conductive material of each of the one sidewalls of each of the pair of transistor gates.

30

19. The method of claim 17 wherein the covering comprises deposition of an insulating layer.

20. The method of claim 17 wherein the covering comprises deposition 35 of an insulating layer, and subsequent anisotropic etching thereof.

21. The method of claim 17 comprising planarizing the insulating layer prior to the contact opening etching.

22. The method of claim 17 comprising:

5 forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at 10 least partially fills the trench and which electrically connects with one of the active area regions.

23. A method of forming a local interconnect comprising:

forming a pair of transistor gates having respective opposing sidewalls over 15 a semiconductor substrate;

depositing an insulating layer over the substrate and between the pair of transistor gates;

etching a first contact opening into the insulating layer to proximate the substrate between the pair of transistor gates and another contact opening 20 through the insulating layer to proximate the substrate proximate an opposing side of one of the pair of transistor gates;

forming insulating sidewall spacers over the opposing sidewalls of the one transistor gate, the insulating layer being received between at least one of said sidewalls and one of said sidewall spacers; and

25 forming a local interconnect layer to overlie the one transistor gate and electrically connect with semiconductor substrate material between the pair of transistor gates and semiconductor substrate material proximate the opposing side of the one transistor gate.

30 24. The method of claim 23 wherein the insulating layer is not received between the other sidewall and the other sidewall spacer.

25. The method of claim 23 wherein the etching exposes material of the semiconductor substrate within the first and another contact openings.

35

26. The method of claim 23 comprising planarizing the insulating layer prior to said etching of it.

27. The method of claim 23 wherein the insulating layer as received
5 between the one sidewall and the one sidewall spacer has a maximum lateral thickness which is greater than or equal to a maximum lateral thickness of the one sidewall spacer.

28. The method of claim 23 wherein the local interconnect layer
10 comprises polysilicon.

29. The method of claim 23 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

15 etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming the local interconnect layer to at least partially fill the trench and which electrically connects with one of the active area regions.

20 30. A method of forming a conductive line comprising:

forming conductive material received over a semiconductor substrate into a line, the line having opposing sidewalls;

depositing insulative material over the line and etching it to be received over one of the opposing sidewalls and not the other;

25 depositing an insulating spacer forming layer over the line and the etched insulative material; and

anisotropically etching the spacer forming layer to form a pair of insulative spacers over the opposing line sidewalls, the insulative material being received between the one sidewall and one insulative spacer formed thereover and not
30 being received between the other sidewall and the other spacer formed thereover.

31. The method of claim 30 comprising planarizing the insulating layer prior to said etching of it.

32. The method of claim 30 wherein the insulative material as received between the one sidewall and the one sidewall spacer formed thereover has a maximum lateral thickness which is greater than or equal to a maximum lateral thickness of the one sidewall spacer.

5

33. A method of forming a conductive line comprising:

forming conductive material received over a semiconductor substrate into a line, the line having opposing sidewalls;

depositing insulative material over the line;

10 planarizing the insulative material;

depositing an insulating spacer forming layer over the line and the planarized insulative material; and

anisotropically etching the spacer forming layer to form a pair of insulative spacers over the opposing line sidewalls, the insulative material being received

15 between at least one of the sidewalls and one insulative spacer formed thereover.

34. The method of claim 33 wherein the insulative material as received between the one sidewall and the one sidewall spacer formed thereover has a maximum lateral thickness which is greater than or equal to a maximum lateral

20 thickness of the one sidewall spacer.

35. A method of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the

25 transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates;

implanting conductivity enhancing impurity into the local interconnect layer in at least two implanting steps, one of the two implantings providing a peak

30 implant location which is deeper into the layer than the other; and

diffusing conductivity enhancing impurity from the local interconnect layer into semiconductor substrate material therebeneath.

36. The method of claim 35 comprising conducting the one implanting relative to one portion of the local interconnect layer to have a peak implant location which is through said layer and within the semiconductor substrate material therebeneath.

5

37. A method of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the

10 gates with semiconductor substrate material proximate another of the transistor gates; and

implanting conductivity enhancing impurity through the local interconnect layer into semiconductor substrate material therebeneath.

15 38. The method of claim 37 further comprising in another implanting step separate from said implanting, implanting conductivity enhancing impurity to a peak concentration location which is within he local interconnect layer.

39. A method of fabricating integrated circuitry comprising:

20 forming a gate dielectric layer over a semiconductor substrate;

forming a conductively doped semiconductive layer over the gate dielectric layer;

forming an insulative capping layer over the semiconductive layer;

forming an etch stop layer over the insulative capping layer;

25 patterning and etching the etch stop layer, the capping layer and the semiconductive layer into a plurality of transistor gate lines;

depositing an oxide layer over the substrate and the transistor gate lines to a thickness greater than that of the combined etched etch stop layer, capping layer and semiconductor layer;

30 chemical mechanical polishing the deposited oxide layer using the etch stop layer as an etch stop;

patterning and etching the polished oxide layer to expose material of the semiconductor substrate in at least two discrete locations proximate different of the plurality of gate lines;

35 depositing a local interconnect layer into electrical connection with said locations and over said plurality of gate lines; and

etching the local interconnect layer into a local interconnect line overlying at least two of said plurality of gate lines.

40. A method of forming a conductive line comprising:

5 forming field isolation material regions and active area regions on a semiconductor substrate;

etching a trench into the field isolation material into a desired line configuration; and

depositing a conductive material to at least partially fill the trench and 10 form a conductive line therein.

41. The method of claim 40 comprising forming the field isolation material to comprise LOCOS oxide.

15 42. The method of claim 40 comprising depositing an insulative layer over the active area and field isolation regions, and planarizing the insulative layer prior to the etching.

43. The method of claim 40 comprising depositing an insulative layer 20 over the active area and field isolation regions, and planarizing the insulative layer prior to the etching; the etching comprising etching the trench to be received within the planarized insulative layer.

44. The method of claim 40 comprising forming the field isolation 25 material to comprise CVD oxide formed within etched substrate trenches.

45. The method of claim 40 wherein the conductive material is initially deposited to overfill the trench, and comprising removing some of the conductive material after the initial deposition to leave the trench only partially filled with 30 the conductive material.

46. A method of forming a local interconnect comprising:

etching a trench into field isolation material formed relative to a semiconductor substrate, the trench in the field isolation material extending to an edge of the isolation material proximate active area substrate material; and

5 forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with said active area substrate material.

47. The method of claim 46 comprising forming the field isolation
10 material to comprise LOCOS oxide.

48. The method of claim 46 comprising forming the field isolation material to comprise CVD oxide formed within etched substrate trenches.

15 49. The method of claim 46 wherein the local interconnect layer is initially deposited to overfill the trench, and comprising removing some of the interconnect layer after the initial deposition to leave the trench only partially filled with the interconnect layer.

20 50. Integrated circuitry comprising:

a semiconductor substrate comprising field isolation material regions and active area regions; and

a conductive line received within a trench formed within the field isolation material.

25

51. The integrated circuitry of claim 50 wherein the field isolation material comprises LOCOS oxide.

52. The integrated circuitry of claim 50 wherein the field isolation
30 material comprises CVD oxide formed within etched substrate trenches.

53. The integrated circuitry of claim 50 wherein the conductive line within the trench is defined by the shape of the trench formed within the field isolation material.

35

54. The integrated circuitry of claim 53 wherein the field isolation material comprises LOCOS oxide.

55. The integrated circuitry of claim 53 wherein the field isolation 5 material comprises CVD oxide formed within etched substrate trenches.

56. The integrated circuitry of claim 50 wherein the trench has opposing insulative sidewalls comprising the field isolation material, conductive material of the line contacting the trench sidewalls.

10

57. Integrated circuitry comprising:

a semiconductor substrate comprising field isolation material regions and active area regions; and

a local interconnect line extending from over and in electrical connection 15 with an active area region to within a trench formed within the field isolation material.

58. The integrated circuitry of claim 57 wherein the field isolation material comprises LOCOS oxide.

20

59. The integrated circuitry of claim 57 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

60. The integrated circuitry of claim 57 wherein the conductive line 25 within the trench is defined by the shape of the trench formed within the field isolation material.

61. The integrated circuitry of claim 60 wherein the field isolation material comprises LOCOS oxide.

30

62. The integrated circuitry of claim 60 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

63. The integrated circuitry of claim 60 wherein the trench has 35 opposing insulative sidewalls comprising the field isolation material, conductive material of the local interconnect line contacting the trench sidewalls.

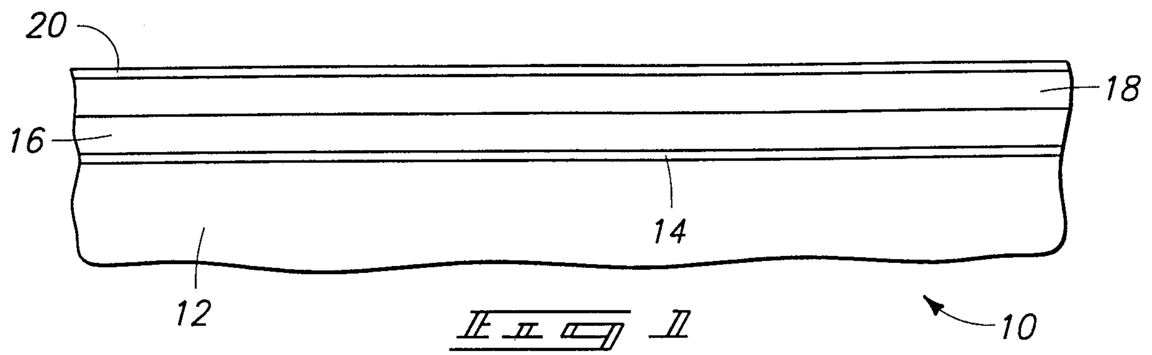

Fig 1

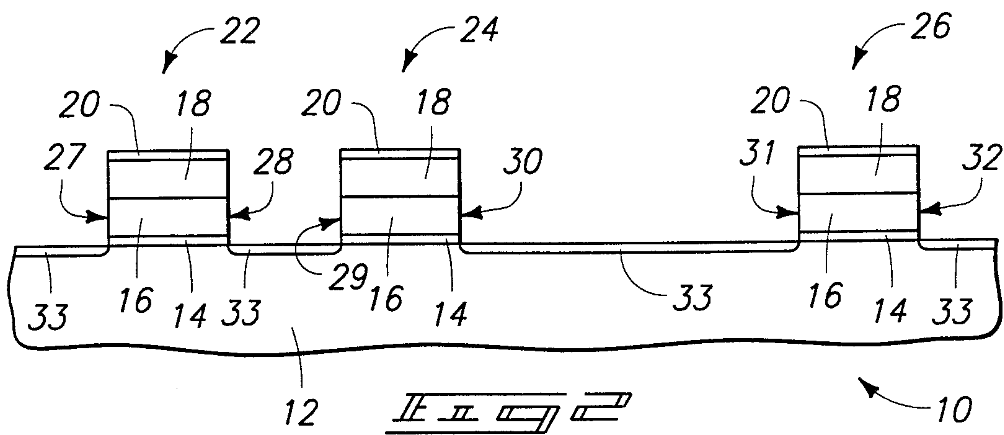

Fig 2

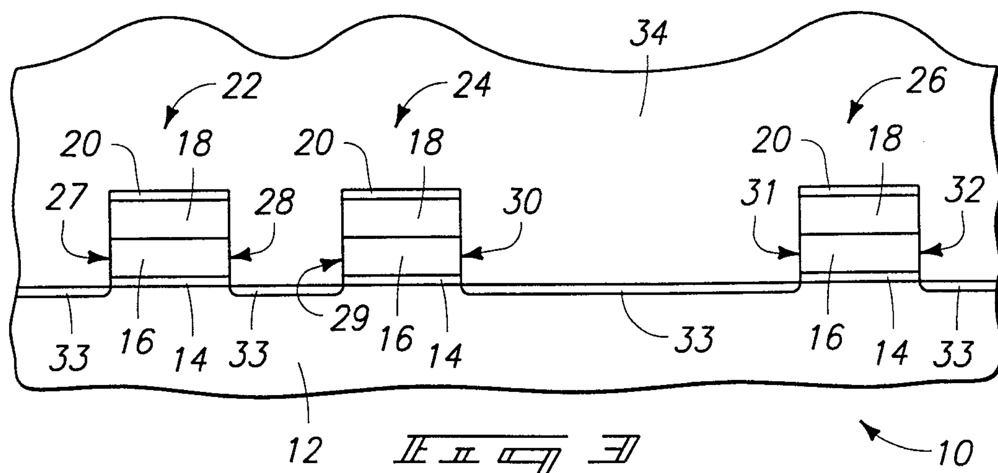

Fig 3

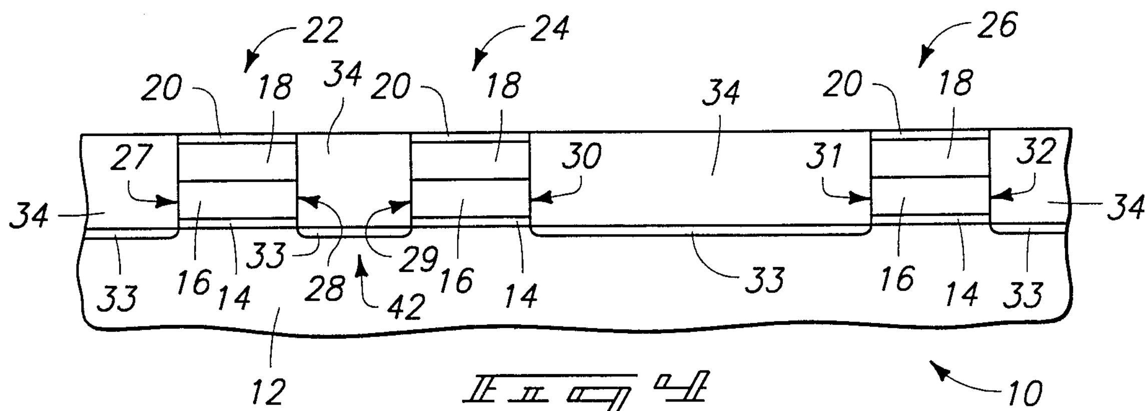

Fig 4

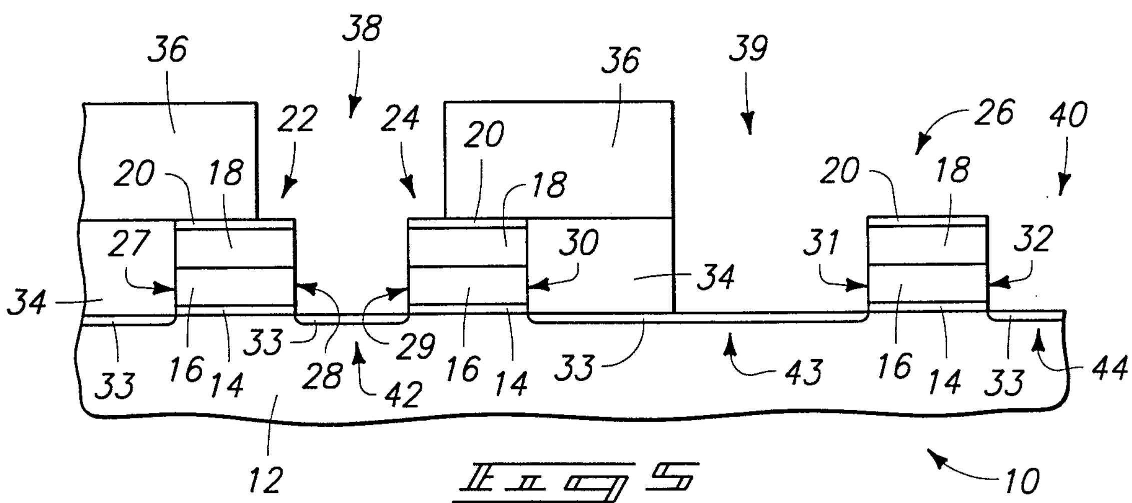

Fig 5

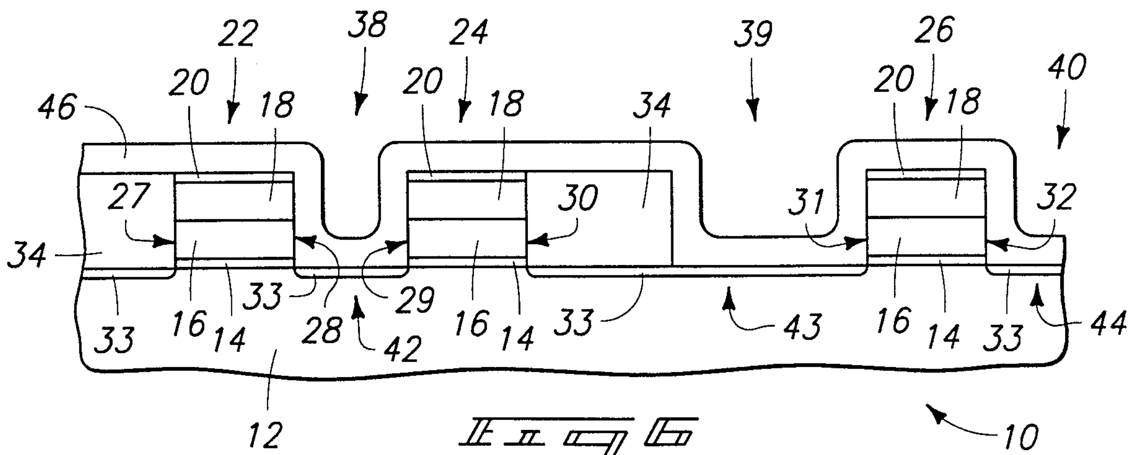

Fig 6

Fig 7

Fig 8

Fig 9

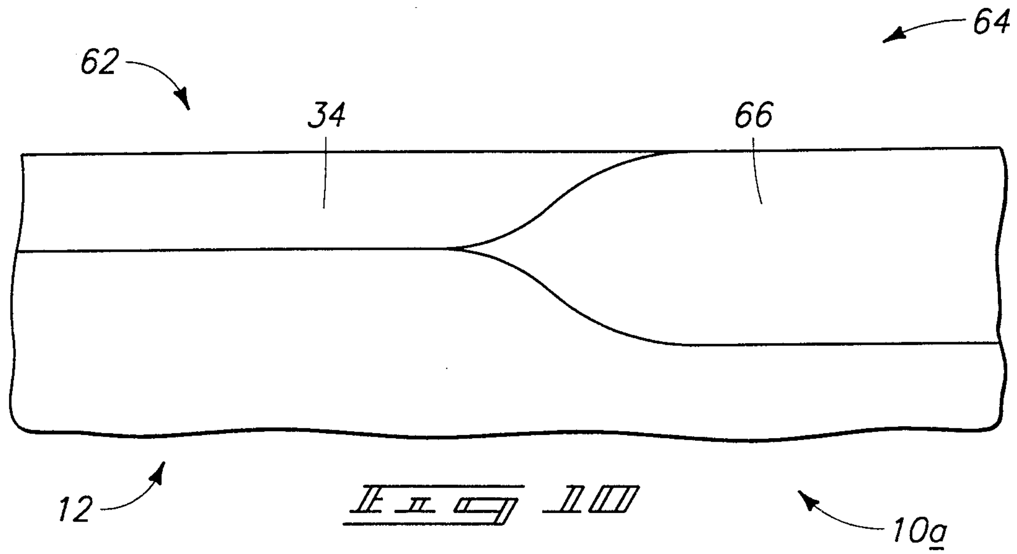

Fig 10

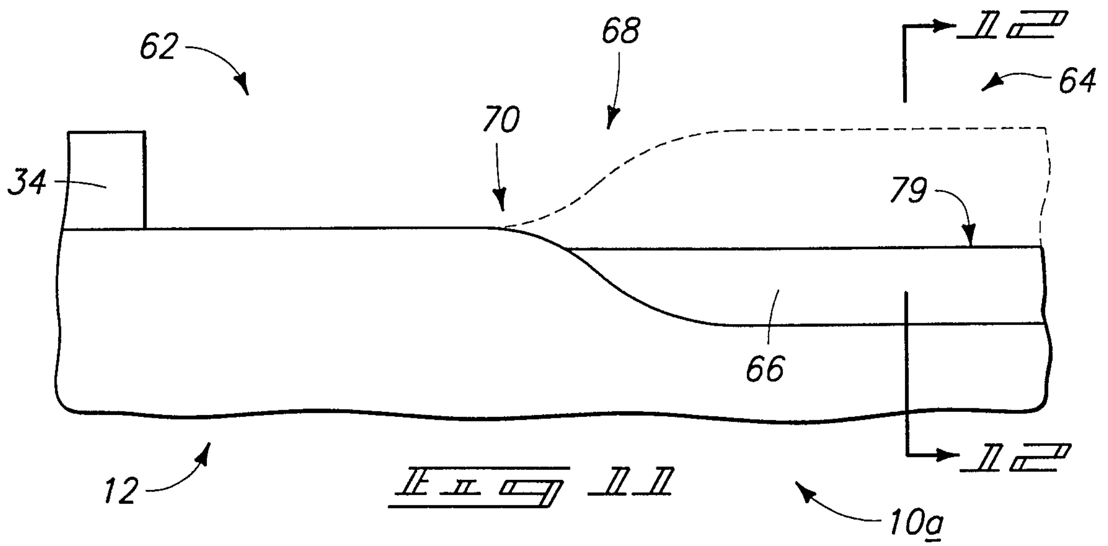

Fig 11

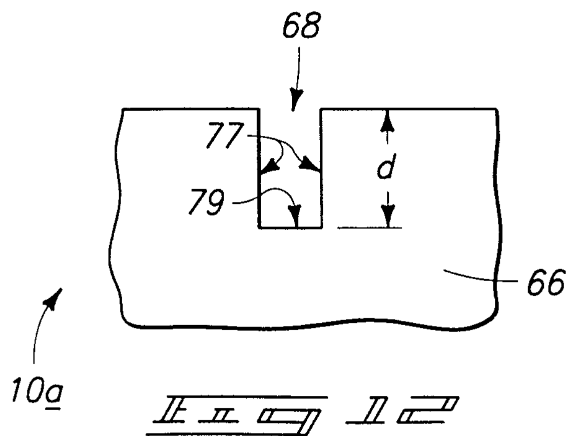

Fig 12

62 68 72 14 64
34 70 79
66
12 14 10a

Fig 13

72
68
77 d
79
66
10a

Fig 14

MISSING AT THE TIME OF PUBLICATION

INTERNATIONAL SEARCH REPORT

Inter. ›nal Application No
PCT/US 00/06248

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 656 520 A (WATANABE TAKESHI) 12 August 1997 (1997-08-12) column 3, line 60 -column 4, line 60; figures 2A-E	1,2,6-8, 10-15
X	US 5 413 961 A (KIM JAE K) 9 May 1995 (1995-05-09)	23-28
Y	column 4, line 22 -column 5, line 22; figures 4A-E	1,3,6-8, 30-32
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 397 (E-1120), 8 October 1991 (1991-10-08) -& JP 03 161937 A (SUMITOMO ELECTRIC IND LTD), 11 July 1991 (1991-07-11) abstract; figure 1	1,3,6,7, 30

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 July 2000	09.08.00

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Micke, K

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/06248

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 733 809 A (AHMAD AFTAB ET AL) 31 March 1998 (1998-03-31)	1,6-8
Y		1,3,6-8, 30-32
A	column 5, line 7 - line 39 column 7, line 5 - line 35; figures 9A-C,10A-C	10-15
X	US 5 081 060 A (KIM JAE K) 14 January 1992 (1992-01-14) column 5, line 62 - line 63 column 8, line 19 - line 46; figures 3A-E,5B	1,3,6,8
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 05, 31 May 1999 (1999-05-31) & JP 11 054724 A (SONY CORP), 26 February 1999 (1999-02-26) abstract -& US 6 051 462 A (OHNO KEIICHI) 18 April 2000 (2000-04-18) column 4, line 30 -column 6, line 55; figures 1,2AB	1-3,6-8, 10,11, 15,23-27
P,X	US 5 899 721 A (GARDNER MARK I ET AL) 4 May 1999 (1999-05-04) column 6, line 4 -column 7, line 3; figures 3-7	1,2,7,8

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/06248

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [X] Claims Nos.: 4,5,9,16-22,29,33-63
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. [ ] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 4,5,9,16-22,29,33-63

In view of the large number of independent claims used to define the invention, these independent claims having differing overlapping scopes and/or not reciting features which appear essential in the description, and the adopted vague wording ("proximate the line", "proximate the substrate","being received between", "to be received over") which is also ambiguous as to certain aspects (see "before the depositing" in claim 9, referring to claim 1 containing two different depositing steps), the application fails to comply with the requirements of Art. 6 PCT to such an extent that a meaningful search over the whole scope of the claims is impossible.

Consequently, the search has been carried out for the parts which appear clear and supported by the description, namely:
-claims1-8, 10-15, 23-28.

-claims 30-32 have been searched while considering that the process requires an additional step not included in claim 30, namely the step of planarizing and/or etching back the insulative material over the line sidewall that is still covered by this material, prior to depositing the spacer layer.

Claims not searched: 4,5,9,16-22,29,33-63.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/06248

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5656520 A	12-08-1997	JP 2809080 B	08-10-1998
		JP 7169850 A	04-07-1995
US 5413961 A	09-05-1995	KR 9602064 B	10-02-1996
		JP 2568036 B	25-12-1996
		JP 6236876 A	23-08-1994
JP 03161937 A	11-07-1991	NONE	
US 5733809 A	31-03-1998	US 5494841 A	27-02-1996
		AU 3889395 A	06-05-1996
		CN 1168741 A	24-12-1997
		JP 10507316 T	14-07-1998
		WO 9612301 A	25-04-1996
US 5081060 A	14-01-1992	KR 9205453 B	04-07-1992
JP 11054724 A	26-02-1999	US 6051462 A	18-04-2000
US 5899721 A	04-05-1999	NONE	