Title: MIXED WIRE SEMICONDUCTOR LEAD FRAME PACKAGE

Abstract: An encapsulated semiconductor package (20) includes a lead frame (25) with die pad (22) surrounded by a plurality of first (23) and second leadfingers (24). A semiconductor chip (21) including chip contact pads (33) on its upper active surface is attached to the die pad (22). A plurality of first bond wires (26), comprising a first electrically conductive material, extend between the chip contact pads (33) and the plurality of first leadfingers (23). A plurality of second bond wires (27), comprising a second electrically conductive material, extend between a chip contact pad (33) and a second leadfinger (24). The semiconductor package (20) further includes a plurality of electrically conducting means (32) attached to the second leadfingers (24).
Mixed wire semiconductor lead frame package

The invention relates to an improved mixed wire semiconductor lead frame package and a method for producing the package.

Mixed wire semiconductor lead frame packages which include two pluralities of bond wires, each comprising a different metal, are known. A package 1 of the prior art is shown in Figure 1. The package 1 includes a copper lead frame 2 with a recessed die pad 3 laterally surrounded by a plurality of leadfingers 4 and a semiconductor chip 5 which is mounted to the die pad 3 with die attach material 6. The semiconductor chip 5 includes integrated circuit devices 7 on its upper active surface and a plurality of chip contact pads 8. Some devices are electrically connected to the lead frame 2 by aluminium bond wires 9 and other devices by gold bond wires 10.

Aluminium bond wires 9 of a large diameter are commonly used to electrically connect power devices to the lead frame 2 since a high current capacity is desired. A wedge-bonding technique is commonly used for the aluminium bond wires 9 and a large laterally rectangular bond pad is provided on the chip 5 which increases the chip dimensions. The chip contact pads of devices which require a smaller current capacity are connected to the lead frame by gold wires 10 which typically have a smaller diameter than the aluminium bond wires 9. The gold wires 10 are bonded using a ball bonding technique. Smaller laterally square contact pads are provided on the semiconductor chip 5 for the gold ball bonds.

The aluminium bond wires 9 and gold bond wires 10 are bonded to landing pads 11, 12, respectively, provided on the inner
portion of the leadfingers 4. Since a silver-aluminium interface is known to be unreliable, landing pads 11, 12 comprising two different materials are provided. The landing pads 11 comprise NiNiP for the aluminium bond wires 9, whereas the landing pads 12 for the gold bond wires 10 comprise silver, in order that the bond wires 9, 10 form a bond and, therefore, a good electrical connection with the landing pads 11, 12 respectively.

Therefore, in order to manufacture the lead frame 2, which is suitable for the mixed wire semiconductor package 1, the lead frame 2 undergoes two precision electro-plating process steps; one in which the NiNiP landing pads 11 are electroplated and one in which the silver landing pads 12 are electroplated.

The requirement of two precision electroplating process steps leads to high production costs for mixed wire semiconductor packages and the potential risk of cross contamination of the lead frame during the electroplating of the different metals.

Therefore, it is an object of the invention to provide an improved mixed wire semiconductor package and a simplified manufacturing process in which the disadvantages associated with multiple precision electroplating process steps are avoided.

It is a further object of the invention to provide an improved mixed wire multi-chip semiconductor package.

These objects of the invention are solved by the subject matter of the independent claims. Further improvements arise from the subject matter of the dependent claims.
A semiconductor package according to the invention comprises a lead frame which includes a die pad, a plurality of first leadfingers and a plurality of second leadfingers. Each of the first and second leadfingers includes a landing pad positioned on its inner portion towards the inner end of the leadfinger.

The semiconductor package also includes a semiconductor chip including a plurality of integrated circuit devices and a plurality of chip contact pads on its upper active surface. The semiconductor chip is attached to the die pad by its rear passive surface by conventional die attach material, as is well known in the art.

The semiconductor package further includes a plurality of first bond wires comprising a first electrically conductive material. Each first bond wire extends between a chip contact pad and a landing pad positioned on the plurality of first leadfingers.

A plurality of second bond wires, which comprises a second electrically conductive material, is also provided in the semiconductor package according to the invention. Each second bond wire extends between a chip contact pad and a second leadfinger.

A plastic mould mass encapsulates the semiconductor chip, the pluralities of first and second bond wires and inner portions of the pluralities of first leadfingers and second leadfingers to form an encapsulated mixed wire semiconductor lead frame package.
The semiconductor package according to the invention is characterised in that the package further includes a plurality of first electrically conducting means. A first electrically conducting means is attached to the landing pad of each of the plurality of second leadfingers and a second bond wire extends between, and is attached to, a chip contact pad and a first electrically conducting means.

The invention further provides a semiconductor package which includes at least two semiconductor chips. Such packages are commonly referred to as multi-chip semiconductor packages or multi-chip modules. The multi-chip module according to the invention comprises a lead frame having at least a die pad, a plurality of first leadfingers and a plurality of second leadfingers, each including a landing pad on its inner portion.

The multi-chip module further includes at least two semiconductor chips including integrated circuits and chip contact pads on their upper active surfaces. The semiconductor chips are attached to the die pad by their rear passive surfaces.

A plurality of first bond wires comprising a first electrically conductive material is provided, each extending between a chip contact pad and a landing pad of the plurality of first leadfingers. A plurality of second bond wires comprising a second electrically conductive material is provided, each extending between a chip contact pad and a second leadfinger. A plurality of third bond wires comprising a third electrically conductive material extending between the semiconductor chips.

A plastic mould mass encapsulates the semiconductor chips, the pluralities of first, second and third bond wires and inner
portions of the pluralities of first leadfingers and second leadfingers.

The multi-chip module further includes a plurality of first electrically conducting means. A first electrically conducting means is attached to the landing pad of each of the plurality of second leadfingers, and a second bond wire is attached to the first electrically conducting means.

In contrast to the mixed wire packages known in the art, the mixed wire semiconductor packages according to the invention, therefore, include landing pads, which comprise essentially the same material and which are deposited in the same step of the manufacturing process, on both the pluralities of first and second leadfingers. Therefore, multiple precision or selective electro-plating or electro-deposition steps are avoided.

The semiconductor packages of the invention, preferably, includes a lead frame with a recessed die pad and, preferably, at least one die pad lead.

Preferably, the plurality of first electrically conductive means comprises a plurality of electrically conductive bumps or electrically conductive wedges or electrically conductive balls. The first electrically conductive means are advantageously formed using a ball-bonding or a wedge-bonding technique. Since these techniques are used for forming bond connections between the chip and lead frame in the package, the additional complexity and cost of providing new equipment is, therefore, avoided.
The plurality of first electrically conducting means preferably has an approximately rectangular longitudinal cross-section and is positioned on the landing pad of the second leadfinger with its long side of approximately parallel to the length of the second leadfinger or approximately orthogonal to the length of the second leadfinger. A first electrical conducting means positioned approximately orthogonal to the length of the second leadfinger is particularly advantageous if two or more wires are to be bonded to a landing pad of a second leadfinger. Alternatively, the first electrically conductive means can have any lateral orientation with respect to the length of the second leadfinger.

Preferably, the plurality of first bond wires is attached to the landing pads of the first leadfingers with a ball-bond, bump or a wedge-bond and the plurality of second bond wires is attached to the first electrically conducting means on the second leadfingers with a ball-bond, a bump, a wedge-bond or a stitch-bond.

The reliability of the bond connection is improved if the interfacial area between the bond wire and the first electrically conductive means is increased. If, for example, the first electrically conductive means has an approximately rectangular longitudinal cross-section, for example, it is a wedge, its lateral orientation on the landing pad of the second leadfinger is advantageously chosen to increase the interfacial area by laterally orientating the conductive means and bond wire in approximately the same orientation. Alternatively, if the second bond wire is attached by a wedge-bond to the electrically conductive means which itself has an approximately rectangular longitudinally orientated wedge form,
then a bond between the wire and first electrically conductive means can be more reliably formed, as the relative positioning is more flexible, if they are mutually approximately orthogonally orientated.

However, if, for example, the second bond wire is bonded to the first electrically conductive means using a ball-bond and therefore has a symmetrical and approximately circular lateral bond surface and the first electrically conductive means has an approximately rectangular longitudinal cross-section, then the interfacial area between the bond wire and first electrically conductive means is essentially the same for all lateral orientations of the first electrically conductive means. Therefore, the first electrically conductive means can be orientated on the landing pad so as to the advantage of the manufacturing process, for example by minimising the movement of the bonding tool.

Alternatively, the first electrically conductive means may have a variety of orientations or forms on a lead frame of a single package. This advantageously enables an increased flexibility for the bonding process.

Preferably, the plurality of second bond wires and plurality of electrically conducting means comprise a different material. The plurality of first bond wires and the plurality of electrically conducting means preferably comprise essentially the same material. This advantageously enables the first bond wires and first electrically conductive means to be formed in the same manufacturing process step, thus simplifying the manufacturing process and saving time and costs.
Preferably, under typical wire-bonding conditions, the material of the first bond wire and the material of the landing pad form a eutectic, the material of the electrically conducting means and the material of the landing pad form a eutectic, the material of the second bond wire and the material of the landing pad form no eutectic, and the material of the second bond wire and the material of the electrically conducting means form a eutectic. Typical conditions used to form a bond between the bond wires and the landing pads which comprise various materials in, for example, ball-bonding, wedge-bonding and stitch-bonding techniques are known in the art.

The formation of a eutectic between two metals or metal alloys is well known. Under certain conditions, for example temperature and pressure, a eutectic mixture of the two metals is formed. The eutectic mixture has a lower melting point than that of each of the pure metals. This effect is used in the bonding process to form a melt at the interface between the bond wire and landing pad providing a good electrical and mechanical bond between the wire and landing pad without melting the body of the bond wire or landing pad.

Since the material of the second bond wire and the material of the landing pad form no eutectic under typical wire bonding conditions, a good electrical and mechanical bond is not formed. Therefore, a first electrically conductive means comprising a material which forms a eutectic with the material of the landing pad and a eutectic with the material of the second bond wire is placed between the second bond wire and the landing pad. A good electrical and mechanical bond is, therefore, formed between the first electrically conductive means and the landing pad and between the second bond wire and the first
electrically conductive means. Since the material of the first bond wire and the material of the landing pad form a eutectic a good electrical and mechanical bond is formed and a first electrically conductive means is not included.

The first electrically conductive means has the function of an intermediate or a buffer material which advantageously enables the landing pads of the first and second leadfingers to comprise essentially the same material. The landing pads for both the first and second bond wires are deposited in a single electroplating step in the production process, thus providing a simpler process and saving time and costs.

Since the first electrically conductive means preferably comprise a ball-bond or a wedge bond, they are advantageously formed in the same stage of the process as the bond wire connections. If the first electrically conductive means and the first bond wire means comprise essentially the same material and the same type of bond, for example a wedge bond, then they can be formed in the same manufacturing process step. This advantageously avoids a third bonding tool and a third material as well as saving production time, material. Production costs and, ultimately, the cost of the semiconductor package are reduced.

Preferably, the lead frame comprises copper or a copper alloy, the landing pads comprise a layer of nickel positioned on the surface of the first and second leadfingers and a layer of nickel phosphorous positioned on the layer of nickel, the plurality of first bond wires and the electrically conducting means comprise aluminium or an aluminium alloy and the plurality of second bond wires comprise gold or a gold alloy.
In this case, the aluminium or aluminium alloy of the first bond wires and first electrically conductive means forms a eutectic with the NiNiP landing pad under typical bonding conditions and the gold or gold alloy of the second bond wires forms a eutectic with the aluminium conductive means. Gold and gold alloys form no eutectic with NiNiP under typical bonding conditions.

Alternatively, the lead frame comprises copper or a copper alloy, the landing pads comprise a silver layer positioned on the surface of the first and second leadfingers, the plurality of first bond wires and the electrically conducting means comprise gold or a gold alloy and the plurality of second bond wires comprise aluminium or an aluminium alloy.

A lead frame of copper or a copper alloy has the advantage that the production methods are well-known, the material is available in high purity and is relatively inexpensive. Ni, NiNiP and silver landing pads are also well-known and selective electro-deposition techniques are reliable.

The semiconductor package including one or at least two semiconductor chips preferably includes at least one second electrically conducting means attached to at least one chip contact pad. The second electrically conductive means, preferably, comprises electrically conductive bumps, electrically conductive wedges or electrically conductive balls. The second electrically conductive means is, preferably, positioned between, and electrically connected to, the chip contact pad and a bond wire.
The second electrically conducting means has an approximately rectangular longitudinal cross-section and is positioned on the chip pad with its long side of approximately parallel to the length of the chip pad. Alternatively, the second electrically conducting means has an approximately rectangular longitudinal cross-section and is positioned on the chip pad with its long side of approximately orthogonal to the length of the chip pad. Alternatively, the second electrically conductive means is orientated on the chip pad with any lateral orientation. This has the advantage that the interfacial area between the bond wire and the second electrically conductive means can be increased.

Preferably, the second electrically conductive means comprises essentially the same material as the first conductive means. This advantageously allows the first and second conductive means to be formed in the same step of the manufacturing process and reduces manufacturing time and costs.

The semiconductor package according to the invention, preferably, further includes a plurality of grounding pads positioned on the die pad. This enables the chip to be grounded to the lead frame of the semiconductor package. A plurality of grounding electrically conducting means is, preferably, positioned on the grounding pads and a grounding wire extending between a chip contact pad and the grounding electrically conductive means electrically connects the chip with the lead frame.

The provision of the grounding electrically conductive means on the grounding pad enables the grounding pad to comprise essentially the same material as that of the landing pads so
that both the landing pads and grounding pads can be deposited at the same time. This avoids further electro-plating steps, simplifying the fabrication of the semiconductor package and reducing costs.

The plurality of grounding electrically conductive means, preferably, comprises a plurality of electrically conductive bumps or electrically conductive wedges or electrically conductive balls. This advantageously enables the grounding electrically conductive means to be formed during the same stage of the manufacturing process as the first electrically conductive means which are positioned on the landing pads.

The plurality of grounding bond wires is attached to the grounding electrically conducting means on the die pad with a ball-bond, a bump or a stitch bond. Advantageously, the most appropriate bond type is provided so that, for example, the bond type is compatible with the material of the wire.

Preferably, under wire-bonding conditions the material of the first bond wire and the material of the landing pad form a eutectic, the material of the first electrically conducting means forms a eutectic with the material of the landing pad, the material of the second bond wire and the material of the landing pad form no eutectic, the material of the second bond wire and the material of the first electrically conducting means form a eutectic, the material of the grounding electrically conductive means and the material of the grounding pad form a eutectic, and the material of the grounding wire and the material of the grounding electrically conductive means form a eutectic.
Therefore, a good and reliable bond is formed between the first bond wire and the landing pad, the second bond wire and the first electrically conductive means and the first electrically conductive means the landing pad. A good bond is also formed between the grounding wire and the grounding electrically conductive means and the grounding electrically conductive means and the grounding pad. A reliable grounding of the chip to the lead frame is, therefore, provided.

The lead frame, preferably, comprises copper, and similarly to the landing pads, the grounding pads comprise a layer of nickel positioned on the surface of the die pad of the lead frame and a layer of nickel phosphorous positioned on the layer of nickel. Preferably, the plurality of first bond wires, the electrically conducting means and the grounding electrically conductive means comprise aluminium or an aluminium alloy and the plurality of second bond wires and the plurality of grounding wires comprise gold or a gold alloy.

This advantageously allows the grounding pads to be formed in the same electro-plating steps as the landing pads and therefore further processing steps are not introduced into the manufacturing line reducing the production costs. Also, since the grounding and first electrically conductive means comprise essentially the same material, the first and grounding electrically conductive means may be fabricated in the same process step. Since the second and grounding bond wires comprise the same material, the second and grounding bond wires can be provided in the same process step.
The manufacture of the package is, therefore, simplified and costs reduced as the number of different materials used in the package is not increased.

In the multi-chip module according to the invention, the plurality of third bond wires, preferably, comprise essentially the same material as the plurality of second bond wires or the plurality of first bond wires. The plurality of third bond wires is, preferably, attached to the chip pads of the first and second semiconductor chips with a ball bond, a bump or a wedge bond. Alternatively, the plurality of third bond wires is attached to the second electrically conductive means positioned on the chip pads with a ball bond, a bump or a wedge bond.

A first semiconductor chip of the multi-chip module is, preferably electrically connected by first bond wires to the plurality of first leadfingers. A second semiconductor chip is, preferably, electrically connected by second bond wires to the plurality of second leadfingers. This arrangement is advantageous as the most appropriate type of bond wire can be chosen for the integrated circuits of each type of semiconductor chip.

The multi-chip module, preferably, includes at least one logic semiconductor chip and at least one power semiconductor chip. More preferably, the multi-chip module includes at least one power chip electrically connected to the first leadfingers of the lead frame by a plurality of first bond wires and at least one logic chip electrically connected to the first electrical means of the second leadfingers of the lead frame by a plurality of second bond wires.
preferably, in the multi-chip module according to the invention, the first bond wires comprise aluminium or an aluminium alloy, the second bond wires comprise gold or a gold alloy, the first electrical means comprises aluminium, the lead frame comprises copper and the landing pads comprise Ni and NiP.

The bond wires connecting the logic chip to the second lead-fingers, which preferably include first electrically conductive means, preferably, comprise gold. The bond wires connecting the power chip to the first leadfingers of the lead frame and to the logic chip preferably comprise aluminium and, preferably, have a larger diameter than the gold bond wires. The larger diameter is advantageous for the supply of high currents.

The chip pads, preferably, have a rectangular form for the bond wires connected using a wedge bond and a square form for bond wires connected using a ball bond. A rectangular chip pad is advantageous for wedge bonds as the interface formed between the chip pad and the wedge bond is of a rectangular form.

The invention also provides methods to assemble semiconductor packages. A method comprises the following steps.

Firstly, a lead frame comprising a die pad, a plurality of first leadfingers and a plurality of second leadfingers is provided. The lead frame is produced by etching or stamping methods known in the art. Initially, a lead frame strip comprising a plurality of lead frames is formed in which the plu-
rality of lead frames are orientated in rows and columns forming an array. The individual lead frames are connected to the lead frame strip surround and to each other by tie bars which are removed at a later stage of the process to form individual lead frame packages.

A landing pad is then deposited on the inner portion of each first leadfinger and each second leadfinger. A semiconductor chip including a plurality of integrated circuit devices and a plurality of chip contact pads on its upper active surface is provided. The passive rear surface of the semiconductor chip is attached to the die pad using conventional die attach material.

A first electrically conducting means is then formed on each landing pad of the plurality of second leadfingers.

Bond connections are formed between the chip contact pads and landing pads of the plurality of first leadfingers with first bond wires. Bond connections are formed between the chip contact pads and first electrically conducting means of the plurality of second leadfingers with second bond wires.

The semiconductor chip, the first and second bond wires and inner ends of the pluralities of first and second leadfingers are then encapsulated in a plastic mould material.

A method according to the invention to assemble a semiconductor package including at least two semiconductor chips comprises the following steps. A lead frame including a die pad, a plurality of first leadfingers and a plurality of second leadfingers is provided. A plurality of landing pads is depos-
ited on the inner portion of the first leadfinger and second leadfingers and at least two semiconductor chips including integrated circuits and chip contact pads on the upper active surface are attached by the passive rear surface to the die pad.

A plurality of first electrically conducting means is formed on the landing pads of each of the plurality of second leadfingers.

First bond connections are then formed between the chip contact pads and landing pads of the plurality of first leadfingers with first bond wires. Second bond connections are formed between the chip contact pads and electrically conducting means of the plurality of second leadfingers with second bond wires. Third bond connections are formed between the semiconductor chips with third bond wires.

The semiconductor chips, the pluralities of first second and third bond wires and inner ends of leadfingers are encapsulated in a plastic mould material.

 Preferably, the lead frame includes a recessed die pad and at least one die pad lead. A recessed die pad is typically formed by a pressing technique.

 Preferably, the first electrically conducting means has an approximately rectangular longitudinal cross-section and is formed on the landing pad of the second leadfinger approximately parallel to the length of the second leadfinger or approximately orthogonal to the length of the second leadfinger. Alternatively, the first electrically conductive means
laterally positioned with any lateral orientation with respect to the length of the second lead finger.

Preferably, the first electrically conducting means is formed by a wedge-bonding technique or a ball bonding technique. These techniques are reliable well known and widely used. Therefore, start-up costs can be saved as the existing production line can be used.

Preferably, the landing pads are formed by depositing a first layer on the surface of the leadfinger and by depositing a second layer on the first layer. This has the advantage of forming a reliable landing pad which forms a good bond with the material of the lead frame and with the first bond wire and electrically conductive means. Preferably, the landing pads are deposited using a selective electro-deposition or electro-plating technique. Selective electro-plating techniques are well-known in the art.

Since the landing pads of both the first and second lead-fingers are electro-plated at essentially the same time in a single process step, the manufacturing process is simplified and costs are saved. A further advantage of the method according to the invention is that since a conventional lead frame, i.e. all the landing pads comprise essentially the same material, is used, the same lead frame can be used for different semiconductor products and the flexibility of having various products in the internal configuration of the same package without changing the lead frame type is enabled.

Preferably, the plurality of first bond wires is attached to the chip contact pads and the landing pads of the plurality of
first leadfingers using a ball-bonding or a wedge-bonding technique and the plurality of second bond wires are attached to the chip contact pads and the first electrically conducting means of the plurality of second leadfingers using a ball-bonding or a wedge-bonding or a stitch-bonding technique. These techniques are well-known and reliable.

If the first bond wires and electrically conductive means comprise essentially the same material and are formed using the same technique, for example a wedge bonding technique, then they can be formed in the same process step. All of the electrically conductive means can be formed on the landing pads of the second leadfingers in a first stage followed by forming all of the bond connections between the chip contact pad and the landing pad of the first leadfingers by first bond wires or these steps can be reversed. Alternatively, the electrically conductive means and the first wire bonds can be made in a mixed way in the same process step. This has the advantage that the movement of the tool can be minimised and collisions between formed bonds and the movement of the tool can be avoided.

Preferably, the lead frame comprises copper or a copper alloy, the landing pads comprise a layer of nickel positioned on the surface of the first and second leadfingers and a layer of nickel phosphorous positioned on the layer of nickel, the plurality of first bond wires and the electrically conducting means comprise aluminium or an aluminium alloy and the plurality of second bond wires comprise gold or a gold alloy.

More preferably, the gold wires are bonded by a ball bonding technique which uses temperature and pressure to form the bond
and the aluminium wires are, more preferably, bonded using a wedge bonding technique which uses mainly ultrasonic energy and force to form the bond. Gold ball bonding is, preferably, used for bonding over active circuits and chips with delicate, such as low thermal expansion material, layers.

At least one second electrically conducting means is, preferably, attached to at least one chip contact pad. The plurality of second electrically conductive means is, preferably, formed by a ball-bonding or a wedge-bonding technique.

The second electrically conducting means has an approximately rectangular longitudinal cross-section and is formed on the chip pad with its long side of approximately parallel to the length of the chip pad. Alternatively, the second electrically conducting means has an approximately rectangular longitudinal cross-section and is positioned on the chip pad with its long side of approximately orthogonal to the length of the chip pad. The lateral orientation of the second electrically conducting means is, preferably, chosen so as to increase the interfacial area between the bond wire and the second electrically conductive means.

The second electrically conductive means is, preferably, electrically connected to the chip contact pad and a bond wire.

The method to assemble the package according to the invention advantageously further includes the steps of depositing at least one grounding pad on the die pad. A grounding electrically conductive means is then formed on the grounding pad and bond connections are formed between contact pads on the chip
and the grounding electrically conductive means. This enables
the chip to be grounded to the lead frame.

Preferably, the grounding pads are formed by depositing a
first layer on the surface of the die pad and by depositing a
second layer on the first layer. The grounding pads are,
preferably, deposited using a selective electro-deposition
technique which is well-known in the art and inexpensive.
More preferably, the grounding pads are formed in the same
process steps as the landing pads. This further reduces the
costs and complexity of the assembly process as only one
masking step for the electro-plating process is required.

The plurality of grounding bond wires are, preferably, at-
tached to the chip contact pads and the grounding electric-
cally conductive means using a ball-bonding or a wedge-
bonding or a stitch-bonding technique. These techniques are
well known in the art and the most appropriate technique de-
pends on a number of factors known in the art such as the ma-
terial of the bond wire. More preferably, the grounding wire
is attached to the chip pad with a ball-bond and to the
grounding electrically conductive means with a stitch-bond.

In the multi-chip module according to the invention, prefera-
bly, at least one power semiconductor chip and at least one
logic semiconductor chip are attached to the die pad.

Preferably, at least one power chip is electrically connected
to the first leadfingers of the lead frame by a plurality of
first bond wires and at least one logic chip is electrically
connected to the first electrical means of the second lead-
fingers of the lead frame by a plurality of second bond wires.
The plurality of third bond wires is attached to the chip pads of the at least two semiconductor chips by a ball-bonding or a wedge-bonding or a stitch-bonding technique. Alternatively, the plurality of third bond wires is attached to the second electrically conductive means positioned on the chip pads by a ball-bonding or a wedge-bonding or a stitch-bonding technique, and more preferably, by a stitch bond.

Embodiments of the invention will now be described by way of example with reference to the drawings.

Figure 1 shows an encapsulated mixed wire semiconductor lead frame package known in the prior art,

Figure 2 shows an encapsulated mixed wire semiconductor package according to a first embodiment of the invention,

Figure 3 shows an encapsulated mixed wire semiconductor package according to a second embodiment of the invention,

Figure 4 shows an encapsulated mixed wire semiconductor package according to a third embodiment of the invention,

Figure 5 shows a schematic diagram of the first step in the formation of a wedge according to the invention,

Figure 6 shows a schematic diagram of the second step of in the formation of a wedge according to the invention,
Figure 7 shows an encapsulated mixed wire semiconductor package according to a fourth embodiment of the invention,

Figure 8 shows a first multi-chip module according to the invention,

Figure 9 shows a second multi-chip module according to the invention, and

Figure 10 shows a schematic perspective view of a section of a mixed wire semiconductor package including grounding connections according to the invention.

Figure 2 shows an encapsulated mixed wire semiconductor lead frame package 20 which includes a semiconductor chip 21 attached to a recessed die pad 22. The semiconductor chip 21 is electrically connected to a plurality of lead fingers 23, 24 of the lead frame 25 by a first plurality of aluminium bond wires 26 and a second plurality of gold bond wires 27. The diameter of the aluminium bond wires 26 is larger than that of the gold bond wires 27.

The copper lead frame 25 comprises a central recessed die pad 22 laterally surrounded by two pluralities of lead fingers 23, 24. The die pad 22 is positioned lower in the package 20 than the lead fingers 23, 24 so that the upper surface of the die pad 22 is positioned slightly lower than the bottom surface of the lead fingers 23, 24 with respect to the top surface of the semiconductor package 20.
The lead frame 25 also includes two die pad leads 28 which extend from the die pad 22 to the outside of the encapsulated package 20. The die pad leads 28 enable the rear surface of the semiconductor chip 21 to be grounded at the same potential as that of the lead frame 25. There are no bond connections between the chip 21 and the die pad leads 28.

The inner portion of each of the lead fingers 23, 24 is located inside the plastic encapsulation 39 of the package 20. Each lead finger 23, 24 includes a landing pad 29 positioned on its upper surface towards the inner end of the inner portion. Each landing pad 29 comprises two layers 30, 31 which were deposited by an electroplating technique. Each landing pad 29 comprises a layer of nickel 30 located on the surface of the copper lead finger 23, 24 and a layer of nickel phosphorous 31 positioned on the nickel layer 30.

The lead frame 25 according to the invention includes two pluralities of lead fingers 23, 24. They are distinguished in that the second plurality of lead fingers 24 further include an aluminium wedge 32 which is located on the upper surface of the landing pad 29. The first plurality of lead fingers 23 include only a landing pad 29. The aluminium wedge 32 is laterally orientated on the landing pad 29 so that its length lies approximately parallel to the length of the second lead finger 24. In this cross-sectional view, the aluminium wedge 32 has an approximately rectangular cross-section in which the long side is horizontal. The two end portions of the wedge 32 are raised slightly above the surface of the landing pad 29 so that only the central portion of the length of the wedge 32 is in contact with the landing pad 29.
The semiconductor chip 21 includes a plurality of chip contact pads 33 on its upper surface and two pluralities of integrated circuits 34, 35. The back side of the chip 21 is attached by die attach material 36 to the die pad 22 of the lead frame 25. The chip 21 is electrically connected by the first plurality of aluminium bond wires 26 connected between the chip contact pads 33 of the first plurality of integrated circuit devices 34 and the landing pads 29 of the first lead fingers 23. The second plurality of integrated circuit devices 35 are electrically connected by a second plurality of gold bond wires 27 to the aluminium wedges 32 which are located on the landing pads 29 of the second lead fingers 24.

The aluminium bond wires 26 are bonded to the chip contact pads 33 and landing pads 29 of the first lead fingers 23 by wedge-bonds 37 formed using a wedge-bonding technique. Therefore, the end portions of the aluminium wire bonds 26 are positioned approximately parallel to the upper surface of the chip contact pad 33 and landing pad 29 respectively.

The gold wires 27 are bonded to the chip contact pads 33 and the aluminium wedge 32 located on the second lead fingers 24 using a ball bonding technique. A gold bump 48 is formed on the surface of the aluminium wedge 32. A gold wire ball bond 38 is then formed at the chip contact pad 33 and the gold wire 27 extends between the chip contact pad 33 and the gold bump 48 positioned on the aluminium wedge 32 and electrically connects the chip pad 33 with the second lead finger 24. The ball bond 38 formed at the end portion of the gold wire bond 27 where the wire joins the surface of the chip contact pad 33 has an approximately circular or oval cross-section.
The two pluralities of bond wires 26, 27, semiconductor chip 21, die pad 22 and inner portions of the two pluralities of lead fingers 23, 24 are encapsulated by a plastic mould material 39 to form the mixed wire semiconductor lead frame package 20 of the invention. The outer portions of the lead fingers protruding from the plastic encapsulation 39 form the outer contacts of the package 20. The outer contacts enable the package 20 to be mounted on an external substrate such as a printed circuit board which is not shown in the diagram.

Figure 3 shows a second embodiment of a mixed wire semiconductor lead frame package 40 according to the invention. Parts of the package 40 which are essentially the same as those of the first embodiment 20 shown in Figure 2 have the same reference number and are not necessarily described again.

In this embodiment of the invention, the aluminium wedge 41 is attached to the landing pad 29 of the second lead finger 24 approximately orthogonally with respect to the length of the lead finger 24. Therefore, in the cross-sectional diagram shown in Figure 3 the wedge 41 has an approximately oval cross-section.

In the second embodiment of the invention, the gold wire 27 is bonded to the chip contact pad 33 by a ball-bond 38 and, therefore, has the characteristic ball or oval cross-section. In contrast to the embodiments shown in Figure 2, the gold wire 27 is bonded to the aluminium wedge 41 by a stitch bond 59. The stitch bond 59 has a thin approximately rectangular cross-section.
Figure 4 shows a third embodiment of a mixed wire semiconductor lead fame package 42 according to the invention. Parts of the package 42 which are essentially the same as shown in the embodiments of the invention of Figures 2 and 3 have the same reference number and are not necessarily described again.

In this third embodiment, the aluminium wedge 32 is positioned on the landing pad 29 of the second lead finger 24 as shown in the first embodiment of the invention. The wedge 32 is positioned so that its long length is approximately parallel to the long length of the second lead finger 24. In this embodiment of the invention, the gold wire 27 is bonded by a ball bond 38 to the chip contact pad 33 and to the aluminium wedge 32 by a stitch bond 59.

Figure 5 shows a schematic diagram of a detail in the first step of the process to produce the aluminium wedge 32 according to the invention. A second lead finger 24 including a landing pad 29 on its upper surface is provided. The landing pad 29 comprises a first nickel layer 30 positioned on the copper leadfinger 24 and a nickel phosphorous layer 31 positioned on the nickel layer 30.

A wedge bonding tool 43 encloses the end portion of a spool of aluminium source wire 44. The aluminium source wire 44 is spooled out a desired length and pressed using the pressing surface 45 of the wedge bonding tool 43 into the upper surface of the landing pad 29. The pressed portion 46 of the source wire 44 then undergoes a bonding treatment in which it is subjected to an appropriate ultrasonic energy for an appropriate time in order to bond the pressed portion 46 of the source 44 wire to the landing pad 29.
Figure 6 shows a schematic diagram of the second step in the process to form the aluminium wedge 32 according to the invention. After the bonding process is complete, the wedge bonding tool 43 is raised upwards a small distance with respect to the surface of the lead finger 24 as indicated by the arrow. The wire clamp 47 of the wedge bonding tool 43 then closes onto the aluminium source wire 44 and the bonding tool 43 is moved sideways and upwards with respect to the landing pad 29, as shown by the arrow, in order to break the source wire 43 at a position close to the pressed portion 46 and the landing pad 29. In this way an aluminium wedge 32 is formed on the landing pad 29 of the second lead finger 24.

Figure 7 shows a fourth embodiment of a mixed wire semiconductor lead frame package 50 according to the invention. Parts of the package 50 which are essentially the same as those of the first embodiment shown in Figure 2 are indicated by the same reference number and are not necessarily described again.

In this embodiment of the invention, the first lead fingers 23 and a second lead fingers 24 of the copper lead frame 25 include a landing pad 51 positioned towards the end of the inner portion. In contrast to the previous embodiments of the invention, the landing pad 51 comprises silver.

In this fourth embodiment of the invention, a gold bump 52 is positioned on the silver landing pad 51 of the second plurality of lead fingers 24.

The aluminium bond wires 27 are bonded with a wedge bond 37 to the chip contact pads 33 and to the gold bump 52 positioned on
the silver landing pad 51 of the second lead finger 24. The
gold wires 26 are bonded to the chip contact pads by a ball
bond 38 and to the silver landing pad 51 positioned on the in-
ner portion of the first lead finger 23 of the lead frame 25
by a stitch bond 59.

Figure 8 shows a first multi-chip module 53 including two
semiconductor chips 54 and 55 according to the invention.
Parts of the multi-chip module 53 which are similar to those
of the previous embodiments are indicated by the same refer-
ence number and are not necessarily described again.

The multi-chip module 53 includes a copper lead fame 25 in-
cluding a recessed die pad 22 laterally surrounded by a plu-
rality of first lead fingers 23 and a plurality of second lead
fingers 24. A landing pad 29 is positioned towards the end of
the inner portion of the first plurality 23 and second plural-
ity 24 of lead fingers and comprises a Ni layer 30 positioned
on the first 23 and second 24 leadfingers and a NiP layer 31
attached to the nickel layer. The second plurality of lead fin-
gers 24 further include an aluminium wedge 32 which is posi-
tioned on the nickel phosphorous layer 31 of the landing pad
29.

The first 54 and the second 55 semiconductor chip are mounted
laterally adjacent to each other on the die pad 22 by die at-
tach material 36. Each of the semiconductor chips 54 and 55
includes a plurality of first integrated circuits 34, second
integrated circuits 35 and chip contact pads 33 on its upper
active surface. The first semiconductor chip 54 is electric-
ally connected by an aluminium bond wire 26 to the landing
pads 29 positioned on the first lead finger 23.
The first semiconductor chip 54 is also electrically connected to the second semiconductor chip 55 by a gold wire 56 which contacts a chip contact pad 33 of semiconductor chip 54 with a chip contact pad 33 of semiconductor chip 55. The gold wire 56 is connected to the chip contact pads 33 of the semiconductor chip 55 by a ball bond 38 and to the contact pad 33 of the semiconductor chip 54 by a stitch bond 59 on a gold bump 48.

The second semiconductor chip 55 is electrically connected to the second lead finger 24 by a gold wire 27. The gold wire 27 is connected to the chip contact pad 33 by a ball bond 38 and to the aluminium wedge 32 positioned on the landing pad 29 of the second lead finger 24 by a stitch bond 59. The diameter of the aluminium wires 26 is larger than that of the gold wires 27 which connect the second semiconductor chip to the lead-fingers 24 and the gold wires 56 which connect the first 54 and second 55 semiconductor chip.

The first 54 and second 55 semiconductor chips, the die pad 22, bond wires 26, 27, 56 and the inner portions, including the landing pads 29, of the first 23 and second 24 pluralities of lead fingers are encapsulated in a plastic mold material 39. The outer portions of the first 23 and second 24 pluralities of lead fingers extend outside of the semiconductor package 53 and provide the external electrical connection for the package. The outer portions of the lead fingers 23 and 24 enable the package 53 to be mounted on and electrically connected to an external substrate such as a printed circuit board (which is not shown in the diagram).
Figure 9 shows a second multi-chip module 57 including two semiconductor chips 54 and 55 according to the invention. Parts of the second multi-chip module 57 which are similar to those of the previous embodiments are indicated by the same reference number and are not necessarily described again.

The second multi-chip module 57 further includes a chip aluminium wedge 58 positioned on a chip contact pad 33 of the first semiconductor chip 54. A gold wire 56 connects the first 54 and second 55 semiconductor chip of the second multi-chip module 57. The gold wire 56 is bonded to the chip aluminium wedge 58 on the first semiconductor chip 54 by a stitch bond 59 and to a chip contact pad 33 of the second semiconductor chip 55 by a ball bond 38.

The second multi-chip module 57 also includes an aluminium wedge 32 positioned on the second leadfinger 24 as shown in the multi-chip embodiment of Figure 8.

Figure 10 shows a schematic perspective view of a section of a mixed wire semiconductor package 60 which includes grounding connections 61 between the active surface of the chip 21 and the die pad 22. The package encapsulation is not shown for clarity in this figure.

Figure 10 shows a section of a semiconductor chip 21 including chip contact pads 33 on the upper active surface. The chip 21 is mounted by die attach material 36 in approximately the lateral centre of the die pad 22. The die pad 22 is laterally larger than the chip 21. The chip 21 and die pad 22 are laterally surrounded by a plurality of first and second leadfingers
23, 24 of which the inner portion of three second leadfingers 24 are shown in the figure.

Similarly to the embodiments of Figures 2 to 4, the second leadfingers 24 include a landing pad 29, comprising a layer of Ni 30 and a layer of NiP 31, and an aluminium wedge 32 positioned on the landing pad 29. The aluminium wedges 32 are positioned approximately parallel to the length of the leadfingers 24. The integrated circuits 35 on the active surface of the chip 21 are electrically connected to the second leadfingers 24 by gold bond wires 27 which extend between a chip contact pad 33 and an aluminium wedge 32. The gold wires 27 are connected to the chip pad 33 by a ball bond 38 and to the aluminium wedge 32 by a stitch bond 59.

In this embodiment of the invention, the die pad 22 includes grounding pads 62 positioned on the upper surface of the die pad 22 of which one ground pad 62 is shown in the Figure. The grounding pads 62 are laterally positioned towards the outer edge the die pad 22 and are, therefore, positioned between the semiconductor chip 21 and the lead fingers. The grounding pad 62 also includes two electro-plated layers and comprises a layer of Ni 63 positioned on the surface of the copper die pad 22 and a layer 64 comprising NiP positioned on the nickel layer 63.

A grounding aluminium wedge 65 is positioned on the grounding pad 62. The chip 21 is grounded to the die pad 22 by a gold grounding wire 61 which extends between a contact pad 66 on the upper surface of the chip 21 and the grounding aluminium wedge 65 on the grounding pad 62. The grounding gold wire 61
is connected to the contact pad 66 by a ball bond 38 and to the grounding aluminium wedge 62 by a stitch bond 59.
Reference numbers

1 Prior art semiconductor package
2 lead frame
3 die pad
4 leadfinger
5 semiconductor chip
6 die attach material
7 integrated circuit devices
8 chip contact pad
9 aluminium bond wire
10 gold bond wire
11 NiNiP land pad
12 Silver landing pad
15
20 first semiconductor package
21 semiconductor chip
22 recessed die pad
23 first leadfinger
24 second leadfinger
25 lead frame
26 aluminium bond wire
27 gold bond wire
28 die pad lead
29 landing pad
30 Ni layer
31 NiP layer
32 aluminium wedge
33 chip contact pad
34 first integrated circuits
35 second integrated circuits
36 die attach material
37 wedge bond
38 ball bond
39 plastic mold material
40 second semiconductor package
41 second aluminium wedge
42 third semiconductor package
43 wedge bonding tool
44 aluminium source wire
45 pressing surface
46 pressed portion
47 wire clamp
48 gold bump
50 fourth semiconductor package
51 silver landing pad
52 gold bump
53 first multi-chip module
54 first semiconductor chip
55 second semiconductor chip
56 gold bond wire
57 second multi-chip module
58 chip aluminium wedge
59 stitch bond
60 sixth semiconductor package
61 grounding wire
62 grounding pad
63 Ni layer
64 NiP layer
65 grounding aluminium wedge
66 contact pad
30
Claims

1. A semiconductor package (20; 40; 42; 50; 60) comprising:
   - a lead frame (25) comprising:
     5   - a die pad (22),
     - a plurality of first leadfingers (23) and a plurality of second leadfingers (24), each including a landing pad (29) on its inner portion,
     - a semiconductor chip (21) including integrated circuits (34, 35) and chip contact pads (33) on its upper active surface, the semiconductor chip (21) being attached to the die pad (22) by its rear passive surface,
     - a plurality of first bond wires (26) comprising a first electrically conductive material, each extending between a chip contact pad (33) and a landing pad (29) of the plurality of first leadfingers (23),
     - a plurality of second bond wires (27) comprising a second electrically conductive material, each extending between a chip contact pad (33) and a second leadfinger (24),
     - a plastic mould mass (39) encapsulating the semiconductor chip (21), the pluralities of first (26) and second (27) bond wires and inner portions of the pluralities of first leadfingers (23) and second leadfingers (24), characterised in that the semiconductor package (20; 40; 42; 50; 60) further includes a plurality of first electrically conducting means (32; 41), a first electrically conducting means (32; 41) is attached to the landing pad (29) of each of the pluralities of second leadfingers (24), and a second bond wire (27) is attached to the first electrically conducting means (32; 41).
2. A semiconductor package (53; 57) comprising:
   - a lead frame (25) comprising:
     - a die pad (22),
   a plurality of first leadfingers (23) and a plurality of second leadfingers (24), each including a landing pad (29) on its inner portion,
   - at least two semiconductor chips (54, 55) including integrated circuits (34, 35) and chip contact pads (33) on their upper active surfaces attached to the die pad (22),
   a plurality of first bond wires (26) comprising a first electrically conductive material, each extending between a chip contact pad (33) and a landing pad (29) of the plurality of first leadfingers (23),
   a plurality of second bond wires (27) comprising a second electrically conductive material, each extending between a chip contact pad (33) and a second leadfinger (24),
   - a plurality of third bond wires (56) comprising a third electrically conductive material, extending between the semiconductor chips (54, 55),
   - a plastic mould mass (39) encapsulating the semiconductor chip (21), the pluralities of first (26), second (27) and third (56) bond wires and inner portions of the pluralities of first leadfingers (23) and second leadfingers (24),
characterised in that the semiconductor package (53; 57) further includes a plurality of first electrically conducting means (32; 41), a first electrically conducting means (32; 41) is attached to the landing pad (29) of each of the plurality of second
leadfingers (24), and a second bond wire (27) is attached to the first electrically conducting means (32; 41).

3. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that the lead frame (25) includes a recessed die pad (22).

4. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that the plurality of first electrically conductive means (32, 41, 52) comprises a plurality of electrically conductive bumps or electrically conductive wedges (32, 41) or electrically conductive balls (52).

5. A semiconductor package (20; 42; 53; 57; 60) according to claim 1 or claim 2, characterised in that the first electrically conducting means (32) has an approximately rectangular longitudinal cross-section and is positioned on the landing pad (29) with its long side of approximately parallel to the length of the second lead-finger (24).

6. A semiconductor package (40) according to claim 1 or claim 2, characterised in that the first electrically conducting means (41) has an approximately rectangular longitudinal cross-section and is positioned on the landing pad (29) with its long side of
approximately orthogonal to the length of the second lead-finger (24).

7. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that the plurality of first bond wires (26) is attached to the landing pads (29) of the first leadfingers (23) with a ball bond (38), a bump (48) or wedge bond (37) and the plurality of second bond wires (27) is attached to the first electrically conducting means (32; 41) on the second leadfingers (24) with a ball-bond (38), a bump (48) or a stitch bond (59).

8. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that the plurality of second bond wires (27) and the plurality of first electrically conducting means (32; 41) comprise a different material.

9. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that the plurality of first bond wires (26) and the plurality of electrically conducting means (32; 41) comprise essentially the same material.

10. A semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 1 or claim 2, characterised in that under wire-bonding conditions
- the material of the first bond wire (26) and the material of the landing pad (29) form a eutectic,
- the material of the first electrically conducting means (32; 49) and the material of the landing pad (29) form a eutectic,
- the material of the second bond wire (27) and the material of the landing pad (29) form no eutectic, and
- the material of the second bond wire (27) and the material of the first electrically conducting means (32; 41) form a eutectic.

11. A semiconductor package (20; 40; 42; 53; 57; 60) according to claim 1 or claim 2, characterised in that
- the lead frame (25) comprises copper,
- the landing pads (29) comprise a layer of nickel (30) positioned on the surface of the first (23) and second (24) leadfingers and a layer of nickel phosphorous (31) positioned on the layer of nickel (30),
- the plurality of first bond wires (26) and the electrically conducting means (32; 41) comprise aluminium or an aluminium alloy,
- the plurality of second bond wires (27) comprise gold or a gold alloy.

12. A semiconductor package (50) according to claim 1 or claim 2, characterised in that
- the lead frame (25) comprises copper,
- the landing pads (51) comprise silver,
- the plurality of second bond wires (27) comprise aluminium or an aluminium alloy, and
- the plurality of first bond wires (26) and the electrically conducting means (52) comprise gold or a gold alloy.

13. A semiconductor package (57) according to claim 1 or claim 2, characterised in that the semiconductor package (57) includes at least one second electrically conducting means (58) attached to at least one chip contact pad (33).

14. A semiconductor package (57) according to claim 1 or claim 2, characterised in that the at least one second electrically conducting means (58) is electrically connected to the chip pad (33) and a bond wire (26, 27, 56).

15. A semiconductor package (57) according to claim 1 or claim 2, characterised in that the at least one second electrically conductive means (58) comprises an electrically conductive bump or electrically conductive wedge (32, 41) or electrically conductive ball.

16. A semiconductor package (57) according to claim 1 or claim 2, characterised in that the second electrically conductive means (58) comprises essentially the same material as the first conductive means (32; 41).
17. A semiconductor package (60) according to claim 1 or claim 2,
characterised in that
the semiconductor package (60) further includes a plurality of grounding pads (62) positioned on the die pad (22).

18. A semiconductor package (60) according to claim 17,
characterised in that
a plurality of grounding electrically conducting means (65) is positioned on the grounding pads (62), and a grounding wire (61) extending between a chip contact pad (66) and the grounding electrically conductive means (65).

19. A semiconductor package (60) according to claim 18,
characterised in that
the plurality of grounding electrically conductive means (65) comprises a plurality of electrically conductive bumps or electrically conductive wedges (65) or electrically conductive balls.

20. A semiconductor package (60) according to claim 18 or 19,
characterised in that
plurality of grounding bond wires (61) is attached to the grounding electrically conducting means (65) on the die pad (22) with a ball-bond (38), a bump (48) or a stitch bond (59).

21. A semiconductor package (60) according to one of claims 18 to 20,
characterised in that
under wire-bonding conditions
- the material of the first bond wire (26) and the material of the landing pad (29) form a eutectic,
- the material of the first electrically conducting means (32; 49) forms a eutectic with the material of the landing pad (29),
- the material of the grounding electrically conductive means (65) and the material of the grounding pad (62) form a eutectic,
- the material of the second bond wire (27) and the material of the landing pad (29) form no eutectic,
- the material of the second bond wire (27) and the material of the first electrically conducting means (32; 41) form a eutectic, and
- the material of the grounding wire (61) and the material of the grounding electrically conductive means (65) form a eutectic.

22. A semiconductor package (60) according to one of claims 17 to 21,
characterised in that
- the lead frame (25) comprises copper,
- the grounding pads (62) comprise a layer of nickel (63) positioned on the surface of the die pad (22) and a layer of nickel phosphorous (64) positioned on the layer of nickel (63),
- the plurality of first bond wires (26), the electrically conducting means (32; 41) and the grounding electrically conductive means (65) comprise aluminium or an aluminium alloy,
- the plurality of second bond wires (27) and the plurality of grounding wires (61) comprise gold or a gold alloy.
23. A semiconductor package (53; 57) according to claim 2, characterised in that the plurality third bond wires (56) comprise essentially the same material as the plurality of second bond wires (27) or the plurality of first bond wires (26).

24. A semiconductor package (53; 57) according to claim 2, characterised in that the semiconductor package (53; 57) includes at least one power semiconductor chip (55) and at least one logic semiconductor chip (54).

25. A semiconductor package (53; 57) according to claim 24, characterised in that the semiconductor package (53; 57) includes at least one power chip (55) electrically connected to the first leadfingers (23) of the lead frame (25) by a plurality of first bond wires (26) and at least one logic chip (54) is electrically connected to the first electrical means (32; 41) of the second leadfingers (24) of the lead frame (25) by a plurality of second bond wires (27).

26. A semiconductor package (53; 57) according to claim 25, characterised in that the first bond wires (26) comprise aluminium or an aluminium alloy, the second bond wires comprise gold or a gold alloy (27), the first electrical means (32; 41) comprises aluminium, the leadframe (25) comprises copper and the landing pads (29) comprise Ni and NiP.
27. Method to assemble a semiconductor package (20; 40; 42; 50; 60) comprising the following steps:
   - providing a lead frame (25) including a die pad (22), a plurality of first leadfingers (23) and a plurality of second leadfingers (24),
   - depositing a landing pad (29) on the inner portion of each first leadfinger (23) and each second leadfinger (24),
   - attaching a semiconductor chip (22), including integrated circuits (34, 35) and a plurality of chip contact pads (33) on its upper active surface, to the die pad (22),
   - forming a plurality of first electrically conducting means (32; 41) on the landing pads (29) of the plurality of second leadfingers (24),
   - forming first bond connections (26) between the chip contact pads (33) and landing pads (29) of the plurality of first leadfingers (23) with first bond wires (26),
   - forming second bond connections (27) between the chip contact pads (33) and electrically conducting means (32; 41) of the plurality of second leadfingers (24) with second bond wires (27),
   - encapsulating the semiconductor chip (21), the first (26) and second (27) bond wires and inner ends of leadfingers (23, 24) in a plastic mould material (39).

28. Method to assemble a semiconductor package (53; 57) comprising the following steps:
   - providing a lead frame (25) including a die pad (22), a plurality of first leadfingers (23) and a plurality of second leadfingers (24),
- depositing a landing pad (29) on the inner portion of each first leadfinger (23) and each second leadfinger (24),
- attaching at least two semiconductor chips (54, 55) including integrated circuits (34, 35) and chip contact pads (33) on the upper active surface to the die pad (22),
- forming a plurality of first electrically conducting means (32; 41) on the landing pads (29) of each of the plurality of second leadfingers (24),
- forming first bond connections (26) between the chip contact pads (33) and landing pads (29) of the plurality of first leadfingers (23) with first bond wires (26),
- forming second bond connections (27) between the chip contact pads (33) and electrically conducting means (32; 41) of the plurality of second leadfingers (24) with second bond wires (27),
- forming third bond connections (56) between the semiconductor chips (54, 55) with third bond wires (56),
- encapsulating the semiconductor chips (54, 55), the first (26) second (27) and third (56) bond wires and inner ends of leadfingers (23, 24) in a plastic mould material (39).

29. Method to assemble a semiconductor package (20; 42; 50; 53; 57; 60) according to claim 27 or claim 28, characterised in that the first electrically conducting means (32) has an approximately rectangular longitudinal cross-section and is formed on the landing pad (29) of the second leadfinger
(24) approximately parallel to the length of the second leadfinger (24).

30. Method to assemble a semiconductor package (40; ) according to claim 27 or claim 28, characterised in that the first electrically conducting means (41) has an approximately rectangular longitudinal cross-section and is formed on the landing pad (29) of the second leadfinger (24) approximately orthogonal to the length of the second leadfinger (24).

31. Method to assemble a semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 27 or claim 28, characterised in that the first electrically conducting means (32; 41) is formed by a wedge-bonding technique or a ball-bonding technique.

32. Method to assemble a semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 27 or claim 28, characterised in that the landing pads (29) are formed by depositing a first layer (30) on the surface of the leadfingers (23, 24) and by depositing a second layer (31) on the first layer (30).

33. Method to assemble a semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 27 or claim 28, characterised in that the landing pads (29) are deposited using a selective electro-deposition technique.
34. Method to assemble a semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 27 or claim 28 characterised in that
the plurality of first bond wires (26) are attached to the chip contact pads (33) and the landing pads (29) of the plurality of first leadfingers (23) using a ball-bonding or a wedge-bonding or a stitch-bonding technique.

35. Method to assemble a semiconductor package (20; 40; 42; 50; 53; 57; 60) according to claim 27 or claim 28 characterised in that
the plurality of second bond wires (27) are attached to the chip contact pads (33) and first electrically conductive means (32; 41) of the plurality of second leadfingers (24) using a ball-bonding or a wedge-bonding or a stitch-bonding technique.

36. Method to assemble a semiconductor package (57) according to claim 27 or claim 28 characterised in that
at least one second electrically conducting means (58) is attached to at least one chip contact pad (33).

37. Method to assemble a semiconductor package (57) according to claim 36 characterised in that
the plurality of second electrically conductive means (58) is formed by a ball-bonding or a wedge-bonding technique.

38. Method to assemble a semiconductor package (57) according to claim 36 or claim 37 characterised in that
the second electrically conductive means (58) is electrically connected to the chip contact pad (33) and a bond wire (26, 27, 56).

39. Method to assemble a semiconductor package (60) according to claim 27 or claim 28 characterised in that the method further includes the step of depositing at least one grounding pad (62) on the die pad (22).

40. Method to assemble a semiconductor package (60) according to claim 39 characterised in that the grounding pads (62) are formed by depositing a first layer (63) on the surface of the die pad (22) and by depositing a second layer (64) on the first layer (63).

41. Method to assemble a semiconductor package (60) according to claim 39 or 40 characterised in that the grounding pads (62) are deposited using a selective electro-deposition technique.

42. Method to assemble a semiconductor package (60) according to one of claims 39 to claim 41 characterised in that the method includes the further steps of:
   - forming a grounding electrically conductive means (65) on a grounding pad (62),
   - forming bond connections (61) between contact pads (66) on the chip (21) and the grounding electrically conductive means (65).
43. Method to assemble a semiconductor package (60) according to claim 42
characterised in that
the grounding electrically conducting means (65) is formed by a wedge-bonding technique or a ball-bonding technique.

44. Method to assemble a semiconductor package (60) according to claim 42 or 43
characterised in that
the plurality of grounding bond wires (61) are attached to the chip contact pads (66) and the grounding electrically conductive means (65) using a ball-bonding or a wedge-bonding or a stitch-bonding technique.

45. Method to assemble a semiconductor package (53; 57) according to claim 28
characterised in that
at least one power semiconductor chip (55) and at least one logic semiconductor chip (54) are attached to the die pad (22).

46. Method to assemble a semiconductor package (53; 57) according to claim 45
characterised in that
at least one power chip (55) electrically connected to the first leadfingers (23) of the lead frame (25) by a plurality of first bond wires (26) and at least one logic chip (54) is electrically connected to the first electrical means (32; 41) of the second leadfingers (24) of the lead frame (25) by a plurality of second bond wires (27).
### A. CLASSIFICATION OF SUBJECT MATTER

**IPC 7**

H01L23/495

According to International Patent Classification (IPC) or to both national classification and IPC

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

**IPC 7**

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EP0-Internal, PAJ

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category *</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tbody>
<tr>
<td>X</td>
<td>DE 198 28 190 A1 (SIEMENS AG) 23 September 1999 (1999-09-23) column 1, line 20 - column 3, line 51; figure 3</td>
<td>1,6-8,11</td>
</tr>
<tr>
<td>A</td>
<td>EP 0 964 446 A (FORD MOTOR COMPANY) 15 December 1999 (1999-12-15) paragraphs [0005], [0006]; figures 2,3</td>
<td>1,3,6-8,11</td>
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---|---
26 April 2005 | 28.07.2005

Name and mailing address of the ISA

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<th>Category</th>
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<tr>
<td>A</td>
<td>&quot;METAL CHIP COMPONENT FOR WIREBONDING PAD&quot; IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 34, no. 5, 1 October 1991 (1991-10-01), pages 180-181, XP000189706 ISSN: 0018-8689 the whole document</td>
<td>1,3,6-8, 11</td>
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<tr>
<td>A</td>
<td>DWIGHT SCHWARZ ET AL: &quot;Leadframe attached composite rivet/weld button for electrical interconnect (Dwight Schwarz, Bill Mummert, Steve Baker)&quot; RESEARCH DISCLOSURE, KENNETH MASON PUBLICATIONS, HAMPSHIRE, GB, vol. 325, no. 71, May 1991 (1991-05), XP007116398 ISSN: 0374-4353 the whole document</td>
<td>1,3,6-8</td>
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<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
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INTERNATIONAL SEARCH REPORT

Box II  Observations where certain claims were found unsearchable (Continuation of Item 2 of first sheet)

This international Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. X Claims Nos.:  
   because they relate to subject matter not required to be searched by this Authority, namely:  
   see FURTHER INFORMATION sheet PCT/ISA/210

2. ☐ Claims Nos.:  
   because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:  
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III  Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

   see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. X No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

   1,3,6-8,11

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.
This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1,3,6-8,11

   The lead frame has a recessed die bonding pad.

2. claims: 2,23-26

   Two chips are interconnected by a plurality of bond wires.

3. claims: 4,9,12

   The first electrically conducting means comprises wedges or balls.

4. claim: 5

   The first electrically conducting means has a rectangular longitudinal cross section.

5. claim: 10

   The material of the landing pad form an eutectic with the first bond wire and the material of the second bond wire form an eutectic with the first electrically conductive means.

6. claims: 13-16

   A second electrically conducting means is attached to at least one chip contact pad.

7. claims: 17-22

   A semiconductor package that includes a plurality of ground pads on the die pad.

8. claims: 27-46

   The landing pads are deposited and the first electrically conductive means is attached to the landing pads after chip mounting.
Continuation of Box II.1

The difference between "A first electrically conductive material" and "a second electrically conductive material" in claim 1 is not clear. It has been interpreted based on the description as being "A first electrically conductive material" and "a second electrically conductive material" being different from said first electrically conductive material.