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- (71) **Applicant:** ALCATEL-LUCENT USA INC. [US/US];  
600-700 Mountain Avenue, Murray Hill, NJ 07974-0636 (US).
- (72) **Inventors:** BROWN, Paul; 600 March Road, Ottawa,  
Ontario K2K 2E6 (CA). CHAN, Alex; 600 March Road,  
Ottawa, Ontario K2K 2E6 (CA).
- (74) **Agent:** SANTEMA, Steven, R.; Alcatel-Lucent USA Inc.,  
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Mountain Avenue, Murray Hill, NJ 07974-0636 (US).
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- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

[Continued on next page]

(54) **Title:** 0204 SHIFTED VIAS WITH MERGE PADS

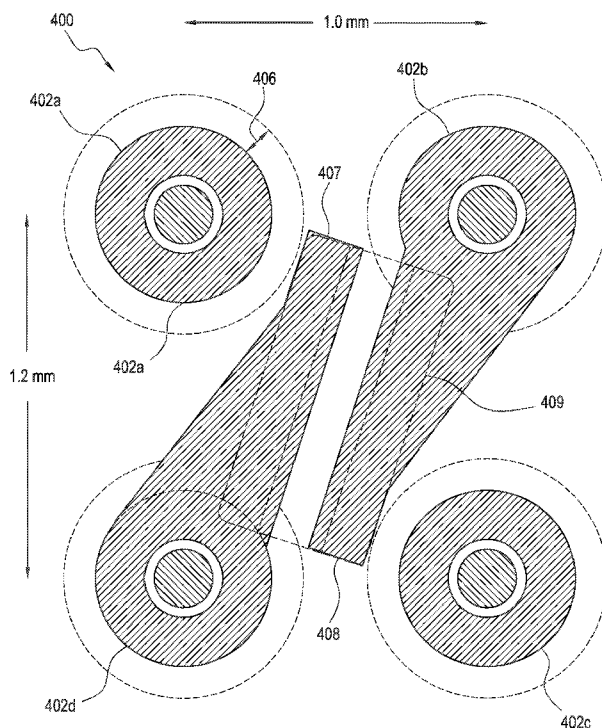


FIG. 4

(57) **Abstract:** A printed circuit board design for 0204 reverse geometry capacitor use between vias on a tight-pitch Ball Grid Array is disclosed. The printed circuit board design for 0204 reverse geometry capacitor use between vias on a tight-pitch Ball Grid Array provides component landing pads (407, 408) sized to accommodate an 0204 surface mount component within a 1.2 mm by 1.0 mm rectangular spacing. The printed circuit board design for 0204 reverse geometry capacitor use between vias on a tight-pitch Ball Grid Array is particularly useful for overcoming the problem of component placement on tight-pitch arrays known in the art.

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LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, **Published:**

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, — *with international search report (Art. 21(3))*  
GW, KM, ML, MR, NE, SN, TD, TG).

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**0204 SHIFTED VIAS WITH MERGE PADS****TECHNICAL FIELD**

The present invention relates to a printed circuit board pad design and is particularly concerned with providing component placement on very tight-pitch grid arrays.

**5 BACKGROUND**

High-speed electronic applications require the mounting of very small components, for example decoupling capacitors, on very tight-pitch grid arrays which are compatible with Ball Grid Array (BGA) components. Examples of very tight-pitch grids include 0.8 mm by 0.8 mm pitch and 1.0 mm by 1.0 mm pitch grids among others.

10 Power supply decoupling challenges are emerging from designs with operating frequencies of 300MHz or greater, integrated circuits with operating voltages below 3 volts and power demand of 15 watts or more. The higher operating frequencies, the ever shrinking lower and upper voltage limits given low operating voltages and the larger power demands all combine to demand higher performance from decoupling  
15 arrangements.

An ideal decoupling capacitor would transfer all its stored energy to a load instantly. A real capacitor has parasitics that prevent instantaneous transfer of a capacitor's stored energy. The actual operating nature of a capacitor can be modeled as an RLC  
20 equivalent circuit. For most purposes, it is possible to model the characteristics of an actual capacitor with the series combination of one capacitor, one resistor, and one inductor. The resistive, inductive, and capacitive values in this model are commonly referred to as equivalent-series-capacitance (ESC), equivalent-series-resistance (ESR), and equivalent-series-inductance (ESL).

25 The equivalent-series-inductance of a capacitor determines the speed of energy transfer to a load. The lower the ESL of an actual capacitor, the faster that energy can be transferred to a load. Historically, there has been a tradeoff between energy storage

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(capacitance) and inductance (speed of energy delivery) in a particular device. Low equivalent-series-inductance devices typically have low capacitance. Likewise, higher capacitance devices typically have higher ESLs. The equivalent-series-inductance of the capacitor has a further inductance added to it by the equivalent-series-inductance of the printed circuit board traces that connect the capacitor to the load -- typically an integrated circuit. This drives a design topology that places the fastest low ESL capacitors as close to the load as possible to minimize the total equivalent-series-inductance.

The key physical characteristic determining equivalent-series-inductance of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the resulting ESL. A standard surface mount capacitor is rectangular in shape with electrical terminations on its shorter sides. There now exists versions of surface mount capacitors known as Reverse Geometry Capacitors (RGCs) which have its terminations on the longer side of its rectangular shape.

Surface mount capacitors have a size characterized by a four digit number of the form "XXYY" wherein "XX" designates the length of one pair of sides, and "YY" designates the length of the other pair of sides which have electrical terminations; and wherein both lengths are in hundredths of an inch. By way of example, a "0402" capacitor would have nominal dimensions of 0.04" by 0.02" and the ends with length 0.02" would possess the solder terminals. Alternatively, a "0204" capacitor would have nominal dimensions of 0.02" by 0.04" and the ends with length 0.04" would possess the solder terminals. Referring to FIG. 1, there may be seen an example of a 0402 capacitor 100 having electrodes 102, and a 0204 capacitor 110 having electrodes 102.

When the distance between the electrodes on the chip capacitor is reduced, the size of the overall current loop is reduced. Since the size of the current loop is the primary driver of equivalent-series-inductance, a 0306 capacitor with a smaller current loop has significantly lower ESL than a 0603 capacitor. Manufacturer reports indicate that the reduction in equivalent-series-inductance varies by standard size increments of the chip

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capacitors; however, ESL is typically reduced 60% or more with a Reverse Geometry Capacitor versus a standard chip capacitor.

Therefore, it would be desirable to provide a method of placing Reverse Geometry components, including capacitors, within tight-pitch BGAs.

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## SUMMARY

A brief summary of various exemplary embodiments is presented below. Some simplifications and omissions may be made in the following summary, which is intended to highlight and introduce some aspects of the various exemplary  
10       embodiments, but not to limit the scope of the invention. Detailed descriptions of a preferred exemplary embodiment adequate to allow those of ordinary skill in the art to make and use the inventive concepts will follow in later sections.

According to an aspect of the invention there is provided a printed circuit board (PCB) having: a ball grid array (BGA) of BGA pads on one side of the PCB, arranged in a  
15       tight-pitch grid pattern; vias, including respective via pads, arranged in the grid pattern and at least one of the vias electrically connected to the BGA pads; a set of four of the vias spaced in a rectangular arrangement of dimensions 1.2 mm by 1.0 mm; two diagonally opposite of the set of vias having component landing pads; a solder mask covering the component landing pads with an opening; a solder pad within each the  
20       opening electrically connected to the component landing pad; and a two-lead component attached to the solder pad.

In some embodiments of this aspect of the invention the component landing pads accommodate an 0204 nominally dimensioned component. In some of these  
25       embodiments the component landing pads comprise a component landing pad of substantially rectangular shape, while in some of these embodiments the component landing pads further comprise a supplemental conductive area.

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In some embodiments of this aspect of the invention at least one the component landing pads has an edge angled at about  $70^\circ$  to a side of the rectangle defined by the four vias.

5 In yet other embodiments of this aspect of the invention the component landing pads accommodate a plurality of 0201 nominally dimensioned components.

According to another aspect of the invention there is provided a method of manufacturing a PCB wherein the PCB has a ball grid array (BGA) of BGA pads on one side of the PCB arranged in a grid pattern, and wherein on the opposite side of the PCB has vias, including respective via pads, arranged in the grid pattern with at least  
10 one of the vias electrically connected to the BGA pads; the method having the steps of: selecting an adjacent set of four of the vias spaced in a rectangular arrangement of dimensions 1.2 mm by 1.0 mm vias on the PCB, wherein two diagonally opposite of the set of vias having component landing pads; covering the component landing pads with a solder mask; removing areas from the solder masks; placing solder pads in the  
15 areas; and attaching a two-lead component to the two adjacent component pads using the solder pads.

In some embodiments of this aspect of the invention the component landing pads accommodate a 0204 nominally dimensioned component. In some of these  
20 embodiments the component landing pads comprise a component landing pad of substantially rectangular shape, while in some of these embodiments the component landing pads further comprise a supplemental conductive area.

In some embodiments of this aspect of the invention at least one of the component landing pads has an edge angled at about  $70^\circ$  to a side of the rectangle defined by the four vias.

25 In yet other embodiments of this aspect of the invention the component landing pads accommodate a plurality of 0201 nominally dimensioned components.

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According to yet another aspect of the invention there is provided a computer aided design tool implemented on a computing device for accommodating a two-lead component on a tight pitch ball grid array (BGA) wherein the PCB will have a ball grid array (BGA) of BGA pads on one side of the PCB arranged in a grid pattern, and  
5 wherein on the opposite side of the PCB will be vias, including respective via pads, arranged in the grid pattern with at least one of the vias electrically connected to the BGA pads having: a design tool mode configured to select an adjacent set of four of the vias spaced in a rectangular arrangement of dimensions 1.2 mm by 1.0 mm vias on the PCB; a design tool mode configured to identify a placement of component landing  
10 pads and shaped of component landing pads on two diagonally opposite vias of the rectangular arrangement; wherein the placement allows a two-lead 0204 component to connect to the component landing pads, and wherein the spacing between component landing pads and adjacent non-connected vias meets a pre-established requirement.

#### BRIEF DESCRIPTION OF THE DRAWINGS

15 In order to better understand various exemplary embodiments, reference is made to the accompanying drawings, wherein:

**FIG. 1** shows a top view of an exemplary 0402 surface mount capacitor and an exemplary 0204 reverse geometry surface mount capacitor;

20 **FIG. 2** shows a bottom view of portions of a fine-pitch circuit board having different grid spacings according to embodiments of the invention;

**FIG. 3** shows a bottom view of a portion of a fine-pitch circuit board having according to an embodiment of the invention;

**FIG. 4** shows alternative component mounting according to another embodiment of the invention; and

25 **FIG. 5** shows a bottom view of a portion of a fine-pitch circuit board according to an embodiment of the invention following the details previously described in FIG. 3.

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To facilitate understanding, identical reference numerals have been used to designate elements having substantially the same or similar structure and/or substantially the same or similar function.

#### DETAILED DESCRIPTION

5       The following description and drawings merely illustrate the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the principles of the invention and are included within its scope. Furthermore, all examples recited herein are principally intended expressly to be only for pedagogical  
10       purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Additionally, the term, "or," as used herein, refers to a non-exclusive or (i.e., and/or), unless otherwise indicated (e.g., "or else" or "or in the alternative"). Also, the various  
15       embodiments described herein are not necessarily mutually exclusive, as some embodiments may be combined with one or more other embodiments to form new embodiments.

Referring now to the drawings, in which like numerals refer to like components or steps, there are disclosed broad aspects of various exemplary embodiments.

20       **FIG. 1** shows a top view of an exemplary 0402 surface mount capacitor **100** having electrodes **102a** and **102b** and an exemplary 0204 reverse geometry surface mount capacitor **112** having electrodes **112a** and **112b** both having nominal physical dimensions illustrated. Also shown for reference is an exemplary 0201 surface mount capacitor **120** having electrodes **122a** and **122b** along with its nominal physical  
25       dimensions.

**FIG. 2** shows bottom views of a portion of a fine-pitch circuit board according to embodiments of the invention. Circuit board portion **220** depicts a portion of a grid of vias on a circuit board which contains a standard ball grid array (BGA) of BGA

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pads on the top side (not shown) and a set of vias **221** also arranged on a grid spaced which is offset from the BGA pad grid, such that they do not overlap the BGA pads. The vias **221** are spaced on a grid spacing of 0.8 mm. Circuit board portion **230** depicts a similar portion of a grid of vias on a circuit board wherein one of the rows of vias has been displaced to effect a 1.2 mm row spacing, and one of the columns has been displaced to effect a 1.0 mm column spacing. The two displacements provide a set of vias defining a rectangular area of 1.2 mm by 1.0 mm which will allow placement of a 0204 component as will be described below in an embodiment of the invention.

Referring now to circuit board portion **240** there may be seen a portion of a grid of vias on a circuit board which contains a standard ball grid array (BGA) of BGA pads on the top side (not shown) and a set of vias **241** also arranged on a grid spaced which is offset from the BGA pad grid, such that they do not overlap the BGA pads. The vias **241** are spaced on a grid spacing of 1.0 mm. Circuit board portion **250** depicts a similar portion of a grid of vias on a circuit board wherein one of the rows of vias has been displaced to effect a 1.2 mm row spacing. This displacement also provides a set of vias defining a rectangular area of 1.2 mm by 1.0 mm which will allow placement of a 0204 component as will be described below in an embodiment of the invention.

**FIG. 3** shows a bottom view of a portion of a fine-pitch circuit board according to an embodiment of the invention. This includes a portion of a circuit board **300**, which contains a standard ball grid array (BGA) of BGA pads on the top side (not shown) and a set of vias also arranged on a grid spaced which is offset from the BGA pad grid, such that they do not overlap the BGA pads. The vias have pads **302** are which are labeled (**302a**, **302b**, **302c**, and **302d**), but other vias may be present outside of the rectangular area defined by these vias. In an exemplary embodiment BGA pads **302** form a rectangular spacing, meaning that vias pads **302a**, **302b**, **302c**, and **302d** are spaced 0.80 mm center-to-center apart in a square grid.

The standard structure of the vias includes via pad **302a** and via **304**, having via barrel **305**. Typically, via pad **302a** will be substantially circular in shape; and via **304** will be

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substantially circular in shape and have a radius of 0.25 mm. All dimensions may have a tolerance of  $\pm 10\%$ . Via barrel **305** has an outer radius to fit in via **304**. Via pad **302a** has an insulative offset distance **306** indicated by the dashed line surrounding the via pad. The other three vias **302b**, **302c**, and **302d** are of substantially the same construction with the addition of component pads to vias **302b** and **302d** as will be described below.

Further evident in **FIG. 3** is component pad **307** upon which a terminal of a surface-mount component may be soldered. Component pad **307** comprises via pad **307a**, component landing pad **307b**, and supplemental conductive area **307c**. Normally component pad **307** comprises a single conductive element. Via pad area **307a** operates as per normal for a via pad. Component landing pad **307b** provides an area for conductive attachment, typically via soldering, of an electrode of a surface mount component. Supplemental conductive area **307c** provides additional conductivity which acts to lower the equivalent series resistance to the electrode of the surface mount component. In some embodiments component landing pad **307b** is angled at  $70^\circ$  from the reference line connecting vias **302c** and **302d**. This angle has been found to be advantageous for maintaining adequate insulative spacings.

Further evident in **FIG. 3** is component pad **308** located at via **302b** which has dimensions and elements similar to component pad **307**. Component pads **307** and **308** are sized such that an 0204 surface mount component may be conductively attached between them. As well, component pads **307** and **308** are spaced apart sufficiently to provide the insulative standoff distance necessary for circuit operation. Prior to component mounting on component pads **307** and **308**, a solder resist film (not shown) is normally applied over the component pads to prevent inadvertent solder contact to other vias, the solder resist film having appropriately sized openings for allowing conductive mounting of the surface mount component to the component pads.

**FIG. 4** shows a bottom view of a portion of a fine-pitch circuit board according to an embodiment of the invention following the details previously described in **FIG. 3**.

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This includes a portion of a circuit board **400**, which contains a standard ball grid array (BGA) of BGA pads on the top side (not shown) and a set of vias also arranged on a grid spaced which is offset from the BGA pad grid, such that they do not overlap the BGA pads. The vias have pads **402** are which are labeled (**402a**, **402b**, **402c**, and **402d**), but other vias may be present outside of the rectangular area defined by these vias. Also evident in **FIG. 4** are component pads **407** and **408** upon which a terminal of a surface-mount component may be soldered. Further evident in **FIG. 4** in an exemplary embodiment, is a two-terminal surface mount component depicted by outline **409** is a two-lead 0204 component, having a length of 0.002 inches and a width of 0.004 inches. In the embodiment the two-terminal surface mount component is a discrete component. In general, this component is a reverse geometry capacitor that can be used for decoupling. In some applications other component types, such as resistors or inductors may be so placed.

Referring now to **FIG. 5** there may be seen a bottom view of a portion of a fine-pitch circuit board according to an embodiment of the invention following the details previously described in **FIG. 3**. This includes a portion of a circuit board **500**, which contains a standard ball grid array (BGA) of BGA pads on the top side (not shown) and a set of vias also arranged on a grid spaced which is offset from the BGA pad grid, such that they do not overlap the BGA pads. The vias have pads **502** are which are labeled (**502a**, **502b**, **502c**, and **502d**), but other vias may be present outside of the rectangular area defined by these vias. Also evident in **FIG. 5** are component pads **507** and **508** upon which a terminal of a surface-mount component may be soldered. Further evident in **FIG. 5** in an exemplary embodiment, is a set of two-terminal surface mount components depicted by outlines **509a**, **509b**, and **509c**. These components are two-lead 0201 components, having a length of 0.002 inches and a width of 0.001 inches. In the embodiment the two-terminal surface mount components are discrete components. In general, these components are a capacitor that can be used for decoupling. In some applications other component types, such as resistors or inductors may be so placed.

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In an exemplary embodiment, a computer aided design tool allows the selection of vias and arrangement of the solder mask, component pads, and vias to be substantially automated. The computer aided design tool may automatically identify appropriate spacing and shape of the solder pad so as to allow placement of the surface mount components on the printed circuit board. A computer aided design tool may also provide instructions to control a machine to manufacture the modified circuit board. Instructions may be exported to the machine or the design tool may directly control the machine.

Thus what has been disclosed is a method a method of placing Reverse Geometry components, including capacitors, within tight-pitch BGAs as well as a method for placing a series of smaller regular geometry surface mount components.

While the figures and descriptions may depict regular circular or rectangular shapes of different elements in exemplary embodiments, it should be understood that alternative shapes may be used such as imperfect polygons and rounded forms. These alternative shapes may be substantially similar to the depicted shapes in area and outline.

Although the various exemplary embodiments have been described in detail with particular reference to certain exemplary aspects thereof, it should be understood that the invention is capable of other embodiments and its details are capable of modifications in various obvious respects. As is readily apparent to those skilled in the art, variations and modifications can be effected while remaining within the spirit and scope of the invention. Accordingly, the foregoing disclosure, description, and figures are for illustrative purposes only and do not in any way limit the invention, which is defined only by the claims.

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What is claimed is:

1. A printed circuit board (PCB) comprising:
  - a ball grid array (BGA) of BGA pads on one side of the PCB, arranged in a tight-pitch grid pattern;
  - vias, including respective via pads, arranged in said grid pattern and at least one of said vias electrically connected to said BGA pads;
  - a set of four of said vias spaced in a rectangular arrangement of dimensions 1.2 mm by 1.0 mm;
  - two diagonally opposite of said set of vias having component landing pads;
  - a solder mask covering the component landing pads with an opening;
  - a solder pad within each said opening electrically connected to said component landing pad; and
  - a two-lead component attached to said solder pad.
2. The PCB of claim 1, wherein
  - said component landing pads accommodate one of a 0204 and 0201 nominally dimensioned component.
3. The PCB of any of claims 1 and 2, wherein
  - at least one said component landing pads has an edge angled at about 70° to a side of the rectangle defined by the four vias.
4. The PCB of any of claims 1 to 3, wherein
  - said component landing pads comprise a component landing pad of substantially rectangular shape.
5. The PCB of claim 4, wherein
  - said component landing pads further comprise a supplemental conductive area.
6. A method of manufacturing a PCB wherein the PCB has a ball grid array (BGA) of BGA pads on one side of the PCB arranged in a grid pattern, and wherein on the opposite side of the PCB

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has vias, including respective via pads, arranged in said grid pattern with at least one of said vias electrically connected to said BGA pads; the method comprising the steps of:  
selecting an adjacent set of four of said vias spaced in a rectangular arrangement of dimensions 1.2 mm by 1.0 mm vias on said PCB, wherein two diagonally opposite of said set of vias having component landing pads;

covering said component landing pads with a solder mask;

removing areas from said solder masks;

placing solder pads in said areas; and

attaching a two-lead component to said two adjacent component pads using said solder pads.

7. The method of claim 6, wherein  
said component landing pads accommodate one of a 0204 and 0201 nominally dimensioned component.
8. The method of any of claims 6 and 7, wherein  
at least one said component landing pads has an edge angled at about 70° to a side of the rectangle defined by the four vias.
9. The method of any of claims 6 to 8, wherein  
said component landing pads comprise a component landing pad of substantially rectangular shape.
10. The method of claim 9, wherein  
said component landing pads further comprise a supplemental conductive area.

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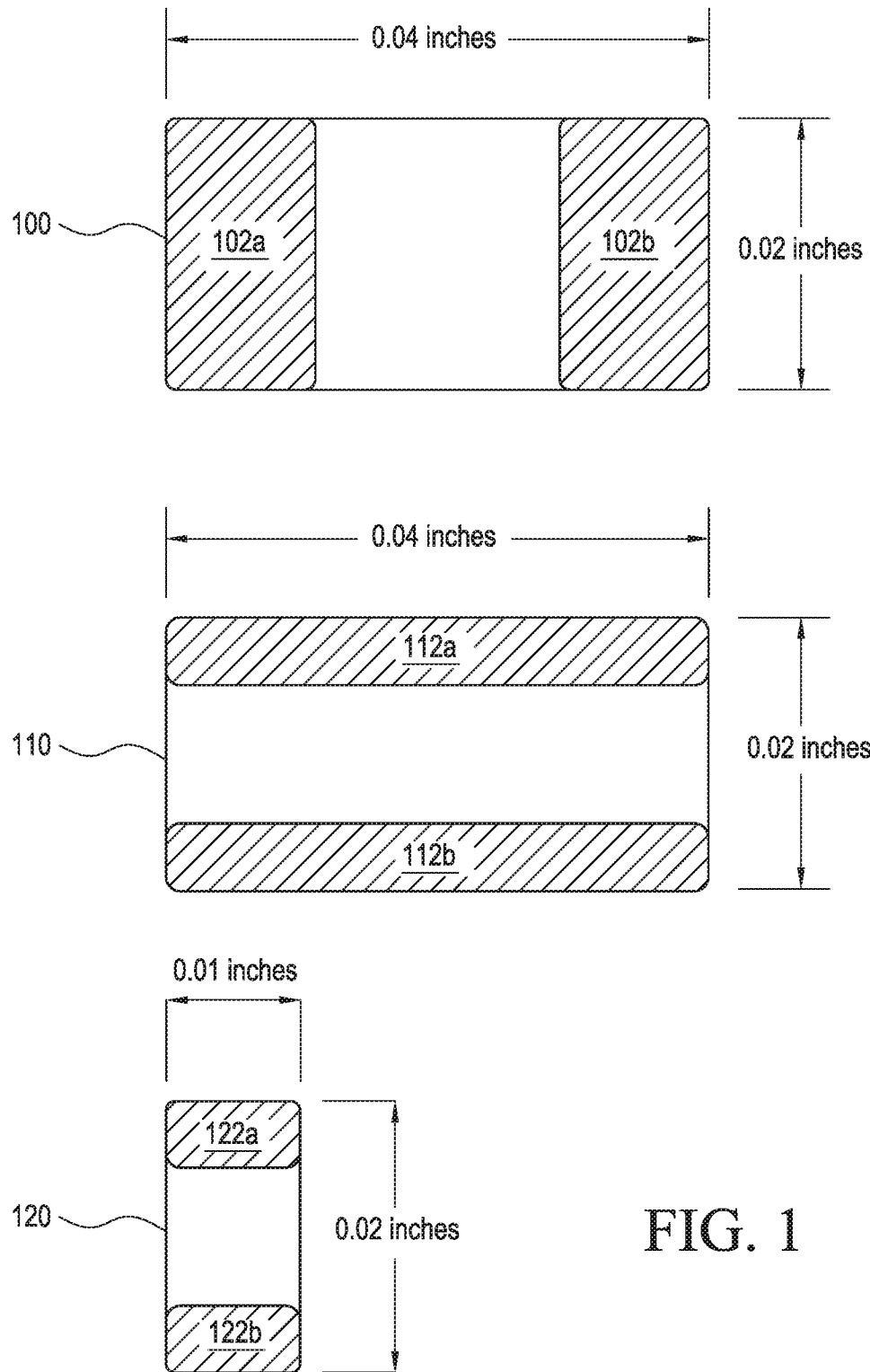


FIG. 1

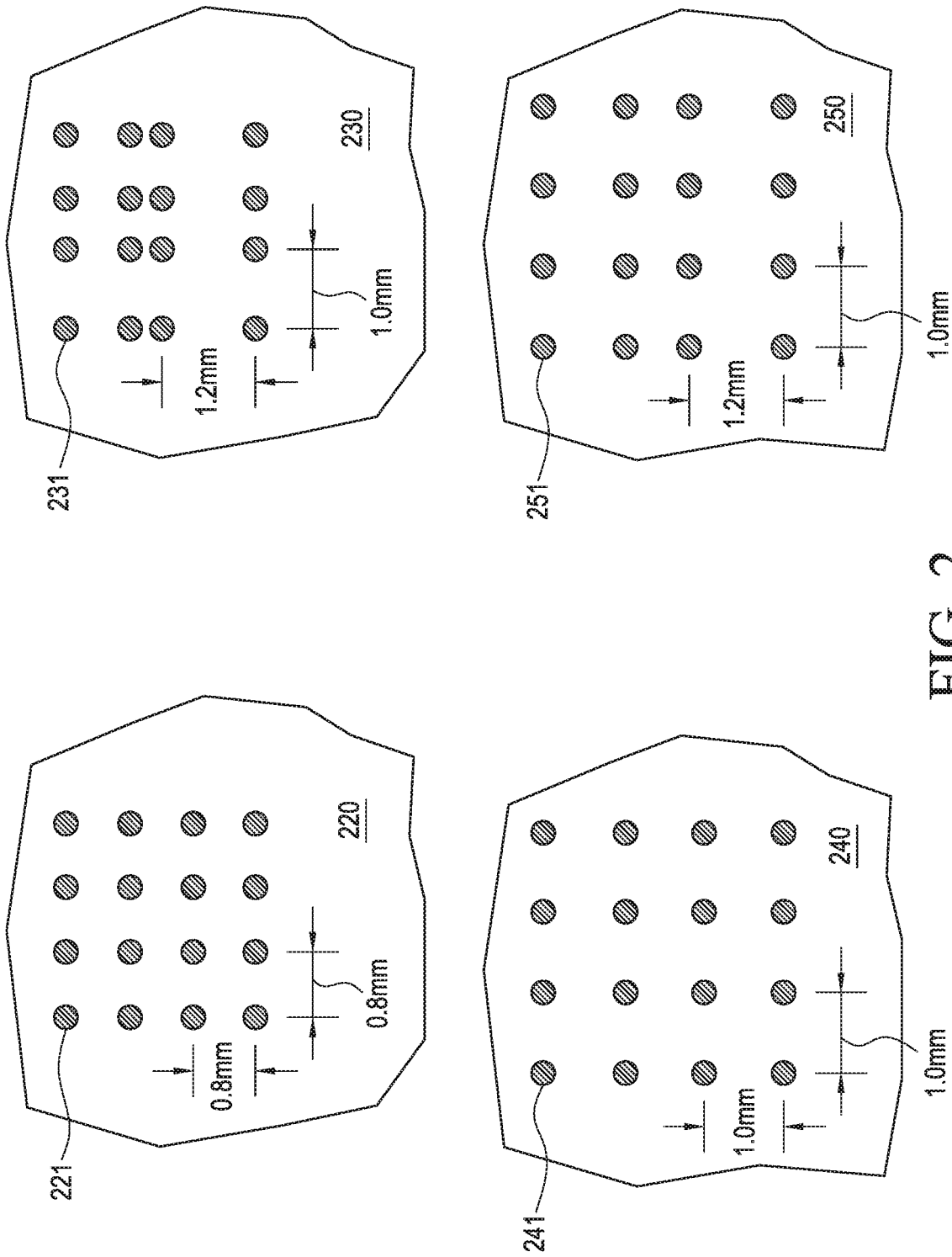


FIG. 2

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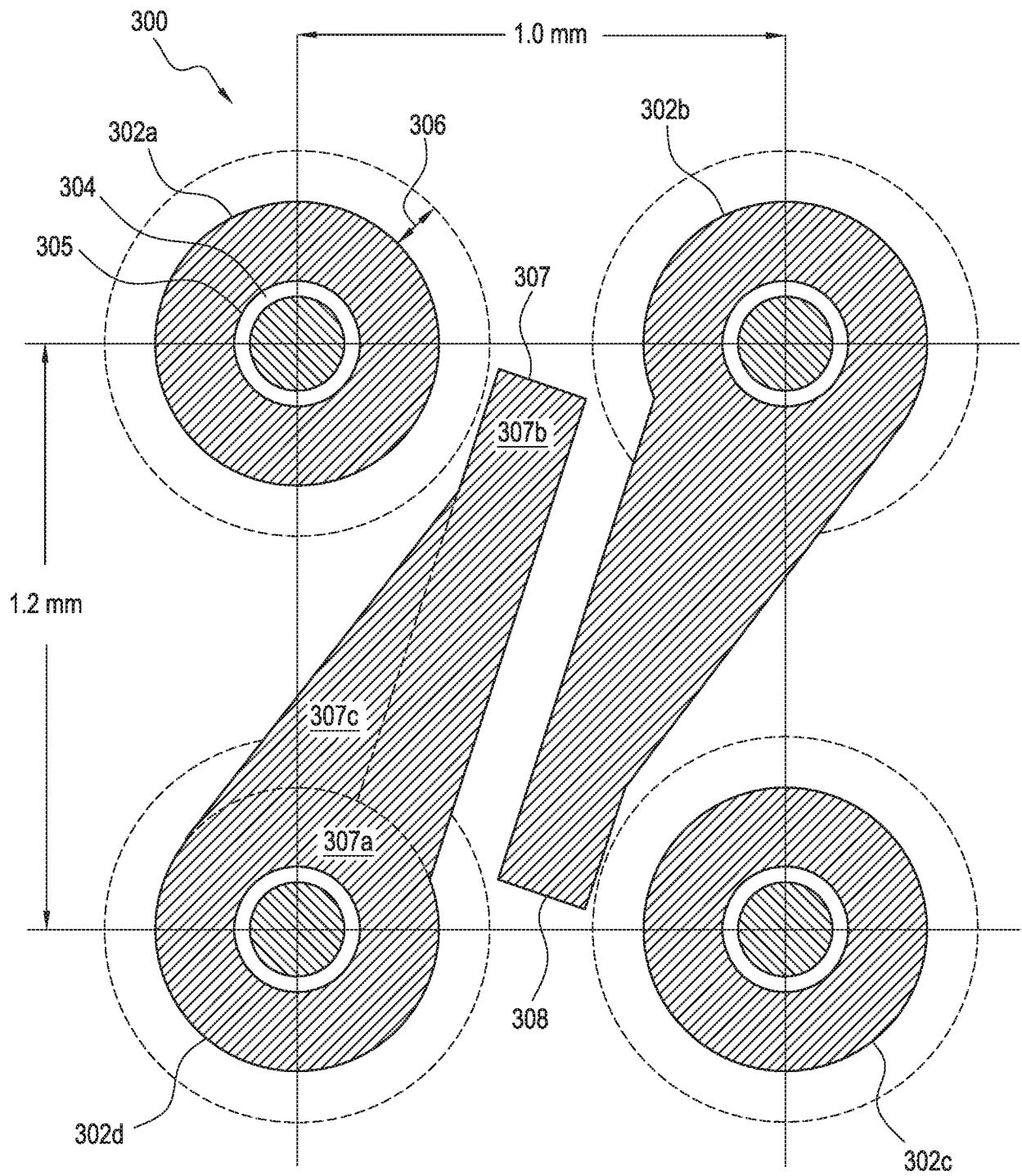


FIG. 3

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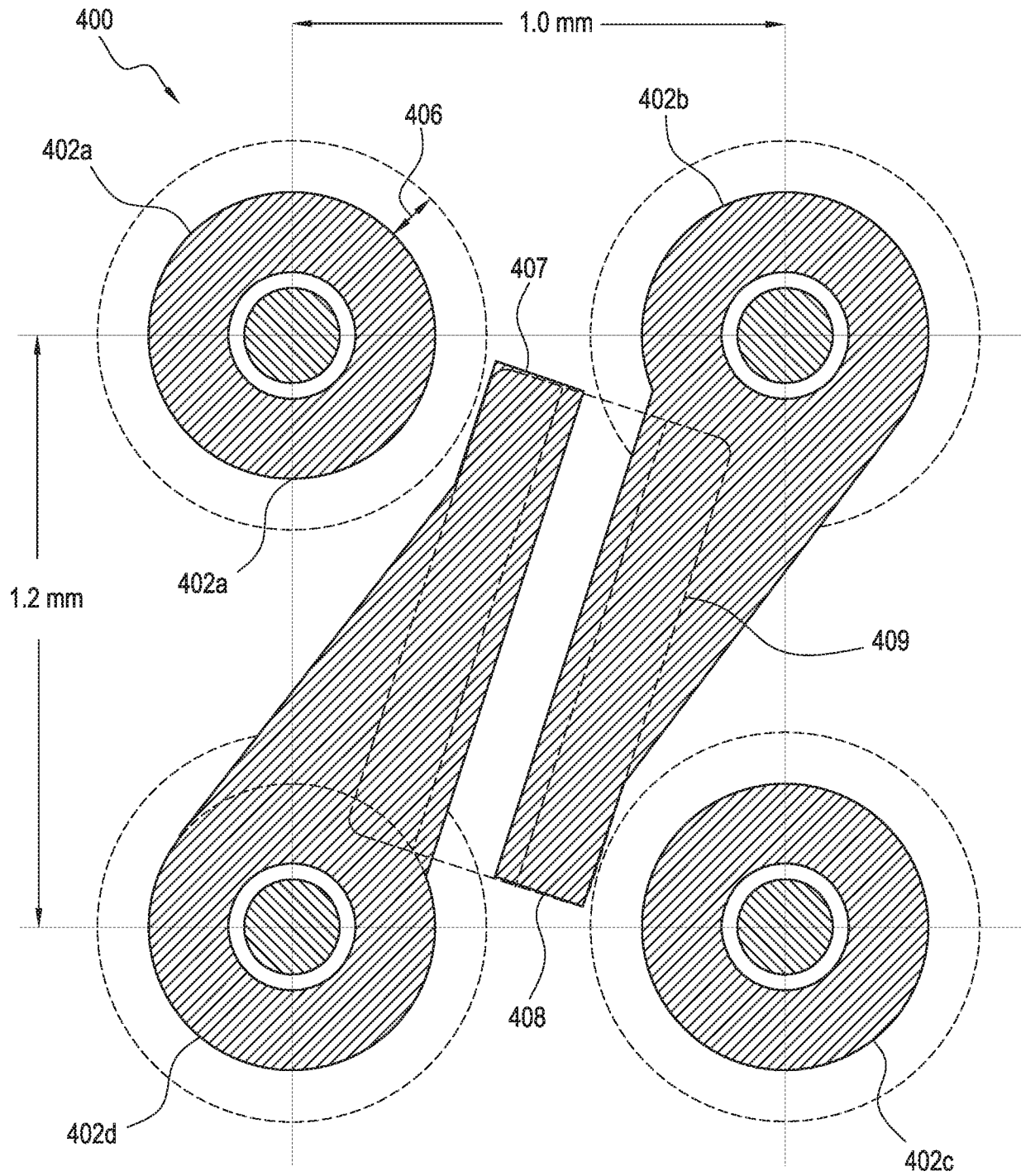


FIG. 4

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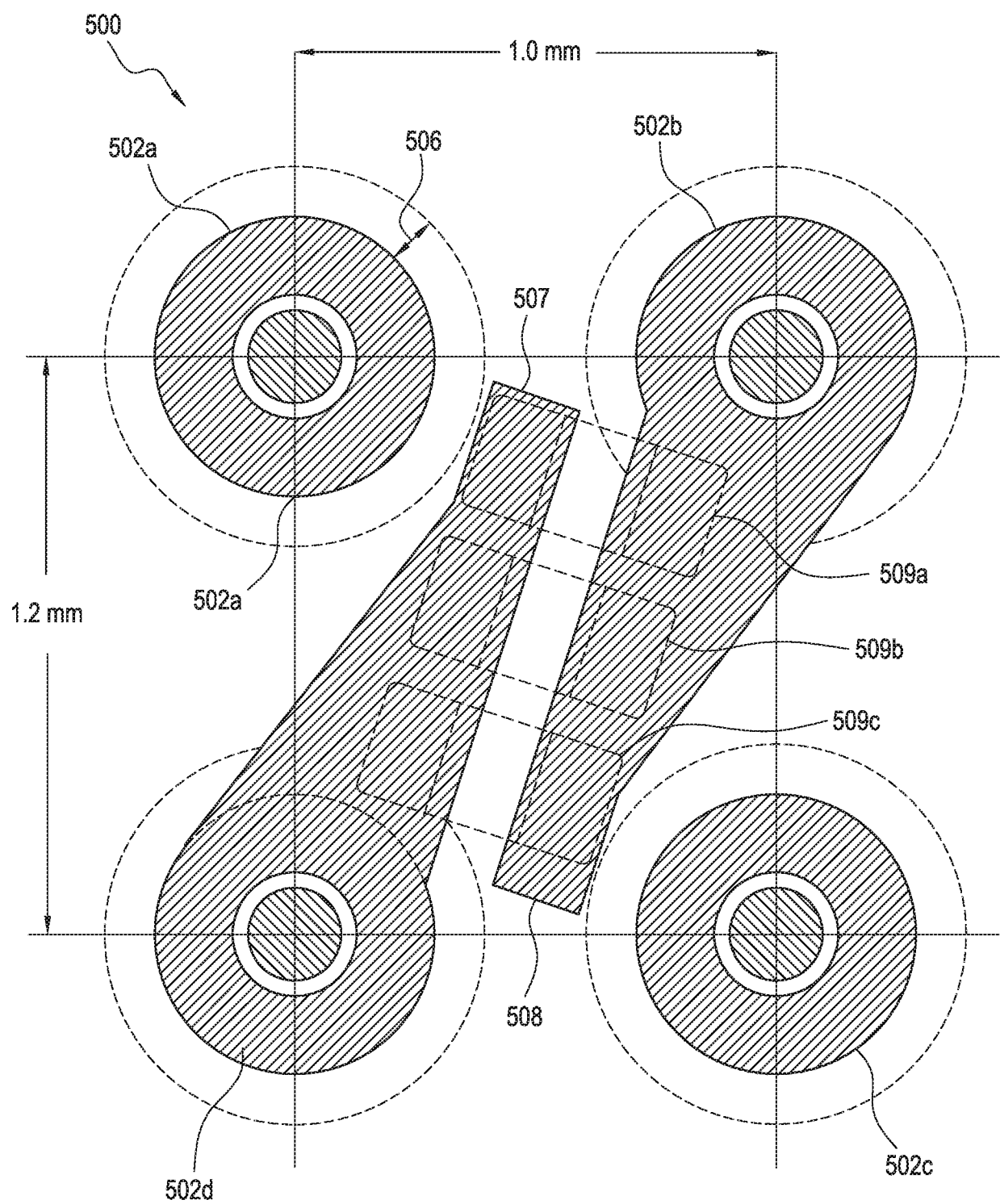


FIG. 5

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2017/013606

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H05K1/11  
ADD. H05K1/02

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                            | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2012/168216 A1 (CHAN ALEX [CA] ET AL)<br>5 July 2012 (2012-07-05)<br>paragraphs [0020] - [0037]; figures 1-4<br>-----                                      | 1-10                  |
| X         | US 2013/100624 A1 (CARPENTER DAVID G [US]<br>ET AL) 25 April 2013 (2013-04-25)<br>paragraphs [0011], [0012], [0014] -<br>[0017], [0019]; figures 1-3<br>----- | 1-10                  |
| A         | US 2013/062762 A1 (CHAN ALEX [CA] ET AL)<br>14 March 2013 (2013-03-14)<br>paragraphs [0024] - [0027]; figures<br>-----                                        | 1-10                  |
| A         | US 2015/213957 A1 (CHOI YOUNG DON [KR] ET<br>AL) 30 July 2015 (2015-07-30)<br>paragraphs [0084] - [0086], [0129] -<br>[0131]; figure 10<br>-----              | 1-10                  |

☐

Further documents are listed in the continuation of Box C.

☒

See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

24 March 2017

Date of mailing of the international search report

11/04/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Batev, Petio

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/013606

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                | Publication<br>date                                  |
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