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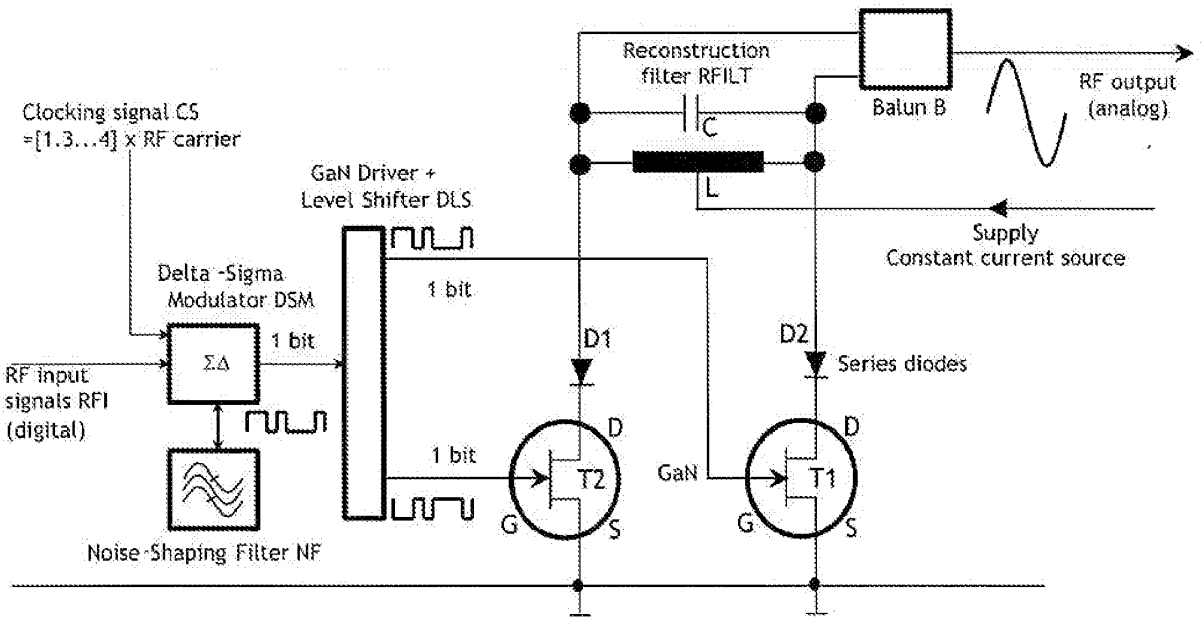
(54) **A method for signal amplification, a current switched power amplifier system, a base station, a mobile station and a communication network therefor**

(57) The invention concerns a method for signal amplification using a current, switched power amplifier system comprising at least two transistors (T1, T2), whereby at least one of said at least two transistors (T1, T2) is shielded from reverse bias between drain (D) and source (S) by means of at least one diode (D1, D2) that is in series with said at least one of said at least two transistors (T1, T2), a base station, a mobile station and a communication network therefor.

Fig. 2



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Description

[0001] The invention relates to a method for signal amplification according to the preamble of claim 1, a current switched power amplifier system according to the preamble of claim 4, a base station according to the preamble of claim 5, a mobile station according to the preamble of claim 6, and a communication network according to the preamble of claim 7.

[0002] Mobile communication, systems like e.g. Universal Mobile Telecommunications System (UMTS), Third Generation Partnership Project Long Term Evolution (3GPP LTE) or Worldwide Interoperability for Microwave Access (WIMAX) require power amplifiers with high output power at frequencies up to 3.8 GHz.

[0003] In the communication industry, there is always a pressure to reduce costs, especially Operational Expenditures (OPEX) and equipment costs (Capital Expenditures CAPEX), to be competitive. Therefore the industry is permanently searching for possibilities to reduce the cost for operation of equipment and of the goods sold. One means to reduce the costs for operation is to increase the power efficiency of the analogue hardware by changing the RF power amplifier architecture.

[0004] As an alternative to the currently used linear operation mode of e.g. A/AB or C class amplifiers, a new architecture may use so-called switched mode amplifiers, as e.g. class-S amplifiers, to improve the power efficiency. This new approach inherently leads to higher efficiency of the power amplifier of theoretically 100%, and by means of the digital approach reduces analogue imperfections and liability to errors.

[0005] Switched mode amplifiers, as e.g. class S amplifiers, are a preferred architecture, as digital power amplifiers fit the general direction of the architecture for software defined radio (SDR) and thus higher level of digitization of the transceiver, and as the switched mode amplifier architecture is the only architecture offering a 100% theoretical efficiency limit. A Class-AB amplifier architecture for instance can never have an efficiency better than 78% due to fundamental physical limitations. It is above all in the operator's interest to get as close as possible to the theoretical efficiency limit.

[0006] In said switched mode radio frequency (RF) power amplifiers, the transistor is not amplifying the input signal linearly, but is acting as a switch in the ideal case. As an ideal switch does not dissipate power, a theoretical power efficiency of 100% could be reachable.

[0007] With a switched mode power amplifier architecture relying on a current switched circuit topology, the switching transistors are part time operated with reverse bias between drain and source. This means that the transistor is operated in the third quadrant of the output current versus output voltage diagram, i.e. with a negative drain-source voltage More generally speaking when using e.g. a bipolar or a field-effect transistor (FET), the leadline of the transistor is no longer limited to the first quadrant of the current versus voltage diagram. With a class-AB, C, D, E, F power amplifier architecture this never happens, i.e. the problem is specific for the switched mode power amplifier architecture. The problem is now that operation with reverse bias between drain and source, i.e. negative drain-source voltage and at the same time negative drain current of the transistor, is associated with losses hurting efficiency. Simulations have revealed an increase of efficiency by around 10% when avoiding operation with reverse bias between drain and source.

[0008] Without such operation with reverse bias between drain and source, energy is reduced leading to less OPEX for operators. Furthermore less effort for cooling the power amplifiers is required allowing for more dense packaging of power amplifiers. This results in a smaller form factor of the base station, which in turn results in less real estate needed. This means a further secondary reduction of OPEX.

[0009] Furthermore, operation with reverse bias between drain and source may also be a risk in terms of reliability for the transistor, as the voltage potential of the gate is no longer lower than that of the drain.

[0010] In the Master of Science Thesis from Anthony Lawrence Long, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106-9560 from May 2003, the basic principle of current switched mode class D power amplifier architecture is disclosed. This document is regarded as the closest prior art for the invention.

[0011] The object of the invention is thus to propose a method to avoid operation of switching transistors of a switched mode power amplifier architecture relying on a current switched circuit topology with reverse bias between drain and source. This object is achieved by a method for signal amplification according to the teaching of claim 1, a current switched power amplifier system according to the teaching of claim 4, a base station according to the teaching of claim 5, a mobile station according to the teaching of claim 6, and a communication network according to the teaching of claim 7.

[0012] The main idea of the invention, is to put diodes in series with the transistors of the current switched circuit topology. This shields the transistors from reverse, bias between drain and source and thus a steering of the leadline into the third quadrant of a drain-source current versus drain-source voltage diagram is avoided.

[0013] Further developments of the invention can be gathered from the dependent claims and the following description.

[0014] In the following the invention will be explained further making reference to the attached drawings.

[0015] Fig. 1 schematically shows a switched mode power amplifier architecture relying on a current switched circuit topology according to the state-of-the-art.

[0016] Fig. 2 schematically shows a switched mode-power amplifier architecture relying on a current switched circuit topology with diodes in series according to the invention.

[0017] Fig. 3. shows on the left side the loadlines in a output current versus output voltage diagram of a transistor in a switched mode power amplifier architecture relying on a current switched circuit topology according to the state-of-the-art, and on the right side the corresponding diagram of a transistor in a switched mode power amplifier architecture relying on a current switched circuit topology with a diode in series according to the invention.

[0018] A current switched power amplifier System according to the state-of-the-art as shown in fig.1 comprises a delta-sigma modulator DSM with inputs for reception of a digital or analogue RF input signal RFI and for reception of a clocking signal CS. An output of the delta-sigma modulator DSM is connected to an input-or a driver and level shifter DLS.

[0019] Preferably, the delta-sigma modulator DSM is connected to a noise-shaping filter NF.

[0020] A first output of the driver and level shifter DLS is connected to the gate of a first transistor T1, and a second output of the driver and level shifter DLS is connected to the gate of a second transistor T2.

[0021] Both the source of the first transistor T1 and the source of the second transistor T2 are connected to ground.

[0022] The drain of the first transistor T1 is connected to a first input of an inductor L and to a first input of a capacitor G, and the drain of the second transistor T2 is connected to a second input of the inductor L and to a second input of the capacitor C. The capacitor C and the inductor L build together a reconstruction filter RFILT. There are variants of the L-C filter topology which however are of no importance for the invention as disclosed.

[0023] The supply of a constant current source is connected to a third input of the inductor L.

[0024] Furthermore, the drain of the first transistor T1 is connected to a first input of a balun B, and the drain of the second transistor T2 is connected to a second input of the balun B. The balun B transforms a balanced input signal to a single ended signal. The balun's output the analogue RF output signal is provided.

[0025] Preferably, the driver and level shifter DLS or the transistors T1 and T2 are fabricated in Gallium Nitride (GaN) technology.

[0026] In a method for signal amplification using a current switched power amplifier system according to the state-of-the-art as shown in fig. 1, digital or analogue RF input signals are sent to the delta-sigma modulator DSM. Furthermore, clocking signals with a multiple of the RF carrier frequency are sent to the delta-sigma modulator DSM.

[0027] In the delta-sigma modulator DSM, the digital or analogue RF input signals are converted into digital 1-bit or higher resolution signals using a so-called sample-and-hold output. The sampling rate is determined by the received clocking signals. The digital 1-bit or multibit signals are provided at the output of the delta-sigma modulator DSM.

[0028] Preferably, the noise shaping filter NF is used to minimize quantization error by means of shifting quantisation noise into frequency ranges that are less or not relevant for signal proceasing.

[0029] Said digital 1-bit signals are sent to the driver and level shifter DLS that generates first driver signals based on the digital 1-bit signals and second driver signals based on the inverted digital 1-bit signals. The first driver signals are sent to the gate of the first transistor T1, and the second driver signals are sent to the gate of the second transistor T2, The output signals of the driver and level shifter DLS are thus in antiphase which means if the first transistor T1 is on, the second transistor T2 is off and vice versa. The described amplifier architecture with two transistors T1, T2 is just an example, and in alternative architectures, more than two transistors are used, which has however no influence on the invention. Such alternative architectures are e.g. multibit architectures, using two transistors more per each bit more,

[0030] In the first transistor T1 and in the second transistor T2, the first driver signals and the second driver signals respecare amplified resulting in first and a second amplifier signals.

[0031] The capacitor C and the inductor L together build a reconstruction filter RFILT used to generate smooth analogue signals out of the first and the second amplifier signals.

[0032] The smoothed first and second analogue signals are sent to the balun B, in which the smoothed first and second analogue signals are added together, thus removing any noise that has been picked up along the way. In other words, the balun B converts balanced signals to unbalanced signals. The unbalanced RF output signals are provided at the output of the balun B.

[0033] The left diagram in fig. 3 schematically shows the loadlines in a drain-sout-ce current I_{DS} versus drain-source voltage U_{DS} diagram of a transistor in a switched mode power amplifier architecture relying on a current switched circuit topology according to the state-of-the-art, Ideally, the drain-source current I_{DS} through the transistors T1, T2 in fig. 1 is rectangular, and the drain-source voltage U_{DS} is sinusoidal.

[0034] It can be seen, that the transistor is part time operated in the third quadrant of the drain-source current I_{DS} versus drain-source voltage U_{DS} diagram. This means the transistor is operated with a negative drain-source voltage. As already mentioned before, the problem of such an operation with reverse bias between drain and source, i.e. negative drain-source voltage and at the same time negative drain-source current, is associated with losses hurting efficiency. Furthermore, operation with reverse bias between drain and source may also be a risk in terms of reliability for the transistor, as e.g. in case of a FET transistor, the voltage potential of the gate no longer is lower than that of the drain.

[0035] According to the invention, in order to avoid operation of the transistors T1, T2 with reverse bias between drain and source, it is proposed to put diodes in

series with the transisters T1, T2 of the current switched circuit topology as depicted in fig.1. In case of e.g. FET transistors, these are shielded from negative drain-source voltage U_{DS} and thus a steering of the loadline into the third quadrant of the drain-source current I_{DS} versus drain-source voltage U_{DS} diagram is avoided.

[0036] A respective current switched power amplifier system according to the invention is shown in fig. 2.

[0037] Said current switched power amplifier system according to the invention is basically identical in construction to the current switched power amplifier system according to the state-of-the-art as shown in fig. 1 with the difference that a diode D1, D2 is connected in series with the drain D of transistor T1 and transistor T2 respectively.

[0038] In the example depicted in fig. 2, it is assumed that the transistor T1 and transistor T2 are both Field Effect transistors (FET). However, the invention is not restricted to a specific class of transistors like FETs. It can be applied in an analogue way also for Bipolar npn or pnp, MISHFET or KISFET transistors and various other classes of transistors or tubes.

[0039] The n-doped part of the diode D1, D2 is connected to the drain D of transistor T1 and transistor T2 respectively, and the p-doped part of the diode D1, D2 is connected to the balun B.

[0040] If the diode is reverse biased, i.e. if the voltage potential is lower on the side of the diode that is connected to the balun B than on the side that is connected to the drain D of transistor T1 and transistor T2 respectively, operation of transistor T1 and transistor T2 respectively with negative drain-source voltage is avoided.

[0041] If prip-transistors are used instead of npn-transistors, the n-doped part of the diode D1, D2 is connected to the balun B, and the p-doped part of the diode D1, D2 is connected to the drain D of transistor T1 and transistor T2 respectively,

[0042] The right diagram in fig. 3 schematically shows the idealized loadlines in a drain-source current I_{DS} versus drain-source voltage U_{DS} diagram of a FETtransistor T1, T2 in a switched mode power amplifier architecture relying on a current switched circuit topology with a diode D1, D2 in series according to the invention.

[0043] It can be seen that the transistor T1, T2 is not operated in the third quadrant of the drain-source current I_{DS} versus drain-source voltage U_{DS} diagram which increases the efficiency of the transistor T1, T2 as already mentioned above.

[0044] Such a current switched power amplifier system according to the invention as described above can be comprised in a transmitter used for transmission in a base station or a mobile station that are part of a communication network.

Claims

1. A method for signal amplification using a current switched power amplifier system comprising at least two transistors (T1, T2), **characterized in, that** at least one of said at least two transistors (T1, T2) is shielded from reverse bias between drain (D) and source (S) by means of at least one diode (D1, D2) that is in series with said at least one of said at least two transistors (T1, T2).

2. A method according to claim 1, **characterized in, that**

- a digital signal is sent from a delta-sigma modulator (DSM) to a level shifter (DLS),
- the digital signal is sent from the level shifter (DLS) to the gate (G) of the first of said at least two transistors (T1) and the digital signal is inverted and sent from the level shifter (DLS) to the gate (G) of the second of said at least two transistors (T2).

3. A method according to claim 2, **characterized in, that**

- the digital signals are sent from the drains (D) of said at least two transistors (T1, T2) through a reconstruction filter (RFILT) resulting in smooth analogue signals,
- and said analogue signals are combined in a balun (B), resulting in an unbalanced analogue output signal.

4. A current switched power amplifier system comprising at least two transistors (T1, T2), **characterized in, that** at least one diode (D1, D2) is in series with at least one of said at least two transistors (T1, T2) shielding said at least one of said at least two transistors (T1, T2) from an operation with reverse bias between drain (D) and source (s).

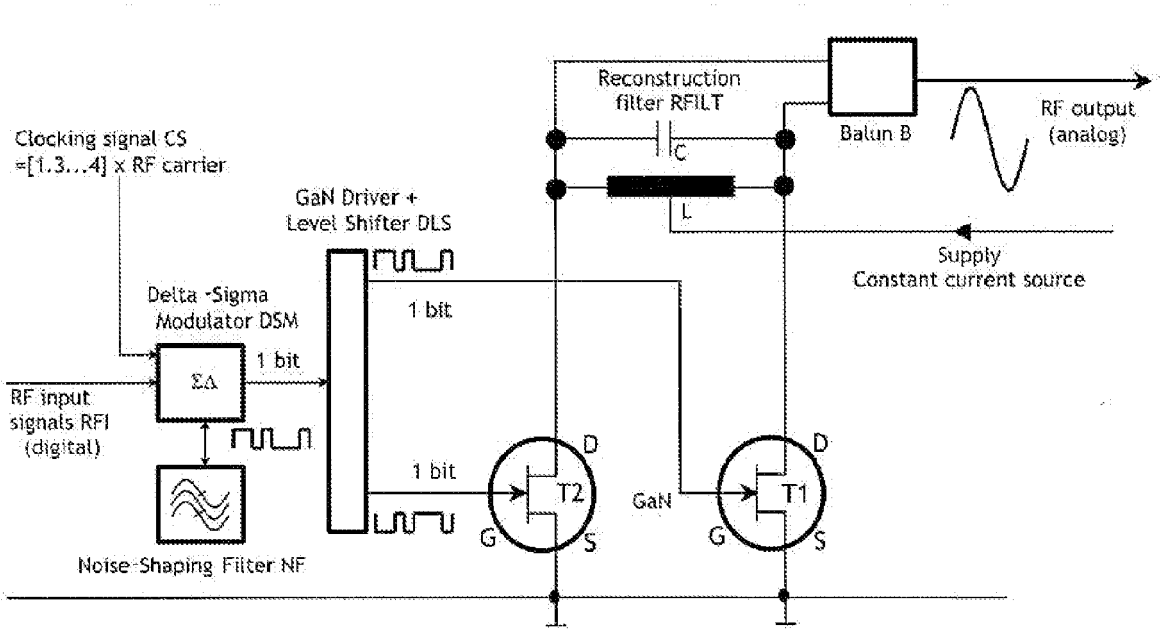
5. A base station comprising at least one current switched power amplifier system comprising at least two transistors (T1, T2), **characterized in, that** at least one diode (Dl, D2) is in series with at least one of said at least two transistors (T1, T2) shielding said at least one of said at least two transistors (T1, T2) from an operation with reverse bias between drain (D) and source (S).

6. A mobile station comprising at least one current switched power amplifier system comprising at least two transistors (T1, T2), **characterized in, that** at least one diode (D1, D2) is in series with at least one of said at least two transistors (T1, T2) shielding said at least one of said at least two transistors (T1, T2) from an operation with reverse bias between drain (D) and source (S).

7. A communication network with at least one base sta-

tion or mobile station comprising at least one current switched power amplifier system comprising at least two transistors (T1, T2), **characterized in, that** at least one diode (Dl, D2) is in series with at least one of said at least two transistors (T1, T2) shielding said at least one of said at least two transistors (T1, T2) from an operation with reverse bias between drain (D) and source (S).

Fig. 1



(prior art)

Fig. 2

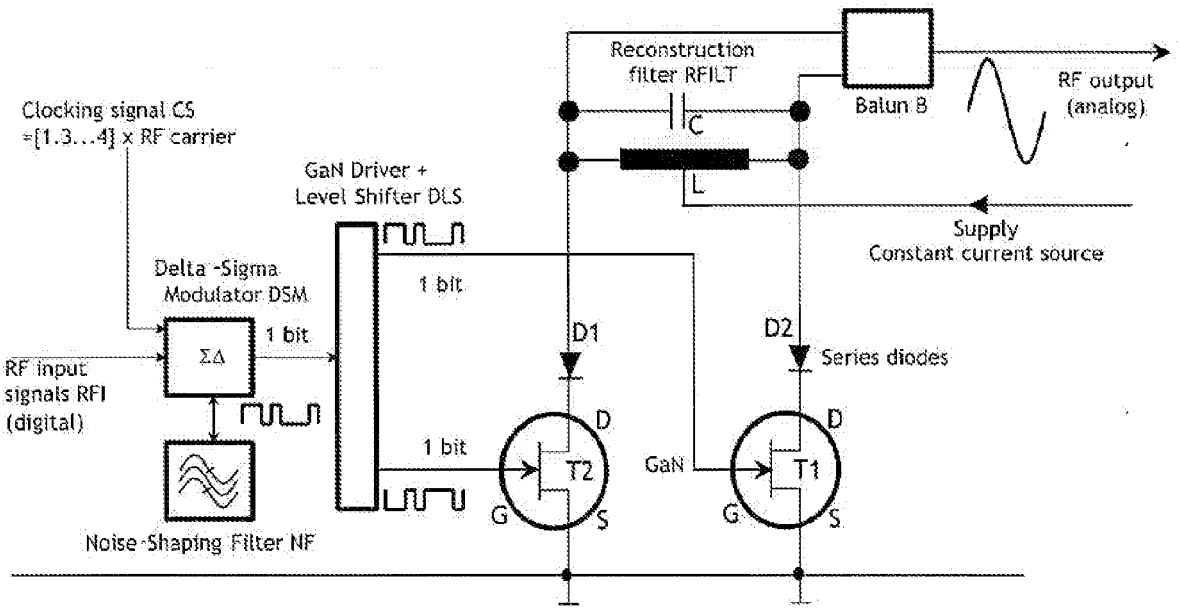
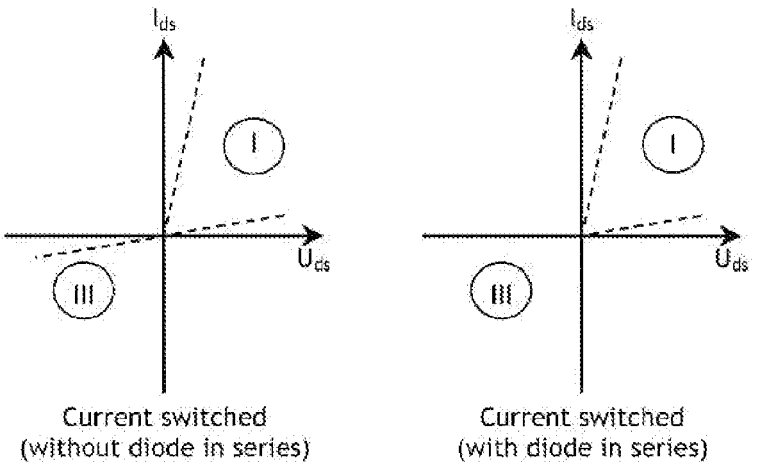

Reconstruction
filter RFILT
C
L
Balun B
RF output
(analog)
Clocking signal CS
=[1.3...4] x RF carrier
GaN Driver +
Level Shifter DLS
Supply
Constant current source
Delta -Sigma
Modulator DSM
1 bit
1 bit
D1
D2
Series diodes
RF input
signals RFI
(digital)
ΣΔ
1 bit
D
D
GaN
T2
T1
G
S
G
S
Noise-Shaping Filter NF

Fig. 3


I_{ds}
I
III
U_{ds}
Current switched
(without diode in series)
I_{ds}
I
III
U_{ds}
Current switched
(with diode in series)

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EUROPEAN SEARCH REPORT

Application Number
EP 07 12 3593

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	2 June 2008	Agerbaek, Thomas

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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EUROPEAN SEARCH REPORT

Application Number
EP 07 12 3593

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims

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Munich	2 June 2008	Agerbaek, Thomas

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