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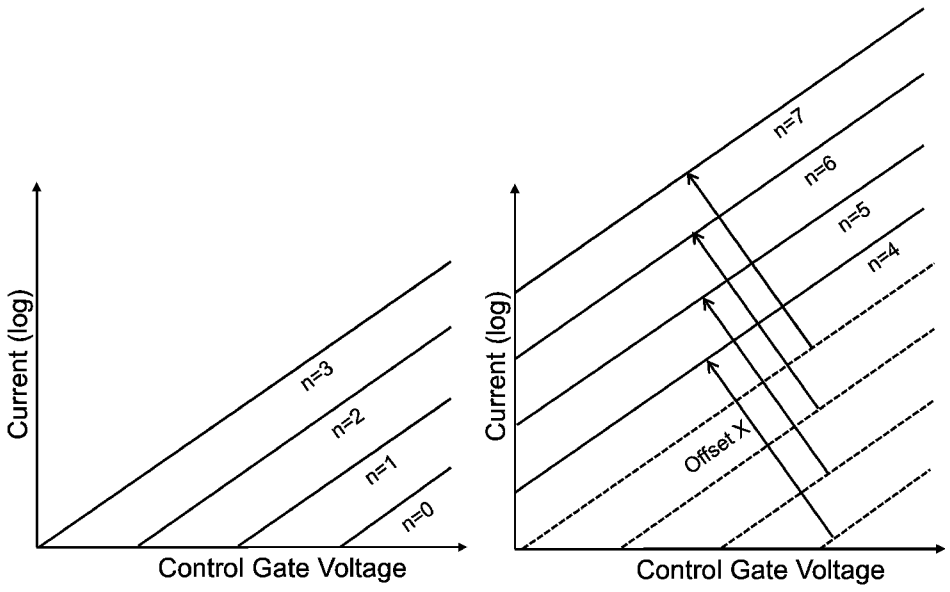

FIGURE 6A
Cell 1

FIGURE 6B
Cell 2

(57) Abstract: A method of reading a memory device having a plurality of memory cells by, and a device configured for, reading a first memory cell of the plurality of memory cells to generate a first read current, reading a second memory cell of the plurality of memory cells to generate a second read current, applying a first offset value to the second read current, and then combining the first and second read currents to form a third read current, and then determining a program state using the third read current. Alternately, a first voltage is generated from the first read current, a second voltage is generated from the second read current, whereby the offset value is applied to the second voltage, wherein the first and second voltages are combined to form a third voltage, and then the program state is determined using the third voltage.

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SYSTEM AND METHOD FOR STORING MULTIBIT DATA IN NON-VOLATILE MEMORY

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/581,489, filed November 3, 2017, and U.S. Patent Application No. 16/148,304, filed on October 1, 2018.

FIELD OF THE INVENTION

[0002] The present invention relates to non-volatile memory devices, and more particularly to increasing the number of bits that can be stored therein.

BACKGROUND OF THE INVENTION

[0003] Non-volatile memory devices are well known in the art. For example, a split-gate memory cell is disclosed in U.S. Patent 5,029,130. This memory cell has a floating gate and a control gate disposed over and controlling the conductivity of a channel region of the substrate extending between source and drain regions. Various combinations of voltages are applied to the control gate, source and drain to program the memory cell (by injecting electrons onto the floating gate), to erase the memory cell (by removing electrons from the floating gate), and to read the memory cell (by measuring or detecting the conductivity of the channel region to determine the programming state of the floating gate).

[0004] The configuration and number of gates in non-volatile memory cells can vary. For example, U.S. Patent 7,315,056 discloses a memory cell that additionally includes a program/erase gate over the source region. U.S. Patent 7,868,375 discloses a memory cell that additionally includes an erase gate over the source region and a coupling gate over the floating gate.

[0005] Fig. 1 illustrates a split gate memory cell 10 with spaced apart source and drain regions 14/16 formed in a silicon semiconductor substrate 12. A channel region 18 of the substrate is defined between the source/drain regions 14/16. A floating gate 20 is disposed over and insulated from a first portion of the channel region 18 (and partially over and

insulated from the source region 14). A control gate (also referred to as a word line gate or select gate) 22 has a lower portion disposed over and insulated from a second portion of the channel region 18, and an upper portion that extends up and over the floating gate 20 (i.e., the control gate 22 wraps around an upper edge of the floating gate 20).

[0006] Memory cell 10 can be erased by placing a high positive voltage on the control gate 22, and a reference potential on the source and drain regions 14/16. The high voltage drop between the floating gate 20 and control gate 22 will cause electrons on the floating gate 20 to tunnel from the floating gate 20, through the intervening insulation, to the control gate 22 by the well-known Fowler-Nordheim tunneling mechanism (leaving the floating gate 20 more positively charged – the erased state). Memory cell 10 can be programmed by applying a ground potential to drain region 16, a positive voltage on source region 14, and a positive voltage on the control gate 22. Electrons will then flow from the drain region 16 toward the source region 14, with some electrons becoming accelerated and heated whereby they are injected onto the floating gate 20 (leaving the floating gate negatively charged – the programmed state). Memory cell 10 can be read by placing ground potential on the drain region 16, a positive voltage on the source region 14 and a positive voltage on the control gate 22 (turning on the channel region portion under the control gate 22). If the floating gate is more positively charged (erased), the positive voltage on the control gate will at least partially couple to the floating gate to turn on the channel region portion under the floating gate, and electrical current will flow from source region 14 to drain region 16 (i.e. the memory cell 10 is sensed to be in its erased "1" state based on sensed current flow). If the floating gate 20 is negatively charged (programmed), the coupled voltage from the control gate 22 will not overcome the negative charge of the floating gate, and the channel region under the floating gate is weakly turned on or turned off, thereby reducing or preventing any current flow (i.e., the memory cell 10 is sensed to be in its programmed "0" state based on sensed low or no current flow).

[0007] Fig. 2 illustrates an alternate split gate memory cell 30 with same elements as memory cell 10, but additionally with a program/erase (PE) gate 32 disposed over and insulated from the source region 14 (i.e. this is a three gate design). Memory cell 30 can be erased by placing a high voltage on the PE gate 32 to induce tunneling of electrons from the

floating gate 20 to the PE gate 32. Memory cell 30 can be programmed by placing positive voltages on the control gate 22, PE gate 32 and source region 14, and a current on drain region 16, to inject electrons from the current flowing through the channel region 18 onto floating gate 20. Memory cell 30 can be read by placing positive voltages on the control gate 22 and drain region 16, and sensing current flow.

[0008] Fig. 3 illustrates an alternate split gate memory cell 40 with same elements as memory cell 10, but additionally with an erase gate 42 disposed over and insulated from the source region 14, and a coupling gate 44 over and insulated from the floating gate 20. Memory cell 40 can be erased by placing a high voltage on the erase gate 42 (and optionally a negative voltage on the coupling gate 44) to induce tunneling of electrons from the floating gate 20 to the erase gate 42. Memory cell 40 can be programmed by placing positive voltages on the control gate 22, erase gate 42, coupling gate 44 and source region 14, and a current on drain region 16, to inject electrons from the current flowing through the channel region 18 onto floating gate 20. Memory cell 30 can be read by placing positive voltages on the control gate 22 and drain region 16 (and optionally on the erase gate 42 and/or the coupling gate 44), and sensing current flow.

[0009] For all the above referenced memory cells, voltages are applied in each of the program, erase and read operations to program the memory cells to a "0" state, erase the memory cells to a "1" state, and to read the memory cells to determine whether they are in the programmed state or the erased state. One drawback to such memory devices is that each memory cell can only store one bit of data (i.e., the cell has only two possible states). There is a need to program more than one bit of data in each memory cell. It is also known to operate the above described memory cells in an analog fashion so that the memory cell can store more than just two binary values (i.e., just one bit of information). For example, the memory cells can be operated below their threshold voltage, meaning that instead of fully programming or fully erasing the memory cells, they can be only partially programmed or partially erased, and operated in an analog fashion below the threshold voltage of the memory cell. It is also possible to program the memory cells to one of multiple program states above the threshold voltage too. However, if discrete programming states are desired,

it can be difficult to reliably program and read the memory cells because the read current values for the various states are so close together.

BRIEF SUMMARY OF THE INVENTION

[0010] The aforementioned problems and needs are addressed by a method of reading a memory device having a plurality of memory cells, by reading a first memory cell of the plurality of memory cells to generate a first read current, reading a second memory cell of the plurality of memory cells to generate a second read current, applying a first offset value to the second read current, and then combining the first and second read currents to form a third read current, and then determining a program state using the third read current.

[0011] A method of reading a memory device having a plurality of memory cells includes reading a first memory cell of the plurality of memory cells to generate a first read current, reading a second memory cell of the plurality of memory cells to generate a second read current, generating a first voltage from the first read current, generating a second voltage from the second read current, applying a first offset value to the second voltage, and then combining the first and second voltages to form a third voltage, and then determining a program state using the third voltage.

[0012] A memory device includes a semiconductor substrate, a plurality of memory cells formed on the semiconductor substrate, and circuitry formed on the semiconductor substrate and configured to read a first memory cell of the plurality of memory cells to generate a first read current, read a second memory cell of the plurality of memory cells to generate a second read current, apply a first offset value to the second read current, and then combine the first and second read currents to form a third read current, and then determine a program state using the third read current.

[0013] A memory device includes a semiconductor substrate, a plurality of memory cells formed on the semiconductor substrate, and circuitry formed on the semiconductor substrate and configured to read a first memory cell of the plurality of memory cells to generate a first read current, read a second memory cell of the plurality of memory cells to generate a second read current, generate a first voltage from the first read current, generate a second voltage

from the second read current, apply a first offset value to the second voltage, and then combine the first and second voltages to form a third voltage, and then determine a program state using the third voltage.

[0014] Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 is a side cross sectional view of a first conventional split gate non-volatile memory cell.

[0016] Fig. 2 is a side cross sectional view of a second conventional split gate non-volatile memory cell.

[0017] Fig. 3 is a side cross sectional view of a third conventional split gate non-volatile memory cell.

[0018] Fig. 4 is a graph illustrating the current versus voltage characteristics for eight program states of a non-volatile memory cell.

[0019] Figs. 5A-5B are graphs illustrating the current versus voltage characteristics for eight program states of two non-volatile memory cell.

[0020] Figs. 6A-6B are graphs illustrating the current versus voltage characteristics for eight program states of two non-volatile memory cells, with the program states of the second cell shifted relative to those of the first.

[0021] Figs. 6C is a graph illustrating collectively the current versus voltage characteristics for eight program states of two non-volatile memory cells.

[0022] Fig. 7 is a plan view of a memory device architecture.

[0023] Fig. 8 is a schematic diagram illustrating the layout of an array of the memory cells.

DETAILED DESCRIPTION OF THE INVENTION

[0024] The present invention is directed to non-volatile memory devices capable of storing more than one bit of information in each memory cell. This can be done by operating the memory cells above and/or below their threshold voltage. For example, instead of fully programming or fully erasing the memory cells, they can be only partially programmed or partially erased, and operated in an analog fashion. The following description focuses on memory cells operating below the threshold voltage of the memory cell. However, it equally applies to memory cells operated above the threshold voltage of the memory cell as well.

[0025] To best illustrate the present invention, the sub-threshold relationship between channel current as a function of control gate voltage is described. For any given programmed state of the memory cell, as the control gate voltage gradually increases, the channel current gradually rises. When plotted as a function of the log of channel current, this relationship is linear. Moreover, as the memory cell programming state is changed (e.g., as the number of electrons programmed onto the floating gate changes), the linear logarithmic relationship of current as a function of control gate voltage shifts up and down.

[0026] This relationship is illustrated in Fig. 4. The linear logarithmic relationship of current (through the channel region) as a function of control gate voltage is represented for multiple different program states. The program state n=0 represents the highest program state of the memory cell (i.e., the most electrons on the floating gate that still allows read current – programming beyond this point essentially turns the memory cell current off for all control gate voltages used to read the memory cells) and the program state n=7 represents the lowest program state of the memory cell (i.e., the least electrons on the floating gate, which corresponds to the highest erase state). The memory cell represented by Fig. 4 can theoretically store multiple bits of information, because it can be programmed into 8 different states. By measuring the current at one or more specific control gate voltages, such as read voltage V_R, the program state n can be determined.

[0027] One issue with a memory cell configured to store n program states as indicated in Fig. 4 is that the difference in read current for two adjacent program states can be too small (i.e., the program states are too close together) for reliable operation when the number of states n exceeds just a few. Program states too close together are susceptible to noise on the program and/or reading of the memory cells. For example, there would be a small range of

variation in terms of how reliably the memory cell can be programmed into any given program state. Similarly, there would be a small range of variation in terms of how reliably the state of the cell can be read by measuring the read currents. Therefore, the n states cannot be located too close to each other, otherwise they could not reliably be distinguished from each other. This places a practical limit on the number of states n that can be programmed into a single memory cell, which means there is a practical limit on the number of states n that can be stored in the memory device.

[0028] Figures 5A-5B illustrate a solution to the above described problem. Specifically, the different states n can be stored over multiple memory cells. For example, the 8 program states stored in a single memory cell of Fig. 4 can be stored in two different cells, the first four states (n=0 to n=3) can be stored in a first cell (Fig. 5A, cell 1), and the last four states (n=4 to n=7) can be stored in a second cell (Fig. 5B, cell 2). Using two cells, the same number of total states can be stored, but with twice the separation between adjacent program states for better reliability. Or, said another way, twice as many states can be stored with a given separation between adjacent program states using two memory cells relative to using just a single cell.

[0029] Splitting up program states over two (or more) cells as described above solves the program state separation issue, but creates another issue. Ideally, to simplify design configuration and operation, the read currents of both cells would be added together, and the combined read current is used to determine which of the 8 possible bits (corresponding to the one of 8 possible program states) is programmed into the pair of memory cells. However, as is evident from Figs. 5A-5B, different states in different cells have the same current/voltage characteristics. For example, state n=0 in cell 1 produces the same read current output as state n=4 in cell 2. The same is true for the other states (n=1 and n=5 produce the same read current, and so on). Therefore, even if one cell is fully programmed to be off when the read voltage VR is applied, there is no way to determine which state the read current applies to. For example, if the bit value corresponds to program state n=6, and cell 2 is programmed to n=6 and cell 1 is programmed to be off, when later reading back a combined read current from the two cells, it could not be determined if the combined read current corresponds with program state 6 or program state 2.

[0030] To overcome this issue, an offset X is applied to the read current from cell 2, so that the read current readings from cell 2 are effectively shifted above any of the possible current readings from cell 1. For example, the current levels for state 3 in cell 1 could be added to the read current of cell 2. Therefore, all the possible read currents for the four states in cell 1 would not overlap with any of the possible read currents for the four states in cell 2. This is represented in Figs. 6A-6B. Therefore, assuming the programming state of n=3 of cell 1 is the maximum program state for both cells (i.e., the read current shown for program state n=3 is the maximum read current for each memory cell), non-overlapping read currents exceeding that of programming state n=3 can be provided by cell 2 for all the possible program states of cell 2. The read currents for both cells for all the possible program states (n=0-3 for cell 1 and n=4-7 for cell 2) are collectively shown in Fig. 6C. This means that the program states of both cells can be uniquely determined using a single read voltage VR on the control gates after the two cell currents are added together, yet the program states are sufficiently separated because the read current for cell 2 is allowed to exceed the maximum read current that could otherwise be generated by the cell. For example, if the bit being stored in the pair of cells corresponds to program state n=6, then cell 2 is programmed to state n=6, and cell 1 is programmed to be off. Then during a read operation, the n=6 state can be read uniquely from any of the other states. Similarly, if the bit being stored in the pair of cells corresponds to program state n=1, then cell 1 is programmed to state n=1, and cell 2 is programmed to be off. Then during a read operation, the n=1 state can be read uniquely from any of the other states.

[0031] Implementing the offset X for cell 2 can be done using an adding circuit that adds a current offset X to the read current from cell 2 before the read current from cell 2 is added to the cell current from cell 1 (e.g., the adding circuit is part of the sense amplifier that is used to detect currents through the cells). Or, the adding circuit can add a voltage offset X to a voltage signal that is generated by the sense amplifier to reflect the current being detected through cell 2. In this case, it would be the voltages signals (corresponding to the detected current levels) that are added together before determining from the combined voltage signal which program state was read from the pair of memory cells. Or, a multiplier circuit can be as part of, or downstream of, the sense amplifier to multiply the current or voltage signal for

cell 2 before being added to the current/voltage signal for cell 1. The offset X, whether it be a voltage offset or a current offset, could be stored in a reference cell (i.e., a memory cell in the memory cell array dedicated for this purpose), so that the proper amount of offset is reliably applied to the voltage or current signal for cell 2 for that given die.

[0032] The architecture of an exemplary memory device is illustrated in Fig. 7. The memory device includes an array 50 of non-volatile memory cells, which can be segregated into two separate planes (Plane A 52a and Plane B 52b). The memory cells can be of the type shown in Figures 1-3, formed on a single chip, arranged in a plurality of rows and columns in the semiconductor substrate 12. Adjacent to the array of non-volatile memory cells are address decoders (e.g. XDEC 54 (row decoder), SLDRV 56, YMUX 58 (column decoder), HVDEC 60) and a bit line controller (BLINHCTL 62), which are used to decode addresses and supply the various voltages to the various memory cell gates and regions during read, program, and erase operations for selected memory cells. Column decoder 58 includes sense amplifiers for measuring the voltages or currents on the bit lines during a read operation. Controller 66 (containing control circuitry) controls the various device elements to implement each operation (program, erase, read) on target memory cells. Charge pump CHRGPMP 64 provides the various voltages used to read, program and erase the memory cells under the control of the controller 66. The offset X and signal adding can be implemented, for example, with circuitry in the controller 66. Alternately or additionally, the offset X and signal adding can be implemented with circuitry in the sense amplifier portion of the column decoder YMUX 58.

[0033] While the above described embodiment was illustrated in the context of two memory cells and 8 states n, different numbers of cells, total states n, and states n per memory cell can vary. The number of total bits, and therefore states, can be enlarged to any desired number simply by increasing the number of cells being used to store the n states. For example, if three cells are used, then a first offset is applied to the read current or voltage of the second cell, and a second (different) offset is applied to the read current or voltage of the third cell, so the program state read currents/voltages for all three cells do not overlap.

[0034] Fig. 8 shows the array configuration for the two-gate memory cells of Fig. 1, where the memory cells are arranged in rows and columns. This array configuration equally

applies to the memory cells of Figs. 2-3, whereby additional lines would be added for the additional gates. Word lines WL each connect to the control gates for one row of memory cells. Bit lines BL each connect to the drain regions for one column of memory cells. Source lines SL each connect to the source regions for one row of a pair of memory cells. Preferably, each of cells having their read currents or voltages added together are disposed in different columns so the read process is faster. Therefore, for the example above where two memory cells are used, cell 1 would be in column 1 connected to bit line BL0, and cell 2 would be in column 2 connected to bit line BL1. During a read operation, the read current for cell 1 is detected on bit line BL0 and the read current for cell 2 is detected on bit line BL1. Circuitry in the sense amplifiers or downstream from there will add the offset X to the read current on bit line BL1 (or the voltage corresponding thereto) and then add the read currents (or voltages) from both cells to each other and then determine from the combined read current/voltage what program state is programmed in the pair of memory cells.

[0035] It is to be understood that the present invention is not limited to the embodiment(s) described above and illustrated herein. For example, references to the present invention herein are not intended to limit the scope of any claim or claim term, but instead merely make reference to one or more features that may be covered by one or more claims. While the invention is described with respect to sub-threshold operation of the memory cells, it could be implemented in memory cells operated above threshold (in which case the logarithmic relationship between the current and the voltage may no longer apply). It should be noted that programming a cell to its highest program state shown in the figures actually involves an erase operation where the highest program state is a fully erased memory cell. Applying offset X is disclosed above by adding to (increasing) the value of the current or voltage by the amount X. However, applying offset X could include a negative offset, which can be achieved by subtracting from (decreasing) the value of the current or voltage by the amount X. Materials, processes and numerical examples described above are exemplary only, and should not be deemed to limit the claims. Further, as is apparent from the claims and specification, not all method steps need be performed in the exact order illustrated. Lastly, single layers of material could be formed as multiple layers of such or similar materials, and vice versa.

[0036] It should be noted that, as used herein, the terms "over" and "on" both inclusively include "directly on" (no intermediate materials, elements or space disposed therebetween) and "indirectly on" (intermediate materials, elements or space disposed therebetween). Likewise, the term "adjacent" includes "directly adjacent" (no intermediate materials, elements or space disposed therebetween) and "indirectly adjacent" (intermediate materials, elements or space disposed there between), "mounted to" includes "directly mounted to" (no intermediate materials, elements or space disposed there between) and "indirectly mounted to" (intermediate materials, elements or spaced disposed there between), and "electrically coupled" includes "directly electrically coupled to" (no intermediate materials or elements there between that electrically connect the elements together) and "indirectly electrically coupled to" (intermediate materials or elements there between that electrically connect the elements together). For example, forming an element "over a substrate" can include forming the element directly on the substrate with no intermediate materials/elements therebetween, as well as forming the element indirectly on the substrate with one or more intermediate materials/elements therebetween.

What is claimed is:

1. A method of reading a memory device having a plurality of memory cells, comprising:

reading a first memory cell of the plurality of memory cells to generate a first read current;

reading a second memory cell of the plurality of memory cells to generate a second read current;

applying a first offset value to the second read current; and then

combining the first and second read currents to form a third read current; and then

determining a program state using the third read current.

2. The method of claim 1, wherein the combining comprises adding the first and second read currents together.

3. The method of claim 1, further comprising:

reading a third memory cell of the plurality of memory cells to generate a fourth read current;

applying a second offset value to the fourth read current;

wherein the combining including combining the first, second and fourth read currents to form the third read current.

4. The method of claim 3, wherein the second offset value is different from the first offset value.

5. The method of claim 3, wherein the combining comprises adding the first, second and fourth read currents together.

6. The method of claim 1, wherein the plurality of memory cells are arranged in an array of rows and columns of the memory cells, wherein each of the columns includes a bit line connected to the memory cells therein, wherein first memory cell is disposed in a first

one of the columns, and wherein the second memory cell is disposed in a second one of the columns different than the first one of the columns.

7. A method of reading a memory device having a plurality of memory cells, comprising:

reading a first memory cell of the plurality of memory cells to generate a first read current;

reading a second memory cell of the plurality of memory cells to generate a second read current;

generating a first voltage from the first read current;

generating a second voltage from the second read current;

applying a first offset value to the second voltage; and then

combining the first and second voltages to form a third voltage; and then

determining a program state using the third voltage.

8. The method of claim 7, wherein the combining comprises adding the first and second voltages together.

9. The method of claim 7, further comprising:

reading a third memory cell of the plurality of memory cells to generate a third read current;

generating a fourth voltage from the third read current;

applying a second offset value to the fourth voltage;

wherein the combining including combining the first, second and fourth voltages to form the third voltage.

10. The method of claim 9, wherein the second offset value is different from the first offset value.

11. The method of claim 9, wherein the combining comprises adding the first, second and fourth voltages together.

12. The method of claim 7, wherein the plurality of memory cells are arranged in an array of rows and columns of the memory cells, wherein each of the columns includes a bit line connected to the memory cells therein, wherein first memory cell is disposed in a first one of the columns, and wherein the second memory cell is disposed in a second one of the columns different than the first one of the columns.

13. A memory device, comprising:

a semiconductor substrate;

a plurality of memory cells formed on the semiconductor substrate; and

circuitry formed on the semiconductor substrate and configured to:

read a first memory cell of the plurality of memory cells to generate a first read current;

read a second memory cell of the plurality of memory cells to generate a second read current;

apply a first offset value to the second read current; and then

combine the first and second read currents to form a third read current; and then

determine a program state using the third read current.

14. The device of claim 13, wherein the combining comprises adding the first and second read currents together.

15. The device of claim 13, wherein the circuitry is further configured to:

read a third memory cell of the plurality of memory cells to generate a fourth read current;

applying a second offset value to the fourth read current;

wherein the combining including combining the first, second and fourth read currents to form the third read current.

16. The device of claim 15, wherein the second offset value is different from the first offset value.

17. The device of claim 15, wherein the combining comprises adding the first, second and fourth read currents together.

18. The device of claim 13, wherein:

the plurality of memory cells are arranged in an array of rows and columns of the memory cells;

each of the columns includes a bit line connected to the memory cells therein;

the first memory cell is disposed in a first one of the columns; and

the second memory cell is disposed in a second one of the columns different than the first one of the columns.

19. A memory device, comprising:

a semiconductor substrate;

a plurality of memory cells formed on the semiconductor substrate; and

circuitry formed on the semiconductor substrate and configured to:

read a first memory cell of the plurality of memory cells to generate a first read current;

read a second memory cell of the plurality of memory cells to generate a second read current;

generate a first voltage from the first read current;

generate a second voltage from the second read current;

apply a first offset value to the second voltage; and then

combine the first and second voltages to form a third voltage; and then

determine a program state using the third voltage.

20. The device of claim 19, wherein the combining comprises adding the first and second voltages together.

21. The device of claim 19, wherein the circuitry is further configured to:

read a third memory cell of the plurality of memory cells to generate a third read current;

generate a fourth voltage from the third read current;

apply a second offset value to the fourth voltage;

wherein the combining including combining the first, second and fourth voltages to form the third voltage.

22. The device of claim 21, wherein the second offset value is different from the first offset value.

23. The device of claim 21, wherein the combining comprises adding the first, second and fourth voltages together.

24. The device of claim 19, wherein:

the plurality of memory cells are arranged in an array of rows and columns of the memory cells;

each of the columns includes a bit line connected to the memory cells therein;

the first memory cell is disposed in a first one of the columns; and

the second memory cell is disposed in a second one of the columns different than the first one of the columns.

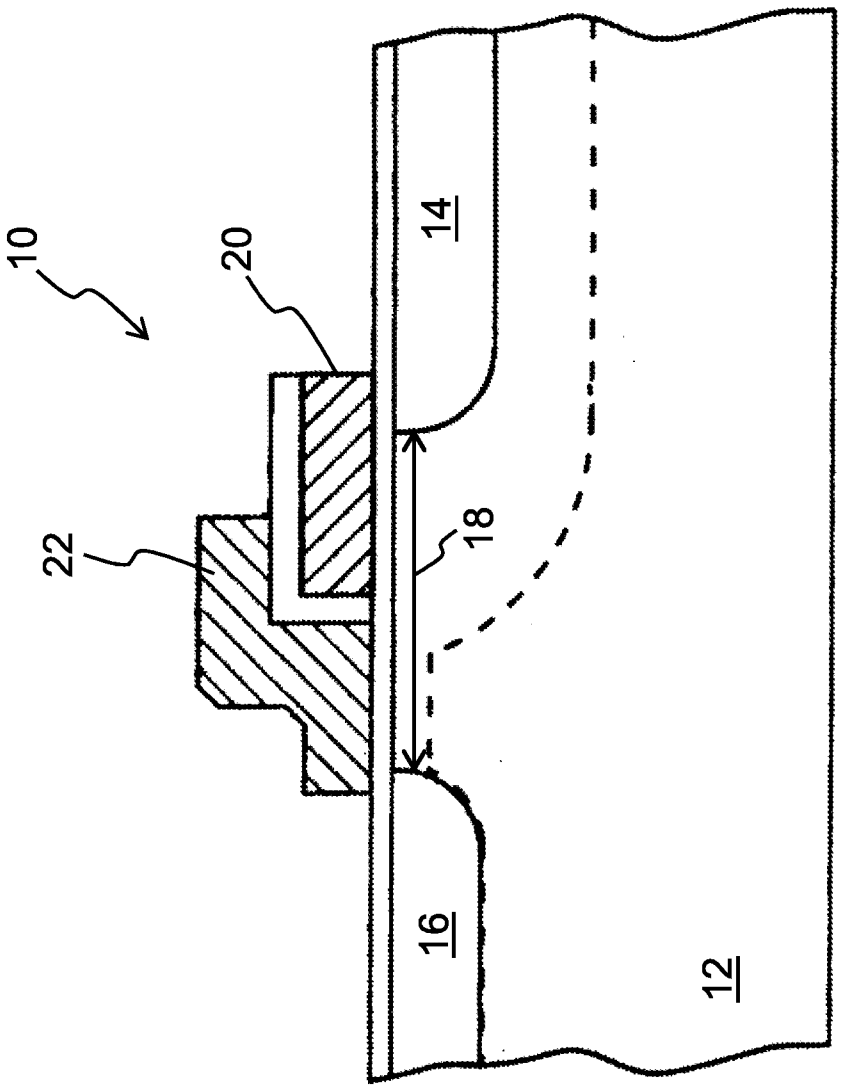

FIGURE 1
(Prior Art)

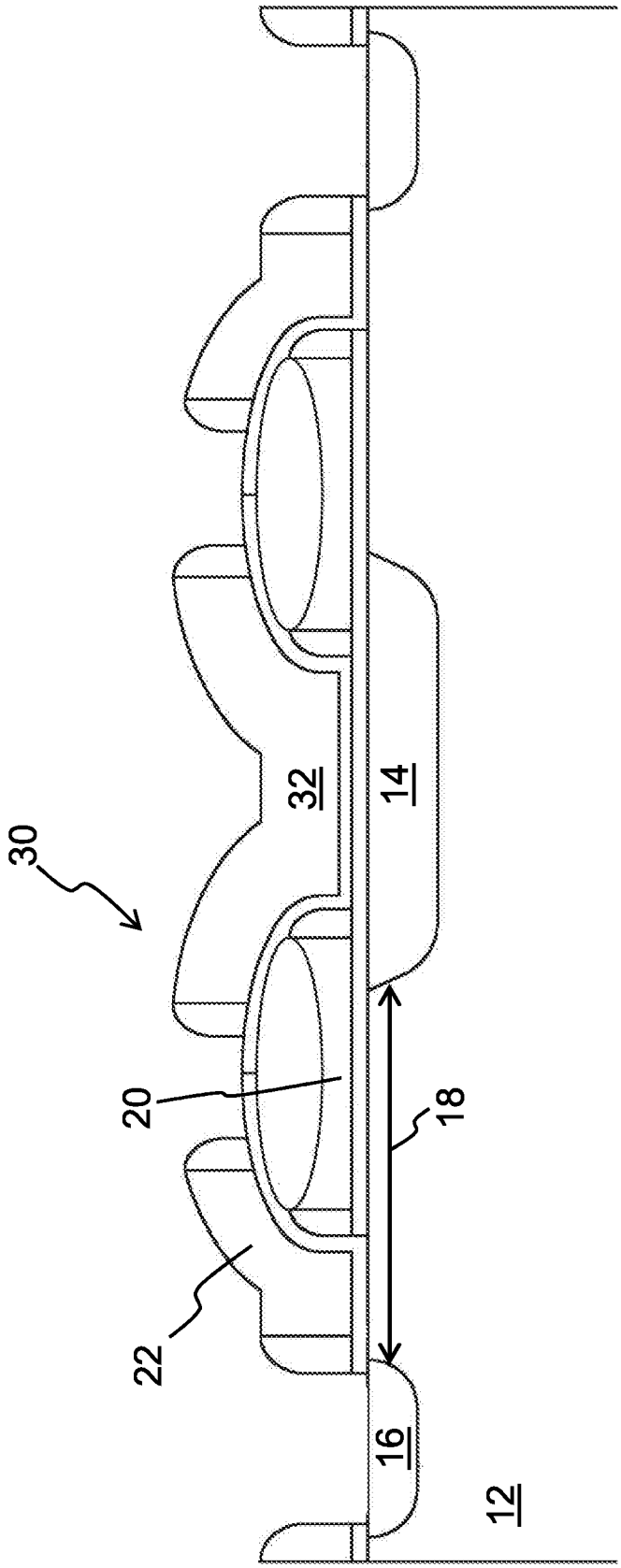

FIGURE 2
(Prior Art)

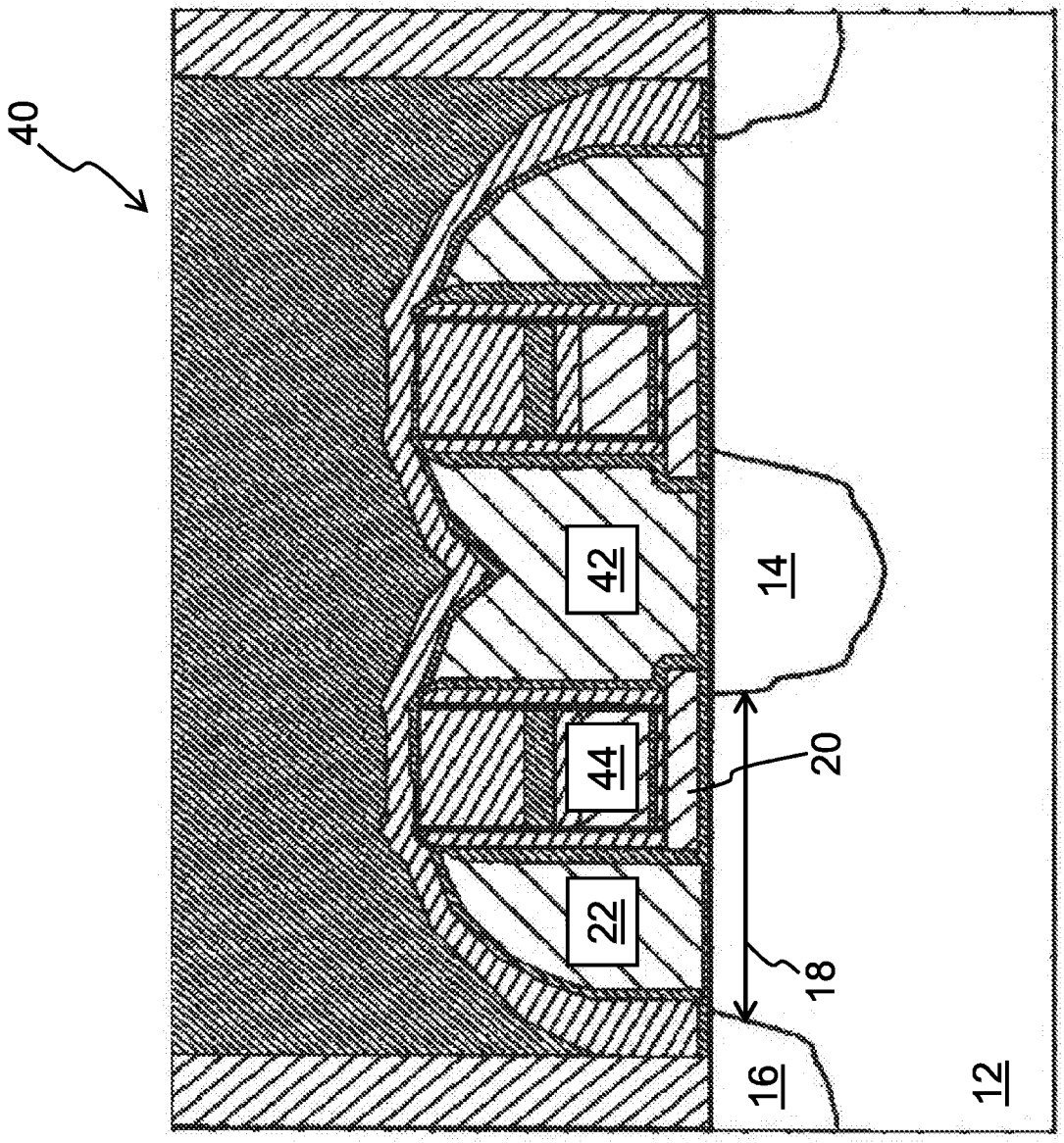

FIGURE 3
(Prior Art)

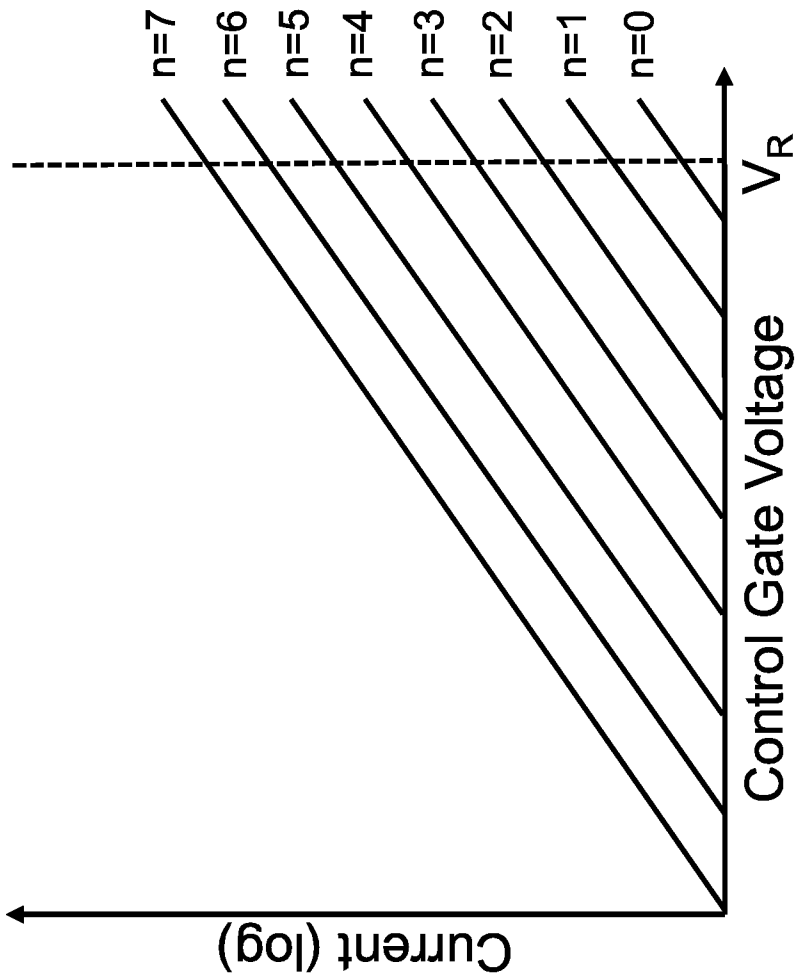

FIGURE 4

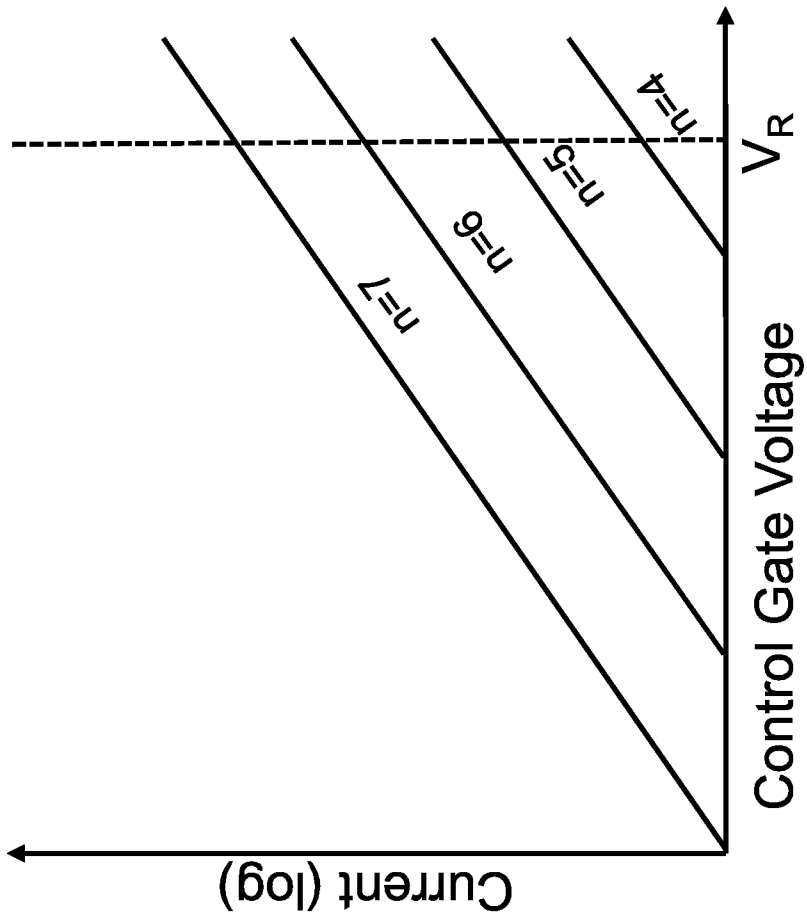

FIGURE 5B
Cell 2

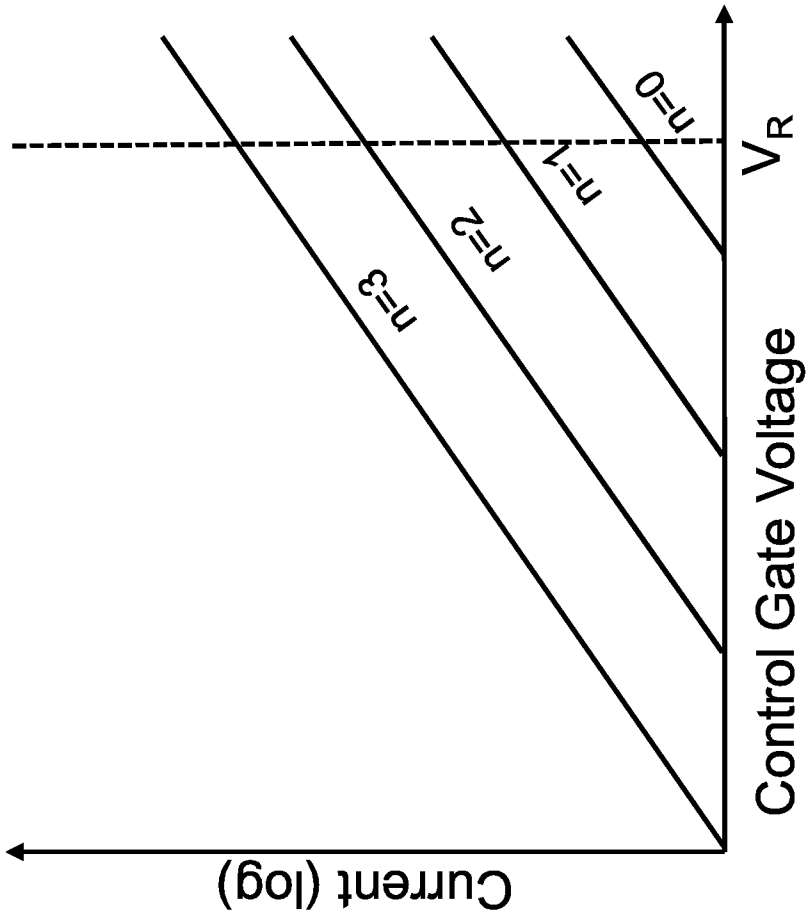

FIGURE 5A
Cell 1

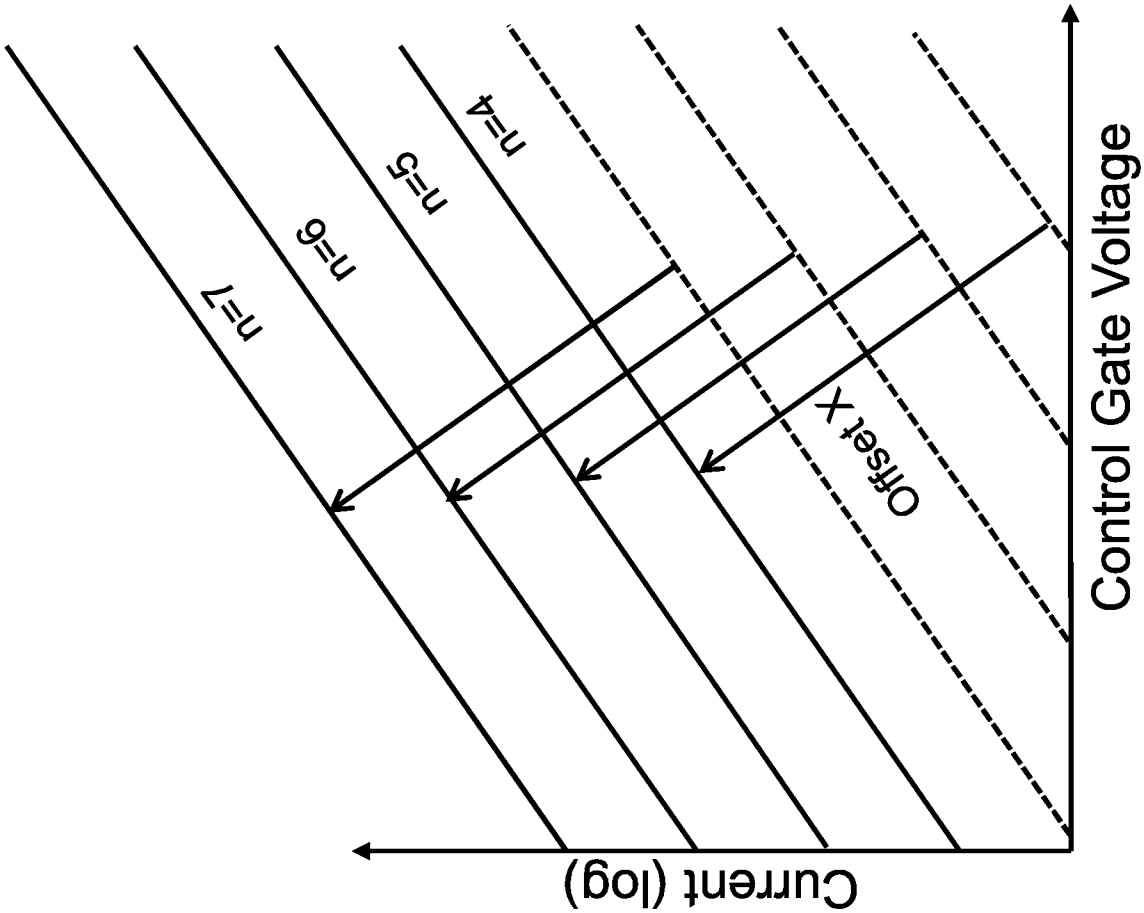

FIGURE 6A
Cell 1

FIGURE 6B
Cell 2

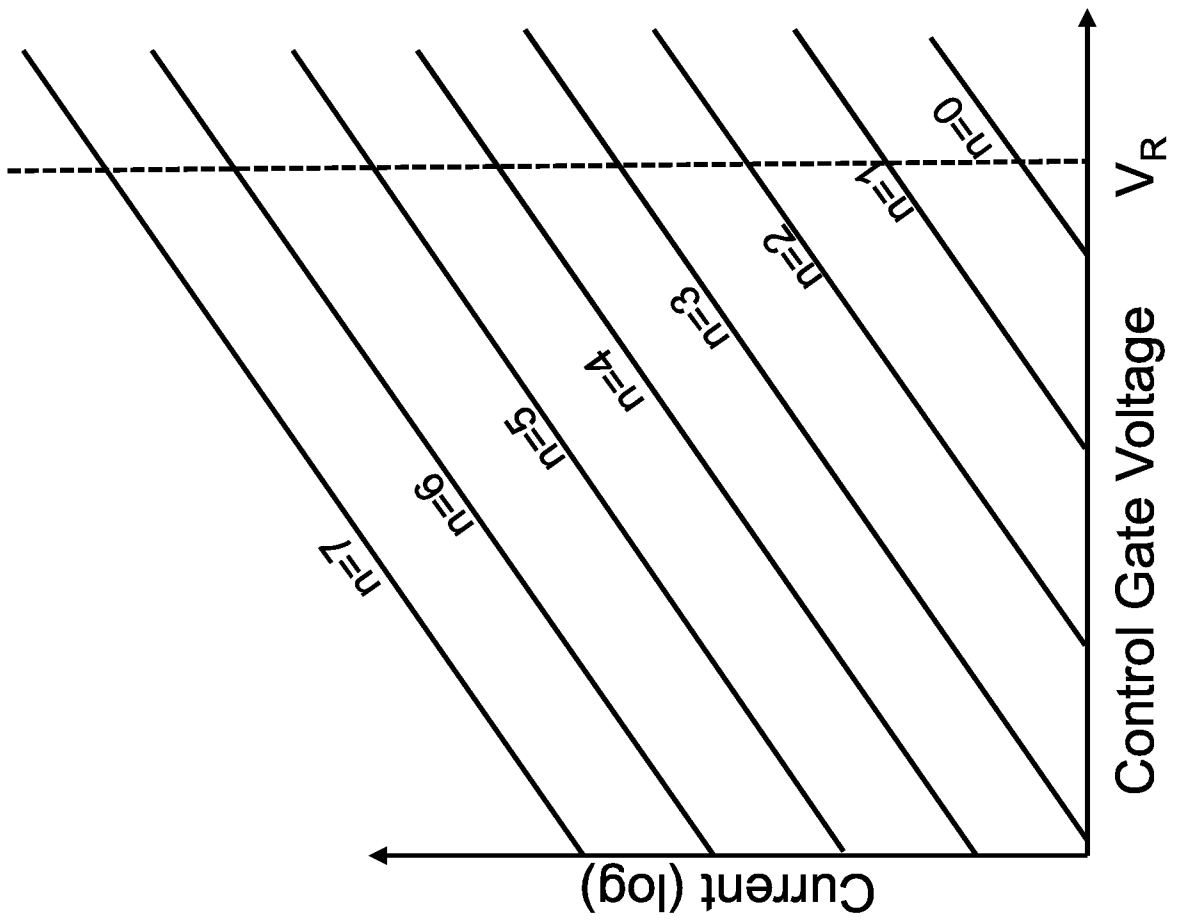

FIGURE 6C
Cells 1 and 2

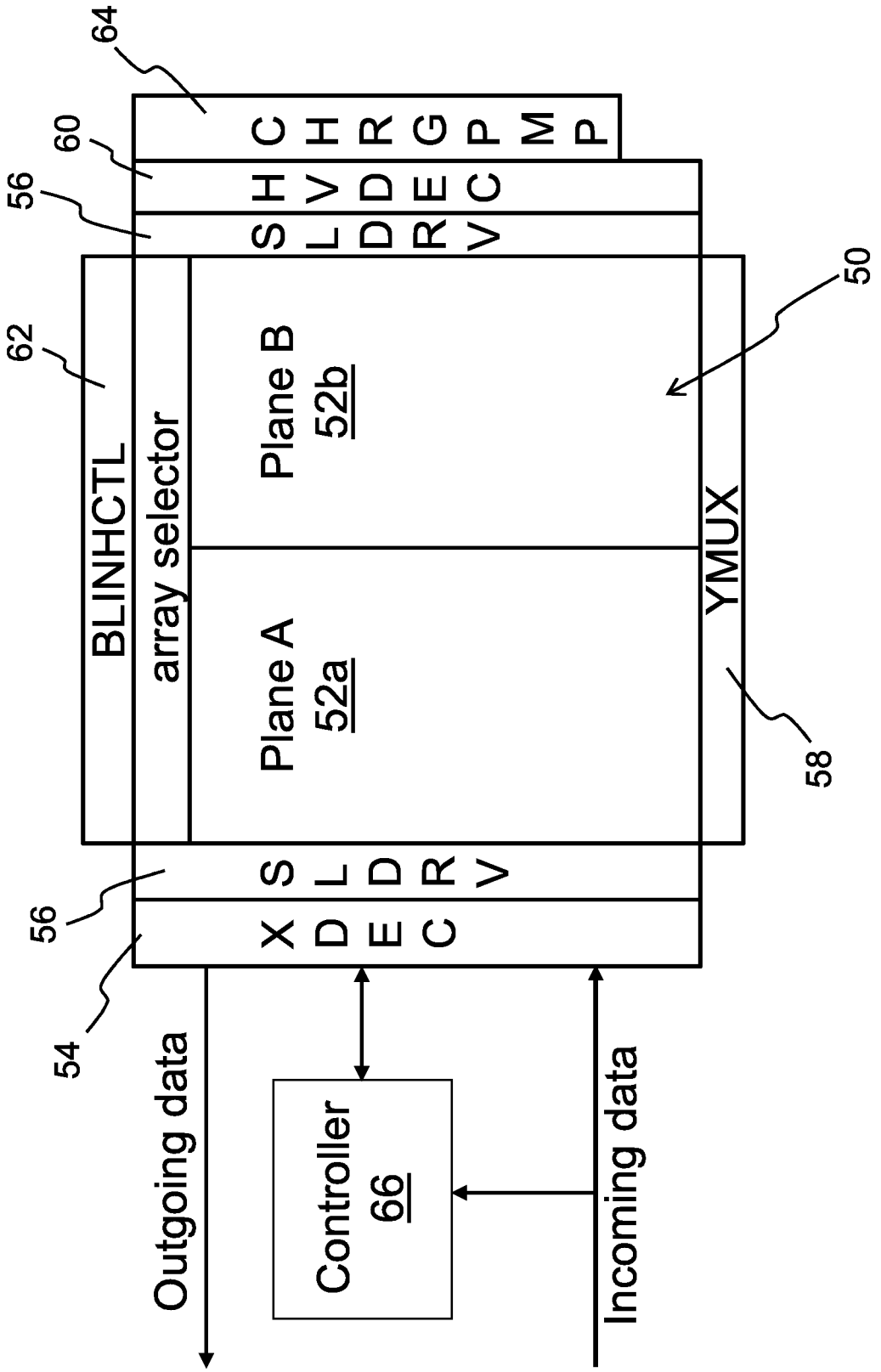
64
60
56
62
50
56
54
CHRGPMP
HVDECV
SLDRV
BLINHCTL
array selector
Plane B
52b
Plane A
52a
YMUX
58
SLDRV
XDECV
Outgoing data
Controller
66
Incoming data

FIGURE 7

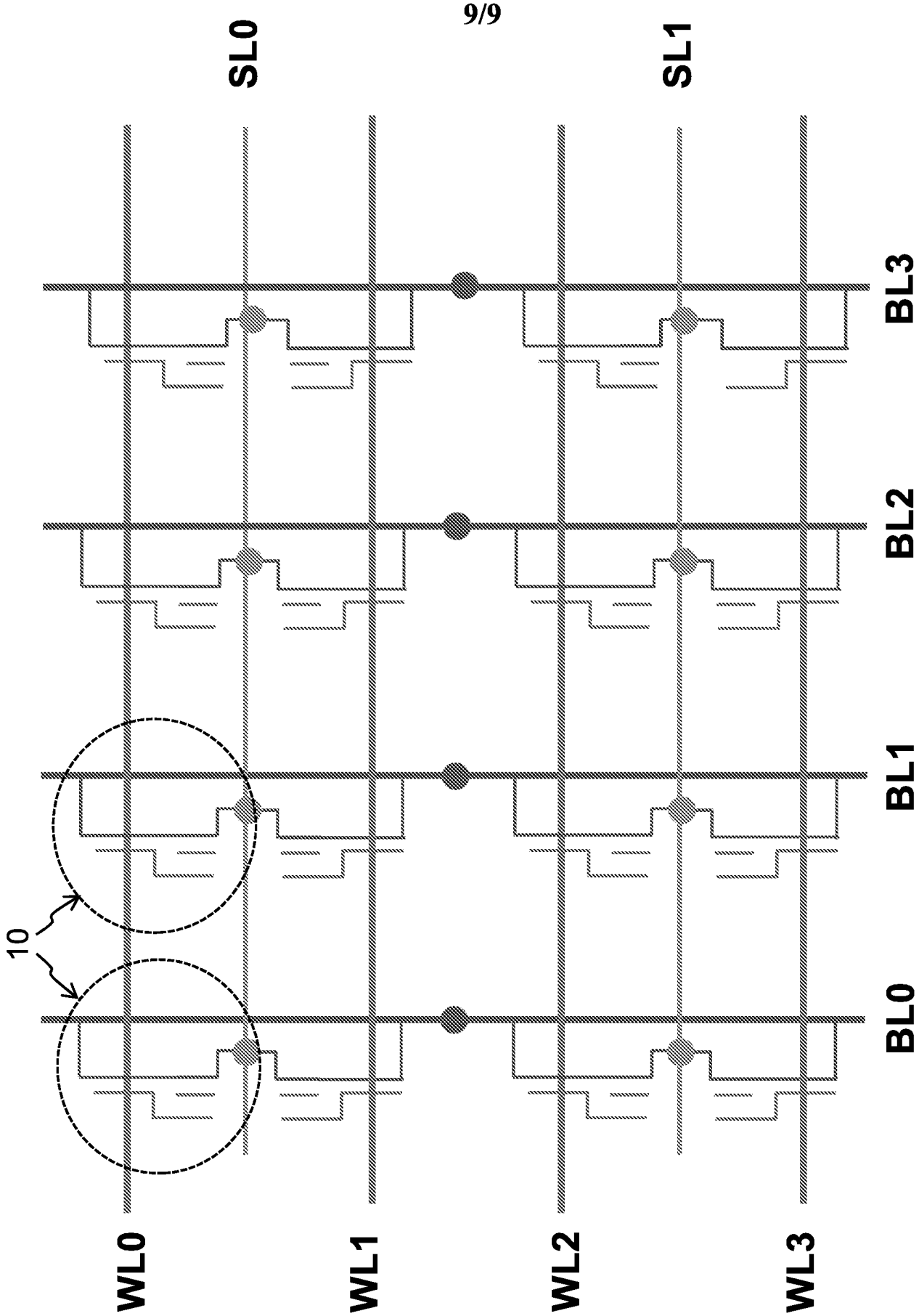

FIGURE 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/53930

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

--- (See Continuation in Supplemental Box) ---

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
Claims 1-6 and 13-18

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/53930

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G11C 13/00 (2018.01)

CPC - G11C 8/08, G11C 16/08, G11C 11/5607, G11C 11/5678, G11C 11/5685, G11C 13/0002, G11C 13/0004, G11C 13/0007, G11C 13/004, G11C 2211/5643, G11C 2211/5645

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014/0241039 A1 (SK hynix Inc), 28 August 2014 (28.08.2014), entire document, especially Abstract; para [0005], [0070], [0074]-[0077], [0093]-[0095]	1-6 and 13-18
Y	US 2012/0250400 A1 (KATAYAMA), 04 October 2012 (04.10.2012), entire document, especially Abstract; para [0016], [0054]	1-6 and 13-18
A	US 2005/0201148 A1 (Chen et al.), 15 September 2005 (15.09.2005), entire document	1-6 and 13-18
A	US 2008/0117678 A1 (Shieh et al.), 22 May 2008 (22.05.2008), entire document	1-6 and 13-18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2019	05 FEB 2019

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/53930

Continuation of:
Box III. Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I - Claims 1-6 and 13-18 are directed to a memory device and method for determining a program state using current values.

Group II - Claims 7-12 and 19-24 are directed to a memory device and method for determining a program state using voltage values.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:

The invention of Group I included the features of applying a first offset value to the second read current; and then combining the first and second read currents to form a third read current; and then determining a program state using the third read current, not required by group II.

The invention of Group II included the features of generating a first voltage from the first read current; generating a second voltage from the second read current; applying a first offset value to the second voltage; and then combining the first and second voltages to form a third voltage; and then determining a program state using the third voltage, not required by group I.

Common Technical Features

Groups I-II share the features of a semiconductor substrate; a plurality of memory cells formed on the semiconductor substrate; and circuitry formed on the semiconductor substrate and configured to: reading a first memory cell of the plurality of memory cells to generate a first read current; reading a second memory cell of the plurality of memory cells to generate a second read current.

However, the shared technical features do not represent a contribution over prior art as being anticipated by US 2012/0250400 A1 (KATAYAMA), 04 October 2012 (04.10.2012).

KATAYAMA teaches a semiconductor substrate (para [0016]- semiconductor memory device according to an embodiment comprises a first cell array including first memory cells arranged in a matrix); a plurality of memory cells formed on the semiconductor substrate and circuitry formed on the semiconductor substrate and configured to (para [0016]- semiconductor memory device according to an embodiment comprises a first cell array including first memory cells arranged in a matrix, the first memory cell having a first variable resistance element and a first select transistor. The semiconductor memory device comprises a second array including second memory cells arranged in a matrix, the second memory cell having a second variable resistance element and a second select transistor); reading a first memory cell of the plurality of memory cells to generate a first read current (para [0081], [0092] - a first reading current of the first memory cell M1; the first memory cell M1 is read, the second reference current Iref2 and the reading current of the first memory cell M1 are compared with each other); reading a second memory cell of the plurality of memory cells to generate a second read current (para [0084], [0092]- third reading current of the second memory cell M2; the second memory cell M2 is read, the first reference current Iref1 and the reading current of the second memory cell M2 are compared with each other).

As the common features were known in the art at the time of the invention, this cannot be considered a common technical feature that would otherwise unify the groups. Therefore, Groups I-II lack unity under PCT Rule 13.