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DATA HANDLING APPARATUS

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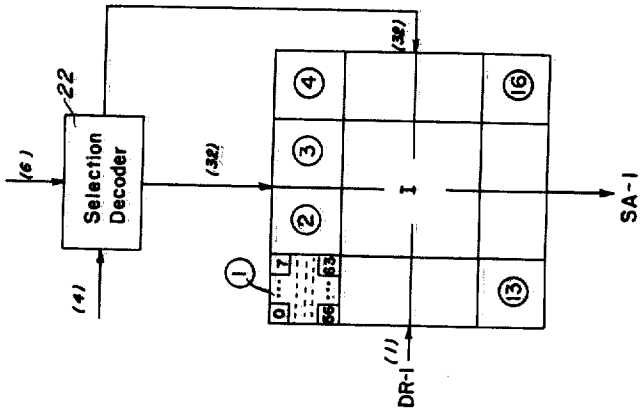


Fig. 2

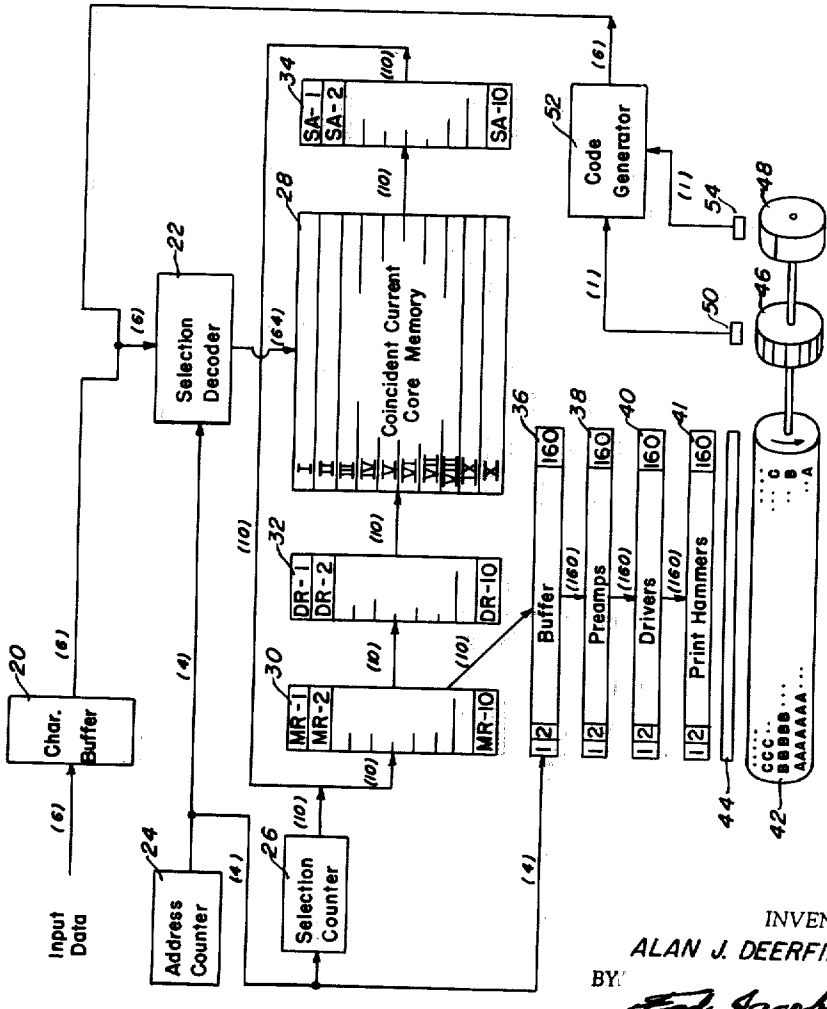


Fig. 1

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DATA HANDLING APPARATUS

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The present invention relates in general to new and improved data handling apparatus, in particular to apparatus for handling binary digital data in cooperation with a high-speed printer.

In high-speed printers of the kind wherein a single line is printed at a time before the paper web is moved to the next print line, a complete set of data characters is periodically presented for printing. In one embodiment, the data characters appear in raised form on a print roll which is rotated about its axis. The organization of the characters is such that a column containing a complete set of data characters is peripherally disposed on the print roll for each character space of the print line. Identical characters of the different columns form character rows on the surface of the print roll parallel to the print roll axis. These character rows successively rotate into printing position at a print station consisting of a set of aligned print hammers, one hammer corresponding to each column of data characters on the print roll. The appropriate print hammers are actuated as each character row reaches the print station to print the desired data characters on the paper web which is positioned intermediate the print hammers and the print roll. After the complete set of data characters has been exposed to the print hammers, i.e. after the print roll has completed one revolution, the paper web which was stationary during this process, is moved to the next line on which printing is to take place.

A system of this kind together with its associated data handling apparatus is disclosed in an application of Charles J. Barbagallo and Richard D. Pasciuto, Serial Number 113,351, filed May 29, 1961, which is assigned to the assignee of the present application. As may be seen in the apparatus disclosed in the above-mentioned patent application, the data arrives in the form of digitally encoded data characters, the respective digital code combinations being stored in a coincident current core memory.

Before printing can take place, each of the character code combinations stored in the memory must be examined, by comparing it against the output of a code generator which provides a code combination corresponding to the print roll character row next moving into printing position. For each true decoding comparison an indication is stored in a buffer which has a storage position corresponding to each print hammer, i.e. to each space of the print line. After the entire memory has thus been examined for a given data character and the necessary information has been stored in the buffer, the latter is read out to energize the appropriate print hammers when the corresponding character row is in printing position. The process is repeated for each different character of the entire set on the print roll.

Since each of the memory locations must be examined individually for each data character in the above-described apparatus, the ultimate printing speed is determined by the number of data character spaces per print line. For example, referring again to the above-identified copending application which normally has a print line containing 120 characters, 120 memory cycles are required to examine the coincident current core memory for the presence of one data character. A memory cycle is defined as the time required to read the information out of the coincident core memory and to write it back into the memory. Data stored in the memory becomes available only in this manner. If, for the sake of example, each memory cycle is assumed to have a duration of the order of 6 microseconds, 720 μs. are required to examine the memory for one data character, disregarding any additional time taken for the comparison with the code combination provided by the code generator. Assuming a 1,000 line-per-minute printer capable of printing 64 different data characters, the time available to examine the 120 locations of the memory for any given character is 930 microseconds, which is adequate under the assumed operating conditions.

If, however, it is desired to have a print line with 160 character spaces, 160 memory locations must be examined for the presence of each data character. Since this will take 960 microseconds under the assumed operating conditions, it is necessary to reduce the printing speed in order to accommodate the larger print line. Inasmuch as the printer is intended to operate with data processing equipment which normally has a much higher data handling capacity than the printer, such an alternative is evidently undesirable.

As previously pointed out, a decoding comparison takes place for each data character whereby every location of the coincident current core memory is compared against all the codes provided by the code generator in order to determine true comparisons. The code generator is synchronized to the rotation of the print roll. The circuitry required to carry out this function significantly adds to the complexity and hence to the cost of the data handling apparatus, particularly when the associated checking equipment is considered. It also requires additional maintenance which further increases its cost.

Accordingly, it is the primary object of the present invention to provide data handling apparatus which is not subject to the foregoing disadvantages.

It is another object of the present invention to provide apparatus which is capable of handling data at speeds several orders of magnitude higher than that found in presently available apparatus.

It is a further object of the present invention to provide data handling apparatus which is simple in construction and economical to build and to maintain.

It is an additional object of the present invention to provide data handling apparatus for operation with a high-speed printer which can accommodate print lines of a size larger than heretofore possible.

In the present invention the foregoing objects are attained by providing apparatus wherein the decoding process occurs on demand in accordance with each arriving data character. More specifically, in applicant's invention an indication of each incoming data character is stored in a coincident current memory at an address corresponding to the nature of the character itself. The address of a stored data character indication itself determines the nature of the character. Accordingly, it is merely necessary to address a storage location in order to determine whether or not the desired data character was received.

The elimination of the comparison process, which is customary in prior art apparatus, markedly reduces the complexity of the equipment required. More importantly, it enables identically addressed storage locations, e.g. corresponding locations in different core planes, to be read out simultaneously to effect a speed-up of the over-all operation by several orders of magnitude.

These and other novel features of the invention together with further objects and advantages thereof will become apparent from the following detailed specifications with reference to the accompanying drawings in which:

FIGURE 1 illustrates a preferred embodiment of the invention; and

FIGURE 2 illustrates in greater detail a portion of the apparatus shown in FIGURE 1.

For the purpose of illustrating the preferred embodiment of the invention, the data is assumed to be organized into data units, each unit constituting a data character. All data is assumed to be composed from a set having a maximum of 64 different data characters. Thus, a 6-bit binary digital code suffices to uniquely represent each data character of the set.

As shown in FIGURE 1, the input data arrives in the form of encoded data characters, i.e. six binary digits at a time. The designation (6) above the input data path shown is representative of the total number of lines schematically represented by a single path. The 6-line input is connected to a character buffer **20** which may consist of six gate buffer amplifiers, each connected regeneratively to store a single binary digit by recirculation.

The buffer output, similarly consisting of six lines, is connected to the input of a selection decoder **22**. An address counter **24** which is capable of incrementally counting up to 16, has a 4-line output connected to a second input of the selection decoder **22**. The output of the address counter **24** is further connected to a selection counter **26** which is capable of counting up to 10.

A 64-line output of the selection decoder **22** is connected to a concident current core memory **28** which includes a stack of ten susbtantially identical core planes I to X. FIGURE 2 illustrates in greater detail the organization of the cores within each core plane as well as their connection to the selection decoder **22**. The core plane I is shown as an example and is seen to have 1,024 cores coordinately arranged into 32 columns and 32 rows. Each column and each row is linked by a corresponding winding that is energized by the selection decoder. The cores are organized into 16 storage cells, each cell containing 64 storage locations, i.e. 64 cores. Each of the latter cores corresponds to one of said 64 different data characters and is located at an address within each cell that is determined by the representative code of a data character. In practice, the storage cells merely define an organizational concept and need not themselves be physically located at the coordinate positions shown in FIGURE 2. All the cores of each core plane are further linked by a single inhibit winding designated DR–1 and by a single sense winding designated SA–1. The connections shown are substantially identical in the remaining core planes.

Referring again to FIGURE 1, a memory register unit **30** is seen to comprise individual registers MR–1 to MR–10, each of which may consist of a gate buffer amplifier regeneratively connected to store a single binary digit dynamically. A 10-line output of the memory register unit **30** is connected to a driver unit **32** comprising individual core drive amplifiers DR–1 to DR–10.

The 10-line output of the driver unit is connected to the core memory **28**, each line linking all the cores of one plane. Similarly, a sense winding in each core plane links all the cores thereof, as explained in connection with FIGURE 2 above. The 10-line output of the core memory **28**, consisting of the ten sense windings of the respective core planes, is connected to a sense amplifier unit **34** comprising individual sense amplifiers SA–1 to SA–10. The output of the sense amplifier unit **34** is connected to the input of the memory register unit **30** and is gated with an output of the above-mentioned selection counter **26**.

An additional 10-line output of the memory register **30** is applied to a buffer **36** which receives a further input from the address counter **24**. In the illustrated example, the buffer comprises 160 storage units, each of which may consist of a gate buffer amplifier regeneratively connected to store a single binary digit by recirculation. A 160-line output of the buffer **36** is applied to a preamplifier unit **38**, comprising 160 preamplifiers each connected to a corresponding drive amplifier of a print hammer driver unit **40**.

Each of the print drivers is connected to energize a corresponding print hammer actuator in a print hammer unit **41**.

Each of the print hammers confronts a column of data characters peripherally arranged on a print roll **42**. The print roll is rotatably disposed about its axis so as to present the respective data characters of each character column to the corresponding print hammer of the unit **42**. Each of the aforesaid columns contains a complete set of data characters from which the input data, represented in 6-bit code, is composed. The characters in the respective columns are arranged to form rows of identical characters parallel to the print roll axis. As such, they are adapted to rotate jointly to the print station where they confront the print hammers. A movable paper web **44** is positioned intermediate the print hammers and the print roll.

A character disc **46** and the index **48** are arranged to rotate in synchronism with the print roll **42**. The character disc contains a marker corresponding to each of the aforesaid character rows. A pick-up **50** is arranged to sense each of the marks of the character disc and has its output connected to a code generator **52**. The index disc **48** contains a single marker adapted to be sensed by a pick-up **54** which similarly has its output connected to the code generator **52**. The latter, which is essentially a counter capable of counting up to 64, is adapted to provide the aforesaid 6-bit code on a 6-line output connected to the input for the above-mentioned selection decoder **22**.

In operation input data characters arrive in 6-bit form, each character being temporarily stored in the character buffer **20**. Thereafter, the data, still in character form, is applied to the selection decoder **22** which, simultaneously, receives an input from the address counter **24**. The action of the address counter on the selection decoder **22** is such that the signals appearing on the output lines of the latter successively select a different storage cell to store an indication of each arriving data character. Upon the initiation of the address counter cycle, the selection counter **26** acts on the memory register unit **30** which in turn actuates the driver DR–1 to select the core plane I for the incoming data to the exclusion of the remaining core planes. Accordingly, data character indications are initially stored in core plane I. The location within each storage cell is determined by the 6-bit code representative of the data character.

Let it be assumed that the character A is represented by the first combination of the 6-bit code (e.g. 000000), the character B is represented by the second code combination (000001), the character C is represented by the third code combination (000010), etc. If the first data character to arrive is an A represented by its appropriate code combination, an indication thereof is stored in the location 0 of the first storage cell in the core plane I. This is done by actuating appropriate outputs of the selection decoder **22** to switch the core which is at the location 0 of the first storage cell to its other bistable state. If, on the other hand, the 6-bit code representing the first character to arrive were to indicate the letter C, the core at the third location of the first storage cell, i.e. the location 2, is switched as an indication of the storage of the aforesaid data character. No further character indications are stored in the first storage cell.

With the arrival of the next input data character, the 4-digit address count is incremented by 1 to select the second storage cell in the core plane I. As in the case of the first storage cell, the particular core which is switched within the second stage cell as a storage indication of the second input data character to arrive, is determined by the 6-bit code representative of the second data character.

Upon the selection of the sixteenth storage cell in the core plane I and the storage of a data character indication in the appropriate location of this cell, the address counter **24** is at the end of its cycle. It is thereupon reset and simultaneously causes the selection counter **26** to be incremented by 1 so as to energize the memory register

MR–2. The driver DR–2 is now activated and the core plane II is selected to the exclusion of all other core planes.

An indication of the next data character, the seventeenth data character to arrive, is stored in the first storage cell of the core plane II at a location determined by its representative 6-bit code. Subsequently arriving data characters are stored in the respective storage cells of the core plane II, substantially in the manner described in connection with the core plane I. The process continues until a single data character indication has been stored in each storage cell of the ten planes of the core memory **28**. The storage of 160 data character indications thus completes the data read-in phase of the operation.

Inasmuch as those cores which are positioned at corresponding locations in the respective core planes have the same address, ten cores may be read out at a time with a single address during the data readout operation. The latter is therefore completed in sixteen memory cycles. Specifically, the rotation of the character disc **46** produces pulses, each of which increments the 6-bit code output of the code generator **52** which is applied to the input of the selection decoder **22**, together with the count of the address counter **24**. During the readout operation, the selection counter operates to jointly energize each of the memory registers MR–1 to MR–10 so that the outputs of the drivers DR–1 to DR–10 are simultaneously active.

The application to the selection decoder **22** of a 6-bit code representative of the character A which is derived from the code generator **52**, together with the output signal of the address counter **24** indicative of the selection of the first storage cell, provides appropriate signals on the output of the selection decoder which are simultaneously applied to the location 0 of the first storage cell of each of the core planes I to X. Ten memory output signals are obtained in response thereto which are applied to the sense amplifiers SA–1 to SA–10, whence they are fed to the memory registers MR–1 to MR–10 respectively. The output of the latter is simultaneously applied to the first ten of the 160 gate buffer amplifiers of the buffer **36**, as determined by the address counter output signal which is simultaneously applied to the buffer **36**.

The code generator output for the character A is maintained for a period of sixteen memory cycles to enable the address counter **24** to select successive storage cells simultaneously in all the core planes, each cell so selected to have its 0 location addressed for the presence of the character A. The action of the address counter output signal on the buffer **36** causes successively derived output signals of the memory register unit **30** for the character A to be stored in successive blocks of ten gate buffer amplifiers each. After sixteen memory cycles have elapsed the buffer **36** is full whereupon it is simultaneously read out to the preamplifier unit **38** which, in turn, energizes the drivers **40**. The latter actuate the appropriate print hammers in a manner whereby when the A character row rotates to the print station, the character A is printed on the paper web **44**.

The readout operation is repeated for subsequent data characters which move into printing position with the rotation of the print roll. The operation proceeds substantially in the manner described above in connection with the character A, corresponding storage locations within each cell being addressed in accordance with each character code generated. Upon the completion of one print roll revolution, the paper web **44**, which remained stationary up to this point, is moved to the position of the next line to be printed.

It will be apparent that the entire core memory is read out in sixteen memory cycles for the presence of one character in a line having 160 character spaces. If the duration of a memory cycle is taken as approximately 6 μs., the operation is completed in 96 μs. As previously explained, the time interval between successive character rows for a 1000-line-per-minute printer is 930 microseconds. Thus, an increase of several orders of magnitude in the speed of the printing operation is possible with the present invention for a print line having 160 character spaces. If desired, the number of spaces in the print line may be expanded considerably.

From the foregoing discussion, it will be seen that the decoding operation in the present invention occurs on demand as the incoming data characters arrive. The storage of decoded character indications permits the core memory to be read out simultaneously in all the core planes merely by addressing a location within a cell. A considerable increase in the operating speed is thus obtained and the data handling apparatus is simplified owing to the elimination of the decoding comparison equipment which is required in prior art apparatus.

Within the scope of the illustrated embodiment, the present invention is applicable to any data handling device which is adapted to operate with input-output apparatus wherein a set of data characters is periodically presented for transfer to an output medium. The core memory may have any desired configuration.

It will also be evident that character codes having a different number of digits may be employed provided the core memory is suitably dimensioned to accommodate them. In the latter case, the proper changes must also be made in the code generator. The generation of codes may occur by means of binary coded discs instead of in the manner shown. The representation of stored character indications need not be restricted to a single digit. The cores associated with a single storage cell need not necessarily be grouped together as shown, provided only that each core is addressable by its corresponding code combination. If the number of characters used is less than the total number of combinations possible with a given character code, the size of the core memory can be reduced since each storage cell need only have as many cores as there are different data characters.

While the invention has been described and illustrated with respect to a preferred embodiment, it applies to any data handling device wherein a plurality of multi-bit data signals is stored in an array comprising a corresponding plurality of individual and separately addressable bistable storage means, so that a predetermined state of respective ones of said storage means is uniquely representative of a multi-bit signal manifestation.

From the foregoing disclosure of the invention, it will be apparent that numerous modifications, changes and equivalents will now occur to those skilled in the art, all of which fall within the true spirit and scope contemplated by the invention.

What is claimed is:

1. In combination with a printer of the kind having a print roll adapted to present successive ones of a set of different data characters to each of a plurality of aligned print hammers, a code generator adapted to generate a different binary digital code combination for each of said print roll characters, means for receiving input data in the form of said data characters represented by said code combinations, a storage device comprising a separate storage cell corresponding to each one of said plurality of print hammers, said storage cells being arranged in groups, each of said different data characters having a corresponding storage location within each of said cells at an address determined by the representative code combination of said character, means for selecting said storage cells in succession for successively arriving data characters, means for storing an indication of each of said arriving data characters in a storage location of the selected storage cell determined by the code of said character, means successively operative on different ones of said groups of storage cells for each generated code combination for simultaneously reading character indications out of all corresponding storage locations in a group, and means for simultaneously energizing said print

hammers in accordance with said readout character indications.

2. In combination with a data output device of the kind wherein successive ones of a set of different data characters are presented for selective transfer to an output medium, a code generator synchronously adapted to provide a different code combination for each character of said set, a storage device having a succession of storage cells arranged in groups, each of said cells including a separate storage location corresponding to each of said data characters addressable by means of the corresponding code combination, means for storing indications of sequentially received data characters in successive ones of said storage cells at a location within each cell corresponding to the representative character code combination, and means successively operative for different groups of said storage cells for simultaneously addressing corresponding storage locations of the storage cells within each group with each of said generated code combinations to read out stored indications of said data characters, and means for transferring data characters to said output medium in accordance with said readout indications.

3. Apparatus for handling incoming data composed from a plurality of different data units, each of said data units being represented by a different combination of a predetermined number of digits constituting a first code, comprising a storage device including a plurality of storage cells arranged in groups, each of said cells including a storage location corresponding to each of said different data units addressable by the first code combination corresponding thereto, means for storing indications of sequentially arriving data units in successive ones of said storage cells at a location within each cell corresponding to the code combination of each data unit, said data unit indications being represented by a second code having a smaller number of digits than said first code, and means successively operative for different groups of storage cells for simultaneously addressing corresponding storage locations in each group for different ones of said first code combinations to extract said stored indications of said data units.

4. Apparatus for handling incoming data composed from a set of data characters each represented by a different binary digital code combination, comprising a coincident current core matrix including a plurality of substantially identical core planes each having the cores thereof organized into storage cells, corresponding storage cells of different core planes forming groups, each of said storage cells including a separate core corresponding to each one of said set of data characters at an address within each cell determined by the representative code combination of said character, means for sequentially selecting different ones of said core planes, means for sequentially selecting the storage cells of each selected plane in accordance with successively arriving data characters, means for addressing a single core in each selected cell in accordance with the representative binary code combination of the arriving data character to store an indication of said character in said core, a plurality of print hammers, a print roll adapted to present successive ones of said set of data characters to each of said print hammers, a code generator operative in synchronism with said print roll to provide a sequence of said code combinations for the corresponding print roll characters, means successively operative on different groups of storage cells for each of said generated code combinations for simultaneously addressing all corresponding cores in a group to read out stored indications of the character represented by said generated code combination, and means for simultaneously energizing said hammers with said readout indications.

5. Apparatus for handling data composed from a set of different data characters each represented by a different combination of a first binary digital code, comprising an address counter for providing a second binary digital code cyclically incremented from zero to its maximum, a coincident current core matrix comprising a stack of substantially identical core planes having the cores thereof arranged in coordinate rows and columns, each group of corresponding core rows and columns respectively in said stack being linked by its own winding, the cores in each of said core planes being organized into storage cells corresponding respectively to different counts of said address counter, each one of said set of different data characters having a corresponding core in each of said storage cells at a location within each cell determined by the representative first code of said character, decoding means connected to receive said first and second codes, the output of said decoding means being connected to energize one of each of said row and column windings respectively in response to each pair of jointly received first and second codes to actuate the core linked by said windings, a selection counter responsive to the completion of each cycle of said address counter to select successive ones of said core planes, one core of each of said storage cells in each selected core plane being adapted to store an indication of a data character at an address determined by said pair of jointly received first and second codes corresponding thereto.

6. The apparatus of claim 5 and further comprising a print station including a plurality of aligned print hammers each corresponding to one of said storage cells of said matrix, a print roll adapted to rotate about its axis, said print roll including a peripheral column containing said set of different data characters positioned opposite each of said print hammers, identical data characters of said columns being positioned to form character rows parallel to said print roll axis, a code generator synchronized with the rotation of said print roll to provide combinations of said first code representative of said character rows, the duration of each of said last-recited first code combinations blanketing a complete cycle of said address counter, means for jointly energizing said decoding means from the output of said code generator and said address counter, means successively operative for different storage cells during one cycle of said address counter for simultaneously addressing those cores in all of said core planes which correspond to the code provided by said generator to obtain readout signals, and means including temporary buffer storage means for energizing said print hammers in accordance with said readout signals.

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