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(71) Applicant: TOYOTA JIDOSHA KABUSHIKI KAISHA [JP/JP]; 1, Toyota-cho, Toyota-shi, Aichi, 4718571 (JP).

(72) Inventor: YASUDA, Yoshifumi; c/o TOYOTA JIDOSHA KABUSHIKI KAISHA, 1, Toyota-cho, Toyota-shi, Aichi, 4718571 (JP).

(74) Agent: KAI-U PATENT LAW FIRM; NAGOYA LUCENT TOWER 9F, 6-1, Ushijima-Cho, Nishi-ku, Nagoya-shi, Aichi, 4516009 (JP).

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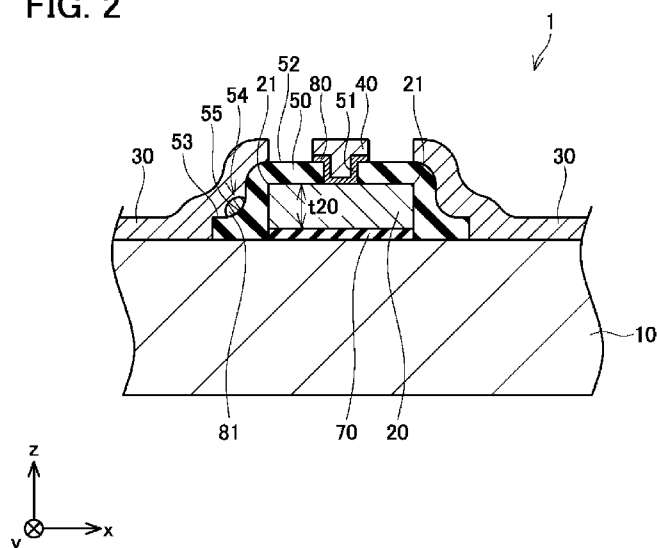
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(54) Title: SEMICONDUCTOR DEVICE

[Fig. 2]

FIG. 2



(57) Abstract: The semiconductor device 1 includes a semiconductor substrate 10 in which a IGBT is formed; a gate electrode 20 of the IGBT; an insulation film 50 covering the gate electrode 20 and the semiconductor substrate 10; and an emitter electrode 30 formed on the insulation film 50. A gate wiring 40 is formed on the insulation film 50, separated from the emitter electrode 30, and in contact with the gate electrode 20. An upper surface of the insulation film 50 includes a first portion, a second portion, and a step portion 54, the first portion being located on the gate electrode 20, the second portion being located on the substrate 10, and the step portion 54 being located between the first and second portions. The emitter electrode 30 covers the step portion 54, and the gate wiring 40 does not cover the step portion 54.

Description

Title of Invention: SEMICONDUCTOR DEVICE

Technical Field

[0001] The teachings disclosed herein relate to a semiconductor device.

Background Art

[0002] A semiconductor device having a semiconductor substrate, an electrode formed on the semiconductor substrate, and wiring connected to the electrode is disclosed in Japanese Patent Application Publication No.S63-104448.

Summary of Invention

[0003] In the above semiconductor device, in order to connect an electrode and wiring formed on a semiconductor substrate, a barrier-metal is formed between the electrode and the wiring. Unnecessary barrier-metals are removed by etching or the like. Even though such unnecessary barrier-metals are removed, a part of them may be unremoved and remained as a residual substance. Such a metallic residual substance may cause an electric short-circuit. The object of the teachings disclosed herein is to provide a semiconductor device capable of suppressing the generation of short-circuits caused by metallic residual substances.

[0004] The semiconductor device disclosed herein comprises: a semiconductor substrate in which a first switching element is formed; a gate electrode of the first switching element formed on the semiconductor substrate; an insulation film covering the gate electrode and the semiconductor substrate; and a first conductive member formed on the insulation film. The semiconductor device further comprises a gate wiring formed on the insulation film, separated from the first conductive member, and being in contact with the gate electrode. An upper surface of the insulation film comprises a first portion, a second portion, and a step portion. The first portion is located on the gate electrode, the second portion is located on the substrate, and the step portion is located between the first and second portions. The first conductive member covers the step portion, and the gate wiring does not cover the step portion.

[0005] The above metallic residual substance is likely to remain in the step portion of the insulation film. In such a configuration, when a metallic residual substance is accumulating in the step portion, the first conductive member contacts the residual substance while the gate wiring does not. As a result, a short circuit between the first conductive member and the gate wiring through the residual substance remaining in the step portion can be inhibited.

Brief Description of Drawings

[0006] [fig.1]FIG.1 is a plan view of a semiconductor device having an emitter electrode and

gate wiring formed thereon (upper surface of the semiconductor substrate is seen from vertical direction).

[fig.2]FIG.2 is a cross-sectional view taken from line II-II of FIG.1.

[fig.3]FIG.3 is a cross-sectional view taken from line III-III of FIG.1.

[fig.4]FIG.4 is a cross-sectional view taken from line IV-IV of FIG.1.

[fig.5]FIG.5 is an enlarged view of an primary part V of FIG.1.

[fig.6]FIG.6 is a plan view of the semiconductor device having an emitter electrode, gate wiring, and sense electrode formed thereon (upper surface of the semiconductor substrate is seen from vertical direction).

[fig.7]FIG.7 is a cross-sectional view taken from line VII-VII of FIG.6.

[fig.8]FIG.8 is a cross-sectional view taken from line VIII-VIII of FIG.6.

[fig.9]FIG.9 is an enlarged view of an primary part IX of FIG.6.

[fig.10]FIG.10 is a view corresponding to FIG.9 of one embodiment.

Description of Embodiments

[0007] Preferred aspects of below embodiments will be listed.

[0008] (Feature 1) In the semiconductor device, a gate wiring may be formed on a first portion of an upper surface of an insulation film that is located on a gate electrode.

[0009] (Feature 2) A first conductive member may be a negative electrode of a first switching element.

[0010] (Feature 3) A second switching element may be further formed in the semiconductor substrate, and the first conductive member may be a negative electrode of the second switching element.

[0011] (Feature 4) The negative electrode may comprise a first region, a second region formed with an interval from the first region, and a connecting region connecting the first region and the second region. The connecting region may cover a step portion of the upper surface of the insulation film.

[0012] (First Embodiment)

Embodiments are explained below with reference to the attached drawings. As shown in FIG.1, one embodiment of a semiconductor device 1 includes an emitter electrode 30 (one example of a first conductive member), and gate wiring 40. As shown in FIGS.2 to FIG.4 (cross sectional views of FIG.1), the semiconductor device 1 includes: a semiconductor substrate 10, gate electrode 20, and insulation film 50.

[0013] Not illustrated though, the semiconductor substrate 10 includes an IGBT formed therein. The emitter electrode 30 is an emitter electrode of the IGBT. The emitter electrode 30 is exposed on the upper surface of the semiconductor device 1. The emitter electrode 30 is a negative electrode. In planar view as shown in FIG.1, the emitter electrode 30 includes: a first region 31; a second region 32; a third region 33;

and a connecting region 34. The first region 31 and the second region 32 are neighboring each other. The first region 31 and the second region 32 have a clearance therebetween. The third region 33 is formed around the periphery of the first region 31 and the second region 32, and enclosing these regions. The connecting region 34 allows the first region 31, second region 32, and third region 33 to connect each other.

[0014] The gate wiring 40 is connected to the gate electrode 20 of the IGBT described above. The gate wiring 40 is exposed on the upper surface of the semiconductor device 1. In planar view, the gate wiring 40 includes: a first region 41; second region 42; and third region 43. The first region 41 of the gate wiring 40 is formed around the periphery of the first region 31 of the emitter electrode 30 and enclosing the first region 31. The first region 41 of the gate wiring 40 is formed between the first region 31 and the third region 33 of the emitter electrode 30. The second region 42 of the gate wiring 40 is formed around the periphery of the second region 32 of the emitter electrode 30 and enclosing the second region 32 of the emitter electrode 30. The second region 42 of the gate wiring 40 is formed between the second region 32 and the third region 33 of the emitter electrode 30. The third region 43 of the gate wiring 40 is formed between the first region 31 and the second region 32 of the emitter electrode 30. The first region 41, second region 42, and third region 43 of the gate wiring 40 are connected to a gate pad 44. The gate pad 44 is electrically connected to an external circuit.

[0015] In planar view, the emitter electrode 30 and the gate wiring 40 are separated apart from each other. The emitter electrode 30 and the gate wiring 40 are insulated each other. A potential different from that for the emitter electrode 30 is applied on the gate wiring 40.

[0016] In cross-sectional view as in FIGS. 2 to 4, the semiconductor device 1 includes: a semiconductor substrate 10; an insulation film 70 formed on the semiconductor substrate 10; and a gate electrode formed on the insulation film 70. The semiconductor device 1 also includes: an insulation film 50 formed on the gate electrode 20 and the semiconductor substrate 10; and an emitter electrode 30 formed on the insulation film 50 and the semiconductor substrate 10. Furthermore, the semiconductor device 1 includes a barrier-metal 80 formed on the gate electrode 20. The gate wiring 40 is formed on the barrier-metal 80.

[0017] For example, silicon (Si), silicon carbide (SiC), or the like can be used as a material for the semiconductor substrate 10. The IGBT (Insulated Gate Bipolar Transistor) is formed by having the inside of the semiconductor substrate 10 be doped with impurities. That is, inside of the semiconductor substrate 10 includes: an n type emitter region; p type body region; n-type drift region; and p type collector region (not shown), and so on, and these regions form the IGBT. More specifically, the semi-

conductor substrate 10 includes: an IGBT as a main element (an example of the first switching elements) having a large area and allowing a large current to flow therein; and an IGBT as a sense element (an example of the second switching elements) having a small area and allowing a small current to flow therein. The emitter electrode 30 is contacting the emitter region of the IGBT of the main element (an example of the first switching elements).

- [0018] The insulation film 70 is partially formed on the upper surface of the semiconductor substrate 10. As a material for the insulation film 70, for example, silicon dioxide (SiO_2) can be used. The insulation film 70 insulates the semiconductor substrate 10 and the gate electrode 20.
- [0019] The gate electrode 20 is formed on the upper surface of the insulation film 70. The gate electrode 20 is formed on the semiconductor substrate 10 through the insulation film 70. The gate electrode 20 has the thickness "t20". As a material for the gate electrode 20, for example, polysilicon can be used.
- [0020] The insulation film 50 is formed on the upper surface of the gate electrode 20. The insulation film 50 covers whole of the gate electrode 20. In addition, the insulation film 50 is also formed on the upper surface of the semiconductor substrate 10. The insulation film 50 covers the gate electrode 20 and the semiconductor substrate 10 from the above. The insulation film 50 covers edges 21 on both sides of the gate electrode 20. As a material for the insulation film 50, for example, silicon dioxide (SiO_2) can be used.
- [0021] The upper surface of the insulation film 50 includes: a high-order section 52; a low-order section 53; and a first step portion 54. The high-order section 52 is placed upper than the low-order section 53. The high-order section 52, low-order section 53, and first step portion 54 are formed according to the thickness "t20" of the gate electrode 20. That is, the high-order section 52 is placed on the gate electrode 20, and the low-order section 53 is placed on the semiconductor substrate 10 (namely, an area on the semiconductor substrate 10 where the gate electrode 20 is not existing). The first step portion 54 is formed on the boundary between the high-order section 52 and the low-order section 53. A bent portion 55 is formed on a part of the first step portion 54. Specifically, the bent portion 55 concavely curved is formed on the upper surface of the insulation film 50 in the boundary portion between the side surface of the first step portion 54 and the low-order portion 53. The step portions on the insulation film 50 are formed on both (right and left) sides of the gate electrode 20 in FIGS.2 to 4, however, in this embodiment, the step portion of the left side (first step portion 54) in the figures is explained.
- [0022] FIG.5 is an enlarged view that illustrates the primary part V of FIG.1. In FIG.5, the dotted line and the dashed-dotted line represent the first step portion 54. In FIG.5, the

first step portion 54 is represented by the dotted line in the area where the emitter electrode 30 covers the first step portion 54. The first step portion 54 is represented by the dashed-dotted line in the area where the emitter electrode 30 does not cover the first step portion 54. Although the first step portion 54 is essentially invisible in planar view in the area where the emitter electrode 30 and the first step portion 54 are overlapping, the first step portion 54 is represented by the dotted line as a matter of convenience. In planar view as shown in FIG.5, the emitter electrode 30 is formed at a place where it overlaps with the first step portion 54.

[0023] An opening 51 is formed on the insulation film 50. The opening 51 is formed in the high-order section 52 of the insulation film 50. The opening 51 penetrates the insulation film 50. In cross-sectional view as in FIG.3, the opening 51 is not formed on the insulation film 50.

[0024] As shown in FIGS.2 and 4, a barrier-metal 80 is formed on the opening 51. The barrier-metal 80 covers the inner surface of the opening 51 and the upper surface of the gate electrode 20. In addition, the barrier-metal 80 covers a part of the upper surface of the insulation film 50. To form the barrier-metal 80, firstly, the barrier-metal 80 is formed over the whole of the insulation film 50. Then, unnecessary portions are removed by selectively etching the barrier-metal 80. In such a manner, the barrier-metal 80 is formed on the opening 51. After forming the barrier-metal 80, a barrier-metal residual substance 81 may be accumulated in the bent portion 55 of the step portion 54 of the insulation film 50. That is, even after carrying out the etching for the barrier-metal 80 formed over the whole of the upper surface of the insulation film 50, the barrier metal may be partially left untouched and remained in the bent portion 55. The residual substance 81 is a barrier-metal deposit, thus, having a conductivity.

[0025] Moreover, the opening 51 of the insulation film 50 is filled with gate wiring 40. The gate wiring 40 is formed on the barrier-metal 80. The gate wiring 40 contacts the gate electrode 20 through the barrier-metal 80. The gate wiring 40 is electrically connected to the gate electrode 20. The gate wiring 40 is formed on the upper part of the gate electrode 20. Therefore, the gate wiring 40 is formed on the high-order section 52 of the insulation film 50 but formed on neither the low-order section 53 nor the first step portion 54. In cross-sectional view as in FIG.3, the opening 51, barrier-metal 80, and gate wiring 40 are not formed.

[0026] Moreover, the emitter electrode 30 covers the upper surface of the semiconductor substrate 10. In cross-sectional view as in FIG.2, the emitter electrode 30 covers the low-order section 53, first step portion 54, and a part of the high-order section 52 of the insulation film 50. The emitter electrode 30 is formed away from the gate wiring 40. In cross-sectional view as in FIG.3, the emitter electrode 30 covers the low-order section 53, first step portion 54, and high-order section 52 of the insulation film 50. On the

other hand, in cross-sectional view as in FIG.4, the emitter electrode 30 does not cover the first step portion 54 of the insulation film 50. As shown in FIGS.2 to 4, the barrier-metal residual substance 81 is present in the bent portion 55. As shown in FIGS.2 and 3, in the portion where the emitter electrode 30 and the first step portion 54 are overlapping, the emitter electrode 30 covers the barrier-metal residual substance 81.

[0027] In planar view as shown in FIG.5, the first step portion 54 is extending in y-direction in the vicinity of the third region 43 while it is extending in x-direction in the vicinity of the first region 41. At the position represented by the dashed-dotted line, the first step portion 54 is not covered by the emitter electrode 30 and is exposing to the surface. That is, the first step portion 54 is not covered by any conductive member other than the emitter electrode 30. The connecting region 34 of the emitter electrode 30 covers the bent portion 55 of the first step portion 54.

[0028] As shown in FIG.5, the gate wiring 40 is formed so as not to overlap with the first step portion 54 at any place. That is, the gate wiring 40 does not cover the first step portion 54. Therefore, the gate wiring 40 does not contact the barrier-metal residual substance 81 which is accumulating in the first step portion 54.

[0029] As above, while the first step portion 54 is covered by the emitter electrode 30, the first step portion 54 is not covered by the gate wiring 40. In addition, as for the first step portion 54, the first step portion 54 is not covered by any conductive member other than the emitter electrode 30. Moreover, outside the range of FIG.5, the first step portion 54 is also not covered any conductive member other than the emitter electrode 30.

[0030] As clarified from above explanation, for the semiconductor device 1 having the above configuration, the first step portion 54 is covered by the emitter electrode 30 but not by the gate wiring 40. Thus, when the conductive barrier-metal residual substance 81 is accumulating in the first step portion 54, the residual substance 81 is contacted by the emitter electrode 30 but not by the gate wiring 40. As a result, the emitter electrode 30 and the gate wiring 40 will never be electrically connected via the residual substance 81 remaining in the first step portion 54. Therefore, the occurrence of short-circuit between the emitter electrode 30 and the gate wiring 40 owing to the conductive residual substance 81 remaining on the insulation film 50 can be suppressed. Moreover, since the first step portion 54 is not covered by any conductive member other than the emitter electrode 30, the occurrence of short-circuit between the emitter electrode 30 and a conductive member other than the gate wiring can also be suppressed.

[0031] In above semiconductor device 1, the emitter electrodes 30 includes the first region 31, the second region 32 separated from the first region 31, and the connecting region 34 for connecting the first region 31 and the second region 32. In such a configuration,

as compared to the configuration having no connecting region 34, the first step portion 54 formed on the upper surface of the insulation film 50 is likely to overlap with the emitter electrode 30. Therefore, the above configuration is especially effective in suppressing the occurrence of short-circuit between the emitter electrode 30 and the gate wiring 40 through the residual substance 81 accumulating in the first step portion 54.

[0032] (Second Embodiment)

One embodiment of the present invention has been explained above, however, specific aspects are not limited to the above embodiment. In the following explanation, the same reference signs used in the above explanation are used here for the same configuration to omit the explanation. In the above embodiment, a configuration for suppressing the occurrence of short-circuit between the emitter electrode 30 and the gate wiring 40 has been explained, however, the present invention is not limited to this configuration. As shown in FIG.6, the semiconductor device 1 of the second embodiment further includes a plurality of sense electrodes 60 (one example of first conductive members). In planar view, the sense electrodes 60 are aligned with clearances in between them. The sense electrodes 60 are connected to the emitter region of the IGBT as sense elements (one example of second switching elements). The sense electrodes 60 are formed between the first region 31 of the emitter electrode 30 and the first region 41 of the gate wiring 40, and between the second region 32 of the emitter electrode 30 and the second region 42 of the gate wiring 40. The sense electrodes 60 are used for detecting electric current and temperature.

[0033] In planar view, the emitter electrode 30, gate wiring 40, and sense electrodes 60 are separated apart from each other. The insulation film 50 is formed between the emitter electrode 30, gate wiring 40, and sense electrodes 60. The emitter electrode 30, gate wiring 40, and sense electrodes 60 are insulated from each other. The emitter electrode 30, gate wiring 40, and sense electrodes 60 have conductivity. Different potentials are respectively applied to the emitter electrode 30, gate wiring 40, and sense electrodes 60.

[0034] In cross-sectional view as in FIGS. 7 and 8, the semiconductor device 1 includes: a semiconductor substrate 10; an insulation film 70 formed on the semiconductor substrate 10; and a gate electrode 20 formed on the insulation film 70. The semiconductor device 1 also includes: an insulation film 50 formed on the gate electrode 20 and the semiconductor substrate 10; and an emitter electrode 30 formed on the insulation film 50 and the semiconductor substrate 10. The semiconductor device 1 further includes: a barrier-metal 80 formed on the gate electrode 20; and gate wiring 40 formed on the barrier-metal 80. The semiconductor device 1 still further includes a sense electrode 60 formed on the insulation film 50. Although two gate electrodes 20 are shown in FIG.8, these are just separated apart from each other in the cross-sectional

view as shown in FIG.8, they are connected at portions that are not depicted in the figure, thus having the same configuration. In this embodiment, the gate electrodes 20 shown in FIG.8 is referred to as: the left side gate electrode 20a for that on the left side; and the right side gate electrode 20b for that on the right side.

[0035] As shown in FIG.7, the upper surface of the insulation film 50 includes: a high-order section 52; a low-order section 53; and a second step portion 54. The high-order section 52, low-order section 53, and second step portion 254 are formed according to the thickness "t20" of the gate electrode 20. The second step portion 254 is formed according to the height positional difference between the high-order section 52 and the low-order section 53. The step portions on the insulation film 50 are formed on both (right and left) sides of the gate electrode 20 in FIG.7, however, in this embodiment, the step portion of the right side (second step portion 254) in the figure is explained. The high-order section 52 is formed on the gate electrode 20. The low-order section 53 and the second step portion 254 are formed on the flank of an edge 21 of the gate electrode 20. The low-order section 53 is formed on the semiconductor substrate 10. The second step portion 254 is formed between the high-order section 52 and the low-order section 53. The height of the high-order section 52 is higher than that of the low-order section 53. A bent portion 55 is formed on a part of the second step portion 254.

[0036] As shown in FIG.8, the upper surface of the insulation film 50 for covering the left side gate electrode 20a includes: a high-order section 52; a low-order section 53; and a third step portion 354. The high-order section 52, low-order section 53, and third step portion 354 are formed according to the thickness "t20" of the gate electrode 20. The third step portion 354 is formed according to the height positional difference between the high-order section 52 and the low-order section 53. The step portions on the insulation film 50 are formed on both (right and left) sides of the left side gate electrode 20a in FIG.8, however, in this embodiment, the step portion of the left side (third step portion 354) in the figure is explained. The high-order section 52 is formed on the left side gate electrode 20a. The low-order section 53 and the third step portion 354 are formed on the flank of the edge 21 of the left side gate electrode 20a. The third step portion 354 is formed between the high-order section 52 and the low-order section 53. The bent portion 55 is formed on a part of the third step portion 354.

[0037] As shown in FIG.8, the upper surface of the insulation film 50 for covering the right side gate electrode 20b includes: the high-order section 52; low-order section 53; and fourth step portion 454. The high-order section 52, low-order section 53, and fourth step portion 454 are formed according to the thickness "t20" of the gate electrode 20. The fourth step portion 454 is formed according to the height positional difference between the high-order section 52 and the low-order section 53. The step portions on the insulation film 50 are formed on both (right and left) sides of the right side gate

electrode 20b in FIG.4, however, in this embodiment, the step portion of the left side (fourth step portion 454) in the figure is explained. The high-order section 52 is formed on the right side gate electrode 20b. The low-order section 53 and the fourth step portion 454 are formed on the flank of the edge 21 of the right side gate electrode 20b. The fourth step portion 454 is formed between the high-order section 52 and the low-order section 53. The bent portion 55 is formed on a part of the fourth step portion 454.

[0038] As shown in FIG.7 and 8, a barrier-metal 80 is formed on the opening 51 of the insulation film 50. After forming the barrier-metal 80, a barrier-metal residual substance 81 may be accumulated in the second step portion 254, third step portion 354, and fourth step portion 454 of the insulation film 50. That is, even after carrying out an etching for the barrier-metal 80 formed over the whole of the upper surface of the insulation film 50, the barrier metal may be partially left untouched and remained on the surface of the second step portion 254, third step portion 354, and fourth step portion 454. Thereby, the residual substance 81 is accumulated in the second step portion 254, third step portion 354, and fourth step portion 454. The residual substance 81 is a barrier-metal deposit, thus, having a conductivity.

[0039] As shown in FIG. 7, an emitter electrode 30 is formed on the upper surface of the insulation film 50. The emitter electrode 30 is formed away from the gate wiring 40. Different potential is applied on the emitter electrode 30 and the gate wiring 40. The emitter electrode 30 covers the high-order section 52, low-order section 53, and the second step portion 254 of the insulation film 50. The emitter electrode 30 is formed on the second step portion 254, and contacts the barrier-metal residual substance 81 accumulated in the second step portion 254.

[0040] As shown in FIG. 8, the opening 51 of the insulation film 50 on the left side gate electrode 20a is filled with gate wiring 40. The gate wiring 40 is formed on the barrier-metal 80. The gate wiring 40 contacts the gate electrode 20 through the barrier-metal 80. The gate wiring 40 is electrically connected to the gate electrode 20. The gate wiring 40 is formed on the high-order section 52, low-order section 53, and third step portion 354 of the insulation film 50. The gate wiring 40 is formed on neither the second step portion 254 (not shown in FIG.8) nor the fourth step portion 454 of the insulation film 50. The low-order section 53 and the fourth step portion 454 are placed on the flank of the gate wiring 40. The gate wiring 40 is formed on the third step portion 354, and contacts the barrier-metal residual substance 81 accumulated in the third step portion 354.

[0041] As shown in FIG. 8, the sense electrode 60 is formed on the upper surface of the insulation film 50 on the right side gate electrode 20b. The opening 51 is not formed on the insulation film 50 on the right side gate electrode 20b. The insulation film 50 covers whole of the right side gate electrode 20b. The sense electrode 60 is formed on

the high-order section 52, low-order section 53, and fourth step portion 454 of the insulation film 50. The sense electrode 60 is formed on neither the second step portion 254 (not shown in FIG.8) nor the third step portion 354 of the insulation film 50. The sense electrode 60 is formed on the fourth step portion 454, and contacts the barrier-metal residual substance 81 accumulated in the fourth step portion 454.

[0042] The forming positions of the second step portion 254, third step portion 354, and fourth step portion 454 are different from that of the first step portion 54 in planar view, however, the configuration of these portions is the same as that of the first step portion 54 in cross-sectional view. That is, the second step portion 254, third step portion 354, and fourth step portion 454 are formed according to the thickness "t20" of the gate electrode 20. The second step portion 254, third step portion 354, and fourth step portion 454 are formed according to the height positional difference between the high-order section 52 and the low-order section 53. The second step portion 254, third step portion 354, and fourth step portion 454 are formed at a curved portion on the upper surface of the insulation film 50. The second step portion 254, third step portion 354, and fourth step portion 454 are formed on the flank of the edge 21 of the gate electrode 20. The second step portion 254, third step portion 354, and fourth step portion 454 are formed between the high-order section 52 and the low-order section 53.

[0043] The second step portion 254 is covered by the emitter electrode 30. The third step portion 354 is covered by the gate wiring 40. The fourth step portion 454 is covered by the sense electrode 60.

[0044] FIG.9 is an enlarged view that illustrates the primary part IX of FIG.6. In planar view as shown in FIG.9, the emitter electrode 30 is formed at a place where it overlaps with the second step portion 254. In FIG.9, the second step portion 254 is represented by the dotted line in the area where the emitter electrode 30 covers the second step portion 254. The second step portion 254 is represented by the dashed-dotted line in the area where the emitter electrode 30 does not cover the second step portion 254. Although the second step portion 254 is essentially invisible in planar view in the area where the emitter electrode 30 and the second step portion 254 are overlapping, the second step portion 254 is represented by the dotted line as a matter of convenience. In the area where the emitter electrode 30 and the second step portion 254 are overlapping, the emitter electrode 30 contacts the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the second step portion 254.

[0045] The second step portion 254 is extending in nearly parallel with the upper surface of the semiconductor substrate 10. In planar view as shown in FIG.9, the second step portion 254 is extending along the edge of the emitter electrode 30. The second step portion 254 is extending in the x direction and y direction of FIG.9. The second step

portion 254 is extending in a position that overlaps with the emitter electrode 30. On the other hand, the second step portion 254 is extending in a position that does not overlap with the gate wiring 40 and the sense electrode 60. The second step portion 254 is extending outside the edge of the gate wiring 40. In addition, the second step portion 254 is extending outside the edge of the sense electrode 60. The area of the second step portion 254 not overlapping with the emitter electrode 30 (the area represented by the dashed-dotted line in FIG.9) is exposed to the outside.

[0046] In planar view as shown in FIG.9, the gate wiring 40 is formed at a place where it does not overlap with the second step portion 254. The gate wiring 40 does not cover the second step portion 254. Therefore, the gate wiring 40 does not contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the second step portion 254. Moreover, in planar view as shown in FIG.9, the sense electrode 60 is formed at a place where it does not overlap with the second step portion 254. The sense electrode 60 does not cover the second step portion 254. Therefore, the sense electrode 60 does not contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the second step portion 254.

[0047] In addition, in planar view as shown in FIG.9, the gate wiring 40 is formed at a place where it overlaps with the third step portion 354. In FIG.9, the third step portion 354 is represented by the dotted line in the area where the gate wiring 40 covers the third step portion 354. Although the third step portion 354 is essentially invisible in planar view in the area where the gate wiring 40 and the third step portion 354 are overlapping, the third step portion 354 is represented by the dotted line as a matter of convenience. In the area where the gate wiring 40 and the third step portion 354 are overlapping, the gate wiring 40 contacts the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the third step portion 354.

[0048] The third step portion 354 is extending in nearly parallel with the upper surface of the semiconductor substrate 10. In planar view as shown in FIG.9, the third step portion 354 is extending along the edge of the gate wiring 40. The third step portion 354 is extending in the x direction of FIG.9. The third step portion 354 is extending as far as it overlaps with the gate wiring 40. On the other hand, the third step portion 354 is not extending as far as it overlaps with the emitter electrode 30 and the sense electrode 60. The third step portion 354 is extending outside the edge of the emitter electrode 30. In addition, the third step portion 354 is extending outside the edge of the sense electrode 60. The area of the third step portion 354 not overlapping with the gate wiring 40 (not shown) is exposed to the outside.

[0049] As planar view as shown in FIG.9, the emitter electrode 30 is formed at a place where it does not overlap with the third step portion 354. The emitter electrode 30 does not cover the third step portion 354. Therefore, the emitter electrode 30 does not

contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the third step portion 354. Moreover, in planar view as shown in FIG.9, the sense electrode 60 is formed at a place where it does not overlap with the third step portion 354. The sense electrode 60 does not cover the third step portion 354.

Therefore, the sense electrode 60 does not contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the third step portion 354.

[0050] In addition, in planar view as shown in FIG.9, the sense electrode 60 is formed at a place where it overlaps with the fourth step portion 454. In FIG.9, the fourth step portion 454 is represented by the dotted line in the area where the sense electrode 60 covers the fourth step portion 454. The fourth step portion 454 is represented by the dashed-dotted line in the area where the sense electrode 60 does not cover the fourth step portion 454. Although the fourth step portion 454 is essentially invisible in planar view in the area where the sense electrode 60 and the fourth step portion 454 are overlapping, the fourth step portion 454 is represented by the dotted line as a matter of convenience. In the area where the sense electrode 60 and the fourth step portion 454 are overlapping, the sense electrode 60 contacts the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the fourth step portion 454.

[0051] The fourth step portion 454 is extending in nearly parallel with the upper surface of the semiconductor substrate 10. In planar view as shown in FIG.9, the fourth step portion 454 is extending along the edge of the sense electrode 60. The fourth step portion 454 is extending in the x direction and y direction of FIG.9. The fourth step portion 454 is extending as far as it overlaps with the sense electrode 60. On the other hand, the fourth step portion 454 is not extending as far as it overlaps with the gate wiring 40 and the emitter electrode 30. The fourth step portion 454 is extending outside the edge of the gate wiring 40. The fourth step portion 454 is extending outside the edge of the emitter electrode 30. The area of the fourth step portion 454 not overlapping with the sense electrode 60 (the area represented by the dashed-dotted line in FIG.9) is exposed to the outside.

[0052] In planar view as shown in FIG.9, the gate wiring 40 is formed at a place where it does not overlap with the fourth step portion 454. The gate wiring 40 does not cover the fourth step portion 454. Therefore, the gate wiring 40 does not contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the fourth step portion 454. In addition, in planar view as shown in FIG.9, the emitter electrode 30 is formed at a place where it does not overlap with the fourth step portion 454. The emitter electrode 30 does not cover the fourth step portion 454. Therefore, the emitter electrode 30 does not contact the barrier-metal residual substance 81 (not shown in FIG.9) which is accumulating in the fourth step portion 454.

[0053] As clarified from above explanation, the semiconductor device 1 having above con-

figuration includes: the second step portion 254; third step portion 354; and fourth step portion 454, these formed on the upper surface of the insulation film 50 that covers the gate electrode 20 according to the thickness "t20" of the gate electrode 20. In addition, the emitter electrode 30 covers the second step portion 254, however, the gate wiring 40 and the sense electrode 60 having different potential from that of the emitter electrode 30 do not cover the second step portion 254. Thus, when the conductive barrier-metal residual substance 81 is accumulating in the second step portion 254, the emitter electrode 30 contacts the residual substance 81, but the gate wiring 40 and sense electrode 60 do not contact the residual substance 81. As a result, the emitter electrode 30, the gate wiring 40, and sense electrode 60 will never be electrically connected via residual substance 81 remaining in the second step portion 254. Therefore, the occurrence of short-circuit between the emitter electrode 30, gate wiring 40, and sense electrode 60 owing to the conductive residual substance 81 remaining in the insulation film 50 can be suppressed.

[0054] Similarly, the gate wiring 40 covers the third step portion 354, however, the emitter electrode 30 and the sense electrode 60 having different potential from that of the gate wiring 40 do not cover the third step portion 354. As a result, the gate wiring 40, emitter electrode 30, and sense electrode 60 will never be electrically connected via conductive residual substance 81 remaining in the third step portion 354. Therefore, the occurrence of short-circuit between the gate wiring 40, emitter electrode 30, and sense electrode 60 owing to the conductive residual substance 81 remaining on the insulation film 50 can be suppressed. Similarly, the sense electrode 60 covers the fourth step portion 454, however, the gate wiring 40 and the emitter electrode 30 having different potential from that of the sense electrode 60 do not cover the fourth step portion 454. As a result, the sense electrode 60, emitter electrode 30, and gate wiring 40 will never be electrically connected via conductive residual substance 81 remaining in the fourth step portion 454. Therefore, the occurrence of short-circuit between the sense electrode 60, emitter electrode 30, and gate wiring 40 owing to the conductive residual substance 81 remaining in the insulation film 50 can be suppressed.

[0055] Embodiments of the present invention have been explained above, however, specific aspects are not limited to those described above. For example, an IGBT was described as a switching element in the embodiment, however, the present invention is not limited to this configuration. A FET may be described as a switching element in other embodiment. In terms of a FET, a source electrode may be described as a first conductive member. The source electrode is a negative electrode.

[0056] In planar view, the locating position and configuration for the emitter electrode 30, gate wiring 40, and sense electrode 60 are not specially limited and may be modified as necessary.

[0057] As explained above, the step portion having a conductive barrier-metal residual substance 81 accumulated therein is covered by the first conductive member, but not covered by the other conductive member having different potential from that of the first conductive member. Thereby, the occurrence of short-circuit between the first conductive member and the conductive member other than the first conductive member through the conductive barrier-metal residual substance 81 can be suppressed.

[0058] (Third Embodiment)

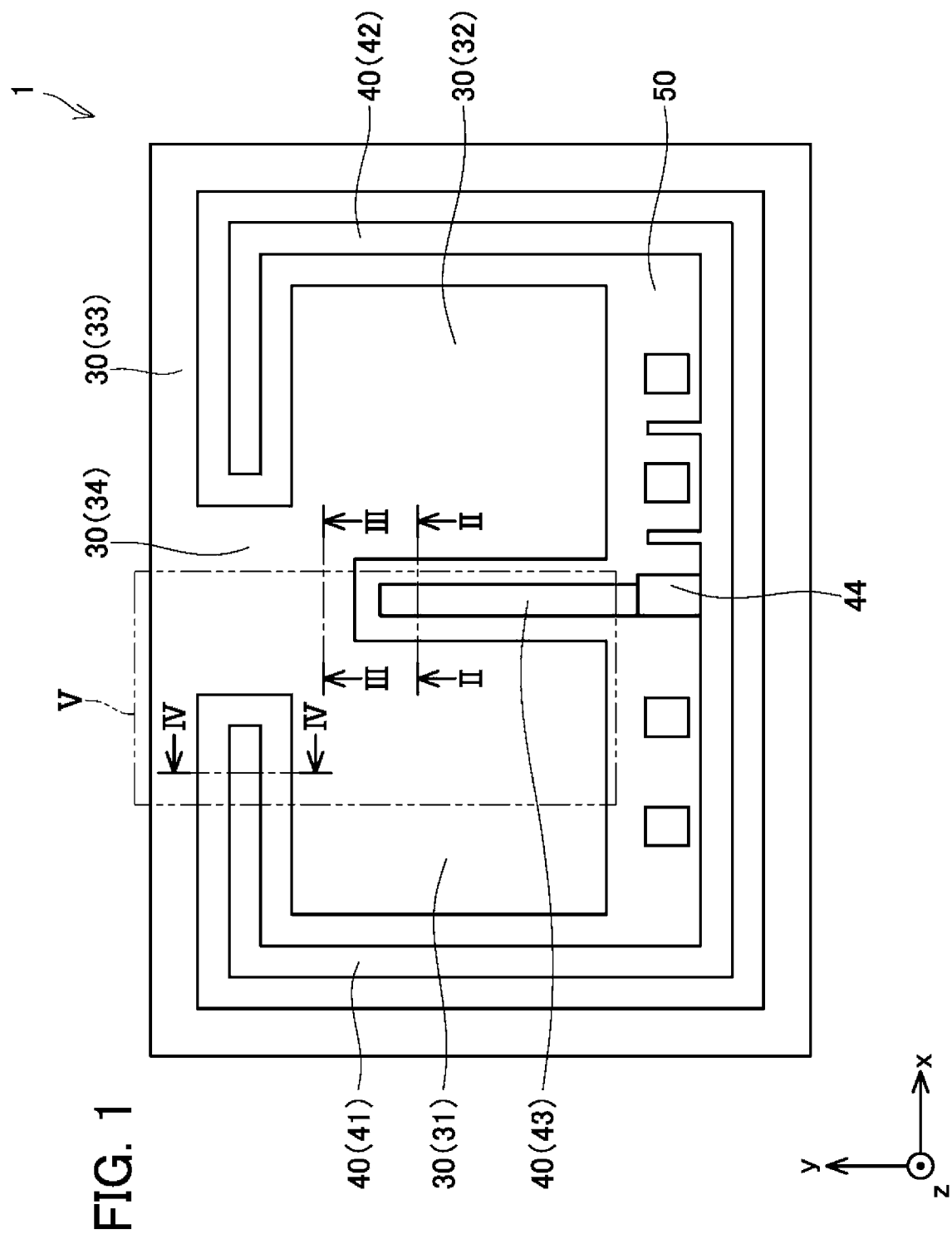
Specific aspects of the semiconductor device are not limited to above embodiments. For example, the configuration of the fourth step portion 454 is not limited to above embodiments. In another embodiment as in FIG.10, a plurality of fourth step portions 454 is formed in planar view. The plurality of fourth step portions 454 are formed with a clearance. Each of the fourth step portions 454 is formed at a place where it overlaps with the sense electrode 60. Each of the fourth step portions 454 is covered by the sense electrode 60. The conductive member other than the sense electrode 60 does not cover the fourth step portion 454.

[0059] Specific examples of the teachings herein have been described in detail, however, these are mere exemplary indications and thus do not limit the scope of the claims. The art described in the claims includes modifications and variations of the specific examples presented above. Technical features described in the description and the drawings may technically be useful alone or in various combinations, and are not limited to the combinations as originally claimed. Further, the art described in the description and the drawings may concurrently achieve a plurality of aims, and technical significance thereof resides in achieving any one of such aims.

Claims

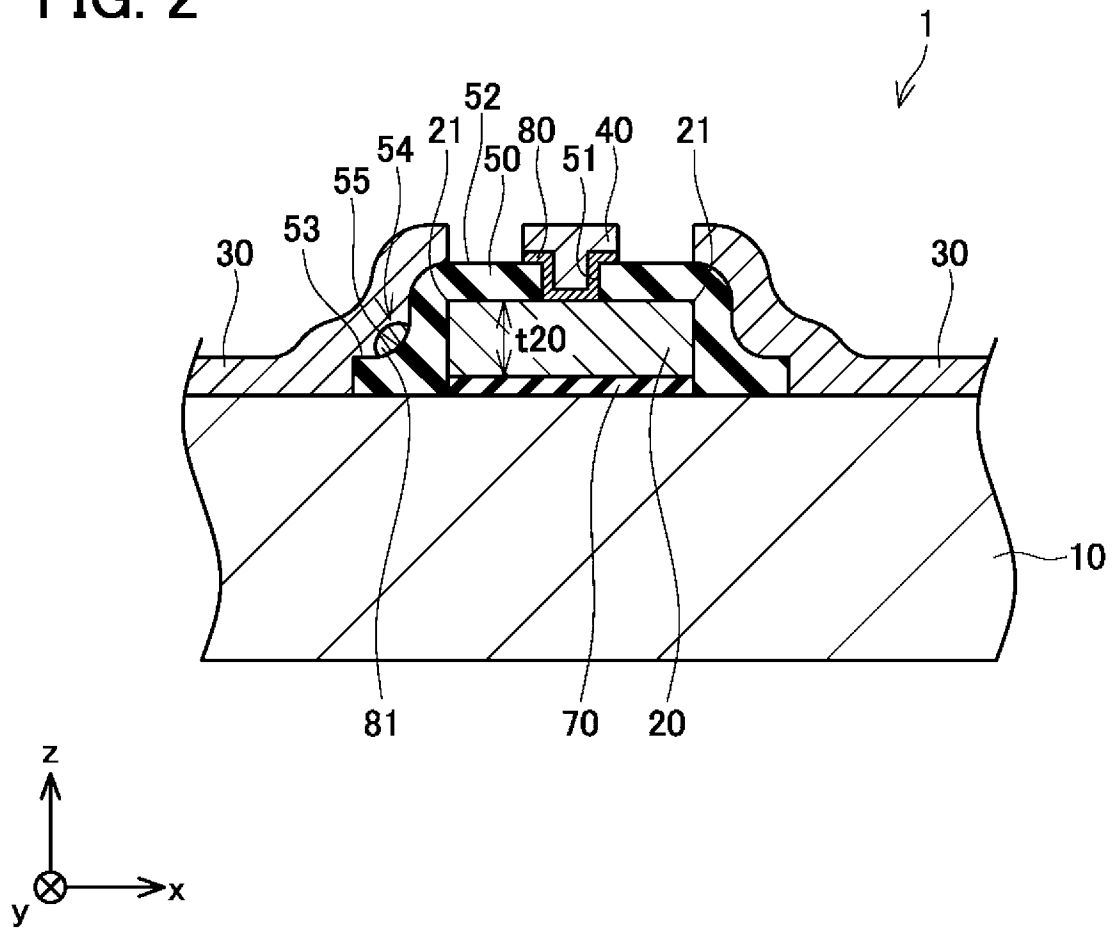
- [Claim 1] A semiconductor device, comprising:
a semiconductor substrate in which a first switching element is formed;
a gate electrode of the first switching element formed on the semiconductor substrate;
an insulation film covering the gate electrode and the semiconductor substrate;
a first conductive member formed on the insulation film; and
a gate wiring formed on the insulation film, separated from the first conductive member, and being in contact with the gate electrode;
wherein an upper surface of the insulation film comprises a first portion, a second portion, and a step portion, the first portion being located on the gate electrode, the second portion being located on the substrate, and the step portion being located between the first and second portions, and
the first conductive member covers the step portion, and the gate wiring does not cover the step portion.
- [Claim 2] The semiconductor device according to claim 1, wherein the gate wiring is formed on the first portion.
- [Claim 3] The semiconductor device according to claim 1 or 2, wherein the first conductive member is a negative electrode of the first switching element.
- [Claim 4] The semiconductor device according to claim 1 or 2, wherein a second switching element is further formed in the semiconductor substrate, and
the first conductive member is a negative electrode of the second switching element.
- [Claim 5] The semiconductor device according to claim 3 or 4, wherein the negative electrode comprises a first region, a second region formed with an interval from the first region, and a connecting region connecting the first region and the second region, and
the connecting region covers the step portion.

[Fig. 1]

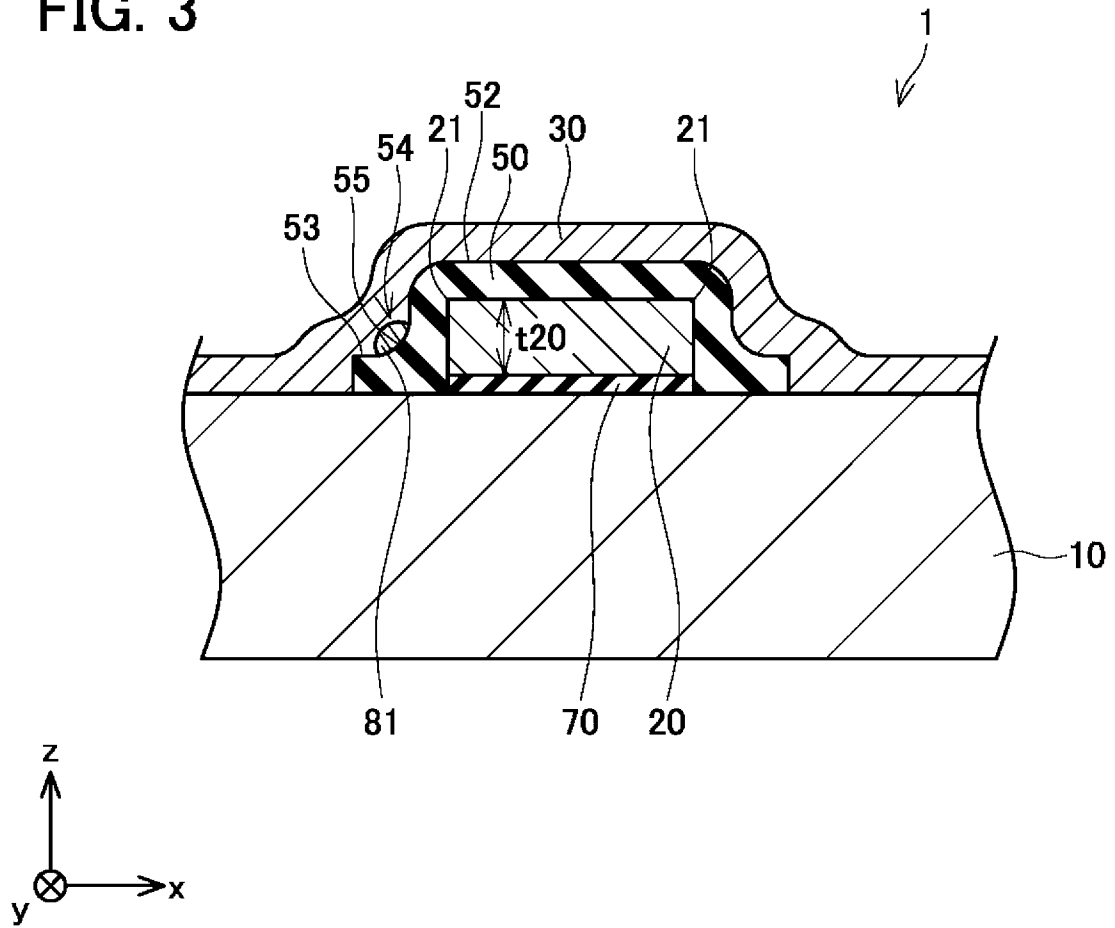


[Fig. 2]

FIG. 2

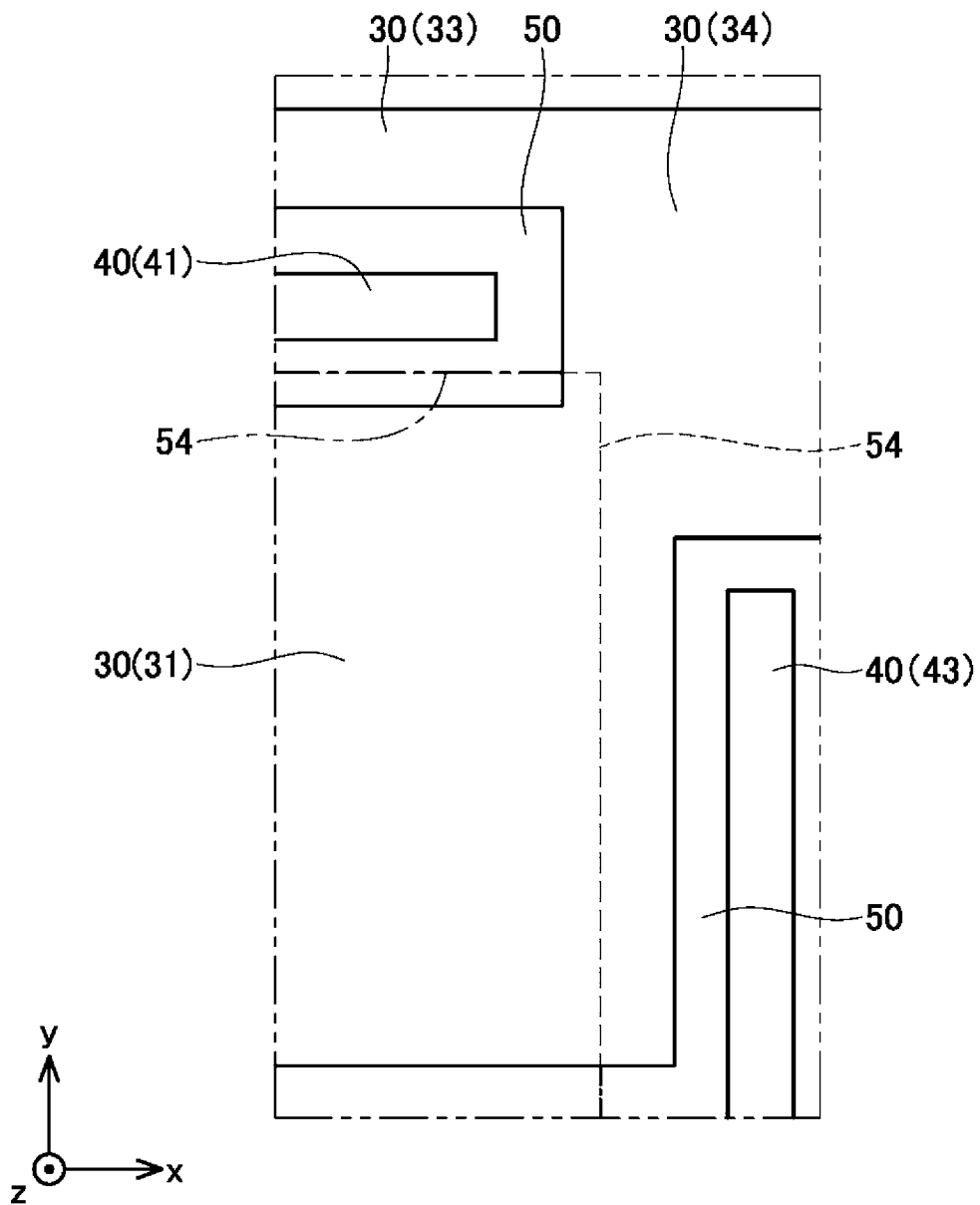


[Fig. 3]

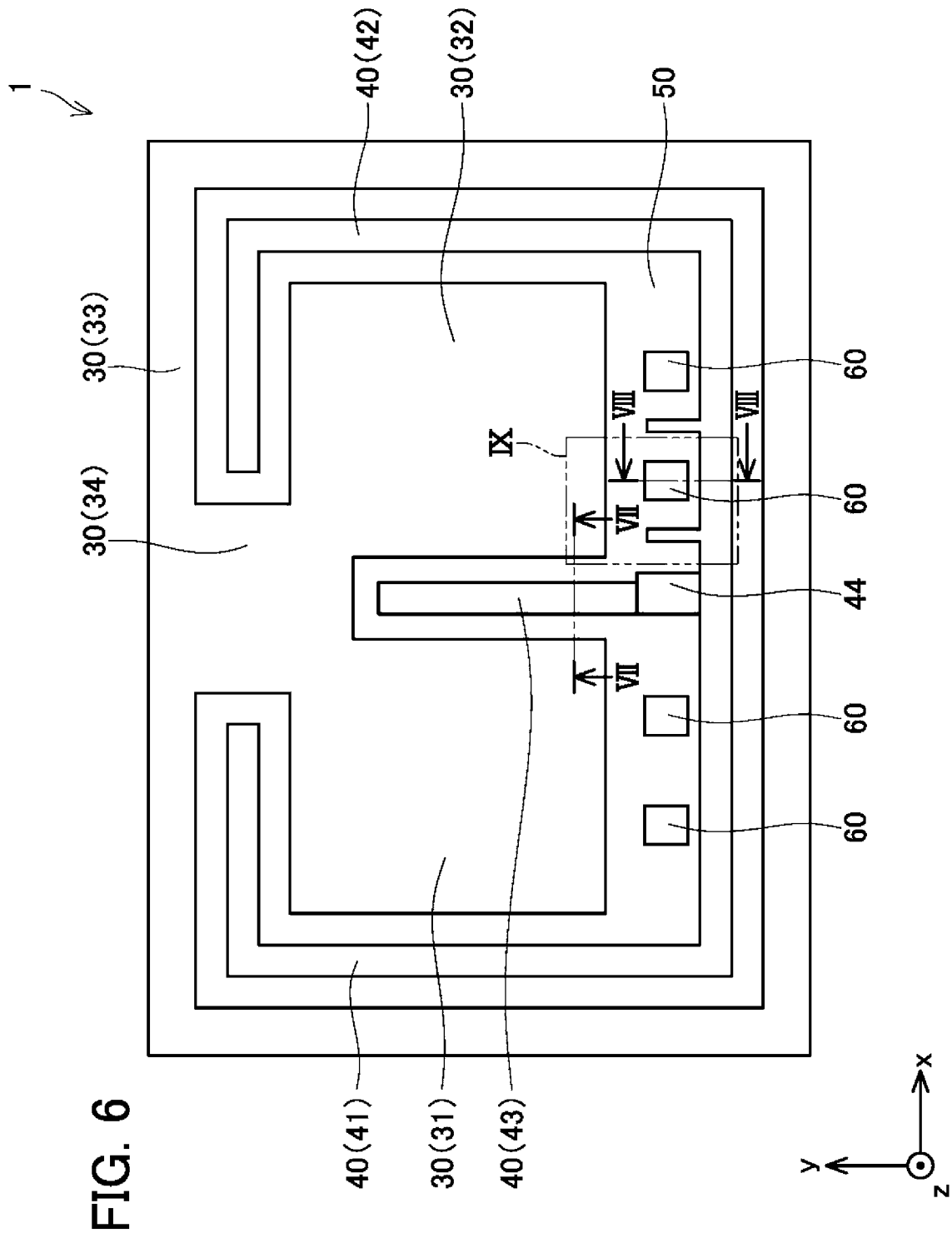
FIG. 3

[Fig. 5]

FIG. 5

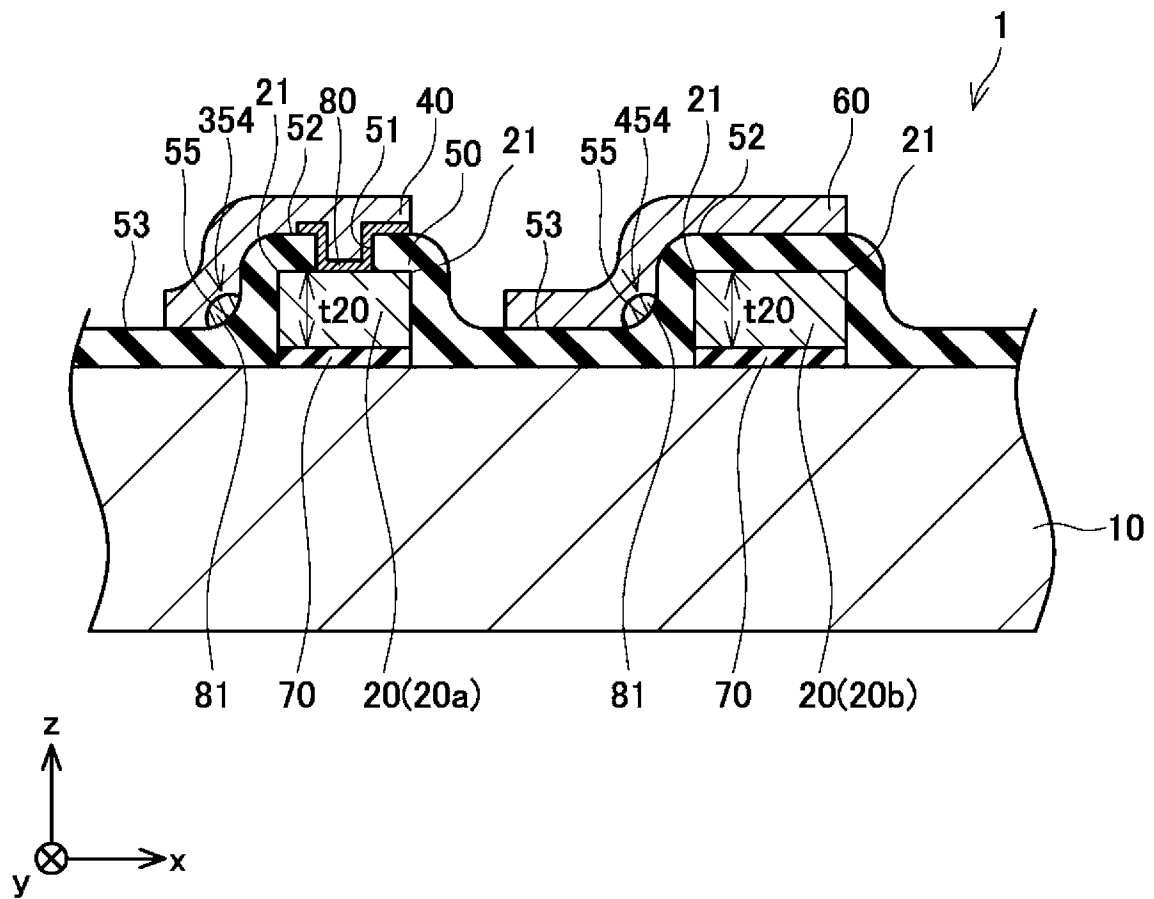


[Fig. 6]

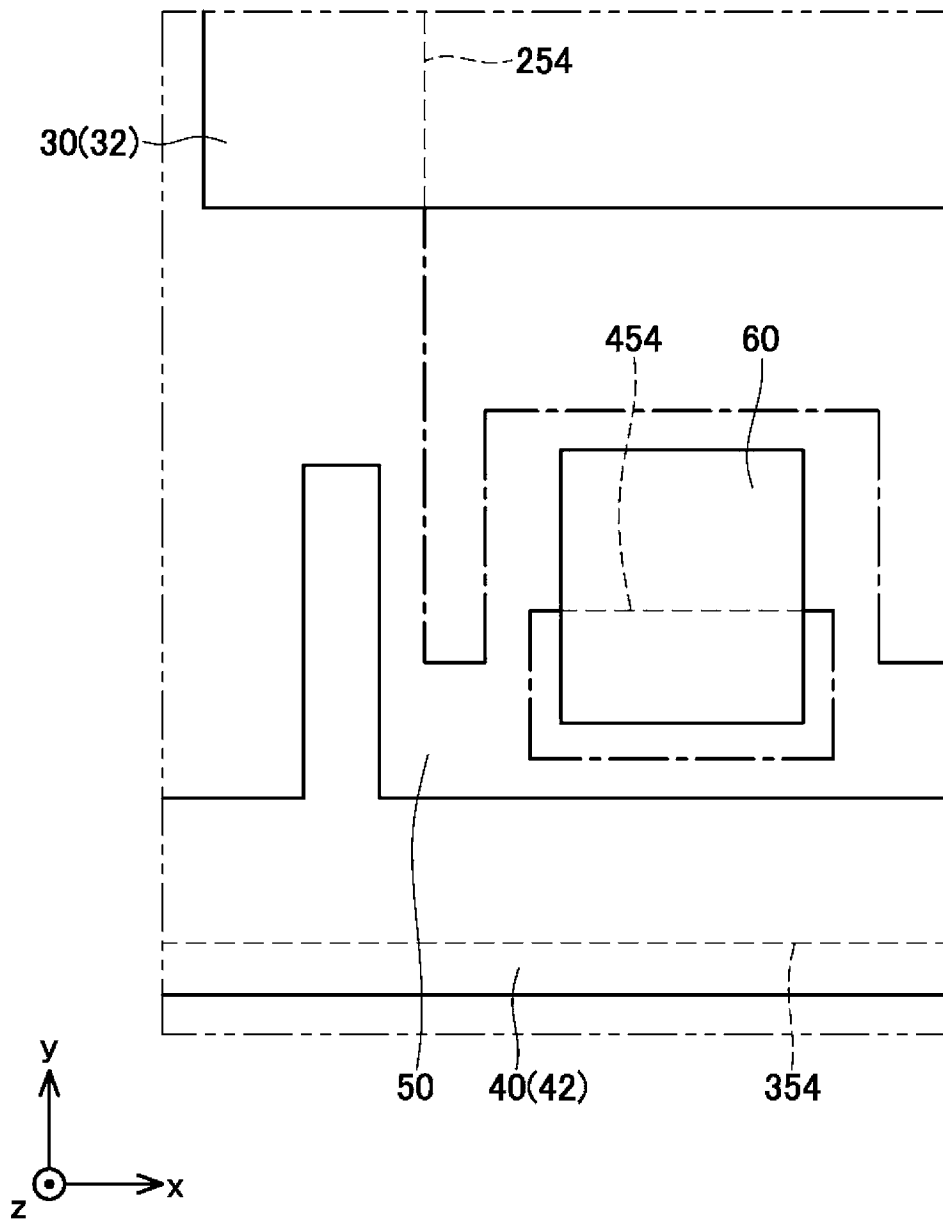


[Fig. 8]

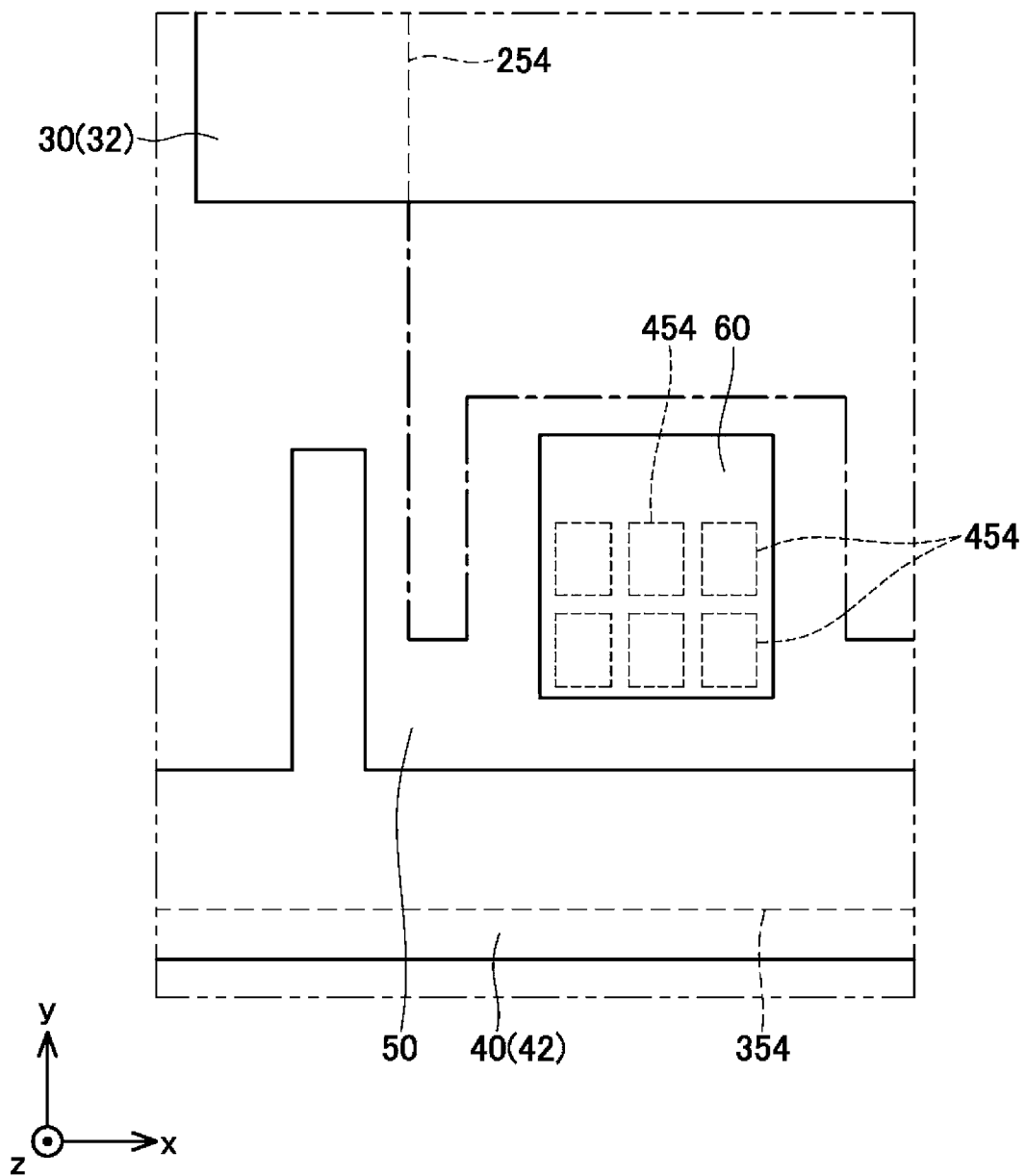
FIG. 8



[Fig. 9]

FIG. 9

[Fig. 10]

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2015/000081

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/739 H01L29/423 H01L29/08 H01L29/417
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/149079 A1 (SPRING KYLE [US]) 17 October 2002 (2002-10-17) paragraph [0009] - paragraph [0013] figure 1	1-5
X	----- US 2012/012861 A1 (NAKANO YUKI [JP] ET AL) 19 January 2012 (2012-01-19) paragraph [0174] - paragraph [0207] figures 15-18G	1-5
X	----- US 2012/267714 A1 (DIKSHIT ROHIT [US] ET AL) 25 October 2012 (2012-10-25) paragraph [0002] - paragraph [0004] figure 1	1-5
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search

11 March 2015

Date of mailing of the international search report

20/03/2015

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Kostrzewa, Marek

INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2015/000081

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 686 750 A (TAKAHASHI MITSUASA [JP]) 11 November 1997 (1997-11-11) column 3, line 52 - column 5, line 19 figures 1-3 -----	1-5
A	US 2008/079081 A1 (HASHIMOTO YASUNORI [JP]) 3 April 2008 (2008-04-03) paragraph [0008]; figure 13 -----	1-5

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/JP2015/000081

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			CN 103855223 A 11-06-2014
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			CN 202796963 U 13-03-2013
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			US 2008079081 A1 03-04-2008