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P/00/001
Section 29

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PATENT REQUEST : STANDARD PATENT

I/We, being the person(s) identified below as the Applicant(s), request the grant of a Standard Patent to the person(s) identified below as the Nominated Person(s), for an invention described in the accompanying complete specification.

Applicant(s) and Nominated Person(s): TANDEM COMPUTERS INCORPORATED

Address: 10435 NORTH TANTAU AVENUE
CUPERTINO
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Invention Title: IMPROVED POWER ON SYSTEM

Name(s) of Actual Inventor(s): MARK A TAYLOR; SAMSON K TOY

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BASIC CONVENTION APPLICATION DETAILS

Application No:	Country:	Application Date:
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Drawing number recommended to accompany the abstract: 1

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TANDEM COMPUTERS INCORPORATED

GRIFFITH HACK & CO.

Patent Attorney for and
on behalf of the Applicant

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Section 29(1)
Regulation 3.1(2)

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NOTICE OF ENTITLEMENT

I/We TANDEM COMPUTERS INCORPORATED

of 10435 NORTH TANTAU AVENUE
CUPERTINO
CALIFORNIA 95014
USA

being the applicant(s) in respect of an application for a patent for an invention entitled IMPROVED POWER ON SYSTEM, state the following:

1. The nominated person(s) has/have, for the following reasons, gained entitlement from the actual inventor(s):

   THE NOMINATED PERSON IS THE ASSIGNEE OF THE ACTUAL INVENTORS.

2. The nominated person(s) has/have, for the following reasons, gained entitlement from the basic applicant(s) listed on the patent request:

   THE APPLICANT AND NOMINATED PERSON IS THE ASSIGNEE OF THE BASIC APPLICANTS.

3. The basic application(s) listed on the request form is/are the first application(s) made in a Convention country in respect of the invention.

DATE: 20 June 1994

TANDEM COMPUTERS INCORPORATED

GRIFFITH HACK & CO.

Patent Attorney for and
on behalf of the applicant

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(54) Title
IMPROVED POWER ON SYSTEM

International Patent Classification(s)
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(56) Prior Art Documents
US 4493000
US 4428020
EP 0126242

(57) Claim

1. A system for supervising a supply voltage to assert a power on signal indicating that the supply voltage exceeds in magnitude a desired voltage value relative to a reference potential, the system including circuit means coupled to receive and monitor the supply voltage, the circuit means including means for providing a current when the supply voltage is less in magnitude than the desired voltage value, the circuit means terminating the current when the supply voltage exceeds the desired voltage value, and further including:

transistor means having a base terminal coupled to receive the current, and a collector terminal coupled to an output; and

shunt regulator means coupled between the base terminal and the reference potential to provide a current path between the base terminal and the reference potential when the supply voltage exceeds in magnitude a basic voltage level;

wherein the transistor means asserts the power on

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signal at the output when the supply voltage exceeds both the basic and the desired voltage levels.

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COMPLETE SPECIFICATION

STANDARD PATENT

Applicant:

TANDEM COMPUTERS INCORPORATED

Invention Title:

IMPROVED POWER ON SYSTEM

The following statement is a full description of this invention, including the best method of performing it known to me/us:

IMPROVED POWER ON SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates generally to circuits for monitoring a supply voltage to provide an indication of that the monitored voltage has reached a certain minimum value sufficient for operation of other electronic circuitry, or that the supply voltage has not dipped below that minimum. More particularly, the invention relates to an improved "power on" circuit capable of providing a valid indication of the state of a supply voltage during the initial stages of supply voltage application.

Power on (PON) circuits are commonly used to provide an indication that a supply voltage is at or exceedS a certain minimum specified value. The indication allows electronic circuitry operating from the supply voltage to be held in an off (non-operating) condition until the supply voltage has reached a voltage level that ensures reliable operation of the electronic circuitry. Alternatively, the indication may be used to reset the electronic (e.g., digital) circuitry, allowing it to begin operation from a known state when the supply voltage is known to have achieved a voltage level sufficient for operation.

A variety of PON circuits capable of performing the supervisory functions outlined above are available. Unfortunately, they are not capable of guaranteeing the validity of the indication of their supervisory operation until the supply voltage has reached at least some minimum voltage level (e.g., approximately 3 volts DC); that is, for a short period of time following application of power to an electronic system, while the supply voltage is building toward its specified voltage level (e.g., 5 volts), the PON circuit is unable to provide a valid reflection of the status of that supply voltage and may, in fact, indicate that a valid operating voltage level exists when, in fact, it does not.

In turn, an erroneous indication of a valid supply voltage, during this initial power-up, could cause a digital system, for example, to attempt operation to write incorrect and indeterminate data to a non-volatile memory. The problem would not be discovered until some time later, manifesting itself in, perhaps, a system failure when the indeterminate data is attempted to be used.

There have been attempts to add to commercially available PON circuits external guard circuits that couple the indication of the supply voltage to the operating electronic circuitry, inhibiting it until the supply voltage reaches a level at which the PON circuit can provide a valid reflection of the supply voltage. However, such guard circuits have been found to be unreliable.

SUMMARY OF THE INVENTION

The present invention provides a system for supervising a supply voltage to assert a power on signal indicating that the supply voltage exceeds in magnitude a desired voltage value relative to a reference potential, the system including circuit means coupled to receive and monitor the supply voltage, the circuit means including means for providing a current when the supply voltage is less in magnitude than the desired voltage value, the circuit means terminating the current when the supply voltage exceeds the desired voltage value, and further including:

transistor means having a base terminal coupled to receive the current, and a collector terminal coupled to an output; and

shunt regulator means coupled between the base terminal and the reference potential to provide a current path between the base terminal and the reference potential when the supply voltage exceeds in magnitude a basic voltage level;

wherein the transistor means asserts the power on

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signal at the output when the supply voltage exceeds both the basic and the desired voltage levels.

The present invention also provides a monitor system coupling to a direct current supply voltage to provide a power on indication at a monitor output that the supply voltage has achieved a desired voltage level relative to an initial voltage level, the system comprising:

supply voltage monitor means coupled to receive and operate from the supply voltage to assert the power on indication when the supply voltage reaches the desired voltage level; and

guard circuit means coupling the supply voltage monitor means to the monitor output to receive and communicate the power on indication to the monitor output only if the supply voltage has exceeded a safe voltage level, the safe voltage level being between the initial voltage level and the desired voltage level.

The present invention also provides a monitor system for supervising a supply voltage to provide a power on indication that the supply voltage exceeds a desired voltage value, the system including circuit means coupled to receive the supply voltage, the circuit means including first transistor means operating to provide a source of current when the supply voltage is below the desired voltage and to terminate the source of current when the supply voltage exceeds the desired voltage, the improvement comprising:

second transistor means having a base terminal coupled to receive the current provided by the first transistor means, an emitter terminal coupled to the supply voltage, and a collector lead;

resistance means coupling the collector terminal to a ground potential;

an output terminal coupled to the collector

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terminal of the second transistor, the power on indication being provided at the output terminal; and

shunt regulator means coupled to provide a current path from the base terminal to the ground when the supply voltage exceeds a first voltage;

wherein the second transistor means is caused to conduct to provide the power on indication when the supply voltage exceeds both the first and desired voltage.

In the preferred embodiment of the invention, the guard circuit includes an output transistor that is coupled to communicate an indication of supply voltage status provided by a conventional supply voltage monitor to an output terminal. Initially (i.e., at supply voltage levels below a predetermined level), the output transistor is held in a non-conducting state by a shunt regulator, blocking whatever supply voltage status indicated by the supply voltage monitor, and

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providing instead an indication that the supply voltage has not reached, or is below, a voltage necessary for valid circuit operation. The shunt regulator is coupled to the supply voltage, and is configured to conduct when the supply voltage reaches a predetermined voltage level that is sufficient for operation of the supply voltage monitor. Conduction of the shunt regulator causes the output transistor to communicate the supply voltage status provided by the supply voltage monitor to the output pin. From that point on, and as long as the supply voltage is above the predetermined voltage level sufficient for operation of the supply voltage monitor, the supply voltage monitor controls the supply voltage status indication that appears at the output terminal.

During the initial stages of a power-up, when the supply voltage has not reached a voltage level at which the conventional supply voltage monitor is capable of providing a valid output indication of supply voltage status, the output transistor is held in a non-conducting state to provide a secondary indication at the output terminal that the supply voltage has not yet reached the predetermined, safe level, regardless of what the conventional supply voltage monitor indicates. When, however, the supply voltage has reached a voltage level at and above which the conventional supply voltage monitor can correctly operate, and give a valid indication of supply voltage status, the shunt regulator conducts. With the shunt regulator in conduction, the secondary indication is controlled by the output of the conventional supply voltage monitor. When the supply voltage reaches the predetermined voltage at which safe operation of other electronic circuitry is ensured, the conventional supply voltage monitor will so indicate, and that indication will be passed to the output terminal of the guard circuit.

Among the advantages achieved by the present invention is that during the initial stages of power up (i.e., when the supply voltage is first applied), the status of the supply voltage is validly reported.

In addition, the guard circuit is configured so that it can be used with appropriate threshold adjustment without a

conventional supply voltage monitor to perform the monitoring functions, albeit without the features provided by conventional monitors.

These, and other advantages and features of the present invention, will become apparent to those skilled in the art to which the invention pertains upon reading of the following description of the preferred embodiment, which should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of supply voltage monitor system incorporating present invention; and

Fig. 2 is a time-voltage diagram, illustrating the operation of the monitor system shown in Fig. 1 as the supply voltage rises from an initial (no voltage) application.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning now to the figures, and for the moment specifically to Fig. 1, designated generally with the reference numeral 10 is a monitor system constructed according to the present invention for monitoring a supply voltage (Vcc). As shown, the monitor system 10 includes a commercially available supply voltage monitor U1 coupled to the supply voltage Vcc. An output terminal 12, connected to an open collector output of a transistor Q1 of the supply voltage monitor, is connected to a base lead of a PNP transistor Q2 that forms a part of a guard circuit 14. The emitter terminal of the transistor Q2 connects to the supply voltage Vcc through resistor R2, and the collector of the transistor Q2 connects to a ground (G) potential through resistor R6. At the junction between the collector of the transistor Q2 and the resistance R6 is an output terminal O whereat a power on (PON) signal is presented to indicate the supply voltage has reached and/or exceeded a voltage level deemed a safe operating voltage. As will be seen, the PON signal is a secondary indication of the supply voltage status during the initial stages of power-on. When the supply voltage reaches a voltage level at which the supply voltage

monitor U1 is considered to be able to give a valid indication, the PON signal will follow the indication supplied at the output 12.

The output terminal 12, is also connected to one terminal of a resistor R3; the other terminal of the resistor R3 connects to the junction between a resistor R1 and a shunt regulator U2. As can be seen, the resistor R1 and the shunt regulator U2 form a series circuit between the supply voltage Vcc and ground potential G.

The shunt voltage regulator U2 includes a control pin 16 that connects to a voltage divider network consisting of resistors R4 and R5. Resistors R4, R5 form a series path between the supply voltage Vcc and the ground potential G to develop between them a control voltage that is indicative of the supply voltage Vcc.

The supply voltage monitor U1 is an off-the-shelf item that is manufactured by Texas Instruments of Dallas Texas, and sold under the Part No. TL7702. It has two open collector outputs, one as shown in Fig. 1 (i.e., Q1), and the other formed by the collector of an NPN transistor. The present invention is shown using ~~uses~~ the open collector output of the PNP transistor. The monitor U1 operates to monitor the supply voltage Vcc, turning on the transistor Q1 to allow it to ~~to it to~~ source current when the supply voltage Vcc is below the predetermined voltage level. When the predetermined voltage level is reached by the supply voltage, the transistor Q1 is turned off.

At low levels of supply voltage, however, such as during, for example, the time that the supply voltage is initially applied, the monitor U1 may not be able to correctly reflect the status of the supply voltage Vcc, i.e., it is indeterminate. It is the function, therefore, of the guard circuit 14 to obviate that indeterminacy and ensure a proper reflection of supply voltage status during low levels (e.g., during initial turn-on or power-up) of the supply voltage.

Operation of the monitoring system 10, and in particular the guard circuit 14, will be understood with reference to Fig. 2, in which a waveform 20 portrays the rise

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of the supply voltage Vcc over time, beginning at an initial time t_0 when the supply voltage was essentially zero volts. The waveform 22 depicts the state of the transistor Q1 of the monitor U1, showing that for an initial period of time (t_0 to t_1) the output 12 from the collector of the transistor Q1 is indeterminate, in the sense that it can be in an state (i.e., conducting or non-conducting). This indeterminacy is indicated on the waveform 22 by the cross-hatched area 23. However, when, at time T_1, the supply voltage Vcc reaches the voltage level v_1, output 12 of the monitor U1 can be relied upon, i.e., it now supplies a valid indication of the status of the supply voltage.

The waveform 24 shows the voltage level at node A. When the shunt regulator U2 is not conducting, the voltage level at node A will be pulled up toward supply voltage level. The values of the resistors forming the voltage divider network R4/R5 are selected so that the shunt regulator will not conduct until the supply voltage Vcc reaches and/or exceeds a voltage level v_2. Thus, during the time period t_0 - t_1, and regardless of the conduction state of the transistor Q1 of the monitor U1, since there is no current path to the ground potential at the base of the transistor Q2, the base will be pulled up toward the supply voltage Vcc, and the transistor Q2 will be in non-conduction. The collector of the transistor Q2 will, therefore, be pulled toward the ground potential G, and the PON output signal will be in a non-asserted state as illustrated by the waveform 26.

When, at time t_1, the supply voltage Vcc has reached a first voltage level V_1, the monitor U1 (validly) turns on the transistor Q1 to that it can source current. The monitor U1 can now validly control the transistor Q2. However, the level of the supply voltage is still below that needed to place the shunt regulator in conduction. Thus, the transistor Q2 remains cut-off for lack of a current path.

At time T_2 the supply voltage Vcc reaches a voltage level V_2, and the shunt regulator conducts. The voltage at node A (waveform 24) will drop toward the ground potential, and the base of the transistor Q2 now has a current path to

the ground potential - through the shunt regulator U2. However, the open collector output of the monitor U1, being set to trip at a higher voltage level (v_3) will continue to source current, keeping the transistor Q2 from conducting because of the increased voltage drop across R3.

At time t_3, when the supply voltage Vcc reaches a voltage level of v_3, the device U1 (which has been programmed to trip at the v_3 level) will turn off the transistor Q1. The shunt regulator U2 alone continues to conduct, and pulls the base of the transistor Q2 toward ground, and placing the transistor in conduction. The current through the resistor R6 asserts the PON signal, indicating that the supply voltage has now reached and/or exceeded the predetermined voltage level (e.g., v_3) considered appropriate for other electronic circuit operation.

The foregoing discussion of the operation of the supply voltage monitoring system 10 illustrates two important points of the present invention. First, even when the supply voltage is at a voltage level insufficient for proper operation of an off-the-shelf monitor, the PON signal remains validly un-asserted. Second, two voltage levels must be reached and/or exceeded by the supply voltage before PON is asserted to reflect an in-regulation status of the supply voltage, the voltage level v_2 to cause the shunt regulator to conduct, and the voltage level v_3 at which the device U1 is programmed to indicate the in-regulation status of the supply voltage.

The shunt regulator U2 is preferably a programmable precision reference, manufactured by Motorola Semiconductor, and sold under the part number TL431. The monitor system 10 was designed to operate to monitor a nominal supply voltage of 5 volts DC. The voltage divider resistor (R4/R5) were selected to cause the shunt regulator to conduct at about 3.8 volts, slightly above the voltage level for which the monitor U1 is guaranteed to provide a valid output. The monitor U1 is programmed to assert an indication of safe supply voltage when the supply voltage level reached or exceeded approximately 4.85 volts. Resistor values are:

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R1:	10K ohms	R4:	1.07K ohms
R2:	470 ohms	R5:	1.58K ohms
R3:	1K ohms	R6:	1K ohms

In summary, there has been disclosed a monitor system 10, including a conventional supply voltage monitor U1 and a guard circuit 14, capable of validly reflecting the status of the out-of-regulation state of a supply voltage at low voltage levels. It will be recognised by those skilled in this art that while the operation of the invention has been described in terms of a rising supply voltage, the invention will perform in the same manner as described for a falling supply voltage. Thus, if after having reached and/or exceeded a valid supply voltage level, and having been indicated as such assertion of the PON signal, the supply voltage drops to a level insufficient for circuit operation, the monitor U1 will turn on the transistor Q1 to cause it to begin sourcing current. This, in turn, will turn off transistor Q2, de-asserting the PON signal to indicate that the supply voltage has dropped below the level considered safe for operation.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A system for supervising a supply voltage to assert a power on signal indicating that the supply voltage exceeds in magnitude a desired voltage value relative to a reference potential, the system including circuit means coupled to receive and monitor the supply voltage, the circuit means including means for providing a current when the supply voltage is less in magnitude than the desired voltage value, the circuit means terminating the current when the supply voltage exceeds the desired voltage value, and further including:

transistor means having a base terminal coupled to receive the current, and a collector terminal coupled to an output; and

shunt regulator means coupled between the base terminal and the reference potential to provide a current path between the base terminal and the reference potential when the supply voltage exceeds in magnitude a basic voltage level;

wherein the transistor means asserts the power on signal at the output when the supply voltage exceeds both the basic and the desired voltage levels.

2. The system of claim 1, wherein the reference potential is a ground potential.

3. The system of claim 2, wherein the supply voltage varies between the ground potential and a positive voltage level.

4. The system of claim 1, wherein the transistor means has an emitter terminal coupled to the supply voltage, and including resistance means coupling the collector terminal to the reference potential and an output terminal coupled to the collector terminal whereat the

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indication is provided.

5. The system of claim 1, wherein the basic voltage level is between the reference potential and the desired voltage level.

6. The system of claim 5, wherein the reference potential is a ground potential.

7. The system of claim 6, wherein the supply voltage is positive.

8. The system of claim 1, wherein the shunt regulator means includes a voltage divider means coupled to the supply voltage to indicate when the magnitude of the supply voltage exceeds the basic voltage level.

9. The system of claim 1, wherein the shunt regulator means includes voltage generating means coupled to the supply voltage for providing an indication of the supply voltage exceeding the basic voltage level, and circuit means coupled to receive the indication and conduct when the indication is provided.

10. A monitor system for coupling to a direct current supply voltage to provide a power on indication at a monitor output that the supply voltage has achieved a desired voltage level relative to an initial voltage level, the system comprising:

supply voltage monitor means coupled to receive and operate from the supply voltage to assert the power on indication when the supply voltage reaches the desired voltage level; and

guard circuit means coupling the supply voltage monitor means to the monitor output to receive and communicate the power on indication to the monitor output

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only if the supply voltage has exceeded a safe voltage level, the safe voltage level being between the initial voltage level and the desired voltage level.

11. The monitor system of claim 10, wherein the initial voltage level is a ground potential.

12. The monitor system of claim 11, wherein the supply voltage is positive.

13. The monitor system of claim 11, wherein the supply voltage is approximately a positive 5 volts.

14. The monitor system of claim 10, wherein the guard circuit means includes transistor means having a base terminal coupled to receive the power on indication from the supply voltage monitor means, a shunt regulator coupled to the supply voltage and to the base terminal, and wherein the transistor means operates to conduct to communicate the power on indication to the monitor output when the supply voltage exceeds the safe voltage level to cause the shunt regulator means to form a current path for the base terminal to the ground potential.

15. A monitor system for supervising a supply voltage to provide a power on indication that the supply voltage exceeds a desired voltage value, the system including circuit means coupled to receive the supply voltage, the circuit means including first transistor means operating to provide a source of current when the supply voltage is below the desired voltage and to terminate the source of current when the supply voltage exceeds the desired voltage, the improvement comprising:

second transistor means having a base terminal coupled to receive the current provided by the first transistor means, an emitter terminal coupled to the supply

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voltage, and a collector lead;

resistance means coupling the collector terminal to a ground potential;

an output terminal coupled to the collector terminal of the second transistor, the power on indication being provided at the output terminal; and

shunt regulator means coupled to provide a current path from the base terminal to the ground when the supply voltage exceeds a first voltage;

wherein the second transistor means is caused to conduct to provide the power on indication when the supply voltage exceeds both the first and desired voltage.

16. The system of claim 15, wherein the first voltage is less than the desired voltage.

17. The system of claim 16, wherein the shunt regulator means includes a voltage divider circuit coupled to the supply voltage to provide the first voltage.

18. The system of claim 17, wherein the shunt regulator means includes means having a control pin coupled to the voltage divider circuit to be placed in a conducting state when the first voltage is provided.

Dated this 18th day of December 1996

TANDEM COMPUTERS INCORPORATED
By Its Patent Attorneys:

GRIFFITH HACK
Fellows Institute of Patent
Attorneys of Australia.

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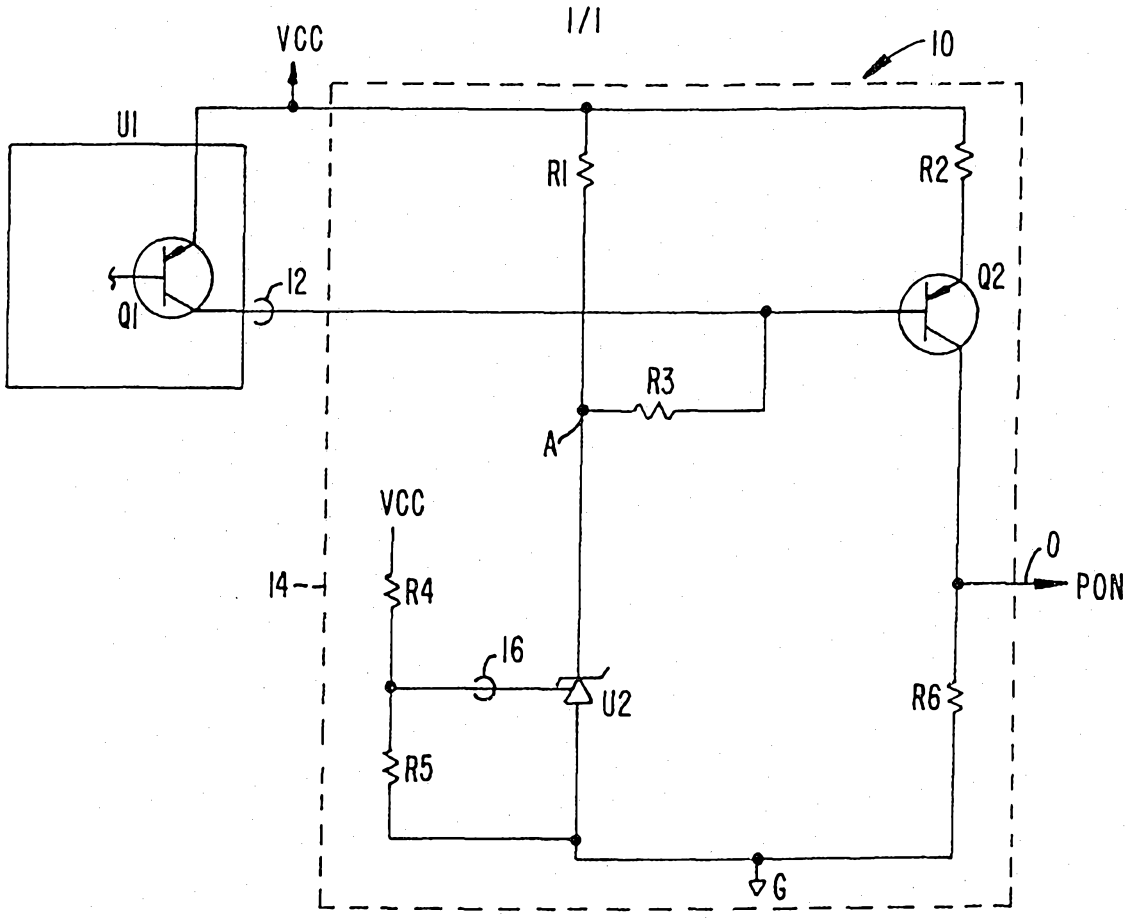
IMPROVED POWER ON SYSTEM

ABSTRACT OF THE DISCLOSURE

A supply voltage monitor for providing an indication of a supply voltage level considered safe for electronic circuit operation includes a supervisory or guard circuit that blocks the output of the monitor in favor of a secondary output for those periods of time when the monitor is considered to not be able of providing a valid reflection of supply voltage status.


VCC
10
U1
R1
R2
Q1
12
Q2
R3
A
VCC
14
R4
16
U2
R6
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PON
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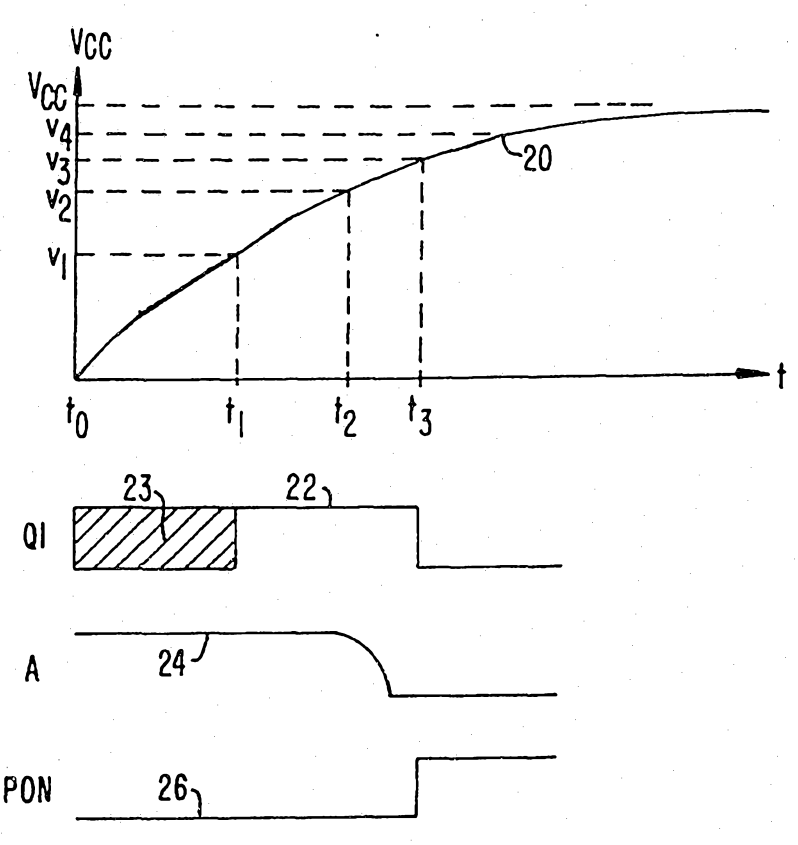
FIG. 1.

FIG. 2.


VCC
V_{CC}
v_4
v_3
v_2
v_1
20
t
t_0
t_1
t_2
t_3
23
22
Q1
A
24
PON
26