May 7, 1968 W. R. ARMSTRONG 3,382,417

TIME DELAY RELAY DEVICE

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FIG. 1.

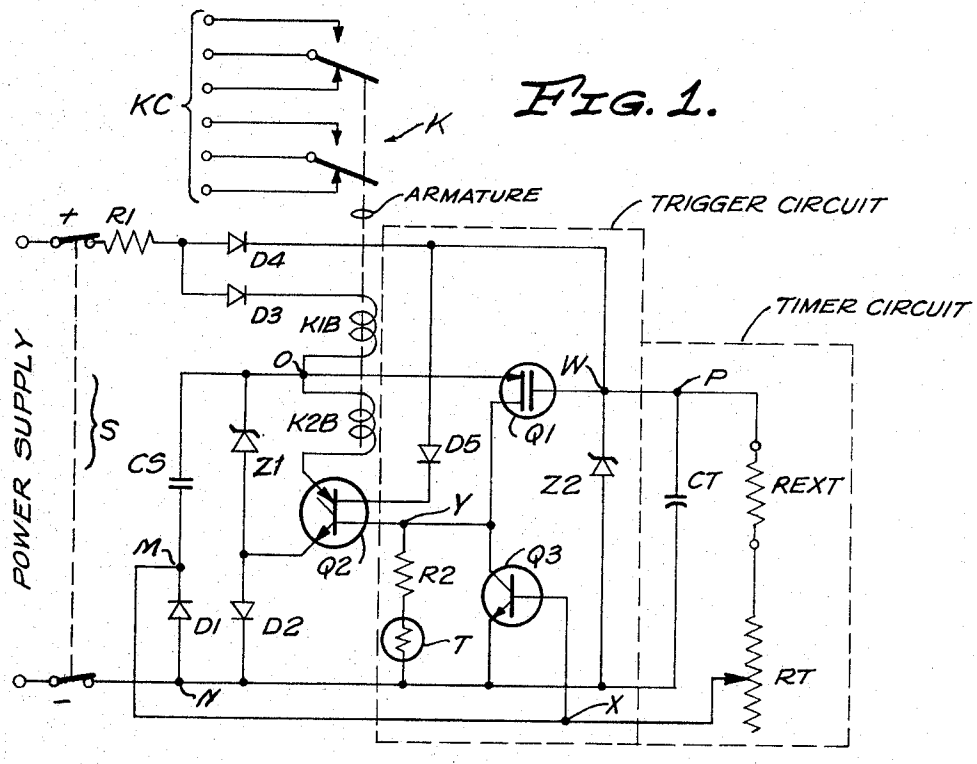
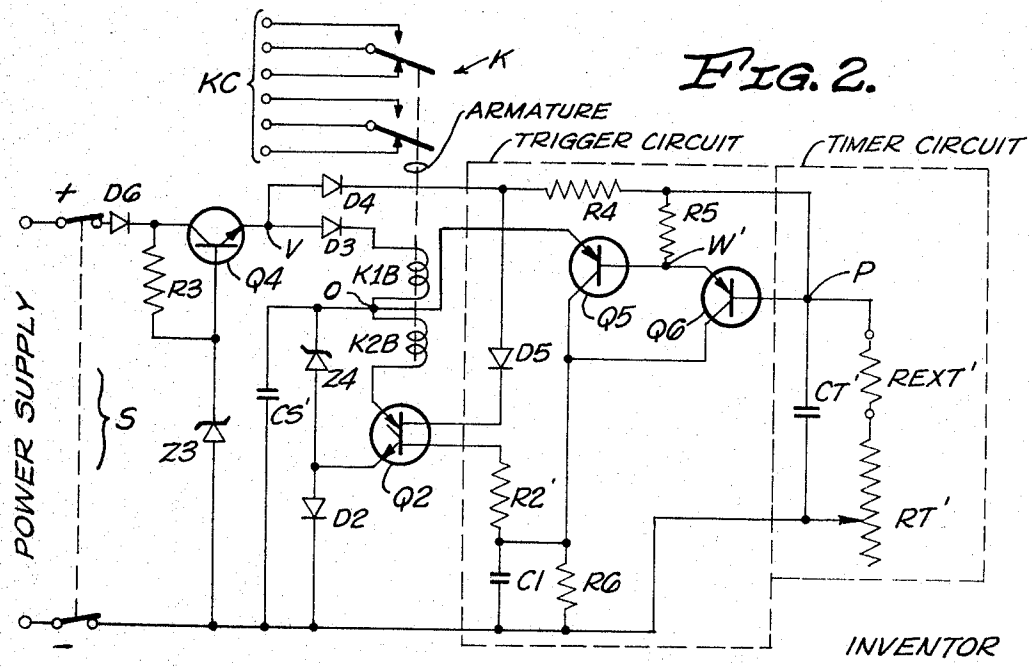


FIG. 2.



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TIME DELAY RELAY DEVICE

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The invention herein disclosed pertains to electrical relays, and more particularly to improvements in means for effecting time-delay in the drop-out of the relay following opening of the relay power circuit. More succinctly stated, the invention pertains to improvements in time-delayed drop-out relay devices, commonly called "dodo" relays.

Various means have heretofore been proposed for the purpose of delaying the drop-out or return to inactive state of the contacts of an electrical relay. Those means include such simple means as conductive slugs arranged to alter the time-rate-of-change of the magnetic field of the relay electromagnet, and electric or electronic circuit means utilizing energy derived separately from the relay energizing line after opening of the relay power source, for causing change-of-position of the relay armature at a more-or-less determinable time following de-energization of the relay electromagnet. Also it is known in the art to use energy derived from the relay-energizing line during the active period of energization and stored in energy-storing means, for effecting drop-out at a more-or-less determinable time after de-energization of the line. Usually such energy-storing means comprises an electrical capacitor connected to receive a charge during the period of active energization of the relay electromagnet and connected to initiate change-of-state of the relay after decay of the stored charge to a determined energy level. In the more modern prior art relays to which the present invention has pertinence the relay armature is arranged to be maintained in either state by latching means, usually a permanent magnet, and the electromagnet means used to move the armature is divided into two coils the first of which is arranged to draw the armature into the set or pull-in state and the second of which is later energized to draw the armature to the fall-out or reset state against the metastable coercion or bias of the latching means.

Typical of prior art time-delay relay devices over which the present invention attains marked improvements are one in which there is continuous flow of current through a circuit shunting the relay-controlling and actuating circuits during operation of the relay, and another in which a special control circuit is used which must be supplied with power continuously. The first of the two noted relays is characterized by rather large power consumption due to the auxiliary shunt circuit, much of which power is in effect wasted and detrimentally creates heat which requires means for dissipation and which adversely raises the temperature of the environment. The second of the noted relays requires continuous supply of power during the entire period from initiation of action of the relay, through pull-in, hold, initiation of reset or drop-out, the period of "time delay" and reset or drop-out; and since drop-out is initiated by opening of the principal power circuit of the relay, a special auxiliary power circuit, continuously energized, is necessary for the control circuit. Obviously, the addition of the last-mentioned circuit adds to the cost and space requirements of the relay, and in operation is a source of undesired heat. As is known to those skilled in the art, the characteristics of electronic components vary with variation of ambient temperature, and are generally adversely affected by increasing temperatures.

The aforementioned adverse and undesirable characteristics of the prior-art relays are obviated or overcome by the present invention. According to the present invention power is supplied to the relay via only a single pair of conductors (a single line), and initiation of pull-in (set) and of drop-out (reset) is effected by closing and opening of the line, respectively, without other or auxiliary power being supplied. Further, during the active period of the relay, that is, while it is in the pulled-in state, there is a small current flow to the circuitry so no significant or adverse rise in ambient temperature occurs. The current used to effect pull-in is stored in capacitive means and is later used, via discharge through the reset or drop-out coil, to return the relay armature to idle or "off" position. By using unique pull-in circuitry and very low-loss gate means, timing and gate-triggering means, not only is the relay device made exceptionally inexpensive to manufacture but also it is made to be substantially insensitive to wide variations of ambient operating temperature and concurrently such as to occupy only a fraction of the space required by the noted prior art devices. Briefly, the relay device according to the invention comprises a capacitive circuit arranged to become charged by current used to activate the pull-in coil of the relay, triggerable gate circuit means normally presenting very high impedance to discharge of the charged capacitor but permitting rapid discharge through the drop-out coil of the relay when triggered, gate-triggering circuit means, and timing-circuit means arranged to control the triggering circuit a determinable time following opening of the relay power line. The triggering circuit means can be of alternate forms, and the circuitry may, and desirably does, include means for rendering the time-delay insensitive to supply-line voltage variations and to variations of temperature of the ambient.

The preceding brief general description of the invention makes it evident that it is a principal object of the invention to provide improvements in relays characterized by predetermined delay of drop-out following opening of the relay input line, that is, in relay devices known as time delay on drop-out relays.

Another object of the invention is to provide a time delay relay device characterized by accurately delayed drop-out following line-opening, irrespective of line voltage fluctuations and variation of ambient temperature.

Another object of the invention is to provide a magnetic latching time delay relay device of improved efficiency and having circuit means utilizing the electricity employed in activating the pull-up coil to later energize the drop-out coil.

Another object of the invention is to provide a time delay relay device having an energy-controlling gate circuit and improved efficient triggering and timing circuit means for controlling the gate circuit.

Another object of the invention is to provide a time delay relay device including improved means for rendering relay operation independent of fluctuations of input line potential variations.

Another object of the invention is to provide a time delay relay device having means for improving the accuracy of the time delay of the drop-out of the armature subsequent to opening of the relay circuit.

The preceding objects are attained by the invention as are other objects hereinafter stated or made evident in the appended claims or the following description of preferred means incorporating the invention as schematically depicted in the accompanying drawings. In the drawings:

FIGURE 1 is a schematic circuit diagram of a relay device embodying the invention in which diagram unbroken

lines represent electrical conductors as is conventional in the art; and

FIGURE 2 is a schematic circuit diagram similar to that of FIGURE 1, illustrating a modified form of circuit means for gate-triggering and effecting immunity from adverse effects of variations of the temperature of the ambient.

In the drawings the relay proper is schematically represented by ordinal K and as comprising a set of terminals and contacts Kc, a "set" or pull-in coil K1B, a "reset" or drop-out coil K2B, and a magnetic-latching armature effective to operate the contacts to a first or set state incident to passage of a current pulse through coil K1B and to return the contacts to the second or reset state incident to passage of a pulse through coil K2B. Between pull-in and drop-out of the armature and contacts, substantially no power is required by the relay device other than the insignificant amount required to compensate for leakage and maintenance of charges on timing-circuit and pulse-storing capacitors. The armature of the relay K is schematically represented by the dash line piercing the coils.

The relay device is supplied D.C. power through + and — terminals as indicated, and is effective to pull in (move the armature to the first, or active, state) within a time period of the order of five milliseconds following application of D.C. power (24 to 32 volts) to the terminals. As will be later herein explained, drop-out (movement of the armature back to the second, or inactive, state) occurs at a determinable delay period next following opening of the power circuit to the + and — terminals, as, for example, by opening of the power supply switch S. Referring first to FIGURE 1, upon application of D.C. potential to the terminals, a low-impedance charging path via resistor R1, diode D3, pull-in coil K1B, and capacitor CS is established, the capacitor also being connected at its other terminal to the — power terminal via transistor Q3. As a consequence, charging current of the character of a decaying pulse passes through coil K1B, causing pull-in of the armature and contacts. The armature is latched in the pull-in or set state by permanent magnet means as is conventional in latching relays. During pull-in and flow of the current required to charge capacitor CS, current flows via resistor R1, diode D4 and junction W, to charge a timing capacitor CT the other terminal of which is connected to the — power terminal as indicated. Additionally, + potential is applied to the anode gate of PNPN silicon controlled switch Q2 via diode D5, thereby blocking Q2 against conduction and thus causing Q2 to present a very high impedance against current flow through drop-out coil K2B. Concurrently, positive gate bias is applied via junction W to MOS field-effect transistor Q1 whereby the latter is blocked.

The potential-level of the potential applied to the source of Q1 is closely regulated by a Zener diode Z1; and similarly the potential applied to the gate of Q1 is held constant by Zener diode Z2. Thus, following initial energization of the circuitry at the + and — terminals, the timing capacitor CT is charged to the accurately determinable potential as regulated by Z2, and the charge is accurately maintained during the period the circuitry is connected to the power supply line. When the power line connected to the + and — terminals is opened, the charge on CS is substantially maintained by virtue of the very high impedance of all of the paths through Z1, Q2 and Q1. The capacitor CT, however, recommences to discharge via external resistor REXT (which may be selected to provide various time-delay ranges) and variable resistor RT (which latter resistor may be used in a particular relay device to precisely set the time delay period duration within the range governed by REXT). The discharge continues as governed by the capacitance of capacitor CT and the resistance of the discharge path through REXT, RT, junction X, and base-emitter of NPN transistor Q3, and thus the gate potential on the field-effect transistor Q1 decreases until it is below the potential provided by the charged storage capacitor CS. At that time Q1 becomes conductive and commences to conduct, current flowing from CS via junction O through Q1, Q3 and diode D1. Current flow through D1 causes junction M to become more negative than junction N, and that relatively negative potential is apparent at junction X and is effective on the base-emitter circuit of transistor Q3 and causes the latter to be biased to the nonconductive state. The latter action causes the discharge current flowing through transistor Q1 to be diverted through junction Y, resistor R2 and thermistor T. Thus junction Y experiences a positive-going potential, which potential is apparent at the cathode gate of switch Q2 and biases Q2 to a fully conductive state. The storage capacitor CS then discharges very rapidly, the pulse of discharge current flowing through reset coil K2B, Q2, D2 and D1 and causing the energized reset coil to return the relay armature to the inactive (reset) state.

From the preceding description it is evident that the setting and the resetting of the relay are effected as an incident of the charging and discharging, respectively, of capacitive means, the charging current being forced by the circuitry to flow through the setting coil (K1B) and the discharging current being forced by the circuitry to flow through the resetting coil (K2B). During the period between setting and resetting of the relay proper, only negligible current-flow (through the very high resistance REXT) occurs, and heat production in the device is of very low order.

Compensation for the variations of electronic characteristics of the several circuit elements as the ambient temperature varies is effected by introduction of the thermistor (T) connected in series with resistor R2 as indicated.

The embodiment of the relay device circuit depicted in FIGURE 1 and hereinabove described utilizes a triggering circuit comprising one component that is costly relative to the other components and which may be such that the supply of that component may be restricted. To avoid possible objections in respect of those features, an alternate form of the relay device circuit, utilizing very inexpensive and readily available trigger-circuit components, is shown in FIGURE 2. In the latter drawing or circuit diagram, the relay contacts and terminals KC, the magnetically latched armature, the set and reset coils K1B and K2B, respectively, and the silicon controlled switch or gate Q2 are the same as the similarly designated components depicted in FIGURE 1. Power (D.C., 24–32 volts) is applied to the + and — terminals, as previously described. The potential derived across the input line, via rectifier (diode) D6, is closely regulated by means including resistor R3, Zener diode Z3 and transistor Q4, connected as indicated in FIGURE 2. Thus the potential available for operating the relay (from junction V) is maintained at a constant level, such as 19 volts, for example, governed by the breakdown potential of Zener diode Z3, which diode is carefully selected in respect of temperature coefficient and to have a positive temperature coefficient.

Operation of the relay device circuit shown in FIGURE 2 during the pull-in phase is substantially the same as that depicted in FIGURE 1 during the initial phase; that is, upon connection of power to the terminals, a pulse is passed through pull-in coil K1B to effect charging of the storage capacitor CS' and the change of the armature and contacts to the active (first) state. Concurrently silicon controlled switch Q2 is biased off hard by application of + potential to the anode gate via diodes D4 and D5; and charging current is supplied to timing capacitor CT' via resistor R4. Following charging of capacitor CT' only very high impedance paths are presented by the circuits for current flow from the + to the — terminal during the period that the terminals remain energized; and, accordingly, substantially no power is consumed by the relay

device during the period the relay is in the first or active state.

Continuing with reference to FIGURE 2 and with the terminals energized and the device in the active state, when potential supply to the terminals is discontinued, timing capacitor CT' commences to discharge through series-connected resistor RT' and (external) resistor REXT'. Discharge continues until the potential at junction P falls below that at junction O, at which time transistor Q6 becomes conductive and substantially instantly biases transistor Q5 to the conductive state. Slow discharge of storage capacitor CS' then commences, via Q5 and R6, whereby a bias is developed across R6 which applies a + potential to the cathode gate of PNPN switch or gate Q2 and triggers the latter to a highly conductive state. Q2 then permits a rapid (pulse) discharge of CS' through reset coil K2B, which restores the armature and relay contacts to the second or inactive state.

To absorb the initial "turn-on" transient of the circuit until the Darlington circuit comprising Q5 and Q6 becomes back-biased, a capacitor C1 is connected in shunt with resistor R6, as indicated. Further, to reduce to a minimum any current leakage through Q5 during active-state operation of the relay, a bias-supplying resistor R5 is connected as shown. The bias is applied to the base of Q5 and effectively drives that transistor hard into the nonconductive state. Since then both gate Q2 and trigger-circuit transistor Q5 are hard-biased into nonconductive status during the period of energization (first state) of the relay, substantially no power whatever is consumed by the relay device circuit during active state operation; excepting only the insignificant power used by Zener regulator Z4. The current pulse used in the charging direction to charge storage capacitor CS' and activate the pull-in coil K1B at initiation of relay operation is stored and used in the discharging direction to activate the drop-out coil K2B as noted.

Typical characteristics and values of exemplary circuit components are as set out in the following table:

R1	270 ohm±5%, 2 watts.
R2	300 kiloohms±5%, ¼ watt.
R2'	10 kiloohms±10%, 100 milliwatts.
R3	2 kiloohms±5%, 150 milliwatts.
R4	100 ohms±10%, 100 milliwatts.
R5	1 megohm±5%, 100 milliwatts.
RT	To 500 kiloohms.
RT'	To 500 kiloohms.
REXT	25–500 kiloohms.
REXT'	25–500 kiloohms.
D1	IN457.
D2	IN457.
D3	IN457.
D4	IN457.
D5	IN457.
Z1	12 volts±5%.
Z2	18 volts ±5%.
Z3	20 volts±5% T.C. +.0005%/C°.
Z4	10 volts±5%.
C1	0.12 microfarads, ±10%.
CS, CS'	40–300 microfarads.
CT, CT'	5–300 microfarads.
Q1	2N3608 MOS FET.
Q2	3N84 SCS.
Q3	T1411 transistor.
Q4	2N760 transistor.
Q5	2N3702 transistor.
Q6	2N3702 transistor.
T	Thermistor 1 megohm at 25° C.

Bourns, Inc. Model 3102 relay, or equivalent

Thus it is made evident that the circuitry according to the invention is such that the triggering circuit is triggered at very low current levels of the order of one microampere without danger of being erroneously triggered by line transients or like disturbances. Further, there is not required any connection to the power supply for operation of timing circuit or other means during the time-delay period. Also, despite the few and inexpensive circuit components used, very long and accurately-determined time delays of the order of 100 seconds and less may be obtained. Due to the hard positive back-biasing of transistor Q5 and the anode gate of switch Q2 and the hard negative biasing of the cathode gate of Q2, substantially no power is consumed by the switch and trigger circuits during the period between pull-in and drop-out of the relay proper. Due to placement or connection of the pull-in coil between the + terminal and the potential-regulating Zener diode Z1, the pull-in coil serves to perform two functions, namely, to actuate the armature, and to limit the current through the regulator.

The preceding detailed description of relay devices including a preferred exemplary form (FIGURE 2) according to the invention and a modified form thereof indicates full attainment of the aforementioned objects. In the light of the disclosure changes within the true spirit and scope of the invention will occur to those skilled in the art and accordingly it is desired that the scope of the invention be limited only as required by the appended claims.

I claim:

1. A relay device adapted to be set incident to supply of electric power thereto and to be automatically reset following expiration of a determined period of time next following discontinuance of supply of power thereto, said relay device comprising:

first means, including electrical power means, arranged, to be energized and de-energized;

second means, including a relay setting coil and a relay resetting coil;

third means, including an electronic gate device susceptible of being biased to either of conductive and nonconductive states, said gate device being a PNPN silicon controlled switch having anode and cathode gate terminals and anode and cathode terminals connected in series with said setting and resetting coils across said power means;

fourth means, including storage capacitor means connected to said power means to be charged through said setting coil incident to energization of the power means and connected to said resetting coil to be discharged through the latter incident to biasing of said gate device to the conductive state; and

fifth means, including capacitive timing circuit means, connected to said power means to be charged therefrom and to said gate device and effective incident to energization of said power means to bias said gate device to nonconductive state and effective incident to de-energization of said power means to relieve said gate device of the said bias following elapse of a determined time period next succeeding de-energization of said power means, said fifth means further comprising a trigger-circuit means connected between said capacitive timing circuit means and said silicon controlled switch for triggering the latter to conductive state incident to decrease of potential across said capacitive timing means to a predetermined potential, said trigger-circuit means being maintained inactive to trigger said silicon controlled switch to the conductive state while the potential of said timing means exceeds said predetermined potential, to thereby permit discharge of said storage capacitor means through said resetting coil to energize the latter at a determined time subsequent to de-energization of said power means.

2. A relay device according to claim **1**, in which said trigger-circuit means includes a field-effect transistor connected to be biased to nonconductive state by the potential of said capacitive timing means during periods when

the latter potential is in excess of said predetermined potential.

3. A relay device according to claim 1, in which said trigger-circuit means includes a Darlington transistor circuit connected to said storage capacitor means and to said capacitive timing means to be back-biased when the potential of the latter is in excess of that of said storage capacitor means.

4. A relay device adapted to be set incident to supply of electric power thereto and to be automatically reset following expiration of a determined period of time next following discontinuance of supply of power thereto, said relay device comprising:

first means, including power means including positive and negative terminals and lines, adapted to be energized and de-energized;

second means, including relay means including a setting coil and a resetting coil;

third means, including a silicon controlled switch having anode and cathode terminals serially connected with said resetting coil;

fourth means, including a storage capacitor means connected in series with said setting coil across said power means whereby upon energization of the power means said storage capacitor means is charged by current passing through said setting coil, said fourth means comprising regulator means including a Zener diode connected in parallel with the series combination of said switch and resetting coil, said storage capacitor means being connected in parallel with said regulator means;

fifth means, including capacitive timing-circuit means connected to said power means to be charged therefrom incident to energization of the latter, and regulator means fixing the potential to which said capacitive timing-circuit means is charged;

sixth means, including trigger-circuit means connected to said storage capacitor means and to said timing-circuit means and connected to said silicon controlled switch to control conductivity of the latter, said trigger-circuit means effective to render said switch conductive incident to decrease of potential of said timing-circuit means to a value below that of said storage capacitor means,

whereby incident to energization of said power means said timing-circuit means and said storage-capacitor means are charged and said trigger-circuit means are effective to bias said switch against conduction, and whereby incident to de-energization of said power means said timing means slowly dissipates power stored therein until the potential thereof is lower than that of said storage capacitor means and thus renders effective said trigger-circuit means to render said switch conductive to permit discharge of said storage capacitor means through said reset coil to cause said relay means to become reset a determinable time next following said de-energization of said power means.

5. A relay device according to claim 4, in which said trigger-circuit means includes a Darlington transistor circuit sensitive to the difference between the potential of said storage capacitor means and that of said capacitive timing means.

6. A relay device according to claim 4, in which said trigger-circuit means includes a field-effect transistor sensitive to the difference between the potential of said storage capacitor means and that of said capacitive timing means.

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