Dec. 12, 1967 J. H. AUER, JR 3,358,126

TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

Filed Sept. 3, 1963 5 Sheets-Sheet 1

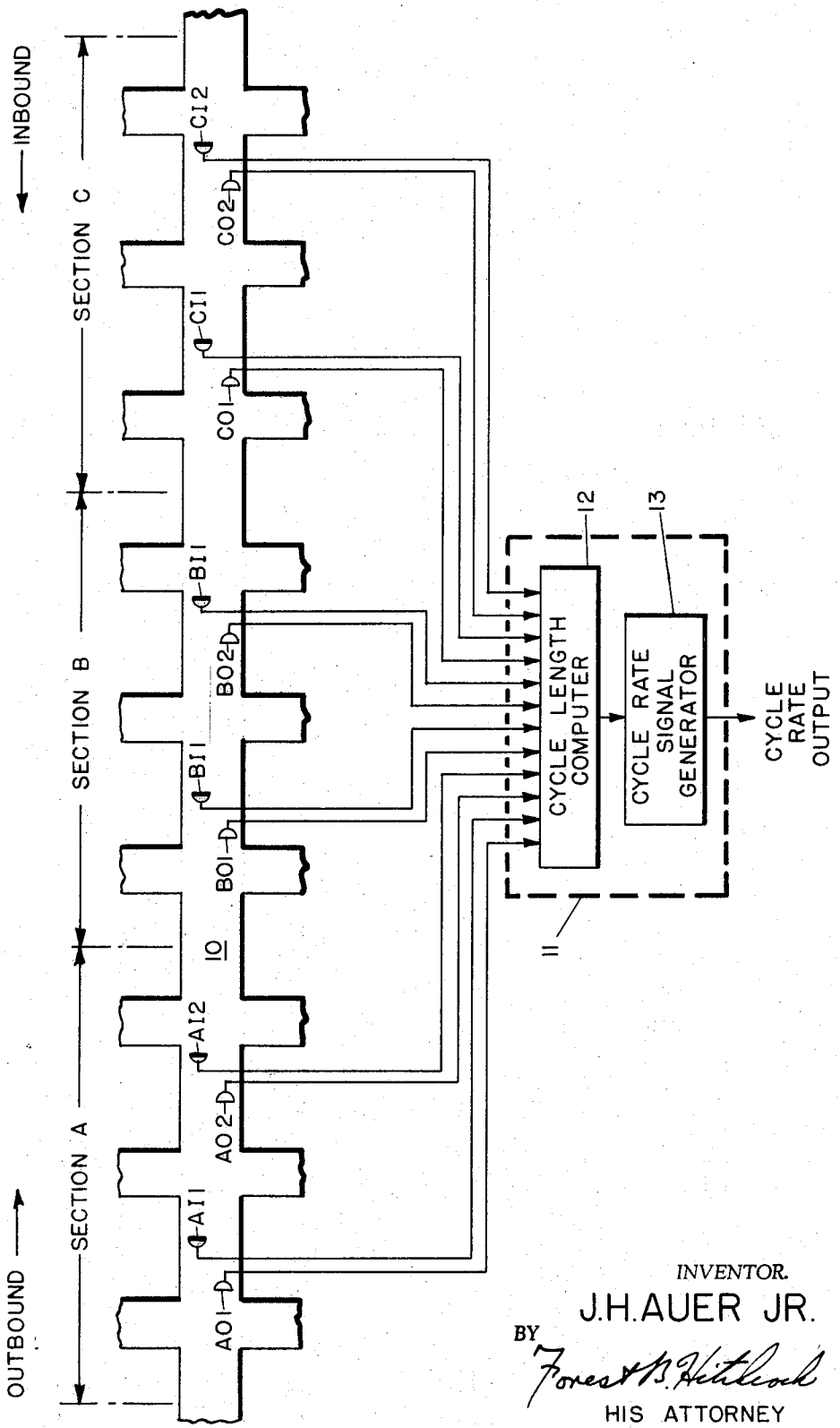


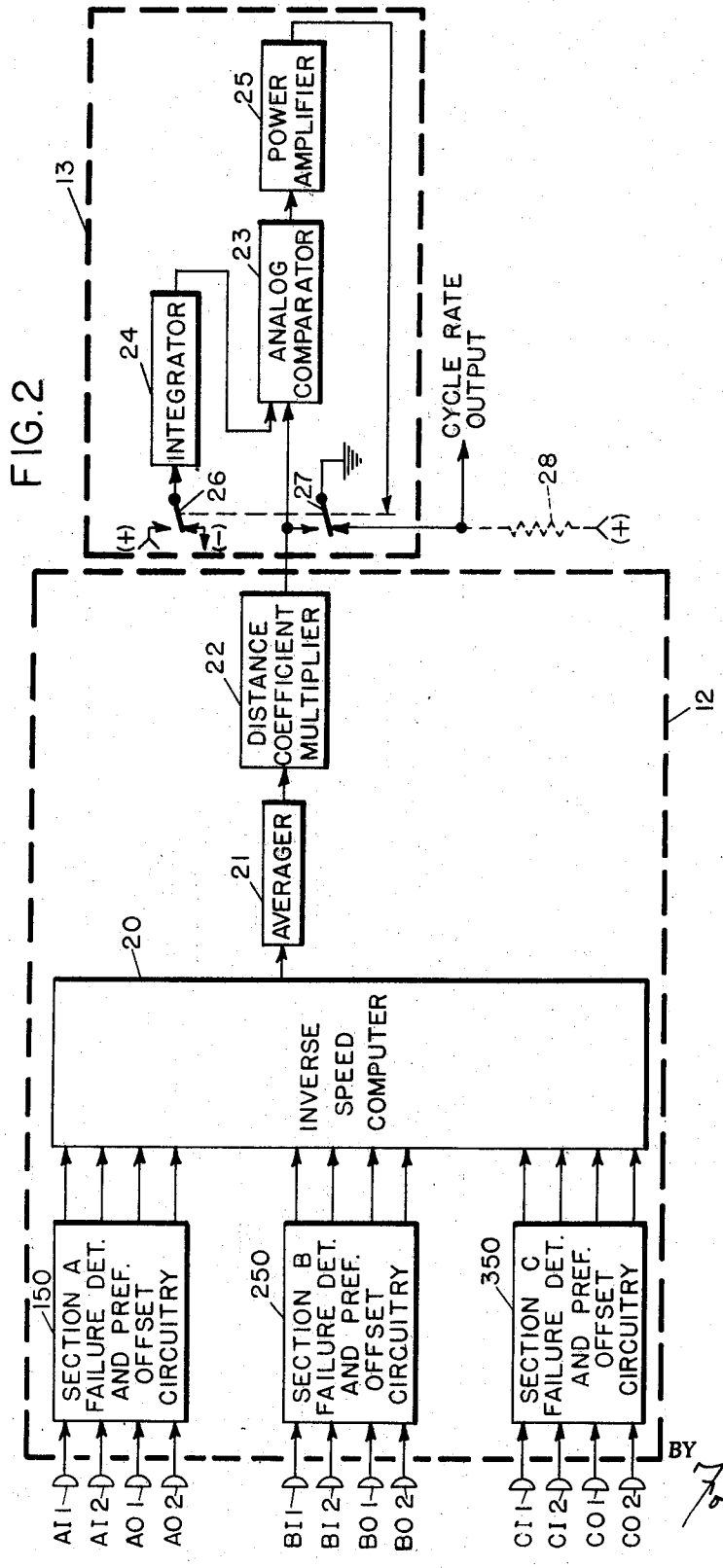
FIG. 1

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TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

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FIG. 2



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TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

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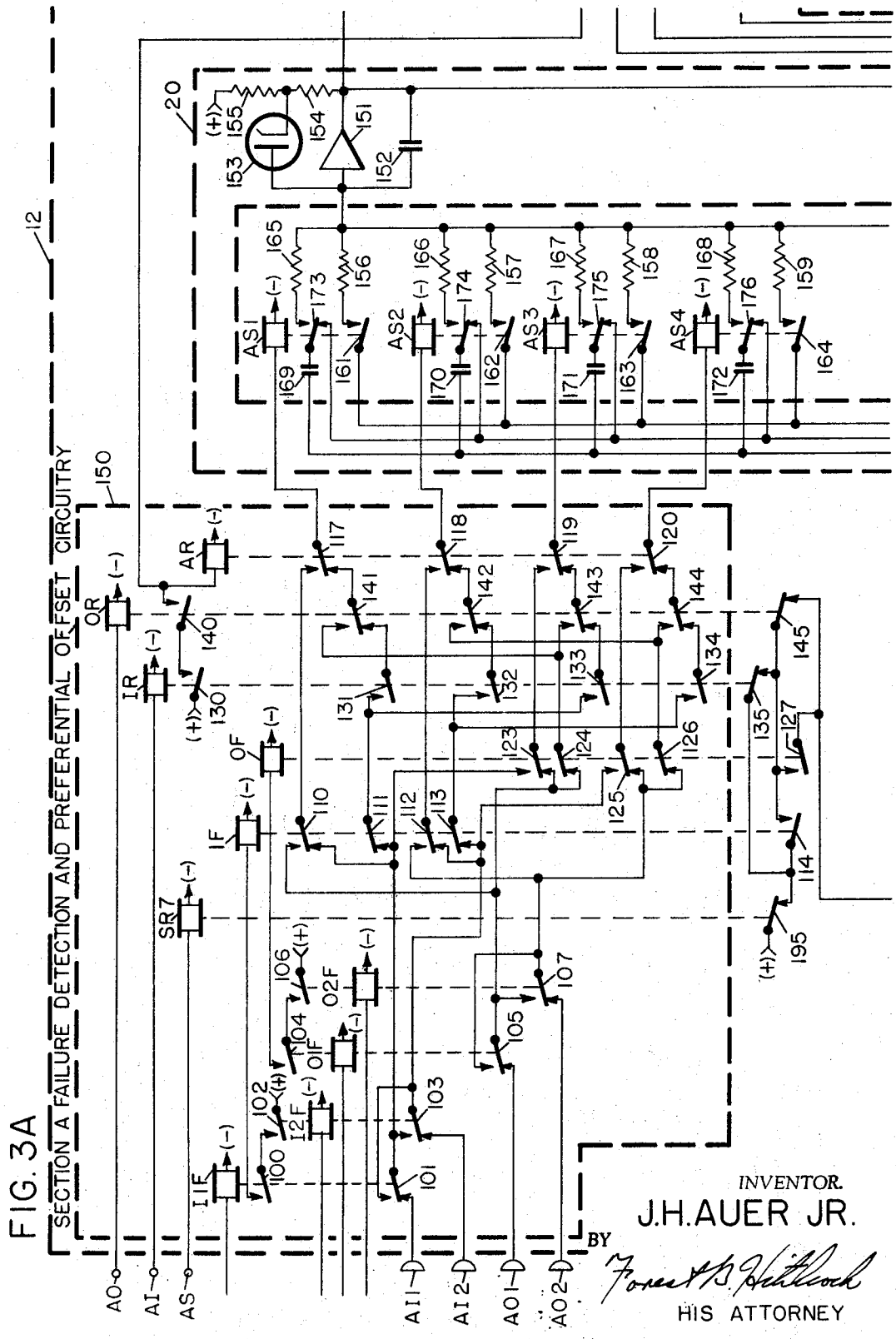


FIG. 3A

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TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

Filed Sept. 3, 1963 5 Sheets-Sheet 4

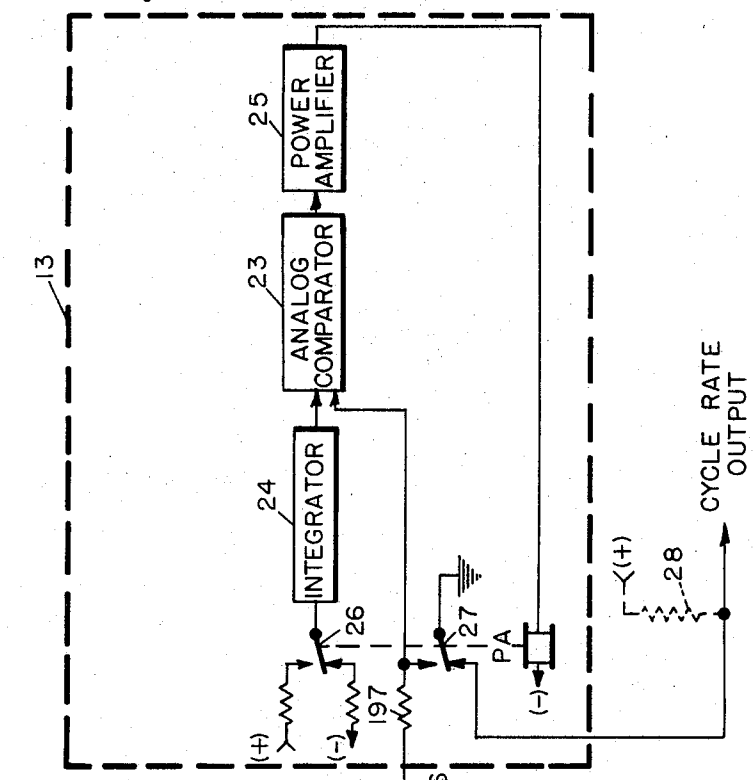


FIG. 4

FIG. 3A	FIG. 3B
	FIG. 3C

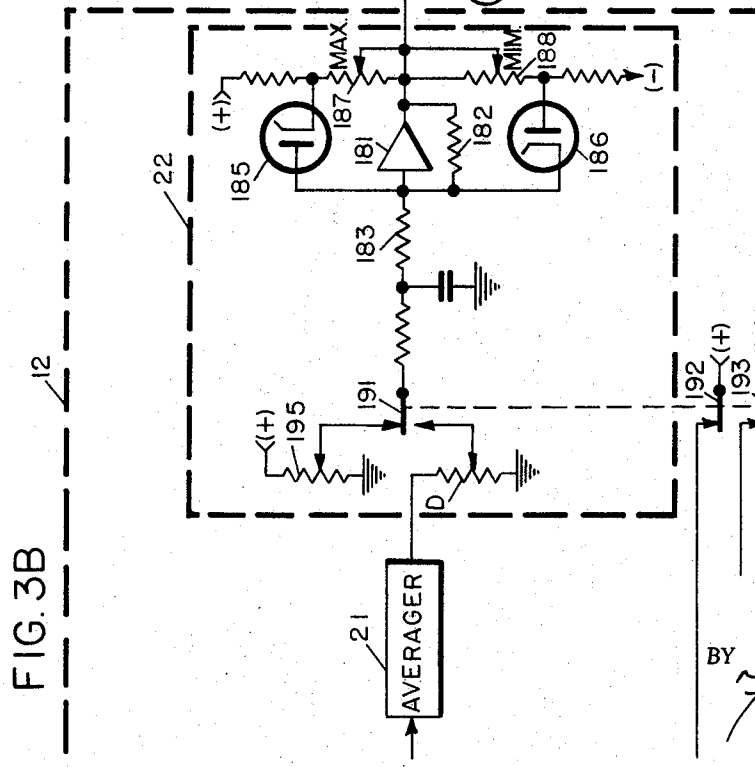


FIG. 3B

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TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

Filed Sept. 3, 1963 5 Sheets-Sheet 5

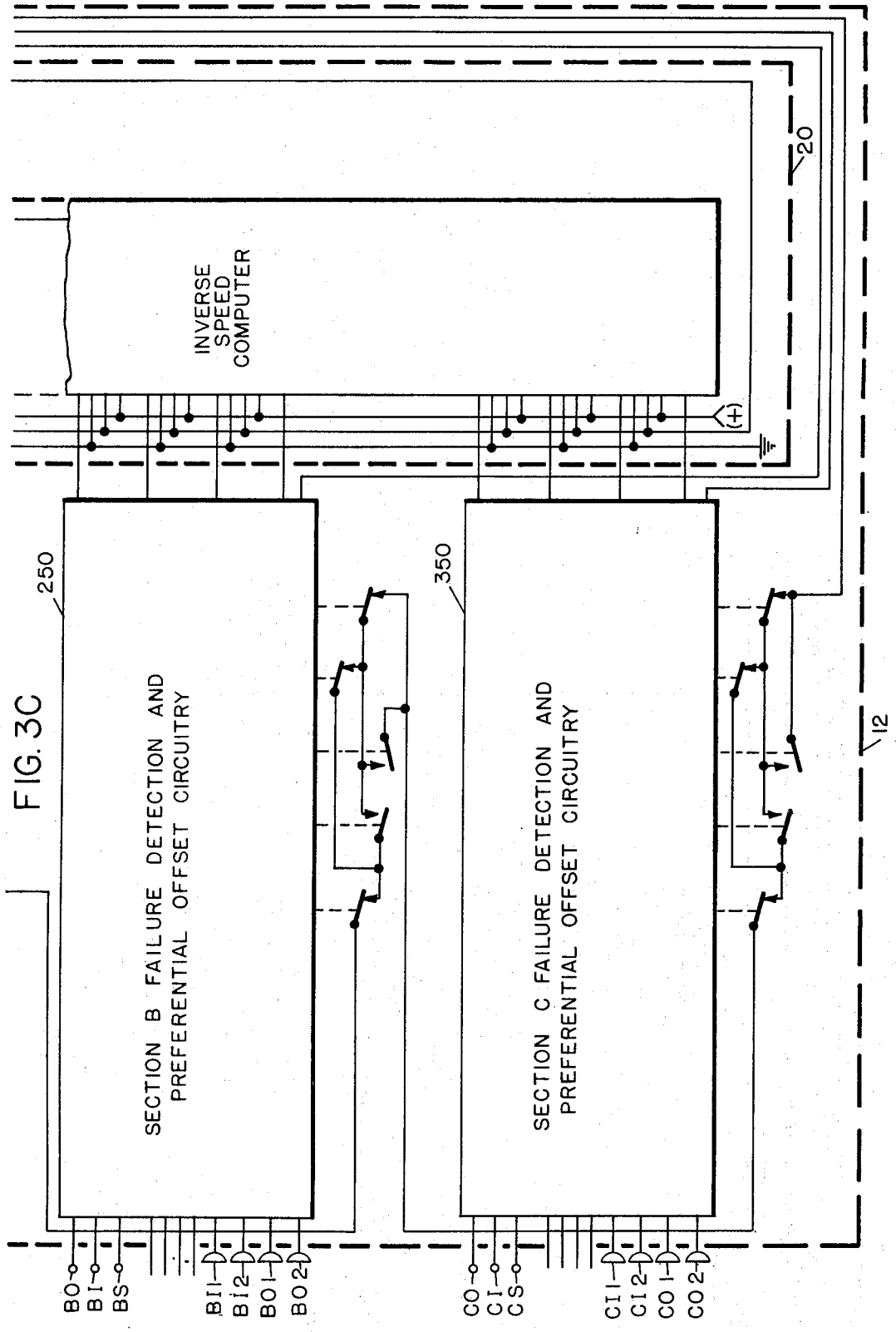


FIG. 3C

United States Patent Office 3,358,126
Patented Dec. 12, 1967

3,358,126

TRAFFIC SIGNAL CONTROLLER CYCLE COMPUTER

John H. Auer, Jr., Rochester, N.Y., assignor to General Signal Corporation, Rochester, N.Y., a corporation of New York

Filed Sept. 3, 1963, Ser. No. 306,036
21 Claims. (Cl. 235—150.24)

This invention relates to traffic control systems, and more particularly to a computer for providing cycle duration control for traffic signals along a section of highway in accordance with demands of traffic.

Cycle duration may be defined as the time period required for one complete sequence of signal indications from a traffic signal. In order to progress traffic smoothly along an urban arterial highway, successive traffic signals encountered by arterial vehicular traffic should be green. This requires that the offset for each successive traffic signal be greater than the offset for the preceding traffic signal. Offset may be defined as the number of seconds or percent of the cycle duration that the green indication starts at a given traffic control signal after a certain instant used as a time reference base. A system for control of traffic signal offsets based upon both absolute and relative levels of traffic lane occupancy is disclosed in the copending application of J. H. Auer, Jr., et al., Ser. No. 305,967, filed Sept. 3, 1963, now Patent No. 3,278,896. However, variation in the speed of traffic flow necessitates adjustment of traffic signal system operatin to compensate for the variation and maintain smooth traffic flow. This compensation may be achieved either by selecting different offsets as speed varies or by varying the cycle duration as speed varies. To adequately match signal progression to vehicle speed by the former approach requires many offsets. This is not particularly desirable due the the frequent offset changes. Therefore, the present invention contemplates adjustment of operation of a progressive signal system by the latter approach.

To compensate for variations in traffic speed, the cycle computer controls cycle duratin as an inverse function of average speed. Hence, in a progressive traffic signal system, cycle duration bears a relationship to distance as well as time. Normal operation of this progressive system is considered to be such as to maintain a fixed cycle distance during progressive signal operation. Cycle distance may be defined as the distance along an artery between a pair of traffic signals which are operating in phase with each other. It may also be considered as the distance along the artery which is travelled by one vehicle moving at the average traffic speed during the time interval of one signal cycle. This cycle distance remains constant if the product of average vehicle speed and cycle duration is held constant. Thus, perfect agreement may be maintained between signal system progressive speed and vehicle speed by so controlling cycle duration.

The novel cycle computer herein disclosed operates most advantageously under certain specific traffic offset conditions. For example, assume that any one of a plurality of offsets, such as seven, may exist in any section of the highway. These seven offsets may be based upon lane occupancy as follows:

(1) Light in both directions.
(2) Moderate outbond.
(3) Expected moderate outbound.
(4) Moderate in both directions.
(5) Expected moderate inbound.
(6) Moderate inbound.
(7) Heavy or expected heavy in either direction.

Thus, the offset selected in a function of both the level of traffic lane occupany and the degree of traffic directivity; that is, the balance between inbound and outbound lane occupancy. When lane occupancy is low in both directions, the light offset is selected, regardless of the degree of traffic lane occupancy unbalance. When the level of lane occupancy exceeds a perdetermined minimum, the offset is seleted on the basis of both traffic direction, or relative lane occupancies, as well as absolute lane occupancy. Hence, if the actual or expected level of traffic lane occupancy exceeds a predetermined value, defined as moderate, which is greater than the predetermined minimum, defined as light, a third lane occupancy level, defined as heavy, is selected.

When all sections of the arterial highway are operated with a light traffic offset, a preselected cycle duration is specified by the cycle computer. This light offset cycle duration is normally manually adjusted to a constant, relatively short interval. However, when any section along the highway requires an offset other than light, cycle duration specified by the cycle computer is determined as a function of traffic measurements made within the various arterial highway sections. On the other hand, whenever a section requires a special offset, such as when the level of lane occupancy or expected lane occupancy in that particular section is heavy, the determined cycle duration information for that section as calculated by the computer is disregarded. Instead, a constant section cycle duration is generated as a function of a preadjusted manual control.

The present invention permits maintenance of perfect agreement between signal system progressive speed and vehicle speed by providing a cycle duration voltage for controlling cycle duration in accordance with variation of traffic speed. This is achieved by means of a computer which generates a rate signal such that a fixed number of rate signal pulses, for example 100, is produced during the desired cycle duration. Moreover, this desired cycle duration is controlled so as to hold the product of cycle duration and average vehicle speed constant and equal to the selected cycle distance.

Accordingly, one object of this invention is to provide a real time computer for producing cycle duration control signals for traffic controllers along a highway in accordance with demands of traffic.

Another object of this invention is to provide a system for computing cycle duration for a plurality of traffic signal controllers located along a section of a vehicle route based upon demands of traffic within the section and within adjacent sections.

Another object is to provide traffic signal cycle duration control information for traffic signals located along a highway based upon average traffic speed along the highway.

Another object is to provide a system for computing traffic signal cycle duration only during occurrence of predetermined traffic offsets.

Another object is to provide means for computing the inverse of average traffic speed in a given direction based upon detection of vehicles travelling in the given direction by vehicle presence detectors.

The invention generally contemplates a traffic signal cycle computer comprising means responsive to average vehicular speed along a highway providing a voltage inversely proportional thereto, and means multiplying the voltage in proportion to distance between traffic signals operating in phase with each other to provide a voltage analog of optimum cycle duration. Additional means dividing the voltage analog of optimum cycle duration into a predetermined number of pulses per cycle are also provided.

The aforementioned means responsive to average vehicular speed along a highway comprises means providing average traffic volume information, means providing

average traffic lane occupancy information, and means dividing the lane occupancy information by the volume information providing a voltage analog of inverse average traffic speed.

The foregoing and other objects and advantages of the invention wlil become apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a sectionalized arterial highway showing vehicle detector connections to the novel cycle computer;

FIG. 2 is a simplified block diagram of the novel cycle computer;

FIGS. 3A–3C constitute a part schematic and part block diagram of the novel cycle computer; and

FIG. 4 is a diagram showing how FIGS. 3A–3C are assembled.

Turning to FIG. 1, there is shown a portion of a traffic artery 10 divided into three sections, designated sections A, B, and C. A cycle computer **11** is associated with all three sections. The cycle computer comprises a cycle length computer **12** and a cycle rate signal generator **13**.

Each arterial section has a number of intersections with secondary streets. Suitable vehicle detectors, such as presence detectors of the type disclosed in H. C. Kendall, J. H. Auer, Jr., N. A. Bolton and K. H. Frielinghaus Patent 3,042,303, issued July 3, 1962, are situated within each section, preferably at a point just inside the intersections formed by the secondary streets crossing each section at either end of the section. At each of these locations, detection of both inbound and outbound traffic is performed. Thus, in each section, two detections are made of both inbound and outbound traffic. For example, in section A, detectors AI2 and AI1 are used for detecting traffic in the inbound direction, while detectors AO1 and AO2 are used for detecting traffic in the outbound direction. Although a single intersection is shown separating the detectors in each section, a plurality of intersections may also exist between the detectors in any section. Moreover, although for simplicity of explanation of the artery is assumed to have but a single inbound and single outbound lane, the system is also applicable to multi-lane arteries. Under such circumstances, traffic conditions in each lane may be detected separately.

In a fashion similar to that described for section A, detectors BI2 and BI1 detect inbound traffic in section B at either end, while detectors BO1 and BO2 detect outbound traffic in section B at either end. Similarly, detectors CI2 and CI1 detect inbound traffic in section C at either end, while detectors CO1 and CO2 detect outbound traffic in section C at either end. Output voltages from all the aforementioned detectors are coupled to the input of cycle length computer **12**. This computer provides a voltage analog of optimum cycle duration in accordance with traffic conditions to cycle rate signal generator **13**, which divides the cycle duration voltage analog into a predetermined number of pulses, such as 100. The same number of pulses recurs during each cycle, so that the pulse repetition rate produced by the cycle rate signal generator is inversely proportional to the amplitude of the output signal of cycle length computer **12** and hence inversely proportional to the computer cycle duration. These output pulses comprises the cycle rate output of cycle computer **11**. The train of pulses comprising the cycle rate output may then be utilized in a master system for control of traffic signals in sections A, B and C.

FIG. 2 shows a generalized block diagram of the cycle computer. Inputs from detectors AI1, AI2, AO1 and AO2 are coupled to a section A failure detection and preferential offset circuit **150**. Similarly, the detectors sensing traffic in section B are coupled to a section B failure detection and preferential offset circuit **250** while the detectors sensing traffic in section C are coupled to a section C failure detection and preferential offset circuit **350**. Each section failure detection and preferential offset circuit provides as many outputs as there are inputs coupled thereto. However, these outputs are coupled straight through any one of circuits **150**, **250** or **350** only when all detectors coupled to the circuit are operative and no single preferential direction offset for the section associated with the circuit exists. In the event of a detector failure or a single preferential direction offset, outputs from certain detectors are substituted for outputs from other detectors, in a manner described, infra.

Outputs from the section failure detection and preferential offset circuits **150**, **250** and **350** are applied to an inverse speed computer **20**. This computer provides an output voltage analog of the inverse of average traffic flow speed within sections A, B and C, which is averaged in an averager **21**, so that the inverse speed voltage analog presented at the output of the average is based upon a long time interval.

Output voltage from averager **21** is then applied to a distance coefficient multiplier **22**. This multiplier provides an output voltage corresponding to the inverse speed voltage produced from averager **21**, multiplied by cycle distance. The cycle distance is manually preselected, and forms a constant coefficient by which the voltage analog of inverse average traffic speed is multiplied. Output voltage from distance coefficient multiplier **22** thereby constitutes an analog of the time duration of a single cycle. This output voltage which also comprises the output voltage of cycle length computer **12**, is then coupled to cycle rate generator **13** to supply a first input voltage to an analog comparator **23**. The cycle rate signal generator also comprises an integrator **24** which provides a second input voltage representing the time integral of a constant voltage to analog comparator **23**. Selection of either positive or negative constant voltages for integration is controlled by the output of a power amplifier **25** through a contact **26**. Power amplifier **25** in turn is responsive to the output of analog comparator **23**. A second contact **27** is controlled by power amplifier **25** to produce pulses at a pulse repetition rate inversely proportional to cycle duration. The output from power amplifier **25** also acts periodically to ground the output of distance coefficient multiplier **22** through front contact **27**, thereby removing the first input voltage from analog comparator **23**.

In inoperation, assume input voltages are applied to inverse speed computer **20** from the vehicle detectors in each of sections A, B and C, through respective failure detection and preferential offset circuits **150**, **250** and **350**. The computer then provides an output voltage of amplitude inversely proportional to average speed of traffic flow through the highway. This output voltage is then applied to long time constant averager **21** so that the inverse speed voltage presented at its output is based upon an average taken over a long time interval. This inverse average speed voltage is then multiplied by cycle distance in distance coefficient multiplier **22**, providing a first input voltage to analog comparator **23** which is always of negative polarity. With back contact **26** closed, negative potential is coupled to integrator **24**, so that integrator output voltage rises from zero in the positive direction. When this voltage rises to a value sufficiently high to exceed the negative voltage from distance coefficient multiplier **22**, the algebraic sum of input voltage to comparator **23** changes to a voltage of positive polarity. The output voltage from analog comparator **23** then abruptly changes from a highly positive to a highly negative value, causing power amplifier **25** to open back contacts **26** and **27** and close front contacts **26** and **27**. This removes the negative input voltage applied to analog comparator **23** from amplifier **181** and applies a positive reference voltage to integrator **24**. The output voltage from integrator **24** then falls from a positive potential toward zero. When this potential reaches zero and actually moves slightly negative, output voltage from analog comparator **23** abruptly changes polarity to again become highly positive. This

causes power amplifier 25 to open front contact 26 and 27 and close back contacts 26 and 27, reapplying a negative input voltage to analog comparator 23 from multiplier 22 and reconnecting the integrator to the negative voltage source. Hence, contacts 26 and 27 alternately open and close at a rate inversely proportional to the amplitude of output voltage from multiplier 22 and therefore also at a rate inversely proportional to the computed cycle time. To provide positive output voltage pulses at a repetition rate inversely proportional to the computed cycle time, it is merely necessary to couple a positive voltage source to back contact 27 through a resistor 28, as shown dotted in FIG. 2.

FIGS. 3A–3C represent one embodiment of a typical cycle computer. For examplary purposes, circuitry responsive to traffic conditions in section A is shown in detail. However, since the circuitry responsive to traffic conditions in sections B and C is similar to that for section A, it is illustrated in block form only.

The inputs to the cycle computer from vehicle detectors AI1, AI2, AO1 and AO2 of section A are shown respectively coupled to back contacts 101, 193, 105 and 107 of relays I1F, I2F, O1F and O2F, respectively. The aforementioned relays comprise failure detection relays for detectors AI1, AI2, AO1 and AO2, respectively. Thus, in the event one of the detectors should become inoperative, the failure detection relay associated therewith is energized. One type of circuit for providing a signal indicative of a detector failure may comprise a timing circuit for energizing the failure detection relay associated with the particular detector when no vehicle has been sensed by that detector for an unduly long time interval. The duration of the required unduly long interval may be varied by a clock throughout a period of time so as to compensate the period in accordance with intervals of normally heavy and normally light traffic flow. The clock, which may complete its cycle through any suitable period, such as 24 hours or 7 days, thereby enables programming of the timer so that the unduly long time interval required by the timer is adjusted to be longer at times traffic conditions are normally light than at times traffic conditions are normally heavy. One such timing circuit is described in detail in a prior application of John H. Auer, Jr., et al. Ser. No. 292,584, filed July 3, 1963.

The heel of contact 101 is coupled through a back contact 110 of a relay IF to a front contact 117 of a relay AR, to front contact 103 of relay 12F, and to a front contact 123 of a relay OF. In like fashion, the heel of contact 103 is coupled through a back contact 112 of relay IF to a front contact 118 of relay AR, to front contact 101 of relay I1F, and to a front contact 125 of relay OF. Relay IF is energized through a front contact 102 of relay I2F and a front contact 100 of relay I1F in series. Similarly, relay OF is energized through a front contact 106 of relay O2F in series with a front contact 104 of relay O1F. In addition, the heel of contact 101 is coupled through a back contact 111 of relay IF to a pair of front contacts 131 and 133 of a relay IR. Similarly, back contact 103 of relay I2F is coupled through a back contact 113 of relay IF to a pair of front contacts 132 and 134 of relay IR.

The heel of relay O1F contact 105 is coupled to front contact 107 of relay O2F, to front contact 110 of relay IF through back contact 123 of relay OF to a front contact 119 of relay AR, and through a back contact 124 of relay OF to a pair of front contacts 141 and 143 of a relay OR. Similarly, the heel of contact 107 of relay O1F is coupled to front contact 105 of relay O1F, to front contact 111 of relay IF, through back contact 125 of relay OF to a front contact 120 of relay AR, and through a back contact 126 of relay OF to a pair of front contacts 142 and 144 of relay OR.

A group of four relays AS1, AS2, AS3 and AS4 is energized from the heels of contacts 117, 118, 119 and 120 respectively. The heels of contacts 141, 142, 143 and 144 are respectively coupled to back contact 117, 118, 119 and 120, while back contacts 141, 142, 143 and 144 are respectively coupled to the heels of contacts 131, 132, 133 and 134. A front contact 130 of relay IR and a front contact 149 of relay OR is actuated through an input terminal AO, relay IR is actuated through an input terminal AI and a relay SR is actuated through an input terminal AS. The circuitry within dotted rectangle 150 represents failure detection and preferential offset switching circuitry for section A. Similar circuitry for sections B and C are represented by blocks 250 and 350 respectively.

Consider now the modus operandi of the section A failure detection and preferential offset circuitry. Assuming all detectors in section A are operative, relays I1F, I2F, O1F and O2F are all deenergized. Relays IR, OR and SR receive section offset information through terminals AO, AI and AS, respectively, Terminal AO is energized in the event an outbound offset exists, terminal AI is energized in the event an inbound offset exists, and terminal AS is energized in the event lane occupancy is heavy in either the inbound or outbound direction. A fourth offset relay would be required if anticipated changes in offset were to be indicated. However, since computation of cycle length does not require information as to the degree of preferential offset, anticipated and actual offsets in a given direction are treated in the same manner. In the event an average offset is indicated, front contact 130 and 140 of relays IR and OR respectively are closed, energizing relay AR. In the event a light traffic offset is specified, relays IR, OR and SR are deenergized.

When an average offset is specified, front contacts 117, 118, 119 and 120 of relay AR are closed. This causes energization of computer input relays AS1, AS2, AS3 and AS4 from respective vehicle detectors AI1, AI2, AO1 and AO2.

When an inbound offset is specified, front contacts 131, 132, 133, 134 of relay IR are closed, causing energization of relays AS1 and AS3 from detector AI1 and relays AS2 and AS4 from detector AI2. For example, relay AS1 is energized from detector AI1 through back contact 101 of relay I1F, back contact 111 of relay IF, front contact 131 of relay IR, back contact 141 of relay OR and back contact 117 of relay AR, in series. Thus, during an inbound offset, the outbound detectors are disregarded, since no complete path exists between detectors AO1 and AO2 and any of the computer input relays. Moreover, each of the inbound detectors now carries twice as much weight in the cycle length computation as when no preferential offset exists. Thus, if one section requires an inbound offset and another section requires but an average offset, the section requiring the inbound offset still carries as much weight as the section requiring the average offset, but its vehicle measurements are made solely on inbound traffic.

In like manner, when an outbound offset is specified, relay OR is energized, closing front contacts 141, 142, 143, and 144. This causes energization of computer input relays AS1 and AS3 from detector AO1, and energization of computer input relays AS2 and AS4 from detector AO2. Thus, during an outbound offset, the inbound detectors are disregarded and each of the outbound detectors carries twice as much as when the inbound detectors are also utilized. Thus if one section requires an outbound offset and another section requires an average offset, the section requiring the outbound offset still carries as much weight in the cycle length computation as the section requiring an average offset, but the vehicle measurements in the section requiring an outbound offset are made solely on outbound traffic.

It should be noted that in the event a light offset is specified, relays IR, CR, and AR are deenergized, preventing energy from any of the vehicle detectors in section A from reaching the computer input relays. Under these

circumstances, a predetermined and constant cycle duration is specified by the cycle computer.

In the event detector AI1 fails, failure detection relay I1F is energized, opening back contact **101** and closing front contacts **100** and **101**. Under these conditions, computer input relay AS1, formerly connected to vehicle detector AI1, is now connected to detector AI2, as is computer input relay AS2. Opening of back contact **101** removes detector AI1 from the circuit, while energization of relay AS1 from detector AI2 occurs through a series circuit comprising back contact **103**, front contact **101**, and either back contact **111**, front contact **131**, back contact **141** and back contact **117** in the event relay IR is energized, or back contact **110** and front contact **117** in the event relays IR and OR are both energized. In like manner, if detector AI2 fails, detector AI1 serves to energize computer input relay AS2, as well as relay AS1. Similar protection against detector failure is provided for detectors AO1 and AO2 through failure detection relays O1F and O2F respectively.

It should now be obvious that during a preferential offset, failure of a vehicle detector sensing traffic flow in the preferential direction causes all four computer input relays associated with section A to be controlled from the remaining operative section A detector. For example during an inbound preferential offset and failure of detector AI2, relays AS1, AS2, AS3 and AS4 are all controlled from section A detector AI1.

If both detectors sensing traffic in a given direction should fail, there remains no sensed information as to traffic in that direction. In such event, the failure detection relay indicative of such condition is energized, if an average offset is called for at that time, the two computer input relays normally connected to the inoperative detectors are instead connected to the operative detectors. If however a preferential offset is called for, and the detectors sensing traffic in the preferential direction both become inoperative, the four computer input relays become disconnected from the detectors and are deenergized. For example, if both inbound detectors AI1 and AI2 fail, there is left no inbound sensing information. This produces energization of inbound failure relay IF through a series circuit comprising front contacts **100** and **102** of failure relays I1F and I2F respectively. If an average offset is called for at that time, computer input relays AS1 and AS2, normally connected to detectors AI1 and AI2 respectively, are instead connected to outbound detectors AO1 and AO2, respectively. For example, relay AS1 is energized from detector AO1 through a series circuit comprising back contact **105** of relay O1F, front contact **110** of relay IF and front contact **117** of relay AR. However, in the event failure of detectors AI1 and AI2 occurs at the time an inbound offset is called for, computer input relays AS1, AS2, AS3 and AS4 are all deenergized. This is readily seen in the fact that although front contacts **131**, **132**, **133** and **134** of relay IR are closed, back contacts **111** and **113** of relay IF are open, preventing energy from being coupled through the aforementioned closed front contacts of relay IR. Moreover, although front contacts **117**, **118**, **119** and **120** of relay AR receive energy from detectors AO1 and AO2, this energy does not reach the computer input relays since relay AR is deenergized.

The circuitry energized by the output from outbound detectors AO1 and AO2 operates in a similar fashion, so that in the event of simultaneous failure of both outbound detectors at the time an outbound offset is called for, no information in the form of energy is applied to computer input relays AS1, AS2, AS3 and AS4.

Associated with inverse speed computer **20** is an operational amplifier **151** having a feedback capacitor **152** shunted across its input and output terminals. In addition, a series circuit comprising a diode **153** and resistor **154** is shunted across the input and output terminals of amplifier **151** in such fashion that the anode is coupled to the input side while the resistor is coupled to the output side. Positive energy is resistively coupled to the cathode of diode **153**.

Positive voltage is applied to the input of amplifier **151** through summing resistors **156**, **157**, **158** and **159**, controlled respectively by a front contact **161** of relay AS1, front contact **162** of relay AS2, front contact **163** of relay AS3 and front contact **164** of relay AS4. A second group of resistors **165**, **166**, **167** and **168** respectively provides discharge paths for capacitors **169**, **170**, **171** and **172** through front contacts **173** of relay AS1, **174** of relay AS2, **175** of relay AS3 and **176** of relay AS4 respectively. Capacitors **169**, **170**, **171** and **172** are charged through back contacts **173**, **174**, **175** and **176** respectively, from voltage stored on capacitor **152**. Hence the output voltage from amplifier **151** which is substantially the voltage stored across capacitor **152** is incrementally reduced each time any of front contacts **173**, **174**, **175** and **176** are closed since the voltage applied as a result to amplifier **151** is of negative polarity.

In operation, computer **20** divides traffic density by traffic volume to provide an output voltage inversely proportional to average speed. Density information is applied to the input of amplifier **151**, thereby adding to the charge accumulated on capacitor **152**, while volume information is applied to the feedback circuit around the amplifier by removing increments of charge from capacitor **152**. In performing this computation for use in the system, only the traffic flow in a preferential direction is included. Thus, as previously explained, when an inbound offset is selected in section A the outboard traffic of section A is disregarded. Under these circumstances only detectors AI1 and AI2 provide input information from section A to the inverse speed computer. In similar fashion, in the event an outbound offset is selected in section A, the inbound traffic of section A is disregarded, since only detectors AO1 and AO2 in section A furnish information as to traffic conditions in section A to computer **20**.

Assume an inbound offset exists in section A. Under these conditions, detector AI2 senses inbound traffic entering section A, while detector AI1 senses inbound traffic leaving section A. Vehicle detections from both inbound detectors are then used for computation of an inverse speed voltage representative of average speed as sensed by the inbound detectors in section A. It should be noted that the inverse speed computer provides an output voltage analog of the average of speeds sensed in each section furnishing an input to the computer. Furthermore, for proper operation of the inverse speed computer, each vehicle detector must be a presence detector which energizes a computer input relay throughout the entire length of time in which a vehicle is sensed by detector coupled thereto. Detectors such as those disclosed in H. C. Kendall and J. H. Auer, Jr. U.S. Patent 3,042,303 are quite suitable for this purpose.

Although computer **20** provides inverse speed information by dividing traffic density by traffic volume, the computer actually operates on lane occupancy information, rather than density information. The parameter of lane occupancy is fully described in H. C. Kendall and J. H. Auer, Jr., application Ser. No. 78,410 filed Dec. 27, 1960, now patent No. 3,233,084, wherein it is defined as being the portion of a highway which is vehicle-occupied. Moreover, this parameter may be expressed as a percentage. Thus, when no vehicles are travelling along a traffic lane, for example, lane occupancy of that lane is zero. However, lane occupancy approaches 100 percent when vehicles are almost bumper-to-bumper along the traffic lane. The system herein disclosed measures lane occupancy separately at each detector, and averages the measurements in computer **20**.

It should be noted that lane occupancy is not necessarily related to traffic volume. For example, when vehicles are travelling with substantial spacing between them but at a relatively high speed, lane occupancy may be low but

traffic volume may nevertheless be quite high. On the other hand, when vehicles are bumper-to-bumper but not moving, whatever the reason, lane occupancy is substantially 100 percent, but traffic volume under those conditions is zero.

Lane occupancy, however, is related to traffic density. Density may be expressed in terms of vehicles per unit length of highway. Lane occupancy on the other hand is expressed in terms of percentage of a highway lane, or segment thereof, occupied by vehicles. Therefore, lane occupancy may be expressed in terms of density multiplied by a factor equal to the average length of vehicles travelling along the traffic lane.

A voltage analog of the inverse of average speed is computed by computer **20** which divides average traffic density by average traffic volume to arrive at the inverse of average traffic flow velocity within the sections of highway sensed by the vehicle detectors providing inputs to computer **20**. An average value of inverse traffic flow velocity is provided by the computer, since each input to the computer is applied through a summing resistor which permits only an algebraic sum of computer input voltages to be coupled to the input of operational amplifier **151** within the computer. Expressed mathematically, for a speed computation resulting from actuation of relay AS1 only:

Let

Q_1=charge on capacitor **169**
Q_2=charge on capacitor **152**
C=capacitance of capacitor **169**
E=amplitude of the positive voltage source
V=traffic volume expressed in

$$\frac{\text{vehicles}}{\text{unit time}}$$

D=traffic density expressed in

$$\frac{\text{vehicles}}{\text{unit length}}$$

A=average length of vehicles
L=traffic lane occupancy
E_o=amplitude of output voltage from ampjlifier **151**
R=ohmic value of resistor **156**
t=time during which a single vehicle is sensed by the detector energizing relay AS1

While relay AS1 is deenergized, capacitor **169** charges according to the equation

$$Q_1=CE_o$$

This charge is supplied by output energy from amplifier **151**.

However, when relay AS1 is energized, capacitor **169** discharges substantially to zero through summing resistor **165**, since the common sides of the summing resistors are substantially at ground potential. This discharge current flows through capacitor **152**, incrementally reducing the charge stored thereon.

While relay AS1 is energized, capacitor **152** charges according to the equation

$$Q_2=\frac{E}{R}t$$

Over a period T of several minutes, the rate at which capacitor **152** charges is

$$\frac{Q_2}{T}=\frac{E}{R}\frac{nt}{T}$$

where n is the number of vehicles sensed during time T. Lane occupancy sensed by the detector energizing relay AS1 may be defined as the length of time in period T during which the relay is energized. Hence

$$L=\frac{nt}{T}$$

Thus, during period T, the rate at which capacitor **152** charges is

$$\frac{Q_2}{T}=\frac{E}{R}L$$

Similarly, during period T, the rate at which capacitor **169** charges, and hence the rate at which capacitor **152** discharges, is

$$\frac{Q_1}{T}=\frac{CE_o}{T}n$$

Traffic volume sensed by the detector energizing relay AS1 may be defined as the number of times in period T during which the relay is energized and subsequently deenergized. Hence

$$V=\frac{n}{T}$$

Thus, during period T, the rate at which capacitor **169** charges is

$$\frac{Q_1}{T}=CE_oV$$

which is also the rate at which capacitor **152** discharges.

Under equilibrium conditions, that is, when the voltage on capacitor **152** correctly represents the traffic speed sensed by the vehicle detector energizing relay AS1, no net charge is added to or removed from capacitor **152** during period T. Thus the rates of charge and discharge of capacitor **152** must be equal. This may be expressed as follows:

$$\frac{Q_2}{T}=\frac{Q_1}{T}$$

or

$$\frac{E}{R}L=CE_oV$$

Therefore,

$$E_o=\frac{EL}{R}\frac{1}{CV}$$

which may be written

$$E_o=\frac{EL}{R}\frac{1}{CV}\frac{A}{A}$$

As previously mentioned, lane occupancy sensed by a vehicle detector may be expresesd in terms of density multiplied by a factor equal to the average length of vehicles travelling past the vehicle detector, or

$$D=\frac{L}{A}$$

Hence, Equation 1 may be rewritten as

(2)
$$E_o=\frac{EA}{CR}\frac{D}{V}$$

Since E, A, C and R are constants, E_o is seen to be directly proportional to the quantity D/V. Moreover, as already mentioned,

$$\frac{D}{V}=\frac{1}{\text{traffic flow speed}}$$

Thus, output voltage E_o from amplifier **151** is inversely proportional to measured speed. Since each detector in the system may provide a separate input voltage to the amplifier, these voltages are algebraically summed in the summing resistors so that the composite input voltage to amplifier **151** represents an average of all vehicle detections in the monitored arterial sections. Thus, E_o is then inversely proportional to the average speed of traffic flow through the monitored arterial highway sections.

Because output voltage amplitude from inverse speed computer **20** can rise to infinity, the series circuit comprising diode **153** and resistor **154** is shunted across the input and output of amplifier **151**, in order to limit the

maximum output voltage level of amplifier **151**. The plate of diode **153** is coupled to the input of amplifier **151**, while the cathode is coupled to resistor **154**. A resistor **155** couples positive voltage to the cathode of diode **153**. In this fashion, the cathode of diode **153** may be held at a positive potential with respect to the plate, when no output voltage is provided from the amplifier. This positive potential is adjustable, according to the comparative values of resistors **154** and **155**. When output voltage from amplifier **151** exceeds a predetermined negative value dependent upon the values of resistors **154** and **155**, the cathode of diode **153** becomes negative with respect to the plate, thereby commencing conduction. Resistor **154** is thereby shunted across the input and output of amplifier **151**, decreasing its gain. This is necessary in order to secure proper operation of the computer by remaining within tolerable voltage limits throughout. It should be noted that any vehicle halted under a detector for any reason whatsoever, produces a zero speed indication since lane occupancy sensed by the detector is 100% and volume sensed by the detector is zero.

Output voltage from inverse speed computer **20** is coupled through averager **21** to distance coefficient multiplier **22**. This multiplier comprises an operational amplifier **181** having a resistor **182** shunted across its input and output. Input voltage to amplifier **181** is provided through a resistor **183**. Hence, operational amplifier **181** functions as a phase inverter amplifier. In addition the plate of a diode **185** is coupled to the input of amplifier **181** and a voltage divider **187** is coupled between the cathode of diode **185** and the output of amplifier **181**. Similarly, the cathode of a diode **186** is coupled to the input of operational amplifier **181** and a voltage divider **188** is coupled between the plate of diode **186** and the output of amplifier **181**. The output taps of voltage dividers **187** and **188** are also coupled to the output of amplifier **181**. A positive voltage is resistively coupled to the cathode of diode **185**, while a negative voltage is resistively coupled to the plate of diode **186**. It will be recognized that the purpose of diodes **185** and **186** is to provide maximum and minimum limitations on cycle time provided from distance coefficient multiplier **22**. These limitations may be varied by manually adjusting the output taps on potentiometers **187** and **188** respectively.

Output voltage from averager **21** is coupled through a potentiometer D to a back contact **191** of a relay L. Cycle distance is set into the multiplier by manually adjusting the tap of potentiometer D. Front contact **191** receives positive energization from a manually adjustable tap on a potentiometer **195**.

In the event relay L is deenergized, output voltage from averager **21** is applied across potentiometer D, and the poriton of voltage appearing between the potentiometer tap and ground is RC coupled from back contact **191** to the input of operational amplifier **181**. However, in the event relay L is energized, the voltage appearing between the tap of potentiometer **195** and ground is RC coupled from front contact **191** of relay L to the input of operational amplifier **181**. Under such circumstances, output of computer **20** is disregarded, and cycled duration is adjusted by positioning the tap on potentiometer **195**.

Relay L is energized when all sections of the system are in a light traffic offset. This is because relays SR, IR and OR in the section failure detection and preferential offset circuits are all deenergized. Hence, relay L is energized through a series circuit comprising a back contact **195** of relay SR in circuit **150**, a back contact **135** of relay IR in circuit **150**, and a back contact **145** of relay OR in circuit **150** connected in series with identical contacts of the SR, IR and OR relays of circuits **250** and **350**. In addition, provision is made in the section failure detection and preferential offset circuits for failure of both inbound or both outbound detectors. For example, in the event both inbound detectors of circuit **150** should fail, relay IF is energized, closing its front contact **114**. This contact is connected in parallel with back contact **135** of relay IR, so that in the event an inbound offset exists in section A, relay L can still be energized provided light offsets exist in sections B and C, since front contact **114** is closed. Similarly, in the event an outbound offset exists in section A and outbound detectors AO1 and AO2 are inoperative, relay OF is energized, closing its front contact **127**, thereby shunting contact **145** and permitting energization of relay L provided light offsets exist in sections B and C. By thus maintaining relay L energized, the preselected voltage from potentiometer **195** rather than the computed voltage from inverse speed computer **20** is coupled to amplifier **181**. This prevents erroneous readings from being introduced into the system from the section A vehicle detectors when light offsets exist in both sections B and C. Identical protection is afforded the sections B and C failure detection and preferential offset circuits.

Energization of relay L closes its front contacts **192**, **193** and **194**, energizing relay AR in each section failure detection and preferential offset circuit. This has the effect of bypassing circuitry associated with relays IR and OR in each failure detection and preferential offset circuit, so as to permit voltages produced by the vehicle detectors for each section to reach the computer input relays for the associated section in computer **20**. This causes all sections to be treated as though an average offset exists, insofar as amplifier **151** is concerned. Thus, during light traffic offsets, the computer input relays of computer **20** are connected to the respective detectors so that a valid average inverse speed is computed at this time. In this manner, when relay L becomes deenergized, due to appearance of a preferential offset, a reasonably valid inverse speed voltage analog will be present at the output of amplifier **151** for immediate use in generating cycle rate with reasonable accuracy.

Hence, it is obvious that when any section changes to an offset other than light, the circuit energizing relay L is interrupted and the output voltage of inverse speed computer **20** is utilized, except that when a preferential offset is called for in one section and all detectors in the preferential direction in that section have failed, and provided all the remaining sections are in a light offset, relay L remains energized.

The output voltage from distance coefficient multiplier **22** may be read on a meter **196**. This meter provides an indication of cycle duration, and may be calibrated directly in units thereof. This voltage is also coupled to cycle rate signal generator **13** by supplying a first input voltage to analog comparator **23** through a coupling resistor **197**. A second input voltage to analog comparator **23** is furnished from integrator **24**. Positive and negative voltages are resistively coupled to front and back contact **26**, respectively. This contact is controlled by a relay PA which is driven from power amplifier **25**, which in turn is driven from analog comparator **23**. Front contact **27** of relay PA grounds output voltage from amplifier **181** through resistor **197** each time the relay is energized, thereby driving voltage applied to the first input of analog comparator **23** to zero. Back contact **27** of relay PA may provide cycle rate output pulses by coupling resistor **28**, shown dotted, between the positive voltage source and back contact **27**.

Assuming relay PA is deenergized, negative potential is applied to integrator **24** so that output voltage from the integrator rises from zero in the positive direction. When this voltage reaches a sufficiently high value to exceed the negative cycle duration analog voltage from amplifier **181** applied to analog comparator **23**, output voltage from the comparator abruptly changes from a highly positive value to a highly negative value. This produces a highly positive output voltage from power amplifier **25** which energizes relay PA. This closes front contacts **26** and **27** and opens back contacts **26** and **27**. Front contact **27** thereby removes the negative cycle duration input voltage from analog comparator **23**, while front contact **26**

applies a positive input voltage to integrator 24. This causes output voltage from integrator 24 to fall from a positive potential toward zero. When this output voltage reaches zero and becomes slightly negative, analog comparator output voltage abruptly changes from a highly negative value to a highly positive value. Output voltage from power amplifier 25 then swings negative, deenergizing relay PA. Thus, relay PA alternately energizes and deenergizes at a rate inversely proportional to output voltage amplitude of amplifier 181, and therefore inversely proportional to computed cycle duration. Moreover, it should be noted that rate signal generator 13 is so designed that the output voltage produced therefrom consists of a constant number of pulses per signal cycle.

Thus, there has been shown a computer for providing cycle duration control of traffic signals along a section of highway in accordance with demands of traffic. The computer provides traffic signal cycle duration information for traffic signals located along a highway based upon average traffic speed along the highway. Moreover, the system computes traffic signal cycle duration only during occurrence of predetermined traffic offsets. The computer is readily adaptable for use with multi-lane highways simply by addition of detectors in each section to separately detect traffic in each lane, and by addition of computer input relays to accommodate additional input voltages to the inverse speed computer. The system is rugged and reliable, requires but a modest amount of power, and is readily adaptable to a traffic artery of any length, having any number of intersections with secondary streets, and handling widely fluctuating traffic loads.

Although but one embodiment of the present invention has been described, it is to be specifically understood that this form is selected to facilitate in disclosure of the invention rather than to limit the number of forms which it may assume, and various modifications and adaptations may be applied to the specific forms shown to meet requirements of practice, without in any manner departing from the spirit or scope of the invention.

What is claimed is:

1. A traffic signal cycle computer comprising means responsive to average vehicular speed along a highway for providing a voltage inversely proportional thereto, means multiplying said voltage by a coefficient proportional to distance between traffic signals operating in phase with each other to provide a voltage analog of optimum cycle duration, and additional means dividing the voltage analog of optimum cycle duration into a predetermined number of pulses per cycle.

2. The traffic signal cycle computer of claim 1 wherein said additional means comprises integrator means, comparator means responsive to the algebraic sum of the voltage analog of optimum cycle duration and the time integral of a constant voltage produced by said integrator means, and means responsive to the comparator means for removing the voltage analog of optimum cycle duration from the comparator means when the algebraic sum changes to a predetermined polarity.

3. The traffic signal cycle computer of claim 1 wherein said responsive means providing a voltage comprises means providing average traffic volume information, means providing average traffic lane occupancy information, and means dividing the lane occupancy information by the volume information for providing a voltage analog of inverse average traffic speed.

4. The traffic signal cycle computer of claim 3 wherein said additional means comprises integrator means, comparator means responsive to the algebraic sum of the voltage analog of optimum cycle duration and the time integral of a constant voltage produced by said comparator means, and means responsive to the comparator means for removing the voltage analog of optimum cycle duration from the comparator means when the algebraic sum changes to a predetermined polarity.

5. A traffic signal cycle computer comprising means responsive to average vehicular speed along a highway for providing a voltage inversely proportional thereto, means multiplying the voltage by a coefficient proportional to distance between traffic signals operating in phase with each other to produce a voltage analog of optimum cycle duration, a source of constant voltage, and switching means responsive to lane occupancy of at least one location along the highway for selecting either the constant voltage or the voltage analog of optimum cycle duration to represent the computed cycle duration.

6. The traffic signal cycle computer of claim 5 wherein said responsive means providing a voltage inversely proportional to average vehicular speed comprises means providing average traffic volume information, means providing average traffic density information, and means dividing the density information by the volume information for providing a voltage analog of inverse average traffic speed.

7. The traffic signal cycle computer of claim 5 including additional means dividing the computed cycle duration into a predetermined number of pulses per cycle.

8. The traffic signal cycle computer of claim 7 wherein said responsive means providing a voltage inversely proportional to average vehicular speed comprises means providing average traffic volume information, means providing average traffic density information, and means dividing the density information by the volume information for providing a voltage analog of inverse average traffic speed.

9. The traffic signal cycle computer of claim 7 wherein said additional means comprises integrator means, comparator means responsive to the algebraic sum of the computed cycle duration and the time integral of a constant voltage produced by said integrator means, and means responsive to the comparator means for removing the computed cycle duration from the comparator means when the algebraic sum changes to a predetermined polarity.

10. In a traffic signal cycle computer having at least a single vehicle presence detector, means responsive to the presence detector for providing a voltage analog of inverse average speed of traffic sensed by the presence detector comprising, operational amplifier means having an input and an output, feedback capacitor means shunted across the input and output of the operational amplifier means, and switching means responsive to the presence detector coupling steady energy to the input of the operational amplifier means and removing a quantum of energy from the feedback capacitor means during each interval in which a vehicle is sensed by the detector.

11. In a traffic signal cycle computer having at least a single vehicle presence detector, means responsive to the presence detector for providing a voltage analog of inverse average speed of traffic sensed by the presence detector comprising, operational amplifier means having an input and an output, at least two resistors coupled to the input of the operational amplifier means, feedback capacitor means shunted across the input and output of the operational amplifier means, and switching means responsive to the presence detector coupling steady energy to one of the resistors and removing a quantum of energy from the feedback capacitor means through a second resistor during each interval in which a vehicle is sensed by the detector.

12. A traffic signal cycle computer comprising at least a single vehicle presence detector; means responsive to the presence detector for providing a voltage analog of inverse average speed of traffic sensed by the presence detector, said responsive means including operational amplifier means having an input and an output, at least two resistors coupled to the input of the operational amplifier means, feedback capacitor means shunted across the input and output of the operational amplifier means,and switching means responsive to the vehicle presence detector coupling steady energy to one of the resistors and removing a quantum of energy from the capacitor means through a

second resistor during each interval in which a vehicle is sensed by the detector; and means multiplying the voltage analog of inverse average traffic speed by a coefficient proportional to distance between traffic signals operating in phase with each other to provide a voltage analog of optimum cycle duration.

13. The traffic signal cycle computer of claim 12 including additional means dividing the voltage analog of optimum cycle duration into a predetermined number of pulses per cycle.

14. The traffic signal cycle computer of claim 13 wherein said additional means comprises integrator means, comparator means responsive to the algebraic sum of the voltage analog of optimum cycle duration and the time integral of a constant voltage produced by the integrator means, and means responsive to the comparator means for removing the voltage analog of optimum cycle duration from the comparator means when said algebraic sum changes to a predetermined polarity.

15. A traffic signal cycle computer comprising at least a single vehicle presence detector; means responsive to the detector for producing a voltage analog of inverse average speed of traffic sensed by the presence detector, said responsive means including operational amplifier means having an input and an output, at least two resistors coupled to the input of the operational amplifier means, feedback capacitor means shunted across the input and output of the operational amplifier means, and switching means responsive to the vehicle presence detector coupling steady energy to one of the resistors and removing a quantum of energy from the capacitor means through a second resistor during each interval in which a vehicle is sensed by the detector; means multiplying the voltage analog of inverse average traffic speed by a coefficient proportional to distance between traffic signals operating in phase with each other to provide a voltage analog of optimum cycle duration; a source of constant voltage; and switching means responsive to lane occupancy of at least one location along the highway for selecting either the constant voltage or the voltage analog of optimum cycle duration to represent the computed cycle duration.

16. The traffic signal cycle computer of claim 15 including additional means dividing the computed cycle duration into a predetermined number of pulses per cycle.

17. The traffic signal cycle computer of claim 16 wherein said additional means comprises integrator means, comparator means responsive to the algebraic sum of the voltage analog of optimum cycle duration and the time integral of a constant voltage produced by the integrator means, and means responsive to the comparator means for removing the voltage analog of optimum cycle duration from the comparator means when said algebraic sum changes to a predetermined polarity.

18. A traffic signal cycle computer comprising, vehicle responsive means for providing a signal representing average traffic volume along a highway, vehicle responsive means providing a signal representative of average traffic lane occupancy along said highway, means dividing said lane occupancy signal by said volume signal for providing an analog representative of inverse average traffic speed, and means for multiplying said analog of inverse average traffic speed by a coefficient proportional to distance between traffic signals operating in phase with each other to provide a voltage analog of optimum cycle duration.

19. In a progressive traffic control system for a plurality of traffic signals controlling traffic at spaced intersections along an artery, means demarcating successive signal cycles of variable duration for said plurality of traffic signals, vehicle responsive means for generating a signal inversely related to the speed of vehicles traveling along said artery, and means for controlling the duration of the signal cycle demarcated by said demarcating means in response to said generated signal.

20. The system of claim 19 which further includes offset control means for determining the offset for each successive traffic signal of said plurality, said offset control means controlling selected traffic signals at predetermined intervals along said artery to operate in phase coincidence and controlling said signals situated in between each pair of said selected signals to operate with a predetermined offset relative to said selected traffic signals, said cycle duration controlling means so controlling the duration of the signal cycle in effect at any time in response to vehicle speed as measured by said vehicle responsive means as to correspond substantially to the time for a vehicle to travel said predetermined distance along said artery.

21. The system of claim 20 wherein said offset control means at times establishes preferential offsets of said traffic signals for a predetermined duration of traffic along said artery and at other times establishes a non-preferential offset for said traffic signals, said vehicle responsive means including detector means individual to the different directions of traffic along said artery, and means controlling said cycle duration controlling means to be responsive to said vehicle detectors for both directions of traffic when a non-preferential offset has been put into effect by said offset control means and to be responsive to said vehicle detector for only one direction of traffic when said offset control means has put into effect a preferential offset for the corresponding direction of traffic.

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