OPTO-ELECTRONIC DEVICES WITH MULTIPLE OXIDE APERTURES

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Appl. No.: 09/800,087
Filed: Mar. 5, 2001

Related U.S. Application Data
Continuation-in-part of application No. 09/603,140, filed on Jun. 23, 2000, which is a continuation-in-part of application No. 09/375,338, filed on Aug. 16, 1999, which is a continuation of application No. 09/060, 227, filed on Apr. 14, 1998, now Pat. No. 5,991,326 and which is a continuation-in-part of application No. 09/603,140, filed on Jun. 23, 2000 and which is a non-provisional of provisional application No. 60/184,706, filed on Feb. 24, 2000.

Publication Classification
Int. Cl. 7 .................................................. H01S 5/00
U.S. Cl. .......................................................... 372/43

ABSTRACT
A vertical cavity apparatus includes a die with a top surface and a plurality of planar electrically conducting layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. A plurality of oxide apertures are formed by via holes connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. An optoelectronic device is coupled to a single oxide aperture in the die.
FIG. 9

FIG. 10
FIG. 24
OPTO-ELECTRONIC DEVICES WITH MULTIPLE OXIDE APERTURES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of Ser. No. 09/603,140, filed Jun. 23, 2000, which is a continuation-in-part of Ser. No. 09/375,338, filed Aug. 16, 1999, which is a continuation of Ser. No. 09/060,227, filed Apr. 14, 1998 (now U.S. Pat. No. 5,991,326), said Ser. No. 09/603,140 also being a continuation-in-part of and claiming the benefit of provisional application Ser. No. 60/184,706 filed Feb. 24, 2000, all of which applications are fully incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention
[0003] This invention relates generally to a vertical cavity apparatus, and more particularly to a vertical cavity structure that includes a die with a plurality of oxide apertures formed by via holes, trench structures and mesas.

[0004] 2. Description of the Prior Art
[0005] Continued advances in long-distance, fiber-optic communications depend on high-quality laser sources. Since optical fibers exhibit lowest attenuation and dispersion at the wavelengths of 1.3 μm and 1.55 μm, suitable sources should emit at these relatively long wavelengths in single-mode operation.

[0006] Traditionally, long-wavelength distributed feedback (DFB) lasers are employed in fiber-optic communications systems for their single longitudinal and transverse mode characteristics. However, fabricating DFB lasers involves very complicated and low-yield processes. Furthermore, the DFB laser performance is very sensitive to the surrounding temperature change. Thus, complicated electronics are needed in the transmitter to control the operating environment. These disadvantages render the DFB laser a very expensive light source and severely limit its application in the fiber-optic communications field.

[0007] Vertical Cavity Surface Emitting Lasers (VCSELs) emitting in the 1.3 μm and 1.55 μm ranges have been visualized as promising candidates for replacing DFBs in telecommunications applications. Due to their extremely short cavity length (on the order of one lasing wavelength), VCSELs are intrinsically single longitudinal mode devices. This eliminates the need for complicated processing steps that are required for fabricating DFB lasers. Furthermore, VCSELs have the advantage of wafer-scale fabrication and testing due to their surface-normal topology.

[0008] Unfortunately, VCSELs suffer material limitations that are negligible in the case of short-wavelength VCSELs but drastically affect the performance of long-wavelength VCSELs. The small available refractive index difference Δn between reflective layers of the Distributed Bragg Reflectors(DBRs) requires that a large number of layers with high composition and thickness precision be used to achieve sufficient reflectivity. Another object of the present invention is to reduce loss in a vertical cavity apparatus. Due to the small Δn the relatively thick DBR's result in high diffraction losses. Furthermore, high free-carrier absorption loss limits the maximum achievable reflectivity and the high non-radiative recombination rate increases the electrical current for reaching the lasing threshold.


[0010] Unfortunately, these methods do not allow one to efficiently grow long-wavelength VCSELs.

[0011] Tunneling in GaAs, at a n+p+ junction, is well known (see, for example, N. Holonyak, Jr. and I. A. Lesk, Proc. IRE 48, 1405, 1960), and is generally of interest for its negative resistance. Tunneling InGaAs can be enhanced with an InGaAs transition region (see, for example, T. A. Richard, E. I. Chen, A. R. Sugg, G. E. Holter, and N. Holonyak, Jr., Appl. Phys. Lett. 63, 3613, 1993), and besides its negative resistance behavior, can be used in reverse bias as a form of "ohmic" contact. This allows, for example, the reversal of the doping sequence of an Al sub x Ga sub 1-x As—GaAs quantum well heterostructure laser (n forward arrow p to p forward arrow n) grown on an n-type GaAs substrate. See, for example, A. R. Sugg, E. I. Chen, T. A. Richard, S. A. Maranowski, and N. Holonyak, Jr., Appl. Phys. Lett. 62, 2510 (1993) or the cascading of absorbing regions to produce higher efficiency solar cells (see for example D. L. Miller, S. W. Zehr and J. S. Harris Jr, Journ. Appl. Phys., 53(1), pp 744-748, (1982) and P. Basmajian, M. Guittard, A. Rudra, J. E. Carlin and P. Gibart, Journ. Appl., Phys., 62(5), pp 2103-2106, (1987)).

[0012] Unfortunately, these methods do not allow one to efficiently grow long-wavelength VCSELs.

[0013] A variety of devices are formed on wafers including but not limited to lasers, photodetectors, filters electronic circuits and MEMS. These devices are formed on the wafers utilizing a variety of standard multi-processing steps and procedures. The wafer is typically moved from one process station to another until the final device is completed on the wafer. The devices are then tested. Following testing, the wafer is diced and individual devices are then mounted, electrical connections are made and then there is a final sealing.
Laser diodes typically include an n-type substrate, an active layer, a p-type clad layer and a p-type cap layer that is laminated over the n-type substrate. In one such semiconductor laser, the n-type substrate is formed of AlGaAs and the active layer is formed of GaAs. An electrode is selectively formed on the reverse surface of the laser diode in an opening of the p-type cap layer. A rear electrode is formed on the reverse surface of the substrate. The resulting structure is a laser diode chip more commonly known as a double heterostructure (DH structure). This laser diode chip can be mounted on a radiation plate. The assembly is then encapsulated to hermetically seal the device.

U.S. Pat. No. 5,896,408 discloses a VCSEL with at least one mirror that includes a plurality of planar electrically conducting layers with different indices of refraction. One of the layers includes an oxidizable material. To expose the oxidizable layer to an oxidizing agent, and convert the material to an electrical insulator, three or more holes are etched down from the top surface of the VCSEL to the layer containing the oxidizable material. The oxidizing agent is then introduced into the top of these holes. The partial oxidation of the layer converts the layer to one having a conducting region surrounded by an electrically insulating region, the conducting region being positioned under the top electrode.

U.S. Pat. No. 5,978,408 discloses a VCSEL structure with well-defined and well-controlled oxidized regions that are used to define the lasing aperture of the VCSEL. These oxidized regions are formed by the use of a multiplicity of cavities arranged in a predefined pattern in the laser structure. The lasing aperture is an oxidized region bounded by these oxidized regions centered about the cavities. During the oxidation process, an AlGaAs layer with high aluminum content embedded in the semiconductor structure is oxidized radially outwards from each of these cavities until the oxidized regions between two adjacent cavities overlap. However, the devices in the above-referenced patents fail to change the pitch of individual groups of via holes to form different oxide aperture sizes. There is a need for electro-optic devices with an array of via holes, trench structures or mesas that are used to form several oxide apertures of different sizes, with the oxide apertures coupling light from an active region underneath and while being electrically isolated from their neighbors.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide improved electro-optic devices.

Another object of the present invention is to provide improved micro-optomechanical, micro-electromechanical and micro-optoelectrical devices that are formed on a single die.

A further object of the present invention is to provide electro-optic devices with an array of via holes to form several oxide apertures of different sizes, with the oxide apertures being electrically isolated from each other and coupling light from an underlative active region.

A further object of the present invention is to provide electro-optic devices with an array of trench structures to form several oxide apertures of different sizes, with the oxide apertures being electrically isolated from each other and coupling light from an underlative active region.

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Further objects of the present invention are provided in the following paragraphs.

In another embodiment of the present invention, a vertical cavity apparatus includes a die with a top surface and a plurality of planar electrically conducting layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. A plurality of oxide apertures are formed by via holes connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. An optoelectronic device is coupled to a single oxide aperture in the die.

In another embodiment of the present invention, a vertical cavity apparatus includes a die with a top surface and a plurality of planar electrically conducting layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. A plurality of oxide apertures are formed by via holes connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. An optoelectronic device is coupled to a single oxide aperture in the die.

In another embodiment of the present invention, a vertical cavity apparatus includes a die with a top surface and a plurality of layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. The die includes a plurality of via holes/trenches/mesas connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. A tunable laser is coupled to the single oxide aperture in the die.

In another embodiment of the present invention, a multi-modulus device includes a die with a top surface and a plurality of layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. The die includes a plurality of via holes/trenches/mesas connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. A tunable laser is coupled to the single oxide aperture in the die.

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In another embodiment of the present invention, a multi-modulus device includes a die with a top surface and a plurality of layers. At least one of the layers is an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. The die includes a plurality of via holes/trenches/mesas connecting the top surface to the oxide layer. A majority of the individual oxide apertures have different sizes. A tunable laser is coupled to the single oxide aperture in the die.
material to an electrical insulator, the die including a plurality of via holes/trenches/ mesas connecting the top surface to the oxide layer. A majority of individual oxide apertures having different res. A tunable laser is formed in one of the oxide apertures. The laser includes an active region with first and second opposing reflectors that define a laser gain vity. A first photodetector is positioned outside of the laser gain cavity. An adjustable wavelength selective filter is includes and splits the output beam into a transmitted portion and a reflected portion. The adjustable wavelength selective filter is positioned at an angle $\theta$ relative to the optical axis to provide an angular dependence of a wavelength reflection of the wavelength selective filter and direct the reflected output beam towards the first photodetector. The wavelength selective filter provides wavelength selectivity by changing the angle $\theta$ and a ratio of the transmitted and reflected portions is a function of wavelength of output beam and the angle $\theta$.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIG. 1(a) is a cross-sectional view of a VCSEL structure of the present invention with two active layers, a tunnel junction positioned between the top and bottom mirror and an oxide layer positioned between the top mirror and the top active layer.

[0028] FIG. 1(b) is a cross-sectional view of a VCSEL structure of the present invention with a tunnel junction positioned between the top and bottom mirrors and an oxide layer positioned adjacent to the bottom mirror.

[0029] FIG. 1(c) is a cross-sectional view of the VCSEL structure of FIG. 1(a) with a second tunnel positioned between the top and bottom mirrors.

[0030] FIG. 2 is a cross-sectional view of the VCSEL structure of FIG. 1(a) with three active layers, two tunnel junctions and an oxide layer positioned between the top mirror and the top active layer.

[0031] FIG. 3 is a cross-sectional view of the VCSEL structure of FIG. 2 with two additional oxide layers, each positioned between a tunnel junction and an active layer.

[0032] FIG. 4 is a cross-sectional view of the VCSEL structure of FIG. 2 with partial DBR’s, each positioned between a tunnel junction and an active layer.

[0033] FIG. 5 is a cross-sectional view of the VCSEL structure of FIG. 4 with two additional oxide layers, each positioned between a tunnel junction and an active layer.

[0034] FIG. 6 is a perspective view of the substrate from the FIG. 1(a) through FIG. 5 VCSELs with an etched pattern formed on a top or bottom surface.

[0035] FIG. 7 is a cross-sectional view of a top mirror used with the present invention that includes a metallic layer.

[0036] FIG. 8 is a cross-sectional view of a top mirror used with the present invention that is coupled to a tunable filter.

[0037] FIG. 9 is a cross-sectional view of a tunnel junction used with the present invention, illustrating the tunnel junction’s opposing first and second sides.

[0038] FIG. 10 is a cross-sectional view of an active layer of the present invention that includes quantum wells and barriers.

[0039] FIG. 11 is a cross-sectional view of a VCSEL structure of the present invention with a tunnel junction positioned between the top mirror and an oxide layer, and the top mirror is an n-doped DBR.

[0040] FIG. 12 is a cross-sectional view of a VCSEL structure of the present invention with a tunnel junction positioned between the top mirror and an oxide layer, and the top mirror is an n-doped DBR.

[0041] FIG. 13 is a cross-sectional view of a VCSEL structure of the present invention with an oxide layer positioned between the top mirror and the top active layer, and a tunnel junction positioned between the oxide layer and the top active layer.

[0042] FIG. 14 is a cross-sectional view of a VCSEL structure of the present invention with an ion implantation layer.

[0043] FIG. 15 is a cross-sectional view of a VCSEL structure similar to the VCSEL structure of FIG. 5 with ion implantation layers substituted for the second and third oxide layers.

[0044] FIG. 16 is a cross-sectional view of a VCSEL structure similar to the VCSEL structure of FIG. 1(a) with the inclusion of an etched layer.

[0045] FIG. 17 is a cross-sectional view of a VCSEL structure similar to the VCSEL structure of FIG. 5 with etched layers substituted for the second and third oxide layers.

[0046] FIG. 18(a) is a cross-sectional view of the etched layer of FIG. 16 with a vertical profile.

[0047] FIG. 18(b) is a cross-sectional view of the etched layer of FIG. 16 with a sloped profile.

[0048] FIG. 18(c) is a cross-sectional view of the etched layer of FIG. 16 with a variable geometric profile.

[0049] FIG. 18(d) is a cross-sectional view of the etched layer of FIG. 16 with another example of a variable geometric profile.

[0050] FIG. 18(e) is a cross-sectional view of the etched layer of FIG. 16 with yet another example of a variable geometric profile.

[0051] FIG. 19 is a cross-sectional view of a vertical cavity structure of the present invention with a fiber grating.

[0052] FIG. 20 is a cross-sectional view of a top mirror used with the present invention that is a fused mirror.

[0053] FIG. 21 is a cross-sectional view of a top mirror used with the present invention that is a cantilever structure.

[0054] FIG. 22(a) is a sectional view of one embodiment of a vertical cavity structure of the present invention that includes a die with a plurality of oxide apertures formed by via holes.

[0055] FIG. 22(b) is a top down view of the FIG. 26(a) structure.

[0056] FIG. 23 is a top down view of an opto electronic device of the present invention illustrating etching trench structures around mesas.
FIG. 24 is a top down view of a DBR of the present invention illustrating four devices of different aperture sizes on one die.

The high-contrast, oxidized top mirror 12 reduces the diffraction loss and eliminates the free-carrier absorption loss.

When top mirror 12 is oxidized, the thickness of high Al-content layers is calculated by taking into account the refractive index and thickness change resulting from the oxidation process. The oxidized part of top mirror 12 is undoped to eliminate free-carrier absorption loss. Oxidation of top mirror 12 can be done in conjunction with the oxidation of the confinement layer. The oxidation procedure can be conducted in a water-saturated nitrogen ambient, at a temperature between 350°C to 450°C.

Top and bottom mirrors 12 and 14, as well as the active regions, can be grown in the same epitaxial process. This procedure allows full wafer growth and processing, and therefore significantly reduces the cost of fabricating long-wavelength VCSELs. The lattice relaxed portion of VCSEL 10 can also be grown by a separate epitaxial growth process. When using the molecular beam epitaxy method, the growth temperature for top mirror 12 is preferably less than 500°C. The lattice-relaxed mirror can incorporate a tunnel junction. At least one layer of VCSEL 10 can be grown while the substrate 24 is held stationary and the other layers are grown while substrate 24 is rotated.

Referring now to FIG. 1(c), a second tunnel junction 26 can be optionally included and positioned between bottom mirror 14 and second active layer 18. Additional tunnel junctions increase the gain. A first partial DBR 28 can also be included and positioned between first and second active regions 16 and 18.

FIG. 2 illustrates an embodiment of VCSEL 10 with a third active region 20. First and second tunnel junctions 20 and 26 are positioned between first, second and third active regions 16, 18 and 30 respectively. Although first oxide layer 22 is shown as being positioned adjacent to top mirror 12, it will be appreciated that another oxide layer 22 can alternatively be positioned between active layers. Additional active layers can be included. Preferably, no more than ten active layers are included. More preferably the number of active layers is five or less or no more than three.

Additional oxide layers can be included. FIG. 3 the inclusion of second and a third oxide layers 32 and 34 are used to reduce current spread. Oxide layers 32 and 34 become insulators and force the current to be funneled in the semiconductor layer (at the center) that is not oxidized. In the embodiment illustrated in FIG. 3, oxide layer 32 is positioned between first tunnel junction 20 and second active layer 18, and third oxide layer 34 is positioned between second junction 26 and third active region 30. This specific arrangement reduces the current spreading between active layers.

As shown in FIG. 4, multiple partial DBR’s can be included and positioned between top and bottom mirrors 12 and 14. First and second partial DBR’s 28 and 36 form several FP cavities with different FP wavelengths in order to stabilize the performance in temperature and the wavelength range of tuning. In FIG. 4, first partial DBR 28 is positioned between first and second active regions 16 and 18. Second partial DBR 36 is positioned between second and third active regions 18 and 30. In the embodiment illustrated in FIG. 4, first tunnel junction 20 is positioned first active region 16 and first partial DBR 28. Second tunnel junction 26 is positioned between second active region 18 and second partial DBR 36.

As illustrated in FIG. 5, the VCSEL 10 from FIG. 4 can also include second and third oxide layers 32 and 34...
that are positioned between the first and second partial DBR’s 28 and 36 and active regions 18 and 30.

[0070] Substrate 24 has a given crystallographic orientation. Examples of suitable crystallographic orientations include but are not limited to (001), (311A), (311B) and (110). As illustrated in FIG. 6, substrate 24 can have an etched pattern 38 formed on a top or bottom surface, where the top surface is adjacent to bottom mirror 14. Substrate 24 can include a dielectric pattern. All or a portion of the substrate 24 layers can be grown using selective area epitaxy.

[0071] Top mirror 12 can be tunable. A metallic layer 40 can be positioned on the top of top mirror 12. Metallic layer 40 boosts the reflectivity of the DBR. Top mirror 12 can be integrated with a tunable filter 42 (FIG. 8).

[0072] Referring now to FIG. 9, tunnel junctions 20 and 26 have first and second opposing sides 44 and 46 which are cladding regions. Cladding regions 44 and 46 can be made of the same material, different materials, have different thickness and have different doping profiles and can be non doped. Tunnel junctions 20 and 26 can be uniformly doped and non-uniformly doped. Tunnel junctions 20 and 26 are doped with opposite dopants (i.e., n-type/p-type). Additionally, tunnel junctions 20 and 26 and cladding regions 44 and 46 can be compositionally graded.

[0073] As illustrated in FIG. 10 each active region 16, 18 and 30 includes a least one quantum well, generally denoted as 48 in FIG. 10. In one embodiment, each active region includes a plurality of quantum wells 48. The quantum wells 48 in each active region 16, 18 and 30 can have different widths, the same widths, different maximum gain wavelengths, the same maximum gain wavelength, different compositions, the same strain and different strain. Quantum wells 48 can be strained quantum wells, tense strained quantum wells, unstrained quantum wells, compression strained quantum well. All quantum wells 48 can be the same type, different types and combinations.

[0074] All or some of the different quantum wells 48 in each active region 16, 18 and 30 can have different widths, generate different maximum gain wavelengths, or generate the same maximum gain wavelengths. In one embodiment, quantum wells 48 in active region 16 generate a first wavelength, those in active region 18 a different wavelength, those in active region 30 yet another wavelength and so on.

[0075] Referring still to FIG. 11, the plurality of quantum wells 48 in each active region 16, 18 and 30 can have a plurality of barriers 50. All or a portion of the plurality of barriers 50 can have the same strain or different strains.

[0076] Each active region 16, 18 and 30 can be a bulk region. The use of a bulk region increases the confinement factor and the modal gain. Bulk regions 52 can be non-doped, uniformly doped or non-uniformly doped. Bulk regions 52 have opposing first and second sides 54 and 56 respectively that can be made of the same material or different materials. The thickness of first and second sides 54 and 56 can be the same or different. First and second sides 54 and 56 can have the same doping profiles, different doping profiles and different widths. Each bulk region 52 can be compositionally graded.

[0077] Due to the higher mobility of electrons compared to holes, reverse biasing enables the injection of holes through a low resistive n region. This is achieved by using an n doped top mirror 12 or using the structures of FIGS. 11 and 12. The structure illustrated in FIG. 11 includes an n doped top DBR 12 that reduces the resistance of the entire VCSEL 10 structure. In this embodiment, tunnel junction 20 allows the current to be injected with a low access resistance than oxide layer 22 which is located in p-regions.

[0078] In FIG. 12 first tunnel junction 20 is positioned between top mirror 12 and first oxide layer 22 and is either partially doped or undoped. The contact taken laterally on top of tunnel junction 20 can therefore flow in the low resistive n-type material before being converted into holes through the reverse biased tunnel junction 20. The current is then tunneled through the oxide aperture in layer 22. In the FIG. 11 embodiment, the current is injected through the top DBR 12 while in FIG. 12 embodiment the current is injected laterally. With the FIG. 12 embodiment, lateral injection of current permits the use of a non-doped DBR which greatly reduces the free carrier losses.

[0079] In another embodiment, illustrated in FIG. 13, first oxide layer 22 is positioned between top mirror 12 and first tunnel junction 20. In this embodiment, first oxide layer 22 is used for index guiding to allow for single mode stability and tunnel junction 20 function is used for current injection through low optical losses materials. In this embodiment, the current confinement is done through an implantation step, plasma etching or undercutting.

[0080] Variations of embodiments illustrated in FIGS. 11, 12 and 13 include use of a double intracavity contact by putting a lateral contact below active region 16 to allow bottom DBR 14 to be undoped which reduces the losses due to bottom DBR 14. Additionally, the embodiments illustrated in FIGS. 14 through 17 can also employ the lateral injection of current shown in the FIG. 11 and 12 embodiments.

[0081] Top mirror 12 can be an n-doped DBR. In order to benefit from the low access resistance of n-doped DBR 12, an injection through a reverse biased tunnel junction 20 are combined with first oxide layer 22 that induces an index guiding. In another embodiment of the present invention, illustrated in FIG. 14, VCSEL 10 includes first tunnel junction 20 and an ion implantation layer 58, each positioned between top and bottom mirrors 12 and 14. Ion implantation is used to locally destroy the conductive properties which enables the creation of a locally conductive area and provides for current localization. In the embodiment illustrated in FIG. 14, first ion implantation layers 58 is substituted for the oxide layers of the FIG. 1 through 13 embodiments. Additional ion implantation layers can be included and be positioned between adjacent tunnel junctions and active regions as shown in FIG. 15. First oxide layer 22 can also be included and positioned between top mirror 12 and top active region, or between bottom mirror 14 and the bottom active region (not shown). In the FIG. 15 embodiment, there is an amount of index guiding and current confinement.

[0082] In the FIG. 15 embodiment, the layers are grown by standard methods, such as molecular beam epitaxy and the like. After this growth a photoresist mask is deposited above the parts where the implantation needs to be prevented. The structure is then exposed to a high energy ion beam. Ions are implanted to depths which are determined by the ion beam energy.
In another embodiment, illustrated in FIG. 16, VCSEL 10 includes first tunnel junction 20 and a first etched layer 60, each positioned between top and bottom mirrors 12 and 14. In the embodiment illustrated in FIG. 16, first etched layer 60 is substituted for the oxide layers of the FIGS. 1 through 13 embodiments. Additional etched layers can be included and be positioned between adjacent tunnel junctions and active regions as shown in FIG. 17. Etching provides formation of current localization because etched portions are electrical insulators.

Each etched layer 60 can have a variety of different profiles. As illustrated in FIGS. 18(a), 18(b), 18(c) through 18(e), etched layer 60 can have with respect to a longitudinal axis of substrate 24, a vertical profile, a slopped profile, a variable geometric profile and an undercut profile.

One or both of top mirror 12 and bottom mirror 14 can be a lattice relaxed mirror. First tunnel junction 20 is positioned between top and bottom mirrors 12 and 14. Additionally, first oxide layer 22 can be positioned adjacent to top mirror 12 or bottom mirror 14. With any of the embodiments illustrated in FIGS. 1 through 17 top and bottom mirrors 12 and 14 can be lattice relaxed mirrors. Lattice relaxed mirrors permit the use of materials with high index contrast, high reflectivities, and low thermal resistivity without the constraint of lattice matching.

In this embodiment, substrate 24 can be made of a lattice defining material such as InP, GaAs and the like. A stack of layers on top of substrate 24 forms bottom mirror 14 and can consist of a combination of material such as InAlGaAs/InAlAs, InGaAsP/InP, AlGaAsSb/AlAsSb, InGaAsP, GaAs, AlGaAsN/GaAs and the like. Bottom mirror 14 can be formed of alternating layers of InAlGaAs and InAlAs. The refractive index is different between the layers. The number of the alternating layers can be, for example, from 2-2000 in order to achieve the desired reflectivity.

Bottom mirror 14 can be lattice matched to the lattice defining material of substrate 24. Bottom mirror 14 can be grown using any epitaxial growth method, such as metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) e-beam, chemical beam epitaxy, and the like.

A spacer layer, not shown, can be deposited on top of bottom mirror 14. The material of the spacer layer can be made of InAlGaAs/InAlAs, InGaAsP/InP, AlGaAsSb/AlAsSb, InGaAs, GaAs, AlGaAsN/GaAs and the like. The spacer layer can be lattice matched to the lattice defining material of substrate 24.

Top mirror 12 can also be a DBR that is grown on top of a confinement layer that can also be considered as part of top mirror 12. The confinement layer and top mirror 12 can be the lattice relaxed portion of VCSEL 10. The lattice mismatch factor may be 0-500%, from the lattice defining material.

Top mirror 12 is made of a material such as AlGaAs, InGaP, InGaAsP and the like. In one embodiment, top mirror 12 is made of a set of alternating layers of AlGaAs and GaAs. The high Al-content AlGaAs layers are the low refractive index layers.

In another embodiment, one or both of top mirror 12 and bottom mirror 14 can be a dielectric mirror. First tunnel junction 20 is positioned between top and bottom mirrors 12 and 14. First oxide layer 22 can be positioned adjacent to top mirror 12 or bottom mirror 14. With any of the embodiments illustrated in FIGS. 1 through 17 top and bottom mirrors 12 and 14 can be dielectric mirrors. Dielectric materials exhibit large index contrast. Therefore a fewer number of pairs is necessary to obtain high reflectivities.

Referring now to FIG. 19, one or both of mirrors 12 and 14 can be a fiber 62 with a grating 64. Suitable fibers 62 include but are not limited to single or multi-mode filters, silicon, plastic and the like. First tunnel junction 20 is positioned between top and bottom mirrors 12 and 14. First oxide layer 22 can be positioned adjacent to mirror 12 or bottom mirror 14. With any of the embodiments illustrated in FIGS. 1 through 17 top and bottom mirrors 12 and 14 can be a fiber 62 with grating 64. Grating 64 can be used to form an external cavity which allows for wavelength tuning by moving fiber 62. Grating 64 also eliminates the need for DBR’s and therefore reduces manufacturing time and costs.

In another embodiment, illustrated in FIG. 20, one or both of top and bottom mirrors 12 and 14 is a fused mirror. Wafer fusion has the same advantages as growth of lattice relaxed mirror except that in the wafer fusion case no threading dislocations are present in the mirror. The use of wafer fusion permits the use of a material system for the DBR that is mismatched from the substrate.

First tunnel junction 20 is positioned between top and bottom mirrors 12 and 14. First oxide layer 22 can be positioned adjacent to top mirror 12 or bottom mirror 14. With any of the embodiments illustrated in FIGS. 1 through 17 top and bottom mirrors 12 and 14 can be fused mirrors.

As illustrated in FIG. 21, top mirror 12 of any of the FIGS. 1 through 20 can be a cantilever apparatus that uses an electrostatic force that pulls on a cantilever arm. The mechanical deflection resulting from this electrostatic force is used to change the length of a Fabry-Perot microcavity and consequently to the resonance wavelength.

In this embodiment, top mirror 12 has a cantilever structure consisting of a base 66, an arm 68 and an active head 70. The bulk of cantilever structure may consist of a plurality of reflective layers 72 which form a distributed Bragg reflector (DBR). Layers 72 can be formed of different materials including but not limited to AlGaAs. Different compositional ratios are used for individual layers 72, e.g., Al0.3Ga0.7As/Al0.5Ga0.5As. The topmost layer of layers 72 is heavily doped to ensure good contact with an electrical tuning contact 74 deposited on top of the cantilever structure.

The actual number of layers 72 may vary from 1 to 20 and more, depending on the desired reflectivity of the DBR. Furthermore, any suitable reflecting material other than AlGaAs may be used to produce layers 72. Active head 70 is made of layers. However, arm 68 and base 66 do not need to be made of layers.

Base 66 can have a variety of different geometric configurations and large enough to maintain dimensional stability of the cantilever structure. The width of arm 68 ranges typically from 2 to 8 microns while its length is 25 to 100 microns or more. The stiffness of arm 68 increases as its length decreases. Consequently, shorter cantilevers require greater forces to achieve bending but shorter canti-
levers also resonate at a higher frequency. The preferred diameter of active head 70 falls between 5 and 40 microns. Other dimensions are suitable.

[0099] Electrical tuning contact 74 resides on all or only a portion of a top of the cantilever structure. Electrical tuning contact 74 be sufficiently large to allow application of a first tuning voltage $V_{t1}$. A support 76 rests on a substrate 78 across which a voltage can be sustained. Substrate 78 can include a second DDB 68. Support 76 can be made of the same material as layers 72. A voltage difference between layers 72 and substrate 78 causes a deflection of arm 68 towards substrate 78. If layers 72 and substrate 78 are oppositely doped, then a reverse bias voltage can be established between them. Substrate 78 is sufficiently thick to provide mechanical stability to the entire cantilever apparatus. Inside substrate 78 and directly under active head 70 are one or more sets of reflective layers with each set forming a second DDB. A more complete description of the cantilever apparatus is disclosed in U.S. Pat. No. 5,629,951, incorporated herein by reference.

[0100] Referring now to FIGS. 22(a) and 22(b), one embodiment of the present invention is a vertical cavity or non-vertical cavity structure 10, with an oxide layer, that includes a die 80 with a top surface 82 and a plurality of planar electrically conducting layers, generally denoted as 84. At least one of the layers 84 is an oxide layer 22. Oxide layer 22 is formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator. A plurality of oxide apertures 86 are formed by via holes, trench structures and mesas FIG. 23. In FIG. 23, the mesas have sizes of 40 $\mu$m, 39 $\mu$m, 37 $\mu$m, and 38 $\mu$m respectively. Oxide apertures 86 connect top surface 82 to oxide layer 22. In one embodiment, a majority of individual via holes 22 have different pitches. For purposes of this specification, pitch is the distance between any two cross via holes, as illustrated in FIG. 23. In another embodiment, all of oxide apertures 22 have different pitches.

[0101] An optoelectronic device 10 is coupled to only one of the oxide apertures 86. An optoelectronic device is coupled to a single oxide aperture in the die. Suitable optoelectronic devices include but are not limited to a vertical cavity or non-vertical cavity, surface emitting laser, detector, filter, pin detector, avalanche photodiode, LED, Resonant cavity LED, modulator, attenuator, amplifier, SOA, ring waveguide, ring waveguide oscillator micromechanical structure, micromechanical structure with a single support member, micromechanical structure with at least two support members and tunable micromechanical structure.

[0102] Oxide apertures 86 are etched into top surface 82 of die 80 to provide access to oxide layer 22. Any number of oxide apertures 86 are formed, preferably the number is 3 to 4. Oxide apertures 86 extend from top surface 82 to at least oxide layer 22. When die 80 is exposed to steam, the steam enters from previously formed via holes, trench structures and mesas and a moving oxidation front is set up. The via holes, trench structures and mesas can be formed by photolithography to define an etch mask, followed by dry or wet etching. The front proceeds radially from the via holes, trench structures and mesas. The process is allowed to continue until the fronts merge leaving oxidized apertures 86.

The shape of the via holes, trench structures and mesas, and hence oxide apertures 86 can be set by conventional photolithographic techniques. The etching of the via holes, trench structures and mesas can be performed with a 1:5:15 mixture of phosphoric acid (H$_3$PO$_4$), hydrogen peroxide (H$_2$O$_2$) and water (H$_2$O). Alternatively, dry etching by reactive ion etching may be used to provide better accuracy and more vertical sidewalls.

[0103] An example of one embodiment of the present invention as follows. At 400 degrees, the oxidation rate of an AlAs VCSEL is about 2.65 micrometers/min average, but varies from 2.52 to 2.74 um/min from run to run. On a 1 cm by 1 cm section size of wafer, the oxidation rate can vary by 5% due to defects and processing caused contaminations. The oxidation rate variation translates into final oxide aperture size difference in the order of micrometers. For example, if the oxidation time is constant for 22 minutes, the size of oxide aperture 86 can vary from 5 um to 15 um for a 125 um square mesa from run to run. If the oxidation time is kept at 11 minutes, oxide aperture 86 can extend from 5 to 10 um for a 65 um square mesa. From these oxidation rate variations, the yield for achieving single mode yield in oxide confined VCSEL devices is very low in manufacturing, by using a fixed size mesa or a via hole array of single pitch, since the optimum oxide aperture size for single mode operation should be less than 6 um. If oxide aperture 86 is larger than that, the VCSEL starts to operate in multi-mode. By using the multi via hole pattern method of the present invention, the yield for single mode devices is increased significantly by a factor of n, where n is the number of arrays in the via pattern. The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. It is intended that the scope of the invention be defined by the following claims and their equivalents.

What is claimed is:

1. A vertical cavity apparatus, comprising:
   a die including a top surface and a plurality of planar electrically conducting layers, at least one of the layers being an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator;
   a plurality of oxide apertures formed by via holes connecting the top surface to the oxide layer, a majority of individual oxide apertures having different sizes; and
   an optoelectronic device coupled to a single oxide aperture in the die.
2. The apparatus of claim 1, wherein the plurality includes at least two oxide apertures.
3. The apparatus of claim 1, wherein the plurality includes at least three oxide apertures.
4. The apparatus of claim 1, wherein the plurality of oxide apertures are formed from a plurality of via holes that create individual oxide apertures, wherein a distance between any pair of via holes in one group is different from a distance between another pair of via holes in another group.
5. The apparatus of claim 1, wherein the device is a VCSEL.
6. The apparatus of claim 1, wherein the device is a detector.
7. The apparatus of claim 1, wherein the device is a filter.
8. The apparatus of claim 1, wherein the device is a pin detector.
9. The apparatus of claim 1, wherein the device is an avalanche photodiode.
10. The apparatus of claim 1, wherein the device is a LED.
11. The apparatus of claim 1, wherein the device is a Resonant cavity LED.
12. The apparatus of claim 1, wherein the device is an amplifier.
13. The apparatus of claim 1, wherein the device is an SOA.
14. The apparatus of claim 1, wherein the device is a tunable vertical cavity laser.
15. The apparatus of claim 1, wherein the device is a ring waveguide.
16. The apparatus of claim 1, wherein the device is a ridge waveguide.
17. The apparatus of claim 1, wherein the device is a ring waveguide resonator.
18. The apparatus of claim 1, wherein the device is an SOA.
19. The apparatus of claim 1, wherein the device is a Resonant cavity LED.
20. The apparatus of claim 1, wherein the device is a Resonant cavity SOA.
21. The apparatus of claim 1, wherein the device is an avalanche photodiode.
22. The apparatus of claim 1, wherein the device is a LED.
23. The apparatus of claim 1, wherein the device is a Resonant cavity LED.
24. The apparatus of claim 23, wherein the device is a LED.
25. The apparatus of claim 23, wherein the device is a Resonant cavity LED.
26. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
27. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
28. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
29. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
30. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
31. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
32. The apparatus of claim 23, wherein the device is a SOA.
33. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
34. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
35. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
36. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
37. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
38. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
39. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
40. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
41. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
42. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
43. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
44. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
45. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
46. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
47. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
48. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
49. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
50. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
51. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
52. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
53. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
54. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
55. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.
56. The apparatus of claim 23, wherein the device is a Resonant cavity SOA.

32. The apparatus of claim 23, wherein the device is a LED.
33. The apparatus of claim 23, wherein the device is a Resonant cavity LED.
34. The apparatus of claim 23, wherein the device is an amplifier.
35. The apparatus of claim 23, wherein the device is an SOA.
36. The apparatus of claim 23, wherein the device is a tunable vertical cavity laser.
37. The apparatus of claim 23, wherein the device is a ring waveguide.
38. The apparatus of claim 23, wherein the device is a ridge waveguide.
39. The apparatus of claim 23, wherein the device is a ring waveguide resonator.
40. The apparatus of claim 23, wherein the oxidizable material includes an Al containing III-V compound.
41. The apparatus of claim 23, wherein the oxidizable material includes Al Ga As.
42. The apparatus of claim 23, wherein the oxidizable material includes In Ga As.
43. The apparatus of claim 23, wherein the oxidizing agent includes water.
44. The apparatus of claim 23, wherein the optoelectronic device is a single mode device.
45. A vertical cavity apparatus, comprising:
   a die including a top surface and a plurality of planar electrically conducting layers, at least one of the layers being an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator;
   a plurality of oxide apertures formed by trench structures connecting the top surface to the oxide layer, a majority of individual oxide apertures having different sizes; and
   an optoelectronic device coupled to a single oxide aperture in the die.
46. The apparatus of claim 23, wherein the plurality includes at least two oxide apertures.
47. The apparatus of claim 23, wherein the plurality includes at least three oxide apertures.
48. The apparatus of claim 23, wherein the plurality of oxide apertures are formed from a plurality of trench structures that create individual oxide apertures, wherein the size of one oxide aperture is different from that of another oxide aperture.
49. The apparatus of claim 23, wherein the device is a VCSEL.
50. The apparatus of claim 45, wherein the device is a detector.
51. The apparatus of claim 45, wherein the device is a filter.
52. The apparatus of claim 45, wherein the device is a pin detector.
53. The apparatus of claim 45, wherein the device is an avalanche photodiode.
54. The apparatus of claim 45, wherein the device is a LED.
55. The apparatus of claim 45, wherein the device is a Resonant cavity LED.
56. The apparatus of claim 45, wherein the device is an amplifier.
57. The apparatus of claim 45, wherein the device is an SOA.
58. The apparatus of claim 45, wherein the device is a tunable vertical cavity laser.
59. The apparatus of claim 45, wherein the device is a ridge waveguide.
60. The apparatus of claim 45, wherein the device is a ridge waveguide resonator.
61. The apparatus of claim 45, wherein the device is a ridge waveguide resonator.
62. The apparatus of claim 45, wherein the oxidizable material includes an Al containing II-V compound.
63. The apparatus of claim 45, wherein the oxidizable material includes AlGaAs.
64. The apparatus of claim 45, wherein the oxidizable material includes InGaAs.
65. The apparatus of claim 45, wherein the oxidizing agent includes water.
66. The apparatus of claim 45, wherein the optoelectronic device is a single mode device.
67. A multi-mode device, comprising:
   a die including a top surface and a plurality of layers, at least one of the layers being an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator, the die including a plurality of oxide apertures connecting the top surface to the oxide layer, a majority of individual oxide apertures having different sizes;
   a tunable laser coupled to a single oxide aperture in the die, the tunable laser including, a semiconductor active region positioned between upper and lower confining regions of opposite type semiconductor material, and first and second reflective members positioned at opposing edges of the active and confining regions, the laser producing an output beam.
68. The device of claim 67, wherein the plurality includes at least two oxide apertures.
69. The device of claim 67, wherein the plurality includes at least three oxide apertures.
70. The device of claim 67, the plurality of oxide apertures are formed from a plurality of via holes that create individual oxide apertures, wherein a distance between any pair via holes in one group is different from a distance between another pair via holes in another group.
71. The device of claim 67, wherein the plurality of oxide apertures are formed from a first plurality of trench structures that create individual oxide apertures, wherein the size of one oxide aperture is different from the sizes of any other oxide apertures.
72. The device of claim 67, wherein the plurality of oxide apertures are formed from a first plurality of mesa structures that create individual oxide apertures, wherein a distance between any pair of oxide apertures is different from a distance between another pair of oxide apertures.
73. The device of claim 67, wherein the plurality of oxide apertures are formed by via holes connecting the top surface to the oxide layer.
74. The device of claim 67, wherein the plurality of oxide apertures are formed by trench structures connecting the top surface to the oxide layer.
75. The device of claim 67, wherein the plurality of oxide apertures are formed by mesas connecting the top surface to the oxide layer.
76. The device of claim 67, wherein the tunable laser is a VCSEL laser.
77. The device of claim 67, further comprising:
   a wavelength tuning member coupled to the laser;
   a wavelength measurement member positioned to receive at least a portion of the output beam of the laser, the wavelength measurement member being coupled to the control loop; and
   a control loop coupled to the wavelength measurement and the tuning member, wherein in response to a detected change in wavelength the control loop sends an adjustment signal to the tuning member and the tuning member adjusts a voltage or current supplied to the laser to provide a controlled frequency and power of an output beam.
78. The device of claim 67, wherein each of the top and bottom reflectors is a DBR.
79. The device of claim 67, further comprising:
   a first tunnel junction positioned between the top reflector and the active region.
80. The device of claim 67, wherein the active region includes at least a first quantum well.
81. The device of claim 67, wherein the active region includes a plurality of quantum wells.
82. The device of claim 81, wherein at least a portion of the plurality of first quantum wells have different maximum gain wavelength.
83. The device of claim 67, wherein the active region includes at least a first bulk region.
84. An optical system, comprising:
   a die including a top surface and a plurality of layers, at least one of the layers being an oxide layer formed of an oxidizable material that is oxidized upon exposure to an oxidizing agent to convert the oxidizable material to an electrical insulator, the die including a plurality of oxide apertures connecting the top surface to the oxide layer, a majority of individual oxide apertures having different sizes;
   a tunable laser formed in one of the oxide apertures, the laser including an active region with first and second opposing reflectors that define a laser gain cavity;
   an adjustable wavelength selective filter that splits the output beam into a transmitted portion and a reflected portion, the adjustable wavelength selective filter being positioned at an angle \( \theta \) relative to the optical axis to provide an angular dependence of a wavelength reflection of the wavelength selective filter and direct the reflected output beam towards the first photodector, wherein the wavelength selective filter provides wavelength selectivity by changing the angle \( \theta \) and a ratio of the transmitted and reflected portions is a function of wavelength of output beam and the angle \( \theta \).
85. The system of claim 84, wherein the plurality includes at least three oxide apertures.
86. The system of claim 84, wherein the plurality includes at least four oxide apertures.
87. The system of claim 84, wherein each of an individual oxide aperture in the plurality has a different pitch.
88. The device of claim 84, wherein the plurality of oxide apertures are formed by via holes connecting the top surface to the oxide layer.

89. The device of claim 84, wherein the plurality of oxide apertures are formed by trench structures connecting the top surface to the oxide layer.
90. The device of claim 84, wherein the plurality of oxide apertures are formed by mesas connecting the top surface to the oxide layer.
91. The system of claim 84, wherein the tunable laser is a VCSEL laser.