

[54] **INFORMATION DISPLAY SYSTEM**

[75] Inventors: **Robert W. Schumann**, Madison;
Arthur F. Smith, Verona, both of
Wis.

[73] Assignee: **Nicolet Instruments, Inc.**, Madison,
Wis.

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[58] Field of Search **235/151, 197, 198, 152;**
340/324 A, 347 DA; 315/18; 324/99 D

[56] **References Cited**

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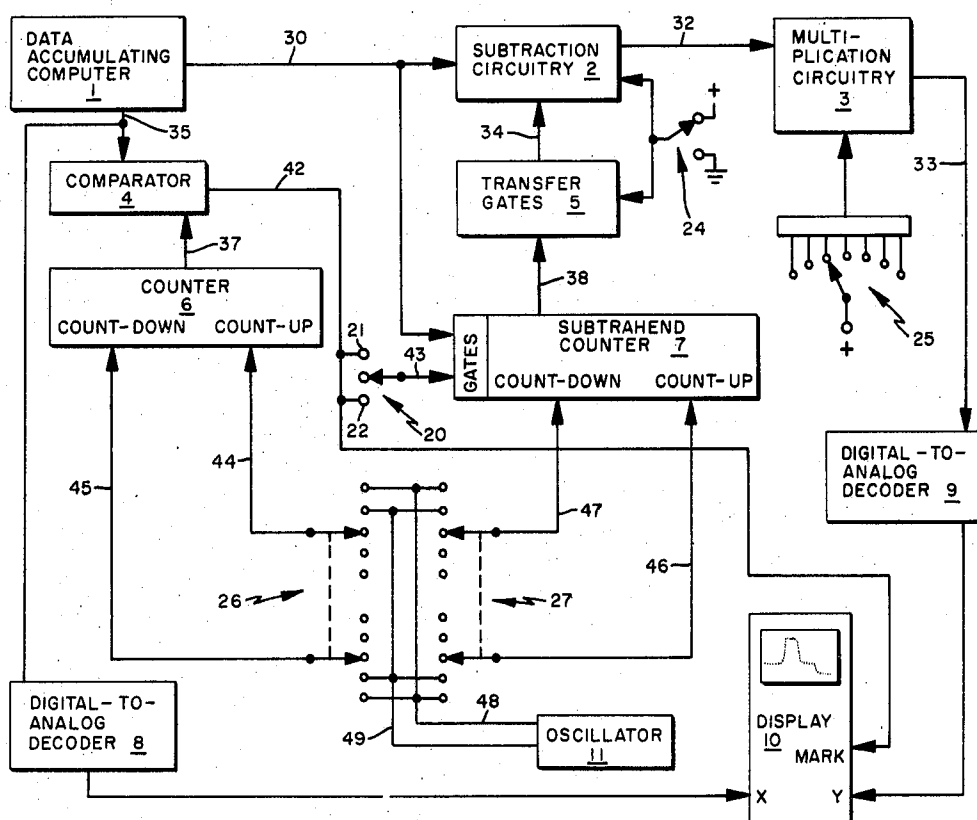
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Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Lew Schwartz

[57] **ABSTRACT**

An information display system including display means for displaying a sequence of coordinate points, each point having an ordinate and an abscissa value. The system having means for subtracting a selectable constant from each ordinate value prior to display, and means for multiplying the difference of the subtraction before display. Pulse means are provided for selectively varying the constant to be subtracted at a selectable rate. Means are also provided for varying the multiplication factor. Also, means are provided for marking a coordinate point on the display means and for selectively using the ordinate value of the selected coordinate as the constant to be subtracted, thus centering or zeroing the displayed figures around the marked point. Finally, limit means are provided at the output of both the subtraction means and the multiplier means for providing maximum and minimum output numbers from each.

31 Claims, 13 Drawing Figures



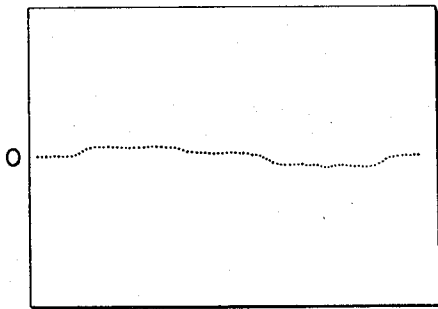


FIG 1A

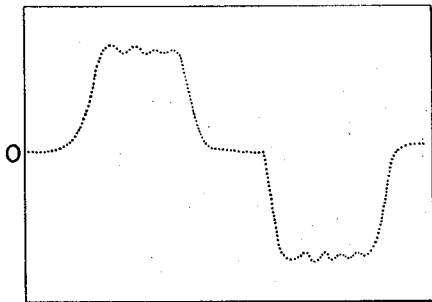


FIG 1B
PRIOR ART

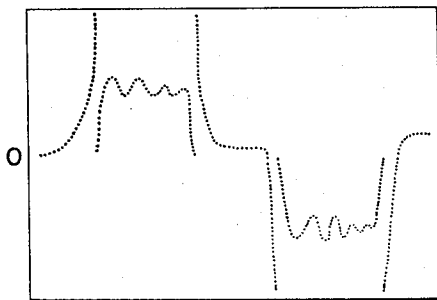


FIG 1C
PRIOR ART

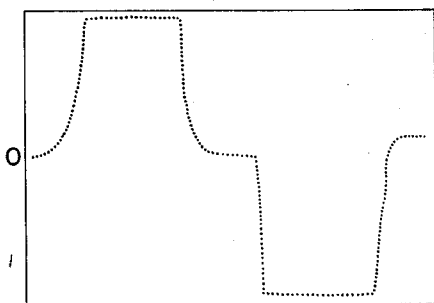


FIG 2
PRIOR ART

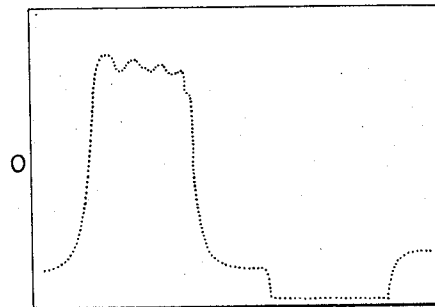


FIG 3

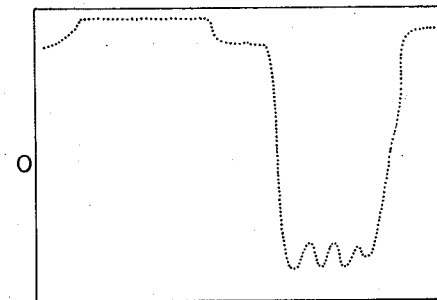


FIG 4

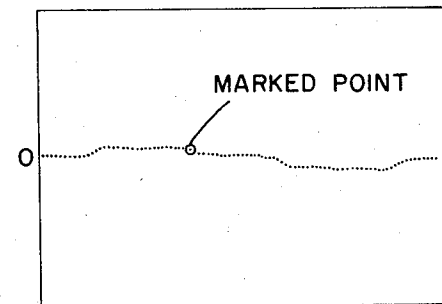


FIG 5

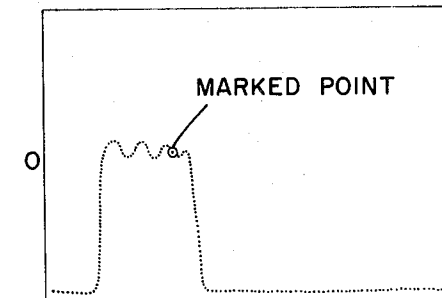


FIG 6

INVENTORS

Robert W. Schumann,
BY Arthur F. Smith

Sew Schwartz
ATTORNEY

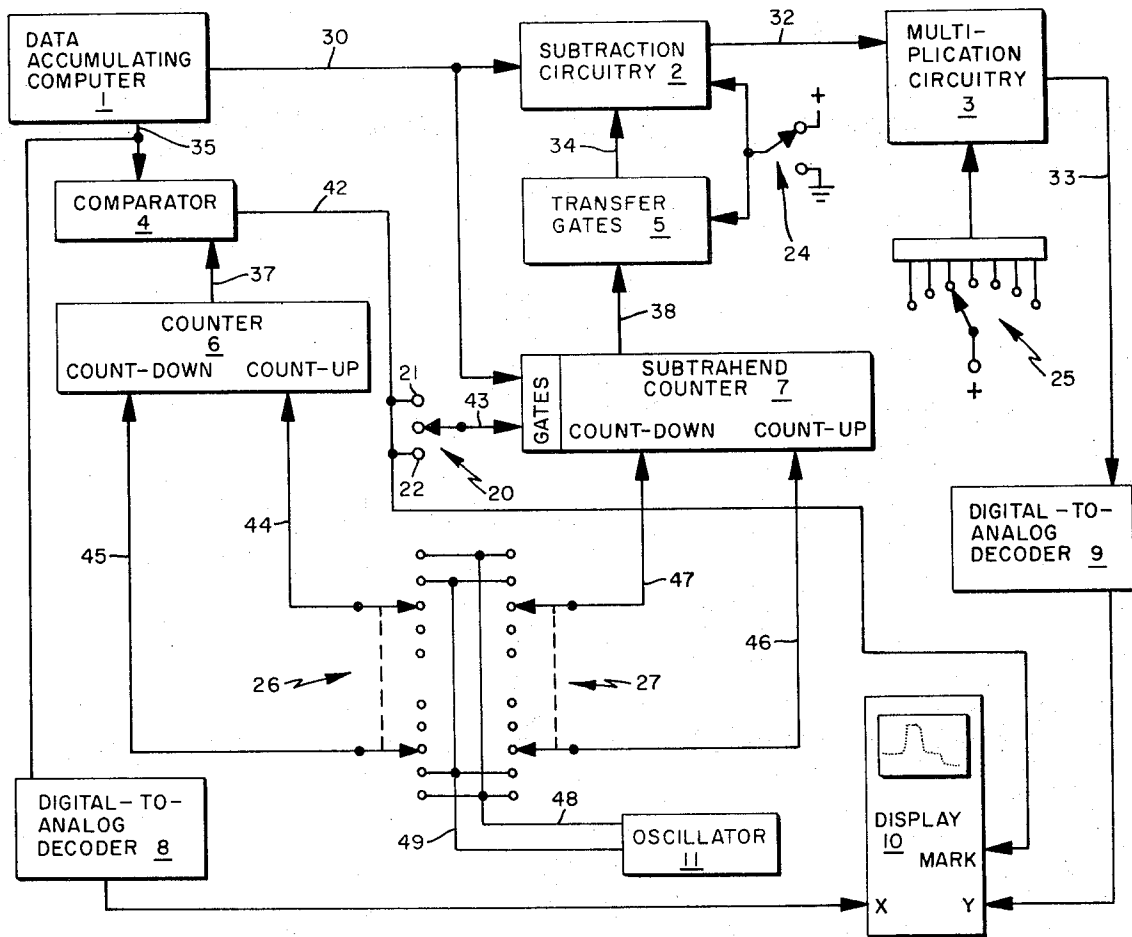


FIG 7

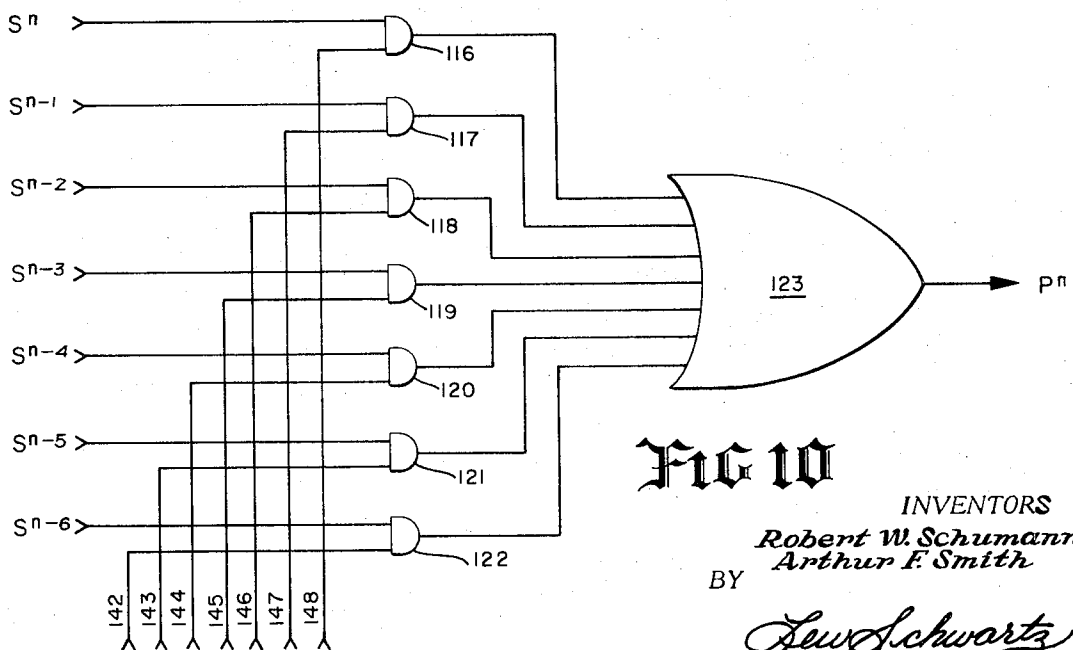


FIG 10

INVENTORS
 Robert W. Schumann,
 Arthur F. Smith
 BY
 Lew Schwartz
 ATTORNEY

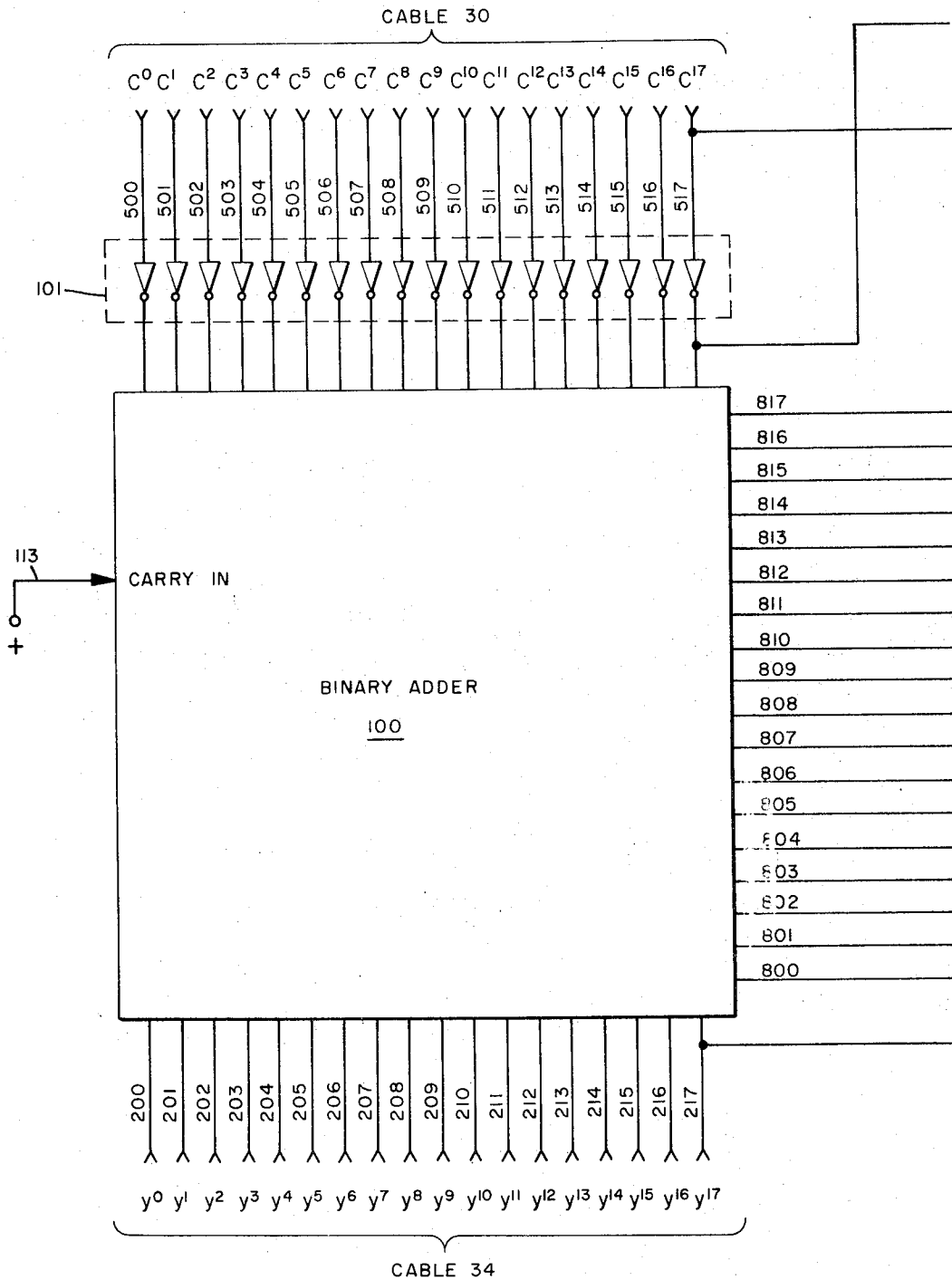


FIG 8

INVENTORS
 Robert W. Schumann,
 Arthur F. Smith
 BY

Levi Schwartz
 ATTORNEY

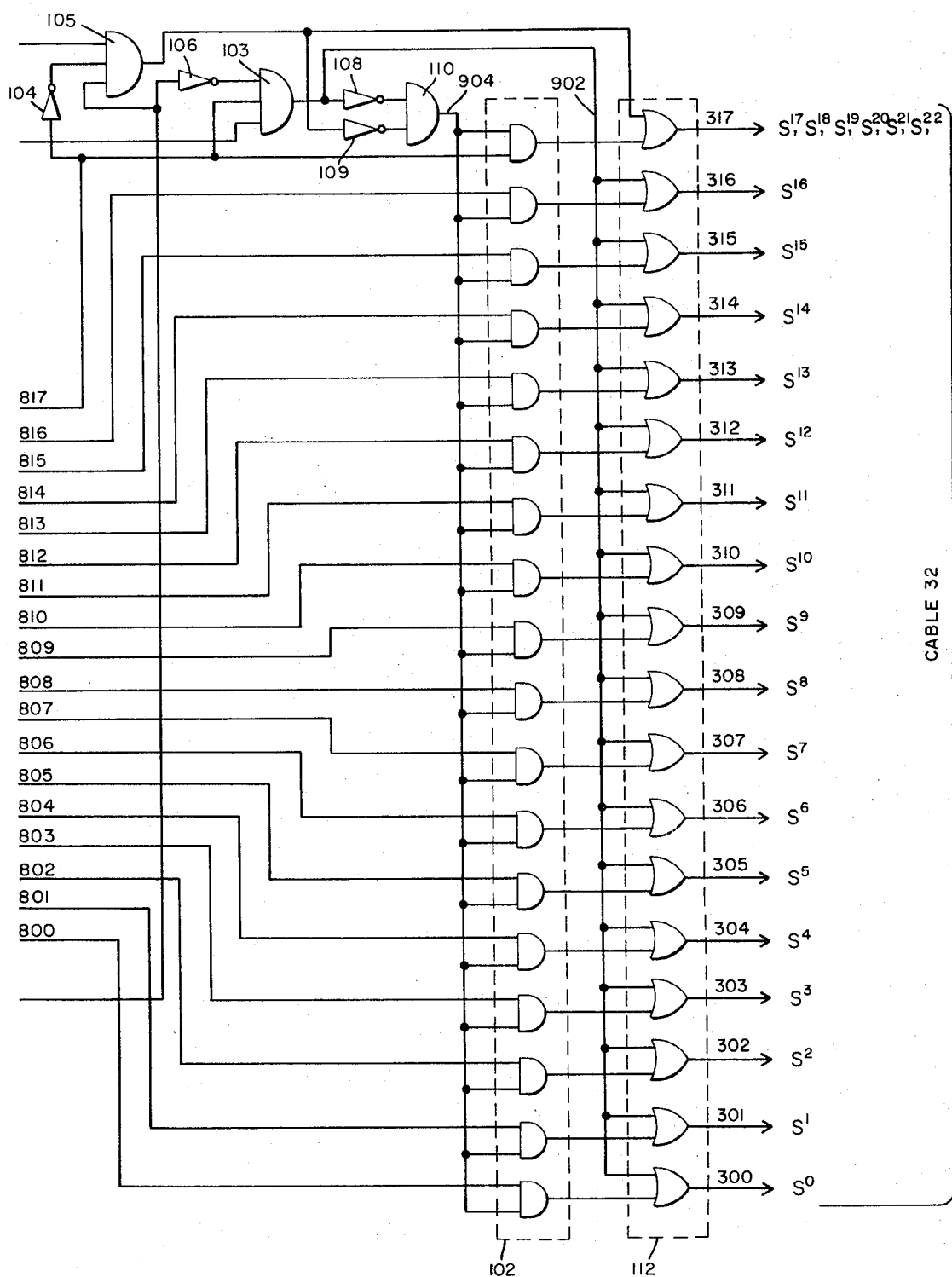


FIG 8A

INVENTORS
 Robert W. Schumann,
 Arthur F. Smith
 BY
Lew Schwartz
 ATTORNEY

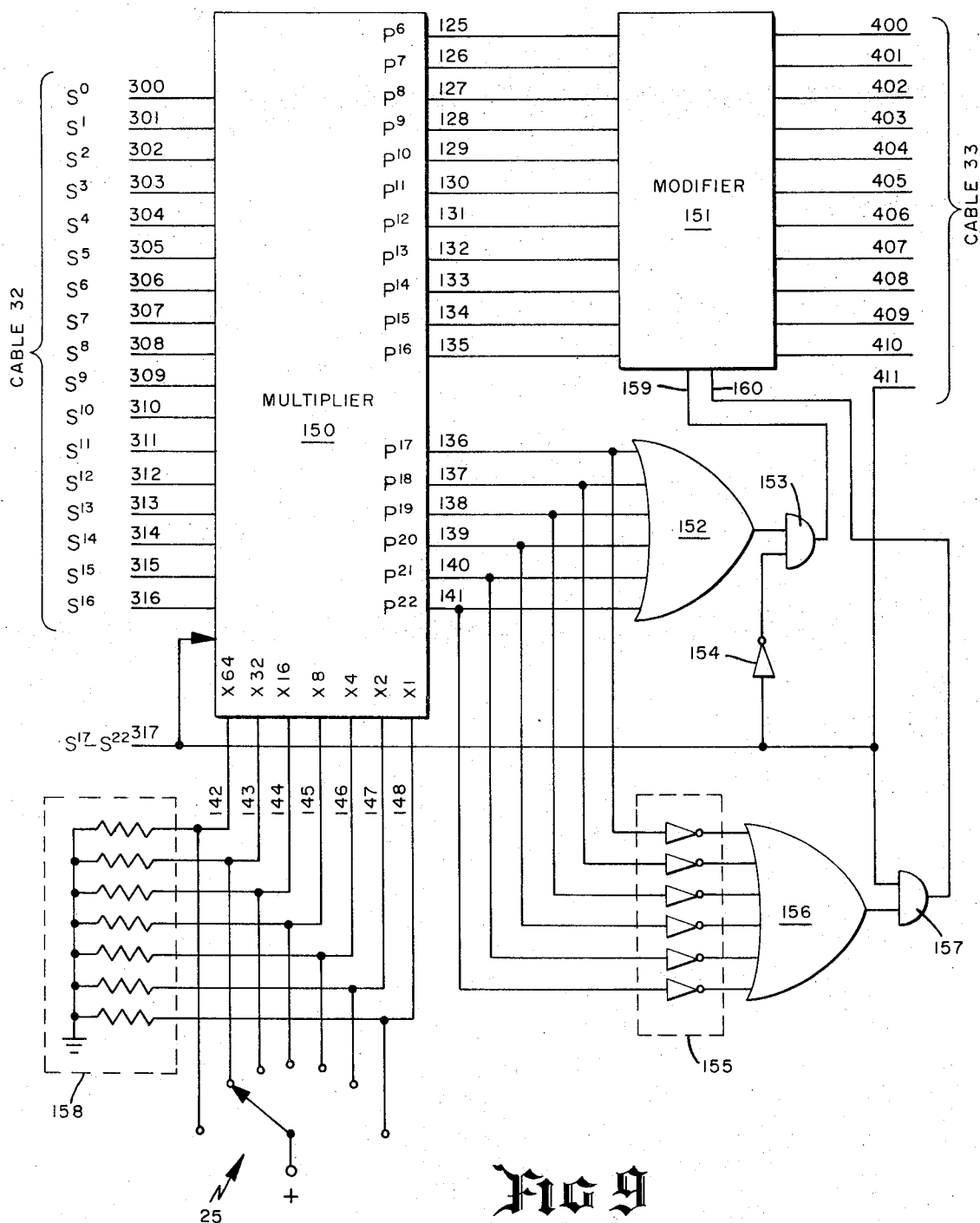


FIG 9

INVENTORS
Robert W. Schumann,
 BY **Arthur F. Smith**

Sew Schwartz
 ATTORNEY

INFORMATION DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

Information display systems are well-known in the art. Digital measuring instruments such as signal averagers, pulse height analyzers and other instruments of the general type include a digital memory in which measured information is stored. These instruments generally include a means for displaying the stored information on a device such as a cathode-ray-tube screen, and the circuitry within the instruments provide for a systematic presentation of ordinate and abscissa values from the memory storage for control of the cathode-ray-tube beam deflections. Thus the display comprises a plot of coordinate points, the plot representing the variable being measured. For example, in the case of a digital signal averager, the display may provide a coordinate plot of hundreds or thousands of coordinate points which represent the voltage-time relationship of the measured signal.

One of the problems involved with the type of display described above is that the vertical resolution of the data often exceeds that of the display means. For example, the range of data values may be from plus 131,071 units to minus 131,072 units for an 18 bit instrument. The decoder usually cannot decode more than 12 bits and higher resolution decoders are both expensive and slow. The resolution of a cathode-ray-tube screen is significantly less than that required in the above example.

A well-known method used in measuring instruments for avoiding the above problem is to connect a digital-to-analog decoder to the most significant 10 or 12 bits of the ordinate value register in the instrument, and to multiply the ordinate values by a constant, usually 2^n where n is an integer. The multiplication is in effect an arithmetic "left shift." It produces the same effect as re-connecting the decoder to less significant bits. Such known multipliers may be changed by the operator to select whatever magnification factor he wishes. However, such a solution to the problem raises ambiguities in the displayed materials when higher magnification is desired. These ambiguities cause the display to become unintelligible, as will be more fully described below with reference to the Figures of the drawings.

The apparatus of this invention overcomes the above-described problem by providing not only magnification through multiplication of the ordinate value, but by allowing the operator to select a constant to be subtracted from each ordinate value of the display, thus keeping that portion of the display in which he is interested on the screen of the display device

SUMMARY OF THE INVENTION

Briefly described, the apparatus of this invention includes a display device and means for providing abscissa and ordinate information for each of a plurality of coordinate points to be displayed as a plot on the display device. The abscissa information is connected by means to the display device. This means may be, for example, a digital-to-analog decoder connecting digital abscissa information to the X-input of a cathode-ray-tube beam deflection device. The ordinate information is first presented to a digital subtracter. A counter is connected to the subtracter to supply the subtrahend, the ordinate information being the minuend. The counter is preferably connected to a pulse generator

which is operated manually so that an observer can vary the subtrahend at a rate and in the direction he desires. Further switch means are provided for completely inhibiting the subtrahend from entering the subtracter. The difference following the subtraction process is presented to a multiplier for magnification purposes. The multiplier has a switch which enables selection by the operator of any one of a plurality of magnification or multiplication factors. The output of the multiplier is connected by means such as a digital-to-analog converter to the Y-input of a cathode-ray-tube beam deflection device. Preferably, both the difference value leaving the subtracter and the product leaving the multiplier are limited to a maximum and minimum number to avoid undesirable displays.

Also provided in the apparatus of this invention, are means for marking a particular coordinate point on the displayed plot of coordinate points, such as a beam intensifier on a cathode-ray-tube screen. The operator of the apparatus may select the particular coordinate point of interest prior to magnification by use of the selection apparatus provided. Then by operating a switch, either momentarily or permanently, he may enter the ordinate value for the selected coordinate point into the counter to become the subtrahend. This will cause a centering or zeroing of the selected coordinate point, as the amount subtracted at the selected abscissa point will be equal to the ordinate value as long as the switch is closed, or even when the switch is opened should the input information not change. Therefore, the operator can center the area of interest and it will stay centered despite change of the magnification factor.

The centering selection apparatus comprises a comparator and another counter adapted to receive signals from the pulse generator. The input abscissa information is provided to the comparator and the operator may vary the information in the counter, at a selected rate, to quickly find the abscissa value of the coordinate point he wishes to mark. When the value in the counter matches that of the abscissa information being presented, the comparator will recognize this and provide an output signal to the beam intensity device, or other marking device used on the display means. Having visually selected the coordinate point of interest, the operator may actuate a switch, either momentarily or permanently, whereby the output of the comparator will cause the ordinate information for the matched abscissa value to be entered into the subtrahend counter, to act as the subtrahend.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1A is a representation of a plot of a plurality of coordinate points, each having an ordinate and an abscissa value, of the type used with the apparatus of this invention;

FIG. 1B is a representation of a prior art magnification of the plot of FIG. 1A;

FIG. 1C is a representation of a further prior art magnification of the plot of FIG. 1B;

FIG. 2 is a representation of an off-scale prior art magnification of the plot of FIG. 1A;

FIG. 3 is a representation of an uncentered magnification of the plot of FIG. 1A, using the apparatus of this invention;

FIG. 4 is another uncentered magnification of plot of FIG. 1A, using the apparatus of this invention;

FIG. 5 is a representation of coordinate points, each having an abscissa and ordinate value, showing a marked coordinate point selectively marked with the apparatus of this invention;

FIG. 6 is a magnification of the plot of FIG. 5 indicating the centering or zeroing of the marked point, using the apparatus of this invention;

FIG. 7 is a block diagram of the information display system of the apparatus of this invention;

FIGS. 8 and 8A are logic diagrams of the subtracter apparatus of this invention;

FIG. 9 is a logic diagram of the multiplier or magnification apparatus of this invention; and

FIG. 10 is a logic diagram of a portion of the multiplier apparatus of this invention.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

As has been stated above, a prior art method of overcoming the problems of vertical resolution in information display devices has comprised use of apparatus for multiplying the vertical or ordinate value by a constant, usually 2^n where n is an integer. FIG. 1A shows a typical display for the case where n is 0 ($2^0=1$). Little detail is present. FIG. 1B shows the effect of shifting twice ($n=2$ and $2^2=4$). This results in a better showing of the details of the coordinate plot, however, there are instances where the operator will wish still greater detail. FIG. 1C shows the effect of such an attempt to achieve greater detail, for example, where m is equal to 3. Still better detail is shown but an ambiguity has been introduced because the shifting or multiplying operation has resulted in the loss of one significant bit for each ordinate in two regions. The left shift effect of the multiplication has resulted in the "shifting out" of a significant bit of information. It will be apparent that it is sometimes desirable or necessary to shift as many as ten times ($m=10$) to observe fine detail, and often in the prior art apparatus this high magnification produces so many ambiguities that the display is unintelligible to the operator.

This particular problem of ambiguities is overcome with one prior art modification with the result shown in FIG. 2. For any ordinate value which, after shifting, has become ambiguous, the value is changed to that corresponding to positive or negative full scale depending on whether the original number was positive or negative. The value change is applied only to the numbers presented to the information display system of this invention, and the original ordinate values are retained in the instrument measuring device memory.

Though the technique resulting in the display of FIG. 2 prevents severely confusing ambiguous displays, it is a method which has seen little use because the offscale values are completely obscured and it is often these values which contain the information the operator seeks to discover.

The apparatus of this invention enables the suppression of ambiguities, but in addition, allows data modification which enables the observer to inspect any region of the data. This modification is accomplished by the subtraction, prior to the magnification or multiplication step, of a selectable constant from each ordinate. The constant may have any value in the range of possible ordinate values, for example, in an 18 bit system, the constant values may be in the range of plus 131,071 to minus 131,072. For example, by subtracting a posi-

tive constant from every ordinate value of the plot of FIG. 2, the result will be the uncentered information shown in FIG. 3 enabling the operator to view the information at the positive peak of the plot. By use of a negative constant, applied to the plot of FIG. 2, the uncentered plot as shown in FIG. 4 will result, enabling the operator to view the information at the negative peak.

It is therefore apparent that utilizing the apparatus of this invention, despite the degree of magnification, it is possible to observe any desired data region on the plot without presenting the observer with confusing ambiguities.

The apparatus of this invention also includes apparatus for the automatic centering or zeroing of the displayed information. The apparatus allows the operator to select a desired coordinate point on the plot. The ordinate value of this point then becomes the subtraction constant and the subtraction results in the entire set of data being moved up or down an amount sufficient to cause the selective point to be at the center or zero level, because the amount subtracted is exactly equal to the ordinate of the selected coordinate. Referring, for example, to the display of FIG. 3, one can see that this plot would have to be manually centered by the operator if a higher magnification than that shown were used. This manual operation can be eliminated by the apparatus of this invention. In FIG. 5, a brightened point is shown on the plot which indicates to the operator what coordinate point he has selected. Apparatus is provided in this invention enabling the operator to move the brightened point along the plot until he reaches a coordinate point in a region of interest. Thereafter, the effect of the automatic centering or zeroing feature is to keep the selected point on the center or zero line, as shown in FIG. 6 which is a magnified representation of the plot of FIG. 5. As will be more fully described below, the automatic centering apparatus is extremely useful if the data are changing, as is the case in many digital measuring instruments, where despite data changes the region of interest remains centered. This feature is also useful for keeping a region of interest centered regardless of what magnification is used.

Referring now to FIG. 7, there is shown a block diagram including the information display system of this invention. The system includes a data accumulating computer 1, subtraction circuitry 2, multiplication circuitry 3, comparator 4, transfer gates 5, counter 6, subtrahend counter 7, digital-to-analog decoders 8 and 9, display means 10 and oscillator 11 all shown in block diagram 4. Computer 1 has an ordinate cable 30 connected to the input of subtraction circuitry 2 and to a set of input gates on subtrahend counter 7. Subtraction circuitry 2 has its output connected by a cable 32 to multiplication circuitry 3. The output of multiplication circuitry 3 is connected through cable 33 to decoder 9, and the output of decoder 9 is connected to a vertical deflection voltage input terminal on display 10, which in this preferred embodiment is an analog display means such as a cathode-ray-tube beam deflection apparatus. Data accumulating computer 1 has an abscissa output connected through a cable 35 to decoder 8 which has an output in turn connected to the horizontal deflection voltage on display means 10. Cable 35 is also connected to the input of comparator 4. Comparator 4 has another input connected to the output of counter 6 by a cable 37. The output of comparator 4 is con-

ected by a line 42 to a marking device on display means 10, such as a beam intensifier input. Line 42 is also connected to a pair of terminals 21 and 22 of a switch 20. The wiper arm of switch 20 is connected by a line 43 to the gates on subtrahend counter 7. The output of counter 7 is connected through cable 38 to the input of transfer gates 5. The output of transfer gates 5 is connected through a cable 34 to the input of subtraction circuitry 2. A switch 24 is connected between gates 5 and circuitry 2 for selective enabling of gates 5. The output of subtraction circuitry 2 is connected by a cable 32 to multiplication circuitry 3. A multiplication factor selection switch 25 has a plurality of terminals connected to multiplication circuitry 3. A multiplication factor selection switch 25 has a plurality of terminals connected to multiplication circuitry 3 for selection of a multiplication factor. Oscillator 11 has a pair of outputs 48 and 49 each carrying pulses at different frequencies. Lines 48 and 49 are connected to terminals on a switch 26 and a switch 27. Switch 26 has a first wiper arm connected through a line 44 to a count-up input terminal on counter 6 and a second wiper arm connected by line 45 to a countdown input terminal on counter 6. Switch 27 has a first wiper arm connected by line 46 to a count-up input terminal on counter 7 and a second wiper arm connected by a line 47 to a count-down input terminal on counter 7.

To best understand the operation of the apparatus shown in block diagram in FIG. 7, it will be of value to first discuss the operation in general terms. For the operation of this preferred embodiment, it is assumed that display means 10 is of the type having a cathode-ray-tube and that, therefore, the digital or binary form of information must be transferred to the form of analog voltages for beam deflection purposes. This necessitates digital-to-analog decoders 8 and 9, which would not be necessary in other embodiments of the invention which may use other display media such as a matrix array of light emitting elements which can operate directly from digital signals. However, the same problems in device or human eye resolution would exist for other types of display media as exist for the cathode-ray-tube, and the same kind of alterations on the number value presented to the device would apply as are needed for the numbers presented to the digital-to-analog converters in this preferred embodiment of the invention.

It is also assumed that the resolution of the digital-to-analog converters 8 and 9 is 12 bits. This choice is made for the preferred embodiment because this is a practical resolution limit for a low cost fast converter. It will be apparent that the same principles present in the preferred embodiment of the apparatus of this invention would apply if the converter had lower or higher resolution.

As more fully discussed above, because of the imperfect resolution of the digital-to-analog decoders and other display medium and the human eye, significant detail is not always visible on the screen, and the vertical scale of the display must at times be magnified. If there were sufficient resolution in the instruments, it would be sufficient to amplify the digital-to-analog converter output voltage and add a voltage bias to that amplified signal in such a manner that the region of interest is displayed on the screen in adequate detail. This solution is not normally acceptable because such amplification also magnifies instability in the digital-to-

analog converter, thereby causing the displayed information to jitter or wander on the screen. Further, there is a tendency for the displayed points to be fuzzy due to higher frequency noise and crosstalk. Also, it will be apparent that such a solution would not be applicable to display devices directly controlled by digital information which would not utilize digital-to-analog decoders.

For the purposes of this description a particular ordinate value of a coordinate point may be represented as a two's complement number:

$$Y_i = 17k_i 2^{17} + 16k_i 2^{16} + 15k_i 2^{15} + \dots + 0k_i 2^0$$

where the coefficient $17k_i$ may have the value 0 or -1, and the other coefficients k_i may have the values 0 or 1. In all digital circuits the coefficient for all bits will be 0 or 1, with the negative sign implied for the left bit. This is conventional two's complement representation. The digital-to-analog decoder treats a "1" in the 17th bit position as a negative coefficient.

A conventional notation for a two's complement binary number Y_i is a series of ones and zeros representing, in order the coefficients of the terms. An example is:

$Y = 111111000100000110$ which is a negative number equal to the decimal number -3834.

In the embodiment of the apparatus of this invention, an accurate conversion to analog voltage form cannot be made of an 18 bit number, for the digital-to-analog converter has only 12 bits of resolution. A good representation can be obtained by connecting the digital-to-analog converter to the most significant 12 bits, in effect thereby rounding off the numbers to 12 bits. The voltage output would, for the above number, then be proportional to -3840 rather than -3834, because the lower 6 bits would be ignored. Any number Y_i in the range 111111000100000000 to 111111000100111111 would produce the same voltage output from the digital-to-analog converter. No matter what amplification may be used to operate on the output of the digital-to-analog converter to increase the vertical magnification of the display, there would be no regaining of rounded off and therefore lost information as the least significant bits of all applied numbers are ignored.

Multiplication, by a left shift by a number in a register (except the sign bit) makes the digital-to-analog converter responsive to the lower order bits, but may result in the shifting-out of a significant bit, and ambiguities such as in FIG. 1C will result. By "shifting-out" is meant the appearance of a significant bit to the left of the 12 bits to which the converter is connected. In the case of negative numbers, the first "0" and all lower bits are significant. For positive numbers the first "1" and all lower bits are significant.

It is one function of the apparatus shown in FIG. 7 to modify the numbers prior to multiplication, to avoid ambiguities in the region of interest. This is achieved by subtracting a constant of sufficient magnitude and proper sign from the original ordinate values, such that the multiplication operation will not cause the number to exceed 17 significant bits plus the sign bit. This same constant is subtracted from all ordinates.

It will be understood that the ordinate values received from computer 1 are not necessarily of predictable values and that even if they should be, subtraction of a constant from some numbers may prevent ambigu-

ities due to overflows in multiplication but may well cause ambiguities with regard to other numbers. However, though initially the numbers are unpredictable, it is helpful that the appearance of the coordinate plot gives the observer an immediate indication of their general magnitudes. As will be seen, the human operator may use his judgment to decide what magnification may be needed to reveal fine detail of the plot, and will be aware that to avoid ambiguity in some region of immediate interest, he must add or subtract a small or large constant from all ordinates.

FIG. 2 shows a common situation where ambiguities have occurred near the top and bottom of the features of the coordinate plot. If the operator desires to observe the top, a positive constant should be subtracted from all ordinates prior to multiplication. The result of such an operation is shown in FIG. 3. The magnitude of the constant is not critical, as the operator may experimentally increase or decrease the constant value until the region he wishes to observe is unambiguous. In the case of FIG. 3, the operator has chosen a constant which has aggravated the overflow problem in some regions of the waveform, but as the operator wished to see that portion of the positive peak which is shown on scale in FIG. 3, he need not be concerned about the aggravated portion, further, he may later decrease the constant in value until the display of FIG. 4 is achieved, if he is interested in observing the more negative regions of the same plot.

Referring again to FIG. 7 in more particularity, data accumulating computer 1 may be any one of a wide variety of existing devices. To best understand the preferred embodiment it is assumed that computer 1 provides 18 bit two's complement ordinate values and 12 bit abscissa numbers in sequence, repeatedly, with the abscissa and ordinates of each coordinate provided simultaneously. The bit length of the ordinates, and the number of coordinates involved, may be different for different computers but the same principles will apply. It is assumed that the coordinate points are provided systematically, for example, one at a time in sequence of increasing abscissa values, and that cable 30 represents 18 wires and cable 35 represents 12 wires. A reasonable sequence of presentation involves periodic presentation of coordinates at intervals of nominally 10 microseconds, with the sequence repeated as often as the operator wishes to observe the information. It may be desirable to include buffer registers to hold the coordinate values during each 10 microsecond interval to free the computer for other tasks during those times. It will also be apparent that it is not mandatory that the coordinates be presented in order of increasing abscissa values but it is preferable that each coordinate be presented approximately as often and for as long as each other coordinate.

Subtraction circuitry 2 subtracts from the ordinate values presented through cable 30 a constant subtrahend contained in subtrahend counter 7. The constant is passed through gates 5 whenever switch 24 is in the enable position and then through cable 34 to circuitry 2. As will be more fully described below, subtraction circuitry 2 has the property of providing 18 bit two's complement output numbers on cable 32, which numbers or differences in general equal the difference between the ordinate value Y_i and the subtrahend, except that a provision is made in circuitry 2 so that if the difference exceeds plus $2^{17}-1$ or falls below -2^{17} , the out-

put S_i resulting is made to equal $2^{17}-1$ or 2^{17} , respectively.

Multiplier 3 receives the difference S_i through cable 32 and also receives a signal on one of the output wires of multiplication factor selector switch 25. The output product of multiplication circuitry 3 is limited to 12 bits in this preferred embodiment. The 12 bits do not exceed the least significant bits of the product, and include only the next eleven bits and the sign bit of the product. Any product which exceeds $2^{17}-1$ or falls below -2^{17} is replaced with one of those respective values, thereby producing 12 bit output numbers $2^{11}-1$ or -2^{11} .

It is preferred that subtraction circuitry 2 and multiplication circuit 3, be static devices for continually providing the difference and product values described above, except for momentary settling delays following changes in the ordinate or the subtrahend. Therefore, no synchronization is needed between the computer and other components.

The modified product from circuitry 3 passes through cable 33 to decoder 9. Decoder 9 operates in a manner well known to those skilled in the art to provide analog voltages which are proportional to the input digital information on cable 33. The output voltages of decoder 9 are of sufficient magnitude to produce a full scale vertical beam deflection on display means 10 if the modified product from circuitry 3 is $2^{11}-1$ or -2^{11} . The horizontal deflection of display apparatus 10 is controlled by the voltage from digital-to-analog decoder 8, which receives abscissa values from computer 1 through cable 36.

As stated above, the subtrahend is transmitted from counter 7 through gates 5 and cables 38 and 34. When switch 21 is in the enable position, the gates are enabled and the state of counter 7 is transmitted to circuitry 2. When switch 21 is in the downward position, gates 5 are blocked and a zero is presented through cables 34 to subtraction circuitry 2. The design of transfer gates 5 are well-known to those skilled in the arts.

Subtrahend counter 7 is preferably an up-down counter, also well-known to those skilled in the art, which has a count-up input terminal and a count-down input terminal. The state of counter 7 may be altered upwards one count for each pulse supplied on wire 46 to the count-up input terminal, and downwards one count for each pulse supplied on wire 47 to the count-down input terminal. Subtrahend counter 7 also has a gated parallel input such that a pulse on wire 43 enables input gates to insert into the counter the value Y_i representing the instantaneous ordinate value present on cable 30.

Oscillator or pulse generator 11 continually provides pulses on lines 48 and 49. The pulses on wire 48 are of a higher frequency, for example, about 400 Hertz and pulses on wire 49 are of a lower frequency, for example, about 10 Hertz. Switch 27 controls the application of pulses to the count-up input and count-down input of counter 7. When the switch 27 is in its center position, as shown in FIG. 7, no pulses are transmitted to counter 7. When switch 27 is moved one position up or one position down, pulses are transmitted respectively, through wire 47 to the count-down input of counter 7 and through wire 46 to the count-up input of counter 7. Note that an upward position of switch 27 causes the state of subtrahend counter 7 to decrease. This is a preferred condition as decreasing the counter state will

cause an increase in the remainder or difference output of subtraction circuitry 2, and thus cause the displayed data to move upwards, the same direction the switch is moved. Similarly, a downward movement of switch 27 causes the displayed data to move downward on the screen of display device 10. When switch 27 is operated to the second position either upwards or downwards, the state of the counter will change at a higher frequency. It is apparent that the choice of frequencies is completely arbitrary and it is as apparent that more than two frequencies can be provided from one or more oscillators such as 11, and that each of the pluralities of frequencies can be applied to counter 7.

In FIG. 7, the apparatus including comparator 4, counter 6, and switches 20 and 26 will act as a means for automatically centering or zeroing the data for the operator. Counter 6 is preferably an up-down counter having a count-up input terminal and a count-down input terminal. Switch 26 operates in the manner described above with regard to switch 27, but operates independently of switch 27. Thus, the operator may, by actuating switch 26 provide pulses from oscillator 11, of either of the selected frequencies, to either the count-up input terminal or the count-down input terminal of counter 6 through, respectively lines 44 and 45. Comparator 4 is a digital comparator of a type well-known in the art. It is continually comparing the abscissa value present on cable 35 with the counter state present on cable 37. When a comparison or agreement exists, a signal in the form of a selected voltage will appear on wire 42. Wire 42 is connected to the marker input of display device 10, in this preferred embodiment a beam intensifier circuit, which causes a brightening of a displayed coordinate point having the abscissa value stored in counter 6. Thus, the operator may move the intensified beam along the coordinate plot, at various speeds, and in two directions, simply by moving switch 26 upward or downward as desired. Switch 26 is preferably a spring-loaded return-to-center switch, as is switch 27. Therefore, when the operator has moved the marker or intensified beam to a coordinate point in a region of interest, he may simply release switch 26 and the intensified beam or marker will stay at the selected point.

Switch 20 is also a spring-loaded return-to-center switch in one position and is a permanent connection switch in the other position. That is, when the wiper arm of switch 20 is moved to terminal 21, a momentary contact will be made which will be broken when the operator releases the wiper arm. When the wiper arm of switch 20 is moved into contact with lower terminal 22, it will remain in that position even when the operator releases the switch. When the wiper arm of switch 20 is in contact with either of terminals 21 or 22, a signal on line 42 will be transmitted through line 43 to enable the gates at the input of subtrahend counter 7. The ordinate value y_i , then present on cable 30 will then pass through the gates of counter 7 to change the state of counter 7. Therefore, that ordinate value, y_i , will be subtracted from all further ordinate values. The ordinate value thus entered into subtrahend counter 7 is that which corresponds to the coordinate whose abscissa value equals the state of counter 6. Therefore, the data displayed on display device 10 will be vertically centered, that is zeroed, as long as line 43 is connected through switch 20 to terminal 21 or 22. The display will remain centered thereafter even if switch 20

is open, unless the ordinate values provided by computer 1 are changing for some reason, or unless up-down counter 7 is changed by adding pulses with switch 27, or unless gates 5 are disabled through the use of switch 24.

It is apparent that up-down counter 6, as up-down counter 7, could be some other storage means as long as it is variable to enable the operator to select a coordinate point of interest for automatic centering.

Reference is now made to FIGS. 8 and 8A which are logic schematics of subtraction circuitry 2. There is shown a binary adder 100 of a type and design well known to those skilled in the art. Cable 30 carrying ordinate values Y_i is shown as having 18 lines, 200-217 connected to adder 100. Lines 200-217 each carry the indicated bit value of Y_k , Y^0 - Y^{17} ranging from the least significant bit of the ordinate value to the most significant bit. Cable 34 is shown as comprising seventeen lines, 500-517 carrying, respectively, the subtrahend bit values C^0 - C^{17} . Each of lines 500-517 is connected to one of a plurality of inverters 101. The output of inverters 101 are connected to binary adder 100. A carry pulse is presented to binary adder 100 through line 113. The output of binary adder 100 is presented on a plurality of lines 800-817. Each of lines 800-817 is connected to one input of a plurality of two-input AND gates 102. Each output of AND gates 102 is connected to one input of a plurality of two-input OR gates 112.

Also in FIGS. 8 and 8A are shown a pair of three-input AND gates 103 and 105, and another two-input AND gate 100. Line 217, representing the most significant bit y^{17} of the ordinate value presented on cable 30, is connected to a first input of gate 105 and through an inverter 106 to a first input of gate 103. Line 517, representing the most significant bit C^{17} of the subtrahend value presented on cable 34, is connected to a second input on gate 103 and is connected through its inverter 101 to a second input on gate 105. Output line 817 of binary adder 100, representing the most significant of the difference value is connected to the third input on gate 103 and is connected through an inverter 104 to the third input on gate 105. The output of gate 103 is connected through a line 902 to all of the second inputs of OR gates 112 except that OR gate representing the most significant bit of the resulting output from the subtraction circuitry. The output of gate 103 is also connected through an inverter 108 to a first input on gate 110. The output of gate 105 is connected to the second input of the OR gate 112 representing the most significant bit of the result from subtractor circuitry 2, and is also connected through an inverter 109 to the second input of gate 110. The output of gate 110 is connected through a line 904 to the second input on each of AND gates 102. The outputs of OR gates 112 are connected to a plurality of lines 300-317 representing the value of the final difference from subtraction circuitry 2, S^0 - S^{17} .

The subtraction operation of circuitry 2 is accomplished by inverting each bit of the subtrahend C by means of inverters 101, applying a carry into adder 100 through wire 113, and applying to adder 100 the ordinate value on cable 30 through wires 200-217. The subtraction method of inverting the bits of the subtrahend C and including a carry input is well-known to those skilled in the art and will produce the difference value, in this case $y_i - C$.

In this preferred embodiment of the invention ambiguities in the display on device 10 are avoided by preventing or limiting the difference value of circuitry 2 and the product value from multiplication circuitry 3 from exceeding maximum and minimum limits, in this preferred embodiment $2^{17}-1$ or -2^{17} . Gates 102, 103, 105, 110, and 112 serve the purpose of modifying the output numbers on wires 300-317 whenever either limit has been exceeded. It will be apparent that whenever the ordinate value and the subtrahend are of unlike sign, it is possible that there will be a difference in excess of the chosen limits. If y_k is positive and C negative, a positive overflow may occur, which will be indicated by a negative sign on wire 817, the most significant bit of adder 100. Obviously, the difference value should be positive in this case, so that a negative result will indicate a positive overflow. And gate 103 will provide a positive output if C^{17} is a "1" (negative sign), y^{17} is a "0" (positive sign) and the most significant adder output bit on line 817 is a "1" (negative sign). Inverter 106 inverts the signal on line 217, which was bit y^{17} so that all three inputs of gates 103 will be positive if y^{17} is a "0" (positive sign). Whenever the output of gate 103 on wire 102 is positive, all but one of OR gates 112 are enabled to provide "1" outputs on lines 300-316 representing difference values S^0-S^{16} . Also, inverter 108 will then produce a "0" at gate 110, which therefore causes a "0" on wire 904 to AND gates 102 insuring that there is a 0 input to OR gate 112 representing the most significant bit of the output of subtraction circuitry 2. Thus, the sign bit of the modified difference on line 317 is forced to be a "0" (positive sign) as OR gate 112 cannot be receiving a "1" from the output AND gate 105. Therefore, the modified number, S_i , representing the output from subtraction circuitry 2 will be equal to $2^{17}-1$.

The output of gate 105 will be positive if C is positive, Y_i is negative and the most significant bit from the adder appearing on line 817 is a "0," as such a condition can only exist if there was a negative overflow. The output "1" from gate 105 will force OR gate 112, representing the most significant bit of the subtraction circuitry 2 output, to produce a "1" on wire 317 (negative sign). All other output bits from gates 112 representing numbers S^0 to S^{16} , are forced to be "0" because all of AND gates 102 are disabled by the output of gate 110 on wire 904, as the "1" output of gate 105 is inverted by inverter 109 to appear as a "0" at the input of gate 110. Therefore the output number of circuitry 2, S_i , is forced to be equal to -2^{17} in this case.

In FIGS. 8 and 8A, the output on line 317 is shown as representing not only S^{17} but also S^{18} , S^{19} , S^{20} , S^{21} and S^{22} . As will be apparent, this is a convenience in representation only. As will be more fully described in the discussion below of FIG. 9, multiplication circuitry 3 requires that the input multiplicand have 23 bits. The two's complement S_i has the same meaning if the sign bit and the first significant bit of the number are interposed with as many bits as desired, each having the same coefficient as the sign bit. For example, 111001 is of the same value as 11111001 in two's complement representation, and 0000011 has the same value as 00000011. The subtraction circuit 2 output numbers are 23 bit numbers in two's complement form that have a range of possible values from $2^{17}-1$ to -2^{17} .

Referring now to FIG. 9, there is shown a multiplier 150 of a conventional design well-known to those

skilled in the art. Multiplier 150 has inputs connected to lines 300-317 representing the bits of the output of subtraction circuitry remainder, S_i . Multiplier 150 also has a plurality of inputs on lines 142-148 representing, respectively, multiplication factors of 64, 32, 16, 8, 4, 2, and 1. Each of lines 142-148 is connected to a separate terminal on multiplication factor selection switch 25, and each of lines 142-148 is connected through a resistor 158 to ground. The wiper arm of switch 25 is connected to a positive voltage.

Multiplier 150 has a plurality of output lines 125-141 representing the value of the product output P^6-P^{22} . Lines 125-135 are connected to a modifier 151. Lines 136-141 are connected to the inputs of a six input OR gate 162 and are connected through a plurality of inverters 155 to another six-input OR gate 156. The output of OR gate 152 is connected to one input of a two-input AND gate 153 which has an output connected by a line 159 to modifier 151. The output of gate 156 is connected to one input of a two-input AND gate 157 which has an output connected by a line 160 to modifier 151. Line 317, representing bits $S^{17}-S^{22}$, is connected through an inverter 154 to the second input of AND gate 153. Line 317 is also connected directly to the second input of AND gate 157. Modifier 151 has a plurality of output lines 400-410. Another output line 411 is connected to line 317. Lines 400-411 represent cable 33 of FIG. 7.

The operation of the apparatus of FIG. 9 will now be discussed. Multiplier 150 is a conventional binary multiplier that responds to the input multiplicand (without sign) on wires 300-316, and the multiplier signal represented by the positive voltage on one of wires 142-148, in a manner to shift the bit positions 6, 5, 4, 3, 2, 1 or 0 positions to the left depending on whether the multiplier is 64, 32, 16, 8, 4, 2 or 1. As there are seventeen multiplicand bits, there may be as many as 23 product bits produced. All but the least significant six of these product bits appear on wires 125-141 as product bits P^6 through P^{22} .

Bits P^6 through P^{16} will pass through modifier 151 to provide the 11 least significant bits applied to digital-to-analog converter 9 in FIG. 7, and the sign bit S^{17} is always transmitted to converter 9, unchanged. However, if the multiplication operation has caused any of bits $P^{17}-P^{22}$ to be significant, that is to be "1" if the sign bit S^{17} is a "0," or to be "0" if the sign bit is a "1," then modifier circuit 151 causes all of the bits represented by lines 400-410 to be "1" if the sign bit is a "0," or causes them all to be "0" if the sign bit is a "1." Such a significant bit among the bits $P^{17}-P^{22}$ indicates a multiplication overflow, and modifier 151 causes the number presented to converter 9 to be either $2^{17}-1$ or -2^{17} according to the direction of overflow. Gate 152 in combination with converter 154 and gate 153 provides an indication of positive overflow on wire 159. Inverters 155, in combination with gate 156 and gate 157 provide an indication of positive overflow on wire 159. Inverters 155, in combination with gate 156 and gate 157 provide an indication of negative overflow on wire 160. The design of modifier circuit 151 is that of a simple logic circuit. A particular output bit for appearance on any of line 400-410 is caused to be equal to $P^{(n+6)}$ if neither wire 159 nor 160 is positive. If wire 159 is positive, the particular output bit is caused to be positive. If wire 160 is positive, the particular output is caused to be negative.

Referring now to FIG. 10, there is shown the output logic used in multiplier 150 to achieve generation of an output bit P^n . For each output P^n there is provided an OR gate 123 having seven inputs. Also provided are seven two-input AND gates 116-122, each of which has an output connected to an input on gate 123. Gate 116 has one of its inputs connected to the input line representing the input S^n for which the output product P^n is desired. Gate 117 has one of its inputs connected to the line representing S^{n-2} . Gate 119 has one of its inputs connected to the line representing S^{n-3} . Gate 120 has one of its inputs connected to the line representing S^{n-4} . Gate 121 has one of its inputs connected to the line representing S^{n-5} . Gate 122 has one of its inputs connected to the line representing S^{n-6} .

To achieve selective multiplication, each of gates 116-122 is connected to a different of lines 142-148, which are enabled by selector switch 25. Thus, gate 116 has its other input connected to line 148, gate 117 has its other input connected to line 147, gate 118 has its other input connected to line 146, gate 119 has its other input connected to line 145, gate 120 has its other input connected to line 144, gate 121 has its other input connected to line 143 and gate 122 has its other input connected to line 142.

If select switch 25 is set for a "times 1" multiplication then, for example, gate 116 will be enabled and S^n will be passed directly through gate 123 to become P^n . If, on the other hand, selector switch 25 is set for a "times 32" multiplication, then only gate 121 will be enabled and S^{n-5} will be passed through gate 123 to become P^n in the example, thus achieving a five place "left shift."

The apparatus of this invention as described above can be utilized in forms other than the preferred embodiment without departing from the spirit and scope of this invention. For example, the abscissa values may represent an angle, in a polar plot of information, rather than the rectilinear plot described. The selected coordinate can be marked by means other than intensifying the displayed point. It will also be apparent to those skilled in the art that use of addition of constants rather than subtraction is essentially the same process, addition simply being a negative subtraction. Further, it will be recognized by those skilled in the art that factors of multiplication can be selected from any reasonable constants rather than just integer powers of two. Also, the addition or subtraction process, and the multiplication process, may be carried out, for example, with an instrument computer rather than by the external hardware as described in the preferred embodiment. Overflow sensing and ordinate value modification may also be carried out, for example, by a computer rather than with the hardware described. There are other obvious variations in apparatus which may be used to accomplish the objective of vertical scale expansion without ambiguous display.

What is claimed is:

1. In digital instrument apparatus including instrument means for providing sets of binary numbers representative of coordinate points, and means for displaying the coordinate points connected to the instrument means, the improvement comprising: means connected to the instrument means, for subtracting a selectable constant binary number from one binary number of each coordinate set; and means connected intermediate the means for subtracting and the display means,

for multiplying the difference of the one binary number by a selectable binary number.

2. The apparatus of claim 1 in which the means for subtracting includes: binary counter means having input means; and pulse means connected to the binary counter input means, for varying the constant binary number.

3. The apparatus of claim 2 in which: the binary counter comprises an up-down counter; and the binary counter input means includes count-up input means and count-down input means.

4. The apparatus of claim 3 in which the pulse means comprises: pulse generator means having output means; switch means; the switch means connected to the pulse generator output means, the count-up input means and the count-down input means; and the switch means operable to a first position disconnecting the pulse generator output means from the binary counter input means, a second position connecting the pulse generator output means to the count-up input means and a third position connecting the pulse generator output means to the count-down input means.

5. The apparatus of claim 4 in which the switch means includes: lever means manually operable to select each of the first, second and third positions; and means connected to the lever mean for normally biasing the lever means to the first position.

6. The apparatus of claim 4 in which: the pulse generator means includes means for providing pulses at a plurality of frequencies; and said switch means is operable to select any one of the frequencies when in the second or third position.

7. The apparatus of claim 2 including: gate means connected intermediate the binary counter means and the means for subtracting; and gate switch means connected to the gate means for selectively opening and closing the gate means.

8. The apparatus of claim 2 including: further binary counter means; means connecting the further binary counter means to the pulse means for varying the count stored therein; comparator means; means connecting the comparator means to the instrument means, for providing thereto another binary number of each coordinate set; means connecting the comparator means to the further counter means; signal output means on the comparator means for providing an output signal only on comparison between the other binary number in the comparator means and the count in the further counter means; gate means connecting the instrument means to the binary counter input means for providing the one binary number to the binary counter means; switch means connecting the signal output means to the gate means, the switch means having on and off positions; and the gate means responsive to the signal from the signal output means when the switch is in the on position, for entering the one binary number in the binary counter means.

9. The apparatus of claim 8 including: marking means in the display means for marking a selected coordinate point; and means connecting the marking means to the signal output means.

10. The apparatus of claim 1 in which the means for subtracting includes: limit means for establishing a maximum difference of the one binary number and a minimum difference of the one binary number.

11. The apparatus of claim 1 in which the means for multiplying includes: limit means for establishing a

maximum product of the difference of the one binary number times the selected binary number and a minimum product of the difference of the one binary number times the selected binary number.

12. The apparatus of claim 8 in which: the further binary counter means comprises an up-down counter; and the further binary counter means includes input means comprising count-up input mean and count-down input means.

13. The apparatus of claim 12 in which the pulse means comprises: pulse generator means having output means; switch means; the switch means connected to the pulse generator output means, the count-up input means and the count-down input means; and the switch means operable to a first position disconnecting the pulse generator output means from the binary counter input means, a second position connecting the pulse generator output means to the count-up input means and a third position connecting the pulse generator output means to the count-down input means.

14. The apparatus of claim 13 in which the switch means includes: lever means manually operable to select each of the first, second and third positions; and means connected to the lever means for normally biasing the lever means to the first position.

15. The apparatus of claim 12 in which: the pulse generator means includes means for providing pulses at a plurality of frequencies; and said switch means is operable to select any one of the frequencies when in the second or third position.

16. In an information display system in which sets of coordinate points are sequentially displayed on display means, each of the coordinate points having an ordinate value and an abscissa value, the improvement comprising: abscissa input means for receiving digital signals representative of the abscissa value of each coordinate point; ordinate input means for receiving digital signals representative of the ordinate value of each coordinate point; subtraction means having minuend input means, subtrahend input means and difference output means; digital storage means having input means and output means; multiplication means having multiplicand input means, multiplier input means and product output means; means connecting the abscissa input means to the display means; means connecting the ordinate input means to the minuend input means; means connecting the digital storage means output means to the subtrahend input means; means connected to the digital storage means input means, for selectively supplying digital signals thereto for storage; means connecting the difference output means to the multiplicand input means; means connected to the multiplier input means for selectively supplying signals thereto for varying the multiplier value; and means connecting the product output means to the display means.

17. The system of claim 16 in which the means connecting the digital storage means output means to the subtrahend input means includes: inhibit means for selectively inhibiting transfer of information from the digital storage means to the subtrahend input means.

18. The system of claim 17 in which the inhibit means includes: gate means connected intermediate the digital storage means output means and the subtrahend input means; and switch means connected to the gate means for selectively enabling the gate means.

19. The system of claim 16 in which: the digital storage means comprises digital up-down counter means; and the digital storage means input means includes count-up input means and count-down input means.

20. The system of claim 19 in which: the means for supplying digital signals comprises pulse generator means having output means; and switch means connected intermediate the generator output means and the count-up and count-down input means.

21. The system of claim 20 in which: the generator means includes means for generating pulses at different rates; and the switch means is movable to connect a selected rate to the selected one of the count-up and count-down input means.

22. The system of claim 16 in which the difference output means includes: difference limit means for inhibiting transfer of any number to the multiplier means when the number is greater than a first predetermined value or less than a second predetermined value.

23. The system of claim 16 in which the product output means includes: product limit means for inhibiting transfer of any number to the display means when the number is greater than a first predetermined value or less than a second predetermined value.

24. The system of claim 16 including: means for entering the ordinate value corresponding to the selected abscissa value of any selected coordinate point into the digital storage means; and means connecting the means for storing to the abscissa input means, the ordinate input means and the digital storage input means.

25. The system of claim 24 including: mark means on the display means; and means connecting the means for entering to the mark means, for marking a selected coordinate point on the display means.

26. The system of claim 19 including: gated input means on the up-down counter means; further counter means having input and output means; comparator means having input and output means; means connecting the ordinate input means to the gated input means; control means connecting the comparator output means to the gated input means; means connecting the abscissa input means to the comparator input means; means connecting the further counter means output means to the comparator input means; and means connecting the further counter input means to the means for supplying digital signals.

27. The system of claim 26 including: mark means on the display means for marking a selected displayed coordinate point; and the control means connected intermediate the mark means and the comparator output means.

28. The system of claim 27 in combination with the system of claim 20 in which: the further counter means comprises a further up-down counter means having further count-up input means and further count-down input means; and further switch means connected intermediate the generator output means and the further count-up and further count-down input means.

29. The system of claim 28 in combination with the system of claim 21 in which: the further switch means is movable to connect a selected rate to the selected one of the further count-up and further count-down input means.

30. In apparatus for displaying coordinate points on display means, each coordinate point having at least an abscissa value and an ordinate value, the improvement comprising: abscissa input means; ordinate input

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means; means connecting the abscissa input means to the display means; subtraction means for subtracting a selectable value from each ordinate value; and means connecting the subtraction means between the ordinate input means and the display means.

31. The apparatus of claim 30 in which the means

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connecting the subtraction means between the ordinate means and the display means comprises: multiplication means for multiplying a received value by a selectable factor.

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