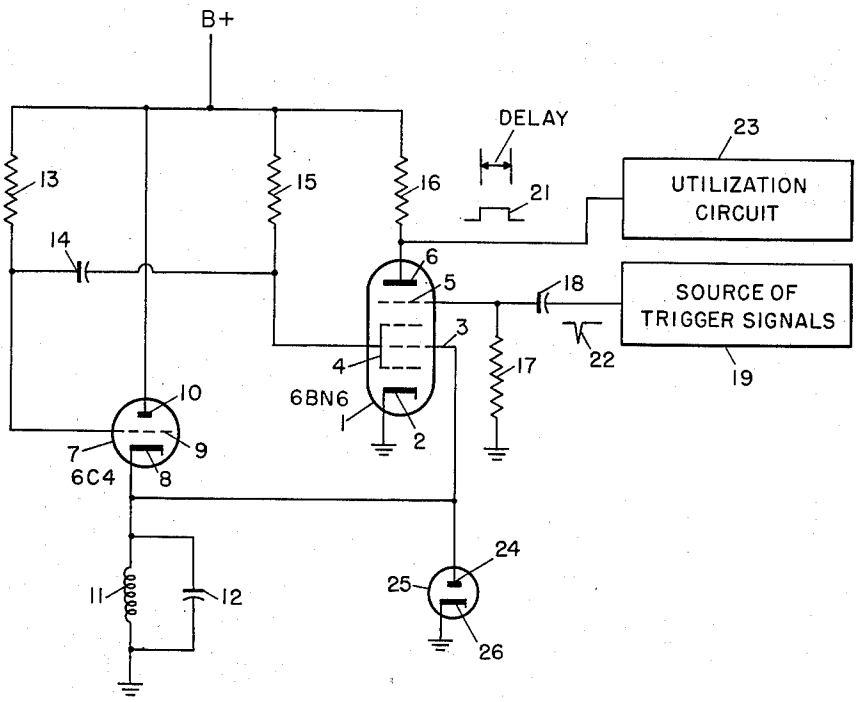
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DELAY CIRCUIT

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DELAY CIRCUIT

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This invention relates to an electronic delay circuit which is relatively stable and substantially free from time-jitter.

The known forms of electronic delay circuits are subject to a phenomenon known as "time-jitter" which manifests itself as a random variation in the duration of the delay.

This jitter is occasioned primarily by small amounts of 60 cycle voltage from the supply line present on the source of positive potential but may also be caused by thermal agitation or any other minute variable voltage present on the grid of the control tube.

Since the initiation and termination of the period of delay is usually based on the rise or fall of voltage in a resistance-capacitance circuit in combination with an electron tube operating on the slope of its grid-plate characteristic, minute variations in the voltage applied to the grid of the tube may cause its operation to be quite erratic.

Accordingly, it is an object of the present invention to provide an improved electronic delay circuit.

This and other objects may be attained by providing a circuit incorporating a "gated beam tube" in such a manner as to utilize the desirable transfer charactceristics of such a tube.

For a better understanding of the invention reference may be had to the drawing in which there is illustrated a schematic diagram of a circuit embodying the present invention.

Referring now to the drawing there is illustrated a control tube 1 which may be of a type commonly known as a "gated beam tube," or a 6BN6. This tube comprises a cathode 2, a limiter grid 3, an accelerator 4, a quadrature grid 5 and an anode 6. An idler tube 7, which may be a triode such as the type 6C4 is shown with its cathode 8 connected to the limiter grid 3 of the control tube 1 and through the parallel combination of the inductor 11 and the capacitor 12 to ground, to form a pulsed or shock-excited oscillator. The plate 24 of a diode 25 is connected to the cathode 8 and the cathode 26 of this diode is connected to ground to prevent the cathode 8 from swinging positive and further to damp out the oscillations produced in the inductance-capacitance circuit 11—12 when the tube 7 is cut off as described hereinafter. The control grid 9 of the idler tube is connected through a resistor 13 to a source of positive potential designated B+ and through a capacitor 14 to the accelerator of the control tube. The anode 10 of the idler tube is connected directly to the source of positive potential B+ as shown.

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The anode 6 of the control tube is connected through a load resistor 16 to the source of positive potential B+ and it is from this anode that the output is taken. A source of negative trigger signals 19 is connected through a capacitor 18 to the quadrature grid 5 of the control tube and through a resistor 17 to ground.

The operation of my invention is as follows:

In the operation of the circuit a substantial current flows through the idler tube 7 because of the positive bias on its grid applied through resistor 13 from the source B+. This current flows to ground through the inductor 11 which because of its inherent resistance, causes the cathode 8 to become slightly positive with respect to ground. This positive potential is applied to the limiter grid 3 of the control tube, causing a small current to flow between the accelerator electrode and the cathode. Since the quadrature grid 5 is maintained at substantially ground potential by resistor 17, a small amount of current flows between the anode and the cathode also. At the same time a substantial current is flowing between the anode 10 and the cathode 8 of the idler tube 7 because of the positive bias on its grid applied through resistor 13 from the source of potential B+.

Upon the application of a negative trigger pulse 22 from source 19 to the quadrature grid 5 of the control tube 1, the anode current of tube 1 is diverted to the accelerator electrode causing the anode voltage to rise. At the same time the accelerator current is increased causing the accelerator voltage to drop. Thus there is produced a negative pulse at the accelerator which is coupled through capacitor 14 to the grid 9 of the idler tube 7. This negative pulse effectively cuts off the current through this tube and the inductor 11. Due to the collapse of the magnetic field in this inductor, a high negative voltage is produced at the cathode 8 and is applied to the limiter grid 3. Because of the resonant effect of capacitor 12 and inductor 11, an oscillation in this circuit is started, but is damped out after the first half cycle by the action of diode 25, which presents a low impedance to the positive swings of the voltage at cathode 8. This first half cycle of negative polarity is applied to the limiter grid 3 of the control tube 1, completely cutting off the flow of current in this tube.

Since the current flow in tube 7 is cut off, its cathode circuit is completely disassociated from any variations in positive potential, and since there is very litle resistance in the cathode circuit to introduce voltage variations due to thermal agitation, the point at which the control

tube is cut off is not subject to the variations as mentioned above. Thus there is produced at the plate of the control tube a rectangular positive pulse 21, the leading edge corresponding in time to the negative trigger pulse 22, the trailing edge being determined by the circuit constants, particularly the period of oscillation of the inductance-capacitance circuit in the cathode of the idler tube. This rectangular pulse is applied to a utilization circuit shown diagrammatically as block 23, which may take the form of a differentiation circuit to derive pulses from both the leading and trailing edges of the rectangular pulse 21, which pulses will have a fixed time period therebetween.

In a practical embodiment of this circuit it has been found that the time constant of the resistance-capacitance elements 13 and 14 should be approximately ten times as great as the product of the inductance and capacitance of elements 11 and 12.

While the invention has been described as a particular circuit arrangement, other embodiments may be devised without departing from the spirit of the invention which is defined in the following claims.

1. A circuit for predetermining the time interval between the leading and lagging edges of a voltage pulse, said circuit comprising a gated beam tube having a plurality of input and output electrodes, a source of trigger signals connected to one of said input electrodes to initiate said leading edges, a pulsed oscillator for providing a series of substantially sinusoidal oscillations, a connection between one of said output electrodes and said oscillator for initiating said series of oscillations in synchronism with said trigger signals, a connection between said pulsed oscillator and a second of said input electrodes to apply said oscillations to said input electrode to initiate said lagging edges.

2. A circuit for predetermining the time interval between the leading and lagging edges of a voltage pulse, said circuit comprising a gated beam tube having a quadrature grid; a limiter grid and a plurality of output electrodes, a source of trigger signals connected to said quadrature grid to initiate said leading edges, a pulsed oscillator for providing a series of substantially sinusoidal oscillations, a connection between one of said output electrodes and said oscillator for initiating said series of oscillations in synchronism with said trigger signals, and a connecton between said pulsed oscillator and said limiter grid to apply said oscillations thereto to initiate said lagging edges.

3. A circuit for predetermining the time interval between the leading and lagging edges of a voltage pulse, said circuit comprising a gated beam tube having a plurality of input electrodes, an accelerator electrode and an anode, a source of trigger signals connected to one of said input electrodes to initiate said leading edges, a pulsed oscillator for providing a series of substantially sinusoidal oscillations, a connection between said accelerator electrode and said oscillator for initiating said series of oscillations in synchronism with said trigger signals, a connection between said pulsed oscillator and a second of said input electrodes to apply said oscillations to said input electrode to initiate said lagging edges and a utilization circuit connected to said anode to utilize the output thereof.

4. A circuit for predetermining the time interval between the leading and lagging edges of a voltage pulse, said circuit comprising a gated beam tube having a quadrature grid, a limiter grid, an accelerator electrode and an anode, a source of trigger signals connected to said quadrature grid to initiate said leading edges, a pulsed oscillator for providing a series of substantially sinusoidal oscillations, a connection between said accelerator electrode and said oscillator for initiating said series of oscillations in synchronism with said trigger signals, a connection between said pulsed oscillator and said limiter grid to apply said oscillations to said input electrode to initiate said lagging edges and a utilization circuit connected to said anode to utilize the output thereof.

5. A circuit for predetermining the time interval betwen the leading and lagging edges of a voltage pulse, said circuit comprising a gated beam tube having a plurality of input and output electrodes, a source of trigger signals connected to one of said input electrodes to initiate said leading edges, a pulsed oscillator for providing a series of substantially sinusoidal oscillations, a diode connected to said pulsed oscillator for damping said oscillations, a connection between one of said output electrodes and said oscillator for initiating said series of oscillations in synchronism with said trigger signals, a connection between said pulsed oscillator and a second of said input electrodes to apply said oscillations to said input electrode to initiate said lagging edges.

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