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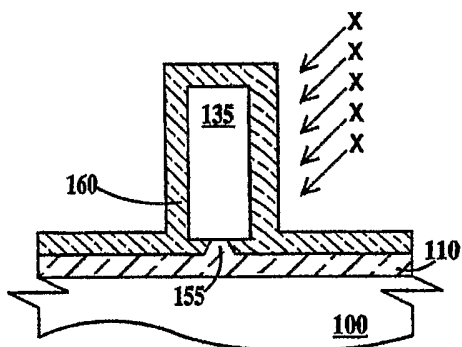
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(54) Title: METHOD OF FABRICATING A FINFET



(57) Abstract: A FinFET structure and method of forming a FinFET device. The method includes: (a) providing a semiconductor substrate (100), (b) forming a dielectric layer (110) on a top surface (105) of the substrate (100); (c) forming a silicon fin (135) on a top surface (115) of the dielectric layer (110); (d) forming a protective layer (160) on at least one sidewall (150A) of the fin (135); and (e) removing the protective layer (160) from the at least one sidewall (150A) in a channel region (175) of the fin (135). In a second embodiment, the protective layer (160) is converted to a protective spacer (210A).

METHOD OF FABRICATING A FINFET

5

TECHNICAL FIELD

The present invention relates to the field of semiconductor devices ; more specifically, it relates to method of fabricating a fin field effect transistor (FinFET).

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BACKGROUND ART

In FinFET technology, a vertical fin of crystalline silicon is used to form the body of a transistor and a gate is formed on a sidewall of the body. When gates are formed on both sidewalls of the body, the transistor is generally referred to as a double gated FinFET.

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As FinFET density increases, both the fin thickness and the gate dielectric thickness formed on the fin decreases. This presents two problems. First, thinner gate dielectrics require cleaner and crystallographically more ideal fin sidewalls than present FinFET fabrication techniques can produce. Second, when present fin fabrication techniques are applied to produce thin fins, the resultant fins are weakly attached to the supporting substrate.

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Therefore, there is a need for a method of fabricating FinFETs having very thin fins that have sidewall surfaces that are crystallographically close to perfect and that overcomes the inherent structural weakness of thin fins.

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DISCLOSURE OF INVENTION

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A first aspect of the present invention is a method of forming a FinFET device, comprising: (a) providing a semiconductor substrate, (b) forming a dielectric layer on a top surface of the substrate; (c) forming a silicon fin on a top surface of the dielectric layer; (d) forming a protective layer on at least one sidewall of the fin; and (e) removing the protective layer from the at least one sidewall in a channel region of the fin.

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A second aspect of the present invention is a method of forming a FinFET device, comprising: (a) providing a semiconductor substrate, (b) forming a dielectric layer on a top surface of the substrate; (c) forming a silicon fin having sidewalls on a top surface of the dielectric layer; and (d) forming a protective spacer on at least a lower portion of at least one of the sidewalls.

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A third aspect of the present invention is a FinFET device, comprising: a semiconductor substrate, a dielectric layer on a top surface of the substrate; a silicon fin having sidewalls, the fin on a top surface of the dielectric layer; and a protective spacer on at least a lower portion of at least one of the sidewalls.

BRIEF DESCRIPTION OF DRAWINGS

The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIGs. 1A through 10A are top views and corresponding FIGs. 1B through 10B are cross-sectional views illustrating fabrication of a FinFET structure according to a first embodiment of the present invention;

FIG. 11A is a cross-sectional view of a FinFET utilizing a conformal gate as illustrated in FIGs. 10A and 10B after interlevel dielectric (ILD) formation;

FIG. 11B is a cross-sectional view of a FinFET utilizing a damascene planarized gate as after interlevel dielectric (ILD) formation;

FIGs. 12A through 16A are top views and corresponding FIGs. 12B through 16B are cross-sectional views illustrating fabrication of a FinFET structure according to a second embodiment of the present invention; and

FIGs. 17A through 17F are cross-sectional views illustrating fabrication of a FinFET structure according to a third embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

FIGs. 1A through 9A are top views and corresponding FIGs. 1B through 9B are cross-sectional views illustrating fabrication of a FinFET structure according to a first embodiment of the present invention.

FIG. 1B is a cross-sectional view through line 1B-1B of FIG. 1A. In FIGs. 1A and 1B, a semiconductor substrate 100 is provided. In one example, substrate 100 is mono-crystalline silicon. Formed on a top surface 105 of substrate 100 is a buried dielectric layer, in the present example a buried oxide layer (BOX) 110. Formed on a top surface 115 of BOX 110 is a silicon layer 120. In one example, silicon layer 120 is about 200 to 2000 Å thick. Silicon layer 120 may be mono-crystalline-silicon, poly-crystalline silicon or amorphous silicon. Substrate 100, BOX 110 and silicon layer 120 may be obtained as a Silicon-on-Insulator (SOI) substrate or a SIMOX substrate. An etch mask 130 is formed on a top surface of silicon layer 125. In one example, etch mask 130 is formed by applying a photoresist layer to top

surface 125 of silicon layer 120 and photo-lithographically patterning the photo-resist layer.

FIG. 2B is a cross-sectional view through line 2B-2B of FIG. 2A. In FIGs. 2A and 2B, a
5 reactive ion etch (RIE) process (using, for example CF₄) is performed to remove
unwanted silicon from silicon layer 120 above BOX 110 and leave a fin 135. Fin 135
has a width W and a height H. The height H is the same as the thickness of silicon
layer 120 of FIG. 1B, which is about 500 to 2000 Å. In one example, W is about 50
10 to 350 Å. A base surface 140 of fin 135 is in direct physical contact with top surface
115 of BOX 110 and this contact and adhesion between the fin and the BOX supports
the fin.

FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A. In FIGs. 3A and 3B,
15 mask 130 (see FIG. 2B) is removed using a buffered hydrofluoric acid (BHF) causing
undercut of BOX 110 under base surface 140 of fin 135. Fin 135 is now supported
only by a pedestal 145 FIG. 4B is a cross-sectional view through line 4B-4B of FIG.
4A. In FIGs. 4A and 4B, a number of cleaning steps including oxidations and BHF
strips are performed to clean sidewalls 150A and 150B and remove crystallographic
20 surface defects from the sidewalls. These cleaning steps cause further undercut of
BOX 110 under base surface 140 of fin 135. Fin 135 is now supported only by
pedestal 155. The undercut of fin is D on each side of the fin. In one example, D is
about 50 to 75 Å. Care must be taken not to completely undercut fin 135. As the
total area of contact between base surface 140 of fin 135 and pedestal 155
25 decreases, the fin becomes more easily broken off.

FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A. In FIGs. 5A and 5B, a
conformal protective layer 160 is formed over sidewalls 150A and 150B and a top
30 surface 150C of fin 135 and over exposed top surface 115 of BOX 110. Protective
layer 160 protects sidewalls 150A and 150B of fin 135 from potential damage from
subsequent processing (described infra), and structurally supports the fin. In a first
example, protective layer 160 is a tetraethoxysilane (TEOS) oxide formed by plasma-
enhanced chemical vapor deposition (PECVD) and is about 15 to 50 Å thick. In a
second example, protective layer 160 is silicon nitride formed by low-pressure
chemical vapor deposition (LPCVD) and is about 15 to 50 Å thick.

35 A series of process steps, necessary to form doping regions, such as source/drain
(S/D) regions and to tailor doping levels of channel regions within fin 135 are next
performed. The steps each include: (1) masking a region of fin 135 with a
photoresist mask, (2) performing an ion implantation, (3) removing the photoresist
40 mask (usually in an oxygen plasma), and (4) performing an optional anneal. These
four steps can be repeated from 2 to 4 or more times, the exact number of times is
dependent upon the dopant level control within fin 135 that is required. Finally,
cleans such as a dilute hydrofluoric acid (HF) clean and/or a Huang A clean, and/or
Huang B clean are performed. An example of an ion-implantation step is illustrated
45 in FIGs. 6A and 6B and described infra. Without protective layer 160 in place

damage may occur to the surfaces of sidewalls 150A and 150B and fin 135 may be undercut to the point where the fin detaches from BOX 110.

FIG. 6B is a cross-sectional view through line 6B-6B of FIG. 6A. In FIGs. 6A and 6B, a photoresist mask 165 is formed over S/D regions 170 of fin 135 and an ion implant performed in channel region 175 of the fin. Ion implant species X may be any species commonly implanted such as B, P, As, and Ge. For a source/drain ion implantation, channel region 175 is masked and the implant performed into S/D regions 170.

FIG. 7B is a cross-sectional view through line 7B-7B of FIG. 7A. In FIGs. 7A and 7B, a photoresist mask 180 is formed over portions of protective layer 160 and BOX layer 110 and the protective layer is removed from fin 135 where it is not protected by the photoresist mask. In the example of protective layer 160 comprising silicon nitride a fluorine based RIE or a hot phosphoric acid etch may be used. In the example of protective layer 160 comprising silicon dioxide a fluorine based RIE or a dilute HF acid etch may be used.

FIG. 8B is a cross-sectional view through line 8B-8B of FIG. 8A. In FIGs. 8A and 8B, a gate dielectric layer 185 is formed on exposed sidewalls 150A and 150B and top surface 150C of fin 135. In one example, gate dielectric layer 185 is thermal oxide about 15 to 50 Å thick.

FIG. 9B is a cross-sectional view through line 9B-9B of FIG. 9A. In FIGs. 9A and 9B, a gate 190 is formed over gate dielectric 185 and fin 135 in channel region 175 of the fin. In the present example, gate 190 is formed by a conformal blanket deposition of a conductive material, a photolithographic masking step and an RIE. Examples of suitable gate materials include doped and undoped polysilicon and metals such as W or Al. Since gate 190 is formed over both sidewalls 150A and 150B of fin 135, the resultant FinFET will be double gated.

FIG. 10B is a cross-sectional view through line 10B-10B of FIG. 9A. In FIGs. 9A and 9B, any remaining protective layer 160 (see FIG. 9A) is removed using a dilute HF etch or fluorine based RIE or using H_3PO_4 if protective layer 160 is silicon nitride. Fin 135 is now supported by gate 190 until an ILD is deposited over the entire FinFET structure.

FIG. 11A is a cross-sectional view of a FinFET utilizing a conformal gate as illustrated in FIGs. 10A and 10B after ILD formation. In FIG. 10A, an ILD layer 195 is deposited on top of gate 190, exposed surfaces of fin 135 and exposed surfaces of BOX 110. A chemical-mechanical-polish (CMP) process is performed to planarize a top surface 200 of the ILD layer. Examples of ILD materials included TEOS PECVD oxide and fluorine doped glass (FSG). The resultant FinFET is completed by making contacts to the S/D regions 170 (see FIG. 6A) of fin 135 and gate 190 through vias formed in ILD 195.

FIG. 11B is a cross-sectional view of a FinFET utilizing a damascene planarized gate as after interlevel dielectric (ILD) formation. In FIG. 11B, ILD 195 is deposited first and gate 190A is formed by a damascene process. In a damascene process, trenches are formed in an ILD by photo-lithographically patterning a masking layer applied over the ILD, performing a reactive ion etch (RIE) of the ILD, removing the masking layer, depositing a conductive material of sufficient thickness to fill the trench and performing CMP process to co-planarize the top surfaces of the conductive material and the ILD. In FIG. 11B, top surface 200 of ILD 195 is co-planer with a top surface 205 of gate 190A. With a damascene gate, it may be necessary to form gate dielectric 185 after the trench is etched. The resultant FinFET is completed by making direct contact to gate 185 and contacts to the S/D regions 170 (see FIG. 6A) of fin 135 through vias formed in ILD 195.

FIGs. 12A through 16A are top views and corresponding FIGs. 12B through 16B are cross-sectional views illustrating fabrication of a FinFET structure according to a second embodiment of the present invention.

FIG. 12B is a cross-sectional view through line 12B-12B of FIG. 12A. The starting point for the second embodiment is immediately after deposition of protective layer 160 as described supra in reference to FIGs. 5A and 5B and includes all prior steps illustrated in FIGs. 1A(B) through 4A(B). FIGs. 12A and 12B are the same as FIGs. 5A and 5B respectively.

FIG. 13B is a cross-sectional view through line 13B-13B of FIG. 13A. In FIGs. 13A and 13B, an RIE of protective layer 160 (see FIG. 12B) is performed to form supporting spacers 210A and 210B on lower portions 215A and 215B of sidewalls 150A and 150B of fin 135 respectively. Spacers 210A and 210B provide structural support for fin 135.

A series of process steps, necessary to form doping regions, such as source/drain (S/D) regions and tailor channel regions within fin 135 are next performed. The steps each include: (1) masking a region of fin 135 with a photoresist mask, (2) performing an ion implantation, (3) removing the photoresist mask (usually in an oxygen plasma), and (4) performing an optional anneal. These four steps can be repeated from 2 to 4 or more times, the exact number of times is dependent upon the doping level control within fin 135 that is required. Finally cleans such as a dilute hydrofluoric acid (HF) clean and/or a Huang A clean, and/or Huang B clean are performed. An example of an ion-implantation step is illustrated in FIGs. 14A and 14B and described infra.

FIG. 14B is a cross-sectional view through line 14B-14B of FIG. 14A. In FIGs. 14A and 14B, a photoresist mask 165 is formed over S/D regions 170 of fin 135 and an ion implant performed in channel region 175 of the fin. Ion implant species X may be any species commonly implanted such as B, P, As, and Ge. For a source/drain ion implantation, channel region 175 is masked and the implant performed into S/D regions 170.

FIG. 15B is a cross-sectional view through line 15B-15B of FIG. 15A. In FIGs. 15A and 15B, a gate dielectric layer 185 is formed on exposed sidewalls 150A and 150B and top surface 150C of fin 135. In one example, gate dielectric layer 185 is thermal oxide about 15 to 50 Å thick. Spacers 210A and 210B will be incorporated into the completed FinFET device. Alternatively, support spacers 210A and 210B may be first removed by RIE prior to formation of gate dielectric 185.

FIG. 16B is a cross-sectional view through line 16B-16B of FIG. 16A. In FIGs. 16A and 16B, a gate 190 is formed over gate dielectric 185 and fin 135 in channel region 175 of the fin. In the present example, gate 190 is formed by a conformal blanket deposition of a conductive material, a photolithographic masking step and an RIE. Examples of suitable gate materials include doped and undoped polysilicon and metals such as W or Al. Since gate 190 is formed over both sidewalls 150A and 150B of fin 135, the resultant FinFET will be double gated. The FinFET may be completed as describes supra for the first embodiment of the present invention.

FIGs. 17A through 17F are cross-sectional views illustrating fabrication of a FinFET structure according to a third embodiment of the present invention. In FIG. 17A, a semiconductor substrate 300 is provided. Formed on a top surface 305 of substrate 300 is a BOX 310. Formed on a top surface 315 of BOX 310 is a mandrel layer 320. In one example, mandrel layer 320 is silicon nitride. In FIG. 17B, mandrel layer 320 (see FIG. 17A) is photo-lithographically patterned and an RIE performed to form a mandrel 325. In FIG. 17C, an amorphous silicon or poly crystalline silicon layer 330 is conformally deposited on a top surface 335, on a sidewall 340 of mandrel 325 and on exposed top surface 315 of BOX 310. In one example, silicon layer 330 is formed by sputtering silicon. Silicon layer 330 is subjected to a high temperature anneal to convert it to a monocrystalline silicon layer. In FIG. 17D, silicon layer 330 (see FIG. 17C) is an RIE performed to form a fin 345. An inner sidewall 350A of fin 345 is in contact with sidewall 340 of mandrel 335. In FIG. 17E, a conformal protective layer 350 is formed over top surface 335 of mandrel 325, a top surface 360 and an outer sidewall 350B of fin 345 and exposed top surface 315 of BOX 310. In FIG. 17F, an RIE process is performed to form a supporting spacer 365 in contact with a lower portion 370 of outer sidewall 350A of fin 345. Further processing as described supra may be performed to complete a FinFET device. Supporting spacer 365 may be removed later in processing or left in place and incorporated into the completed FinFET device.

Thus, the present invention discloses a method of fabricating FinFETs having very thin fins that have sidewall surfaces that are crystallographically closer to perfect and that overcomes the inherent structural weakness of thin fins.

The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to

those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.

CLAIMS

1. A method of forming an FinFET device, comprising:
- 5 (a) providing a semiconductor substrate,
- (b) forming a dielectric layer on a top surface of said substrate;
- 10 (c) forming a silicon fin on a top surface of said dielectric layer;
- (d) forming a protective layer on at least one sidewall of said fin; and
- 15 (e) removing said protective layer from said at least one sidewall in a channel region of said fin.
2. The method of claim 1, further including between steps (d) and (e) performing at least one ion implantation step into said fin.
- 20 3. The method of claim 1, further including:
- (f) forming a gate dielectric on exposed surfaces of said fin in said channel region; and
- 25 (g) forming a conductive gate on said gate dielectric.
4. The method of claim 3, further including:
- 30 (h) removing said protective layer from source/drain regions of said fin.
5. The method of claim 1, further including between steps (c) and (d) removing a portion of said dielectric layer from under said fin.
- 35 6. The method of claim 1, wherein said protective layer comprises tetraethoxysilane oxide or silicon nitride.
7. The method of claim 1, wherein said protective layer is about 15 to 50 Å thick.
- 40 8. The method of claim 1, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

9. The method of claim 1, wherein step (c) comprises:

forming a silicon layer on said top surface of said dielectric layer;

5 forming a mask over said silicon layer;

removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and

10 removing said mask.

10. The method of claim 1, wherein said fin comprises mono-crystalline silicon.

15 11. A method of forming an FinFET device, comprising:

(a) providing a semiconductor substrate,

(b) forming a dielectric layer on a top surface of said substrate;

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(c) forming a silicon fin having sidewalls on a top surface of said dielectric layer; and

(d) forming a protective spacer on at least a lower portion of at least one of said sidewalls.

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12. The method of claim 11, further including:

(e) performing at least one ion implantation step into said fin.

30 13. The method of claim 11, further including:

(e) forming a gate dielectric on exposed surfaces of said fin in at least a channel region of said fin; and

35 (f) forming a conductive gate on said gate dielectric.

14. The method of claim 11, further including between steps (c) and (d) removing a portion of said dielectric layer from under said fin.

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15. The method of claim 11, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

16. The method of claim 11, wherein said protective spacer is about 15 to 50 Å thick.

45

17. The method of claim 11, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

5 18. The method of claim 11, wherein step (c) comprises:

forming a silicon layer on said top surface of said

mask over said silicon layer;

10

removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and

removing said mask.

15

19. The method of claim 11, wherein step (c) comprises:

forming a mandrel on said dielectric layer;

20

depositing a conformal silicon layer on a top surface and a sidewall of said mandrel and on surfaces of said dielectric layer not covered by said mandrel;

removing said conformal silicon layer from said top surface of said mandrel and said surfaces of said dielectric layer not covered by said mandrel.

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20. The method of claim 19, further including after the step of removing, performing a high temperature anneal of said conformal silicon layer.

21. The method of claim 11, wherein said fin comprises mono-crystalline silicon.

30

22. An FinFET device, comprising:

a semiconductor substrate,

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a dielectric layer on a top surface of said substrate;

a silicon fin having sidewalls, said fin on a top surface of said dielectric layer; and

a protective spacer on at least a lower portion of at least one of said sidewalls.

40

23. The FinFET device of claim 22, wherein said fin includes a channel region and source/drain regions.

24. The FinFET device of claim 22, further including:

a gate dielectric on surfaces of said fin in said channel region of said fin; and

5 a conductive gate on said gate dielectric.

25. The FinFET device of claim 22, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

10 26. The FinFET device of claim 22, wherein said protective spacer is about 15 to 50 Å thick.

27. The FinFET device of claim 22, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

15

28. The FinFET device of claim 22, wherein said silicon fin comprises mono-crystalline silicon.

20

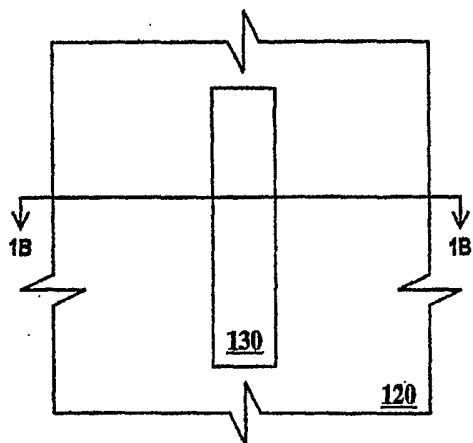


FIG. 1A

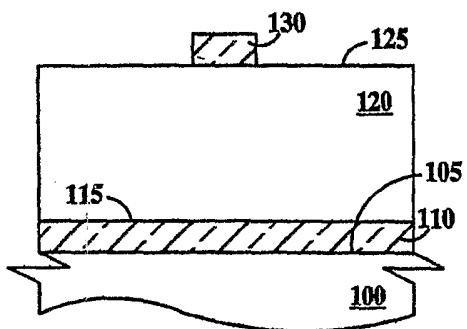


FIG. 1B

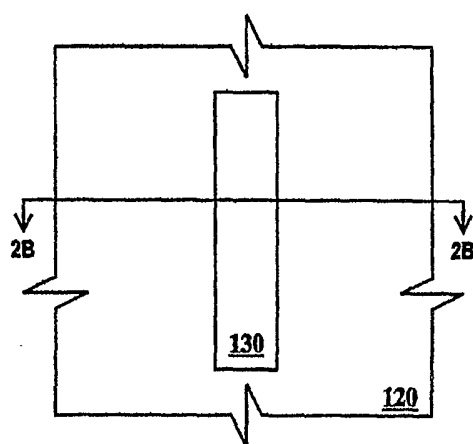


FIG. 2A

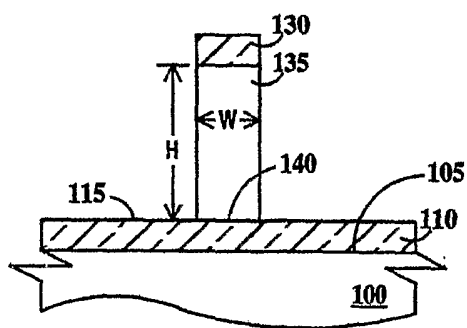


FIG. 2B

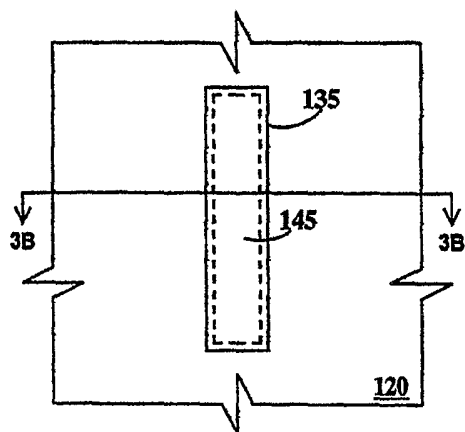


FIG. 3A

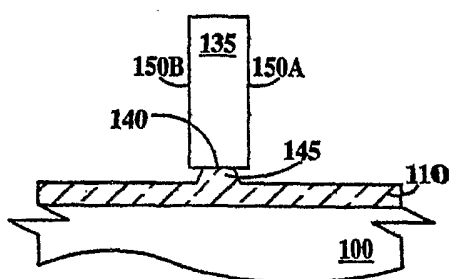


FIG. 3B

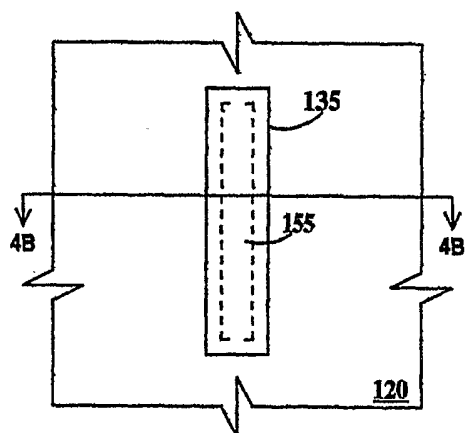


FIG. 4A

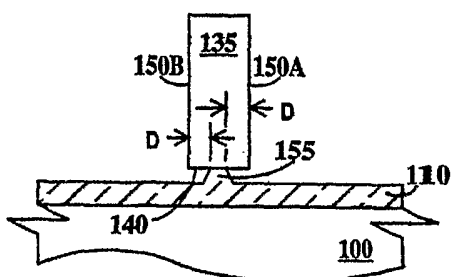


FIG. 4B

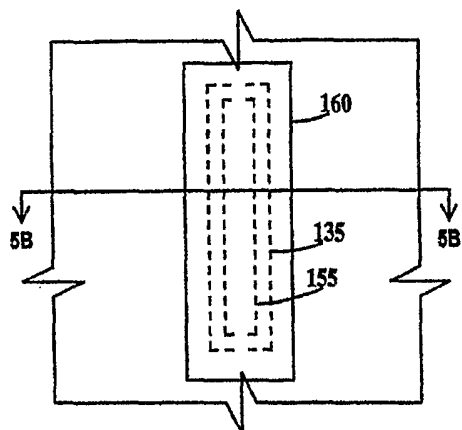


FIG. 5A

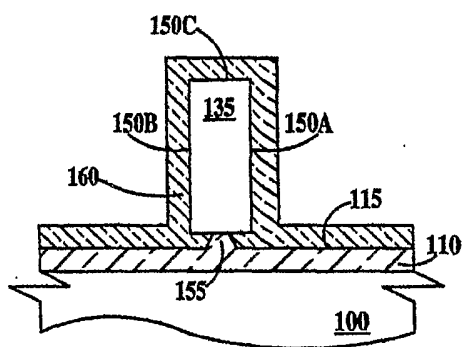


FIG. 5B

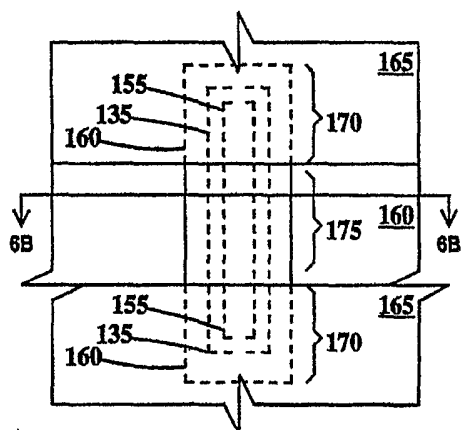


FIG. 6A

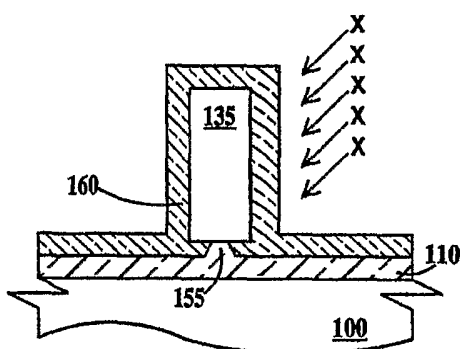


FIG. 6B

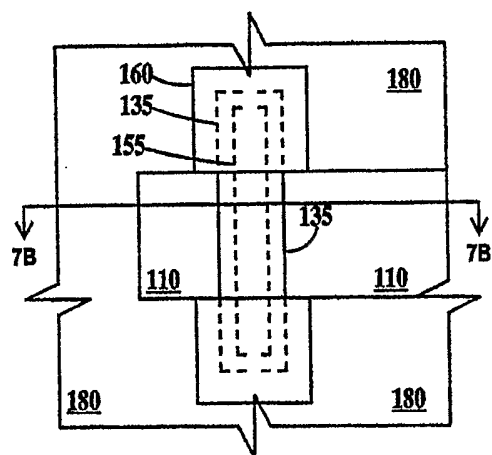


FIG. 7A

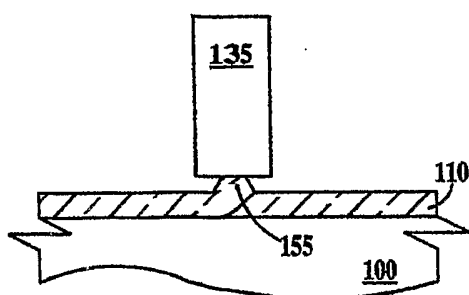


FIG. 7B

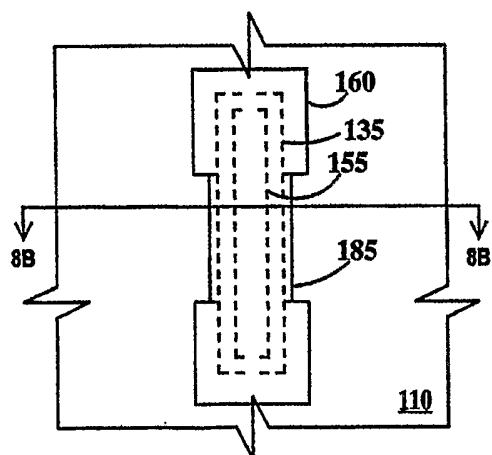


FIG. 8A

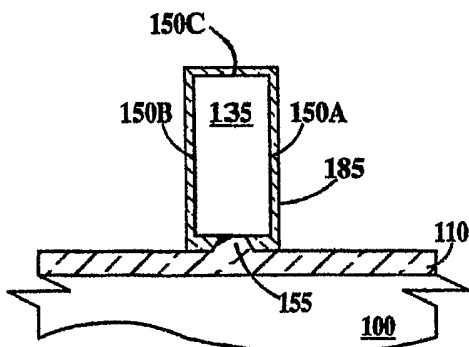


FIG. 8B

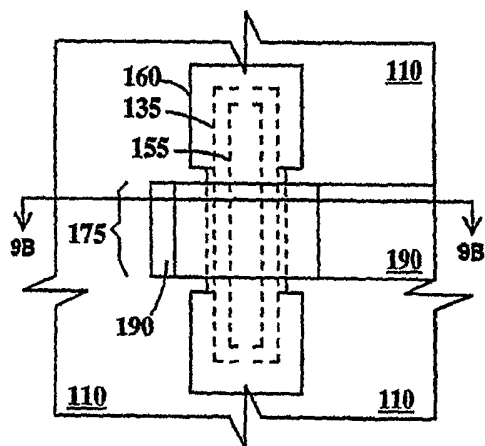


FIG. 9A

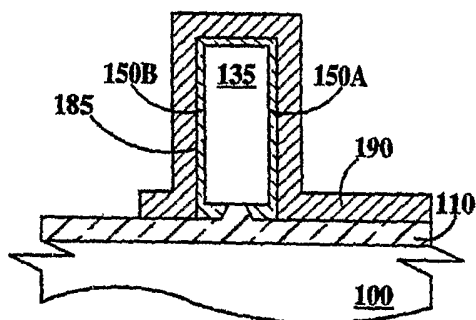


FIG. 9B

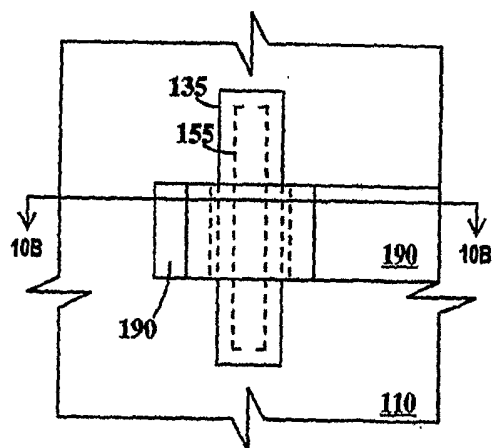


FIG. 10A

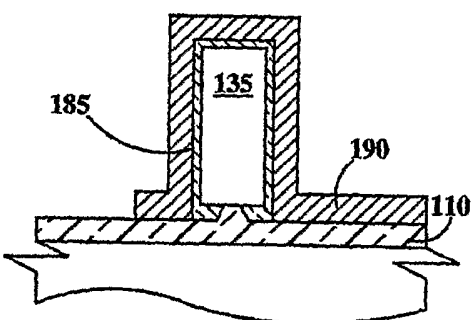


FIG. 10B

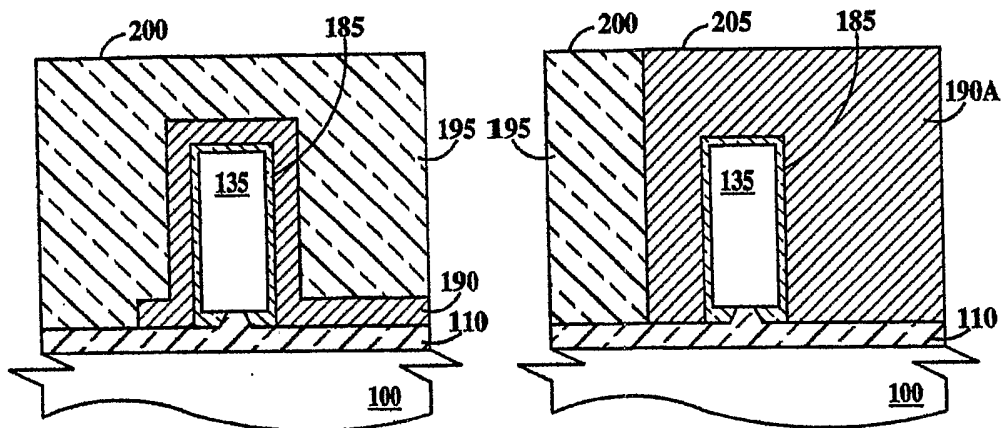


FIG. 11A

FIG. 11B

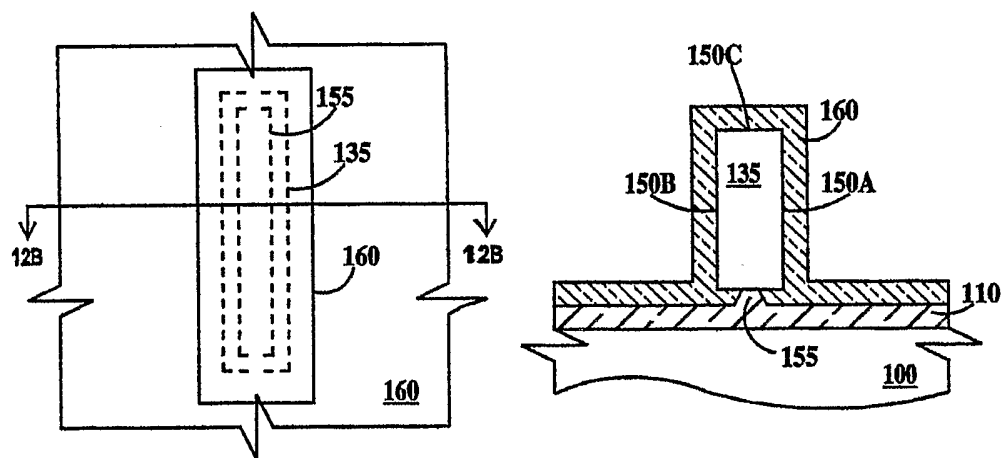


FIG. 12A

FIG. 12B

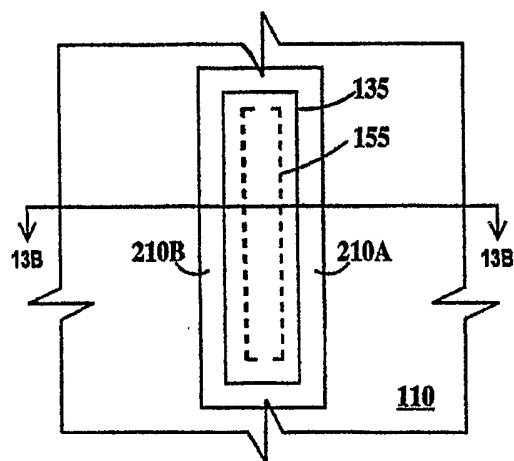


FIG. 13A

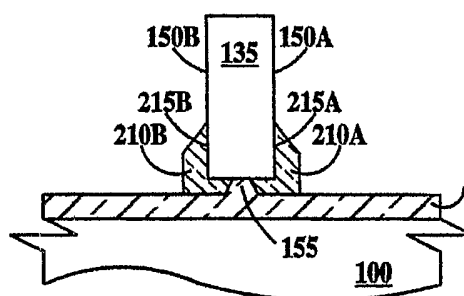


FIG. 13B

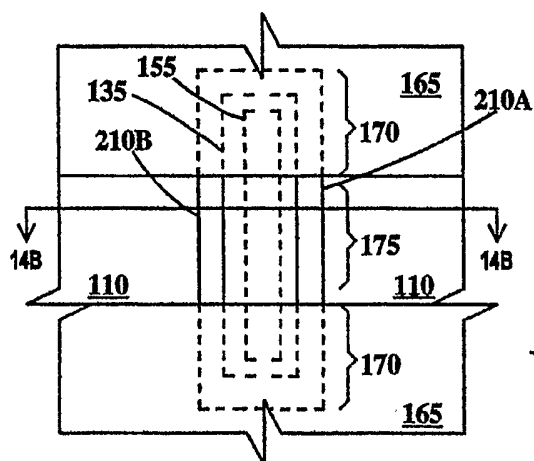


FIG. 14A

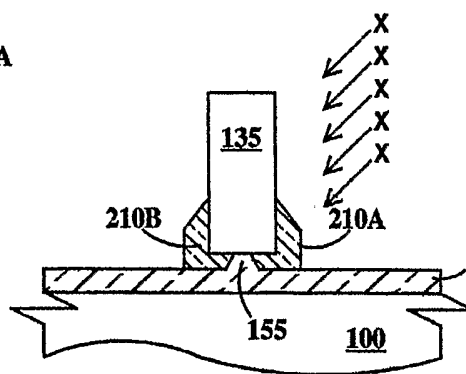
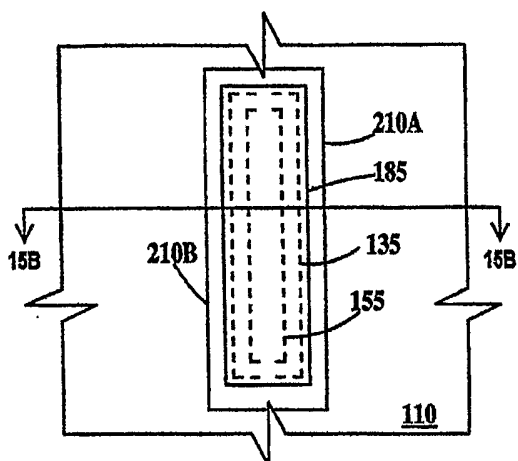
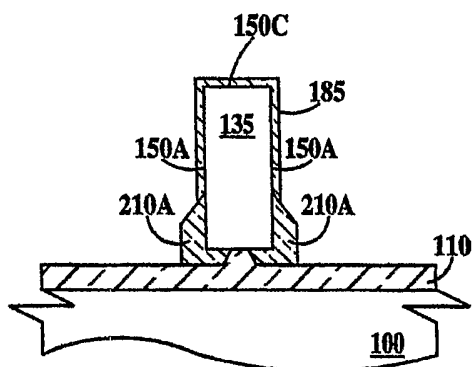
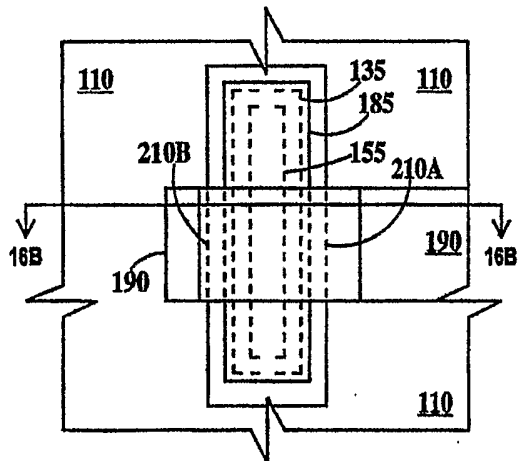
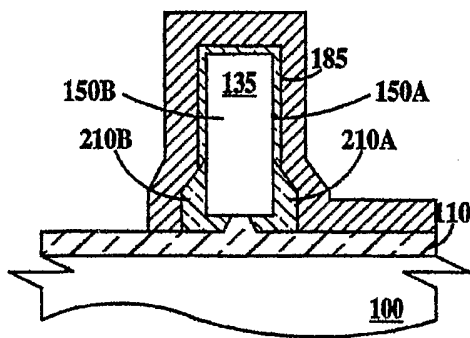
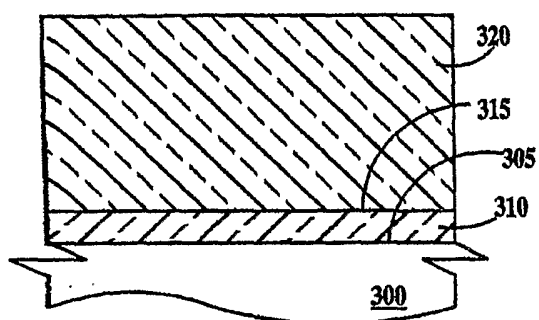
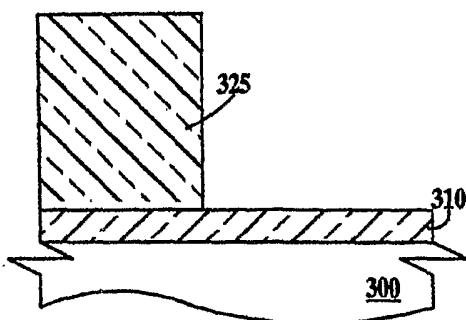
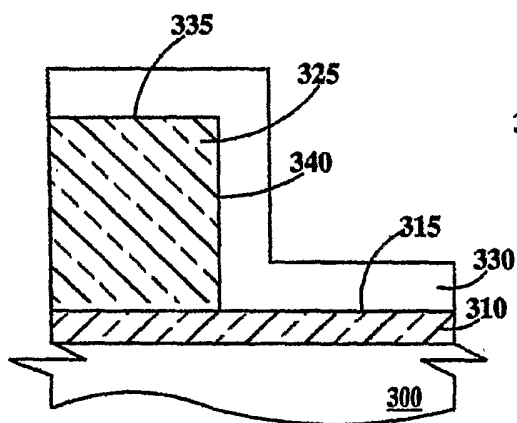
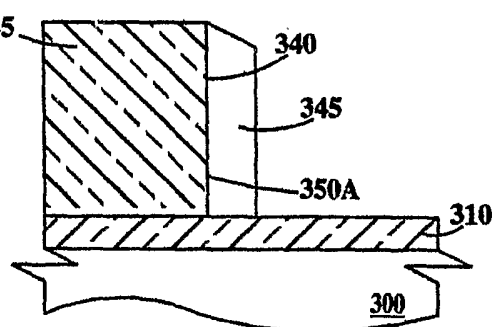
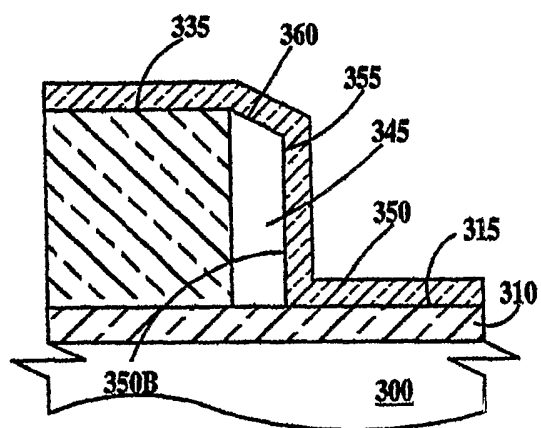
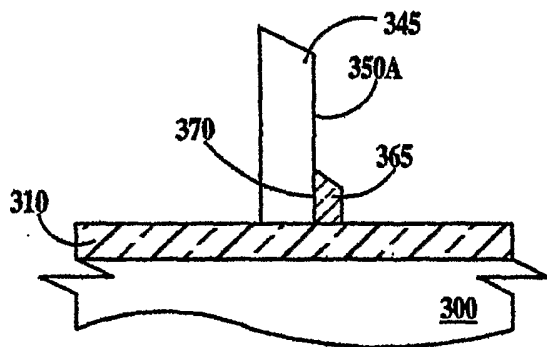


FIG. 14B

**FIG. 15A****FIG. 15B****FIG. 16A****FIG. 16B**

**FIG. 17A****FIG. 17B****FIG. 17C****FIG. 17D**

**FIG. 17E****FIG. 17F**