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(19)

(54) SEMICONDUCTOR DATA STORAGE DEVICES

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to integrated semiconductor data storage devices consisting of a flip-flop with two cross-coupled bipolar switching transistors and two load elements each connected by one of its two terminals to the collector of a respective one of the switching transistors, said storage device being controlled via a word line connected to the other terminal of both load elements and via one bit line each of a bit line pair connected to the emitter of each switching transistor.

Such storage devices are used in particular in storage arrangements of digital data processing systems, whereby the storage devices are arranged in a matrix, so that each individual device can be addressed via corresponding selections means, with binary data being written into or read from it.

In the field of logical circuits with bipolar transistors considerable progress has been made during the past few years, which has attracted great attention on the part of the experts and which under the term MTL (Merged Transistor Logic) or I^2L (Integrated Injection Logic) has become widely known in technical literature. Attention is drawn, for example, to articles in the IEEE Journal of Solid-State Circuits, Vol. SC—7, No. 5, October 1972, pp. 340 ff and 346 ff. Relevant patent specifications, are, for example, US—PS 3 736 477 and 3 816 758. This injection logic concept is essentially based on inverting single- or multiple-collector transistors which by the direct injection of minority charge carriers inside the semiconductor body are fed close to their emitter-base junctions (order of magnitude one diffusion length). This bipolar logic concept has very short switching times. In addition, it is suitable for the manufacture of extremely highly integrated, large-scale logical circuits with a great number of logical elements producible on a single semiconductor chip. For the manufacture of logical circuits in highly integrated technology, essentially three prerequisites have to be fulfilled. The basic circuits must be as simple and space-saving as possible, so that as great a number of them as possible can be arranged on a single semiconductor chip. In addition, the layout of the circuits must be such that an adequate speed does not lead to an excessive increase in the power dissipation on the semiconductor chip, which is tantamount to the requirement that the product of the factors delay time and power dissipation per logical function should be as small as possible. Finally, to obtain a good yield and thus for economical and also for technological reasons the manufacturing process required must be as simple and readily applicable as possible. The inverting logical circuits described are not only outstandingly suitable for the manufacture of logical circuits but they can also be advantageously used as a component for monolithically integrated storage cells, utilizing the fact that in the case of inverting logical circuits two stages each are required to obtain storage cells in the manner of flip-flops. Thus, a storage cell consists of two such basic circuits which are symmetrically designed and whereby the output of one basic circuit is connected to the input of the other circuit to fulfil the feedback condition. In this manner the necessary cross-coupling, as exists with conventional flip-flops, is obtained. From DT—OS 2 307 739 a storage cell is known which is made up of two

of the logical circuits described and whereby the collector of the inverting transistor of one circuit is in each case cross-coupled with the base of the inverting transistor of the other circuit. The two inverting transistors, in their turn, are inversely operated, forming the actual flip-flop transistors or switching transistors. The complementary transistor of each basic circuit, which is connected via a separate line and via which the minority charge carriers are injected, serves as a load element for both switching transistors. For the purpose of addressing, i.e. for writing and reading the storage cell, the base of each switching transistor is additionally connected to the emitter of an associated additional addressing transistor which is also complementary and whose collector and base are respectively connected to the associated bit line and the address line. Thus, in addition to the injecting transistor forming the load element, an addressing transistor is required which in turn is formed by a lateral transistor structure.

By laterally arranging the two circuits forming a storage cell and by merging the zones connected to the same potential, the desired simple semiconductor structure is obtained. By means of this known storage cell a storage matrix can be produced in which the storage cells are arranged at least in two horizontal lines and in at least four vertical columns. A first vertical address line is associated with the first and second column, and a second vertical address line is associated with the third and the fourth column. Furthermore, a first horizontal address line is associated with the first line, and a second horizontal address line is associated with the second line. Finally, a first, second and third bit line pair is respectively associated with the first, the second and the third, and the fourth column. For this purpose each bit line pair extends preferably in a vertical direction between the associated columns. The bit lines are in each case connected to the collectors of the addressing transistors, the first address line is connected to the emitters of the transistors forming the load elements, and the second address line is connected to the bases of the addressing transistors.

According to the invention, we provide an integrated semi-conductor storage device consisting of a flip-flop with two cross-coupled, bipolar switching transistors and two load elements each connected by one of its two terminals to the collector of a respective one of the switching transistors, said storage device being controlled via a word line connected to the other terminal of both load elements and via one bit line each of a bit line pair connected to the emitter of each switching transistor characterized in that the flip-flop consists of two I^2L structures integrated in two separate isolation pockets of the semiconductor body and comprising in a known manner one injector and one associated inverting transistor each, and that in each case the injector of one of the inverting transistors used as switching transistors simultaneously forms the load element of the other switching transistor.

The invention will be described in detail below by means of two embodiments shown in the drawings, of which

Fig. 1A is the equivalent circuit diagram of the known I^2L basic structure serving as a component of the storage cell embodying the invention,

Fig. 1B shows a plan view of one of the known embodiments of the I^2L basic structure shown in the equivalent circuit diagram of Fig. 1A,

Fig. 1C is a sectional view of the known I^2L basic structure in accordance with Fig. 1B,

Fig. 2 is the equivalent circuit diagram of a storage cell embodying the invention,

Fig. 3A is a plan view of a section of the structure of a first embodiment of a storage matrix made up of storage cells embodying the invention,

Fig. 3B is a first sectional view of the structure in accordance with Fig. 3A,

Fig. 3C is a second sectional view of the structure in accordance with Fig. 2A, and

Fig. 4 is a plan view of a section of the structure of a second embodiment of a storage matrix made up of storage cells embodying the invention.

Initially, the I^2L basic structure shown in the equivalent circuit diagram the plan view, and the sectional view of Figs. 1A, 1B, and 1C will be described briefly. This I^2L structure realizes the injection principle and is known, for example, from the afore-mentioned US Patent Specifications 3 736 477 and 3 816 758. The layout and the operation of this structure are described in detail in the afore-mentioned literature, so that merely a summarizing description need be given here. The designations are chosen in such a manner that they simultaneously indicate the conductivity type of the individual zones. In addition, the semiconductor zones

merged in the actual structure and connected to the same potential are provided with the same references.

It is pointed out at this juncture that several modifications and further developments of the I^2L basic structure described here have become known, by means of which the storage cell in accordance with the invention can be advantageously realized.

As may be seen from Figs, 1B and 1C a lowly doped semiconductor substrate P^- of a first conductivity type, for example, of the P-conductivity type, serves as a starting material. On the semiconductor substrate P^- a highly doped, buried zone N^+ of the opposite conductivity type is arranged. Over the buried zone N^+ and N-doped epitaxial layer N1 is arranged. In the epitaxial layer N1 the oppositely doped zones P1 and P2 are embedded at a certain distance from each other. In zone P2 there is a further zone N2 doped oppositely thereto. The zones P1, P2, and N2 are provided with contacts via terminals I, B, and C. To the buried zone N^+ a terminal E is connected. The equivalent circuit diagram of this structure is shown in Fig. 1A, the identical designations of the individual zones permitting a direct comparison between structure and equivalent circuit diagram.

Thus, the inverting logical basic circuit used in accordance with the invention essentially consists of an inverting transistor T1 with the zone sequence N2 P2 N1, which is fed by the direct injection of minority charge carriers.

The inverting transistor T1 is designed as an inversely operated, vertical transistor. For the purpose of minority charge carrier injection, transistor T2 is provided which is complementary to transistor T1. Transistor T2 has the zone sequence P1 N1 P2 and is laterally designed in the structure described. Both transistors are integrated with each other at the highest degree of integration, utilizing common semiconductor zones. The epitaxial layer N1 simultaneously serves as the base zone of the lateral transistor T2 and as the emitter of the vertical transistor T1. The zone P1 forms the emitter of the lateral transistor T2. The zone P2 simultaneously forms the base of the vertical, inverting transistor T1 and the collector of the injecting lateral transistor T2. The zone N2 forms the collector of the inverting transistor T1. At zone P1 forming the emitter of the injecting transistor T2 an injector terminal I is provided, via which a current is externally introduced in the direction of the arrow. This current supplies the operating current for the inverting transistor T1. To zone P2 forming the base of this transistor a control terminal B is connected, via which the state of the inverting transistor T1 is switchable. At the zone N2 collector terminal C is arranged which simultaneously forms the output of the inverting basic circuit. At the buried zone N^+ the emitter terminal E of the vertical transistor T1 is arranged.

In accordance with the invention, the I^2L basic circuit described is optimally used in all the essential points by merging two such basic circuits in accordance with Fig. 1 to give a highly integrated storage cell, as shown in the equivalent circuit diagram of Fig. 2. The individual semi-conductor zones are provided with the same references as in Fig. 1, the designations of one of the two basic circuits being line indexed to permit ready distinction.

The storage cell in accordance with the invention is, in principle, designed in the manner of a flip-flop, the two inverting transistors T1 and T1′ forming the actual flip-flop transistors or switching transistors. As load elements the collector circuits of these switching transistors comprise complementary transistors T2′ and T2, respectively. For realizing the flip-flop function, the collector of one of the switching transistors is to be connected in each case to the base of the other switching transistor, so obtaining the required mutual feedback. An essential feature in accordance with the invention consists in the load element of one branch of the flip-flop simultaneously forming the injector for the switching transistor of the other branch, utilizing the injection principle described above. The injecting transistor T2 forms both the load element of the switching transistor T1′ and the injector for the switching transistor T1. The injecting transistor T2′ forms the load element of the switching transistor T1 and the injector of the switching transistor T1′. A further essential feature of the storage cell in accordance with the invention consists in the two injector terminals of the two injecting transistors T2 and T2′ being jointly connected to a word line WL, while the emitter of each switching transistor T1 and T1′, respectively, is connected to an associated bit line B0 and B1, respectively, of a bit line pair. It is significant for the storage cell in accordance with the invention that the emitter zones N1 and N1′ of the two transistors T1 and T1′ at different switching states of these transistors and at an identical current or voltage value applied have a very small voltage or current difference. When the two

I^2L structures are integrated in separate isolation pockets, the switching state of the storage cell can be read respectively via said isolation pockets and the emitter zones N1 and N1′ embedded therein.

As during the addressing of the storage cell the emitter zones N1 and N1′ of the two switching transistors thus are connected to different potentials, the two switching transistors are to be arranged in separate isolation pockets in an integrated monolithic design, as may be seen from the subsequent description of the structural layout. As the switching transistor of one branch together with the complementary transistor of the other branch, which serves as a load element, form one I^2L circuit each in accordance with the invention, said two transistors are to be arranged in one common isolation pocket in accordance with the known I^2L basic structure described by means of Fig. 1. An essential advantage of the storage cell in accordance with the invention is due to the fact that only one word line WL connected to the two injecting transistors T2′ and T2 is required as an external line. The necessary cross-coupling is effected by means of short lines M1 and M2 which connect the collector zone N2 and N2′, respectively, of one switching transistor to the base zone P2 and P2′, respectively, of the other switching transistor. As will be described below, the two bit lines B0 and B1, connected to the emitter zones N1 and N1′, respectively, of the two switching transistors T1 and T1′, respectively, are preferably realized by means of buried, highly doped zones N^+ arranged in the associated isolation pockets. All further conductive connections shown in the equivalent circuit diagram do not exist in the monolithic structure which in accordance with the I^2L basic structure is realized by merging the zones bearing the same designations. For the purpose of explaining the function, parallel to the two injecting transistors T2′ and T2 two further transistor structures for the respective inverse current direction are shown by broken lines in the equivalent circuit diagram of Fig. 2. These transistors for the inverse current direction do not exist in the structure, since they are identical with the injecting transistor structure. These additional transistor structures in the equivalent circuit diagram are justified, since with a conductive switching transistor T1 or T1′, a current IER2′ or IER2 is injected back into the respective appertaining injector. This back injected current superimposes the actual injection current IE2′ and IE2, respectively.

The monolithic layout of a storage matrix made up of the storage cells in accordance with the invention is shown by way of a plan view in Fig. 3A and by way of sectional views in Figs. 3B and 3C. The section shown in Fig. 3A comprises two lines and two columns, that means four storage cells of a storage matrix. Each storage cell is made up of two of the I^2L basic structures shown in Figs. 1A to 1C. The two basic structures forming one storage cell are separated from each other by an isolation zone IZ. The monolithic layout consist in an epitaxial layer N1 being applied to a semiconductor substrate P^-. This epitaxial layer N1 is subdivided into strips by means of isolation zones IZ extending in line direction. Thus, one line of the matrix comprises two such strip-shaped regions N1 which are isolated from each other by an isolation zone IZ. These isolation zones may be, for example, dielectric zones or P^+-doped zones extending right into the substrate P^-. In each region N1 there is a continuous buried zone N^+ which extends in line direction and which is common to one half of the total number of cells making up a line. These buried zones N^+ serve as bit lines B10, B11, B20, and B21. The two I^2L basic structures forming a storage cell are arranged one below the other in column direction, comprising, as shown in Figs. 1A to 1C, two laterally arranged zones P1 and P2 in the epitaxial layer N1 and a further zone N2 within the zone P2. In this manner a storage cell is obtained which is made up of vertical transistors T1 and T1′ with a zone sequence of N2 P2 N1 and N2′ P2′ N1′, respectively, and of associated lateral transistors T2 and T2′ with a zone sequence of P1 N1 P2 and P1′ N1′ P2′, respectively, which effect the injection. Cross-coupling is established by two lines M1 and M2 which extend on top of an isolation layer IL covering the whole arrangement, and which contact the zones N2 and P2′ and N2′ and P2, respectively. In addition, one word line WL1, WL2 is provided for each column of the matrix. By means of this word line all the P1 and P1′ zones of the various storage cells of a column, which form the emitters of the lateral, injecting transistors T2 and T2′, respectively, are connected to each other. Adjacent storage cells of a line can be isolated from each other by a suitable blocking zone BZ. This blocking zone prevents parasitic couplings between the cell components of two adjacent cells of a line. The blocking zone can be either an N^+-diffusion of a P-diffusion connected to a fixed potential, or a passive zone. The blocking zone reduces the effective area required for a storage cell.

An advantageous modification of the storage matrix shown in Fig. 3A is depicted in Fig. 4. In the structure considered here the negative influence of the blocking zones on the area requirements is reduced. Two successive storage cells in the line are arranged mirror-inverted in relation to each other, the injection zones P1 and P1′, respectively, of the adjacent cells being spaced from each other at a minimum distance, so that the area requirements for the blocking zone occur only every other storage cell. During the selection of the word line WL2 it must merely be ensured that the adjacent word line WL1 is connected to a fixed potential which is chosen in such a manner that from the injection zones P1 and P1′, respectively, associated with the word line WL1 no charge carriers are injected.

With regard to all other points, the storage arrangement in accordance with Fig. 4 corresponds to that of Fig. 3A.

The operation of a storage cell in accordance with the invention will be described in detail below by means of the equivalent circuit diagram of Fig. 2 showing the designations of the operating data necessary for the description of the operational mode. For a practical embodiment typical operating data have been assumed.

In the standby state the two bit lines B0 and B1 are kept at the same potential (about 0 Volt). The emitters P1 and P1′ of the two transistors T2 and T2′ acting as load elements preferably receive a very low standby current via the word line WL, so that the storage cell operates at very low standby power. As the base-emitter voltages VBE and VBE′ of the two transistors T2 and T2′ are of the same magnitude, the emitter currents IE2 and IE2′ are likewise of the same magnitude, so that for the stability of the storage cell the current amplification of the switching transistors T1 and T1′ must merely be larger than one. All storage cells connected to a common word line WL are fed with current IWL from a common current source. Because of the good tracking characteristics of the PNP-transistors T2 and T2′ the current is nearly uniformly distributed to all cells.

For addressing the storage cell, the potential of the word line WL is raised by several hundred millivolts.

For reading the information, there are essentially two different operational modes which can also be combined with each other.

With the first mode, the two bit line potentials VBE and VBE′ on the two bit lines B0 and B1 are kept at the same value, so that the emitter currents IE1 and IE1′ are also identical. (As the potential on the word line is raised by several hundred millivolts, the bit line potentials increase correspondingly). In order to obtain a higher read speed, the current IWL on the word line in increased over that in the standby state. During this process, the nonselected cells on the same bit line pair B0, B1 are practically cut off from the power supply, as the base-emitter voltages of the load transistors T2 and T2′ are reduced by about 500 mV. However, the information is maintained for a long time (in comparison with the read time) as a result of the charge stored in the switching transistor capacitances. As the non-selected storage cells carry practically no current during reading, they cannot supply any current to the bit lines B0, B1 either. The selected storage cell, however, supplies different currents I0 and I1 to the bit lines as a function of the storage state of the cell, so that by means of a differential current, amplifier connected to the bit lines B0 and B1 the storage state of the cell can be determined. The current difference I0—I1 will be calculated in the following paragraph, assuming the T1′ is conductive and that T1 is blocked. This switching state can be associated with a stored binary one, for example. As mentioned above, the two bit lines B0 and B1 are connected to the same potential, so that VBE=VBE′ and IE2′=IE2=IE. The bit line current I0 is derived solely from the base current IB2 of the transistor T2 in accordance with

$$(1)\quad I0=(1-\alpha 2)\cdot IE,$$

since the current IER2 injected back via the load transistor T2 in the inverse direction is zero, and since the switching transistor T1 carries no current. The bit line current I1 is composed of

$$(2)\quad I1=(1-\alpha 2')\ IE+(1-\alpha R2')+IER2'+IE1.$$

In many practical cases the base current IB1′ is low in relation to the emitter current IE2′, so that

$$(3)\quad IER2'\approx\alpha 2'\cdot IE2'=\alpha 2'\cdot IE.$$

In such a case the emitter current IE1′ is about the same as the collector current IC1′ of the transistor T1′, which is equal to the collector current of the transistor T2 in accordance with

$$(4)\ IE1' \approx IC1' = \alpha 2 \cdot IE.$$

When equations (3) and (4) are inserted into equation (2) the following equation is obtained:

$$(5)\ I1 \approx (1-\alpha 2')IE + (1-\alpha R2')\ 2' \cdot IE + \alpha 2 \cdot IE.$$

With symmetrical load transistors T2 and T2′, $\alpha 2$ and $\alpha 2'$ are of the same value, so that from equation (5) the following equation is derived:

$$(6)\ I1 \approx [1+(1-\alpha R2')\alpha 2]IE.$$

With regard to the current ratio I1/I0, the following is obtained from equations (1) and (6):

$$(7)\ I1/I0 \approx \frac{1+\alpha 2-\alpha 2 \cdot \alpha R2'}{1-\alpha 2}$$

$$= 1+\frac{\alpha 2(2-\alpha R2')}{1-\alpha 2} \text{ or}$$

$$I1/I0 \approx 1+\beta 2(2-\alpha R2').$$

This current ratio can be indicated by means of a low-resistivity differential amplifier on the bit lines B0, B1, thus permitting the determination of the state of the storage cell.

With the second read method the bit line currents I0 and I1 are kept at the same value, and the resulting bit line voltage difference VBE—VBE′ is used to determine the state of the storage cell. This voltage difference is calculated below. From equation (1) the following equation is obtained:

$$(8)\ IE2 = I0/1-\alpha 2.$$

From equation (2) the following equation is obtained:

$$(9)\ I0 = I1 = (1-\alpha 2')IE2' + (1-\alpha R2')IER2' + IE1'$$

By means of equations (3) and (4) the following is obtained after corresponding conversion:

$$(10)\ IE2' = I0 \cdot \frac{1-2 \cdot \alpha 2}{(1-2 \cdot \alpha 2' + \alpha 2' \cdot \alpha R2') \cdot (1-\alpha 2)}$$

At the same current amplifications of the load transistors T2 and T2′, thus at $\alpha 2 = \alpha 2'$, the following is obtained:

$$(10)\ IE2' = I0 \cdot \frac{1-2 \cdot \alpha 2}{(1-2 \cdot \alpha 2 + \alpha 2 \cdot \alpha R2') \cdot (1-\alpha 2)}$$

With regard to the current ratio IE2/IE2′, the following equation is obtained from equations (8) and (10):

$$(11)\ IE2/IE2' = 1+\frac{\alpha 2 \cdot \alpha R2'}{1-2 \cdot \alpha 2}$$

As VBE=VT · ln IE2′/IS (VT kT/q=26 mV at 25°C being the thermal voltage and IS the inverse saturation current), the value ΔV=VT · ln IE2/IE2′ or

$$(12)\quad \Delta V = VT \cdot \ln \left[1 + \frac{2 \cdot \alpha R2'}{1 - 2 \cdot \alpha 2} \right]$$

is obtained for the voltage difference ΔV=VBE–VBE′.

This voltage difference is sensed on both bit lines by means of a high-resistivity differential amplifier.

If the signal amplifier in the case of the current measurement [equation in (7)] has a non-neglectable internal reistance or if the value of the input resistance of the differential amplifier in the case of the voltage measurement [equation (12)] is inadequate, an operating mode results which lies between the two extremes "constant current" and "constant voltage".

For the storage cell embodying the invention a voltage difference of

$$\Delta V \approx 26\ \text{mV} \cdot \frac{\alpha 2 \cdot \alpha R2}{1 - 2 \cdot \alpha 2}$$

is obtained in a practical example according to equation (12) with $\alpha R2' = \alpha R2$ and $\alpha 2 \cdot \alpha R2' < 1$. At $\alpha 2 > \alpha R2$ and $\alpha 2 = 0.3$, and $\alpha 2' = 0.2$ this results in a voltage difference of ΔV=3.9 mW.

This value of ΔV is fully sufficient to be amplified with the aid of a tolerable number of technical means.

This write process is relatively simple. As during reading, the word line potential is raised by about 0.5V. If, for example, the switching transistor T1′ is to be cut off, the potential on bit line B1 is raised to an extent that no emitter current IE2′ and thus no base current IB1′ can flow into the switching transistor T1′.

Figs. 3 and 4 show that the storage cell can be realized at very low space requirements. In particular with modern isolation techniques (passive isolation by means of oxide, for example,) the storage cell density is considerably increased over that of known storage cells, because only one metal line, namely the word line WL, is required to wire the cell in a storage matrix. As a result of the reduced number of metal lines, the reliability is considerably increased, and the blocking zones employed prevent two adjacent storage cells of a bit line from being coupled.

WHAT WE CLAIM IS:—

1. An integrated semiconductor storage device consisting of a flip-flop with two cross-coupled, bipolar switching transistors and two load elements each connected by one of its two terminals to the collector of a respective one of the switching transistors, said storage device being controlled via a word line connected to the other terminal of both load elements and via one bit line each of a bit line pair connected to the emitter of each switching transistor characterized in that the flip-flop consists of two I^2L structures integrated in two separate isolation pockets of the semiconductor body and comprising in a known manner one injector and one associated inverting transistor each, and that in each case the injector of one of the inverting transistors used as switching transistors simultaneously forms the load element of the other switching transistor.

2. A device as claimed in claim 1, characterized in that each I^2L structure comprises as an inverting transistor one inversely operated, vertical transistor structure, and a zone arranged laterally to the base of said transistor structure and serving as an injection zone and an emitter zone of a complementary lateral transistor, whose collector simultaneously forms the base and whose base simultaneously forms the emitter of the inverting transistor.

3. A device as claimed in claim 1, or 2, characterized in that the word line of a storage cell is connected to both injection zones, and that each bit line consists of a highly conductive, buried zone within the isolation pocket containing the emitter of the associated switching transistor.

4. An integrated semiconductor data storage matrix consisting of storage devices each as claimed in any of claims 1 to 3, characterized in that the corresponding I^2L structures of all storage devices, which have one bit line pair in common, are strung together in two isolation pockets extending in line direction,

and that the injection zones of the storage cells strung together in column direction are connected by a common word line.

5. A storage matrix as claimed in claim 4, characterized in that the I^2L structures following each other in line direction are separated from each other by one blocking zone each.

6. A storage matrix as claimed in claim 4, characterized in that two I^2L structures each adjoining each other in line direction are arranged mirror-inverted in relation to each other, and that only between the adjacent bases of the switching transistors blocking zones are arranged.

7. An integrated semiconductor storage device substantially as described with reference to Fig. 2 of the accompanying drawings.

8. An integrated semiconductor data storage matrix substantially as described with reference to Figs. 3A to 3C or Fig. 4 of the accompanying drawings.

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Agent for the Applicants.

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1586323 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

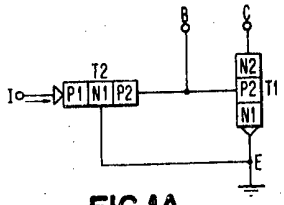


FIG.1A

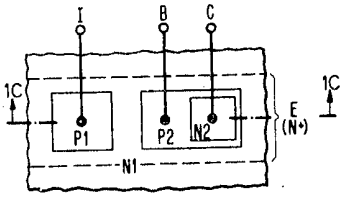


FIG.1B

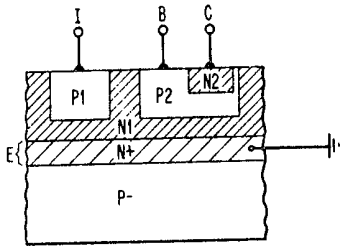


FIG.1C

FIG.2

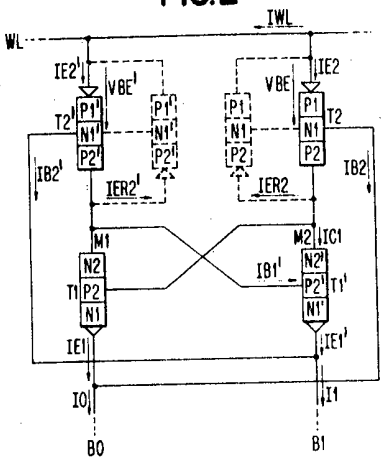
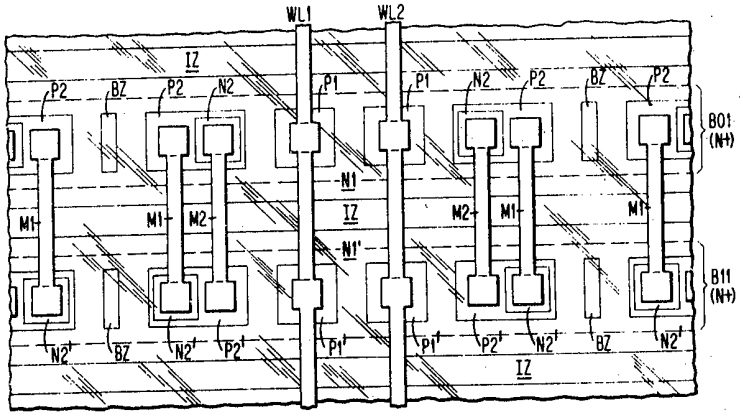


FIG.4



1586323 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 2

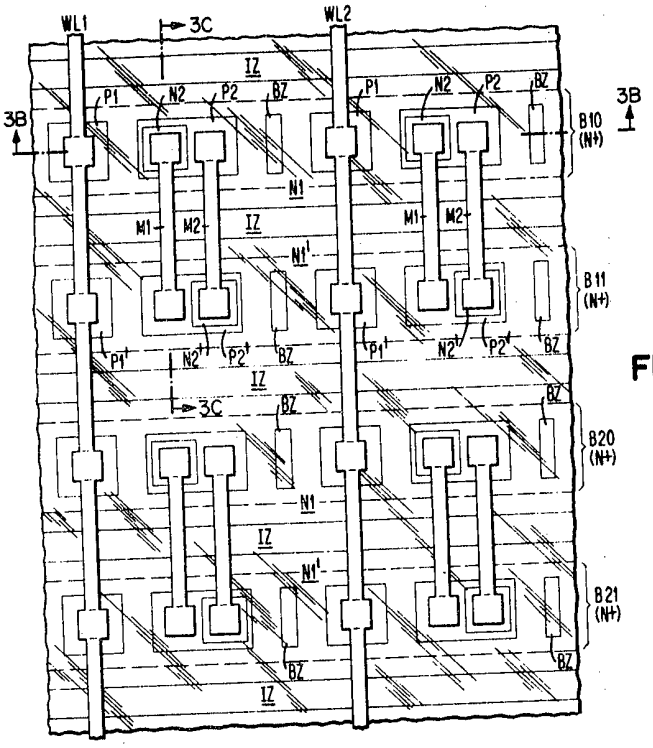


FIG.3A

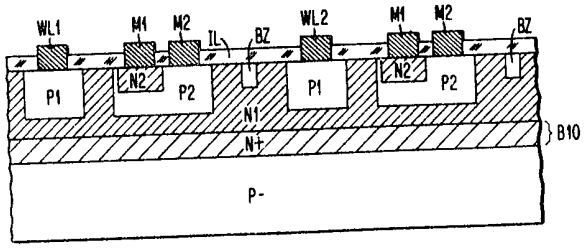


FIG.3B

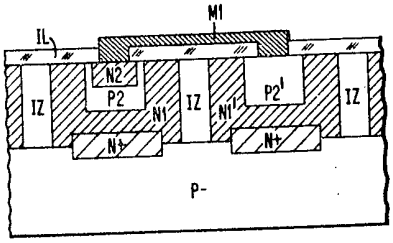


FIG.3C