



- | | |
|--|--|
| <p>(51) International Patent Classification:
 <i>G11C 11/406</i> (2006.01) <i>G11C 7/22</i> (2006.01)
 <i>G11C 11/4076</i> (2006.01) <i>G11C 5/06</i> (2006.01)</p> | <p>(81) Designated States <i>(unless otherwise indicated, for every kind of national protection available):</i> AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.</p> |
| <p>(21) International Application Number:
 PCT/US2016/032912</p> | |
| <p>(22) International Filing Date:
 17 May 2016 (17.05.2016)</p> | |
| <p>(25) Filing Language: English</p> | |
| <p>(26) Publication Language: English</p> | |
| <p>(30) Priority Data:
 14/714,962 18 May 2015 (18.05.2015) US</p> | <p>(84) Designated States <i>(unless otherwise indicated, for every kind of regional protection available):</i> ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).</p> |
| <p>(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
 US 14/714,962 (CON)
 Filed on 18 May 2015 (18.05.2015)</p> | |
| <p>(71) Applicant: MICRON TECHNOLOGY, INC [US/US];
 8000 So. Federal Way, Boise, Idaho 83716-9632 (US).</p> | <p>Published:
 — with international search report (Art. 21(3))</p> |
| <p>(72) Inventor: SHIDO, Taihei; 2-1, Yaesu 2-chome, Chuo-ku,
 Tokyo 104-0028 (JP).</p> | |
| <p>(74) Agents: SCHEER, Bradley, W. et al.; Schwegman Lundberg & Woessner, P.A., P.O. Box 2938, Minneapolis, MN 55402 (US).</p> | |

Published:

— with international search report (Art. 21(3))

(54) Title: APPARATUS HAVING DICE TO PERFORM REFRESH OPERATIONS

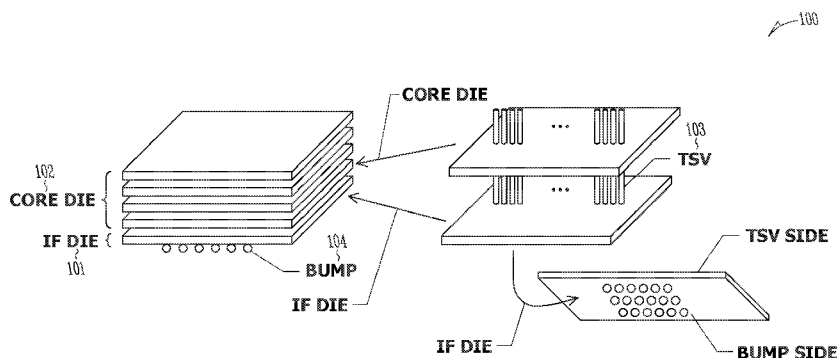


Fig. 1

(57) Abstract: Some embodiments include an apparatus that comprise an interface chip having an oscillator to produce an original clock signal, a first memory chip having first memory cells, and a second memory chip having second memory cells. The first memory cells may be refreshed in response to a first clock signal based on the original clock signal. The second memory cells may be refreshed in response to a second clock signal based on the original clock signal.

APPARATUS HAVING DICE TO PERFORM REFRESH OPERATIONS

5 Priority Application

[1] This application claims the benefit of priority to U.S. Application Serial No. 14/714,962, filed 18 May 2015 which is incorporated herein by reference in its entirety.

10 Background

[2] Some semiconductor devices, such as a DRAM (Dynamic Random Access Memory), perform a refresh operation to restore charge in memory cells to maintain the stored state of logical data. In general, the refresh operation is performed on a periodic basis or on a command basis with regard to a single die of
15 DRAM. When a plurality of dice are involved, operations are more complex, such that current consumption and stability become more difficult to control.

Summary

[3] According to a first aspect of the invention, a apparatus includes an
20 interface chip including an oscillator producing an original clock signal, a first memory chip including a first terminal configured to receive a first clock signal in response to the original clock signal, a second terminal supplied with a first control signal, and first memory cells that are subject to a data refresh operation in response to the first clock signal when the first control single is active, and a second memory
25 chip including a third terminal configured to receive a second clock signal in response to the original clock signal, a fourth terminal supplied with a second control signal, and second memory cells that are subject to a data refresh operation in response to the second clock signal when the second control signal is active.

[4] According to a second aspect of the invention, a apparatus includes a
30 chip stack structure including first and second memory chips stacked over each

other, and an interface chip coupled to the chip stack structure. The first memory chip includes first and second terminals and a plurality of first memory cell. The second memory chip includes third, fourth and fifth terminals. The first and second memory chips are stacked over each other such that the second terminal of the first memory chip is electrically connected to the fifth terminal of the second memory chip. The interface chip includes sixth, seventh, and eighth terminals, and is coupled to the chip stack structure such that the sixth, seventh and eighth terminals of the interface chip are electrically connected to the third, fourth and fifth terminals of the second memory chips, the second terminal is coupled to a first command decoder circuit of the first memory chip, and the fourth terminal is coupled to a second command decoder circuit of the second memory chip. The first and second command decoder circuits work independently from each other.

[5] According to a third aspect of the invention, an apparatus includes an interface chip that includes an oscillator circuit to provide an oscillator signal, a first memory chip on which a first refresh operation is performed in response to a first refresh enable signal supplied at a first node and a first oscillator enable signal supplied at a second node, a second memory chip on which a second refresh operation is performed in response to a second refresh enable signal supplied at a third node and a second oscillator enable signal supplied at a fourth node. The first and third nodes are configured to receive from the interface chip the first and second refresh enable signals independently of each other. The second and fourth nodes are configured to receive, based on the oscillator signal, the first and second oscillator enable signals in different timings from each other so that the first and second refresh operations are performed in different timings from each other even when the first and third nodes receive the first and second refresh enable signals simultaneously.

Brief Description of the Drawings

[6] FIG. 1 illustrates an example of a high bandwidth memory according to a first embodiment.

[7] FIG. 2 illustrates an example structure having a high bandwidth memory and a graphics processing unit according to the first embodiment.

[8] FIG. 3 illustrates an example of the circuitry of the interface die according to the first embodiment.

5 [9] FIG. 4 illustrates an example of a high bandwidth memory according to a second embodiment.

[10] FIG. 5 illustrates an example of self-refresh timing according to the second embodiment.

[11] FIG. 6 illustrates another example of self-refresh timing according to
10 the second embodiment.

[12] FIG. 7 illustrates an example of a high bandwidth memory according to the first embodiment.

[13] FIG. 8 illustrates a third example of a high bandwidth memory according to a third embodiment.

15 [14] FIG. 9 illustrates an example of a self-refresh timing according to the first embodiment.

[15] FIG. 10 illustrates an example of a core die according to the first embodiment.

[16] FIG. 11 illustrates an example of self-refresh waveforms in a core die
20 according to the first embodiment.

[17] FIG. 12 illustrates a fourth example of a high bandwidth memory according to a fourth embodiment.

[18] FIG. 13 illustrates a fifth example of a high bandwidth memory according to a fifth embodiment.

25

Detailed Description

[19] The description that follows includes illustrative an apparatus including semiconductor devices (circuits, systems, and the like) and processes (e.g., timing, waveforms, and the like) that embody the disclosed subject matter. In
30 the following description, for purposes of explanation, numerous specific details are

set forth in order to provide an understanding of various embodiments of the subject matter.

[20] FIG. 1 illustrates an example of a high bandwidth memory (HBM) according to a first embodiment. The HBM 100 may include an interface die 101, a stack of core dice 102 over the interface die 101, through-silicon-vias (TSVs) 103 to connect the core dice 102 with each other, and bump pads 104, and the HBM 100 may include a high band width memory explained below for example by referring to FIGS. 7, 8, 12, and 13.

[21] In some embodiments, the bump pads 104 may include micro bumps 104, and may receive signals from a host controller (not shown). The interface die 101 may buffer signals from the bumps 104 to the TSVs 103. In some embodiments, the core dice 102 may include memory cells, while the interface die 101 may not include any memory cells. In some embodiments, the core dice 102 may include one or more command decoders (such as a command decoder 116 as shown in FIG. 7).

[22] In some embodiments, the interface die 101 may be divided into some independent channels. These channels may be independent of one another. The HBM 100 may have a wide data interface that may perform an operation with a high-speed and low-power-consumption. A self-refresh operation may be performed in the HBM 100.

[23] FIG. 2 illustrates an example structure 200 including a HBM 100 and a Graphics Processing Unit (GPU) 105 according to the first embodiment. In some embodiments, a re-driver 106 may be disposed between the HBM 100 and the GPU 105 to drive a signal. The structure 200 may be called as a semiconductor device, an apparatus, or a system, that is accessed via a connection portion by a controller (not shown) or a processor (not shown). The connecting portion may be a bump, a ball, or a solder ball. FIG. 3 illustrates an example of the circuitry of the interface die 101 according to the first embodiment. In some embodiments, the circuitry of the interface die 101 may include a memory Built-In-Self-Test (BIST) circuit 107 to test the core die 102, internal circuits 108 (as shown in FIG. 4 for example), and an

input buffer 109 to receive signals from a corresponding micro bumps 104 and to convey the signals to corresponding TSVs 103.

[25] FIG. 4 illustrates a first example of a HBM 400 according to a second embodiment. As shown in FIG. 4, the HBM 400 may include an interface die 401, and a stack of core dice 402 (such as core die 402A and core die 402B), which are connected to each other by TSVs 403.

[26] In some embodiments, the interface die 401 may include bumps 404 (such as bump_A and bump_B), and internal circuits 408 (which may have receivers (Rx) 410, transmitters (Tx) 411, transceivers (Tx Rx) 412, logic 413, and buffers 414).

[27] In some embodiments, the core die 402A may include memory cells located in a DRAM memory array 415, a command decoder 416, a self refresh oscillator 417, and a data controller 418. Similarly, the core die 402B may include memory cells located in a DRAM memory array 415, a command decoder 416, a self refresh oscillator 417, and a data controller 418. The core die 402A and the core die 402B may operate on commands respectively, and may thus work independently from each other.

[28] FIG. 5 illustrates an example of self-refresh timing when both the core A and the core B as shown in FIG. 4 are in a self-refresh state according to the second embodiment. FIG. 6 illustrate another example of self-refresh timing when the core A as shown in FIG. 4 is in a self-refresh state and the core B as shown in FIG. 4 is not in a self-refresh state according to the second embodiment. In FIG. 5 and FIG. 6, self_osc represents a Self Refresh Oscillator signal, ACT represents an Active Command (which can be provided by a GPU), WR represents a WRITE signal, and RD represents a READ signal.

[29] A DRAM die 102 A has a self refresh function and a DRAM die 102B also has a refresh function. The refresh function may be known as a self refresh mode of a DRAM. In self-refresh mode, the DRAM may automatically refresh the memory cell data, and all banks in the DRAM may be activated to refresh the memory cell data of the banks.

[30] In the second embodiment, refresh operations of the two dice 102A and 102B are performed independently of each other, and thus those two refresh operation may sometimes occur simultaneously, which may be indicated as same timing in FIG.5. Therefore, consumption current in the same timing of refresh
5 operations of two dice 102A and 102B may become higher than consumption current in different timing of refresh operations. So to speak, peak current in the second embodiment HBM may sometimes become high in the same timing refresh operations. The DRAM dice of HMB may consume a large amount of power at the same time, and thus may induce power noise, possibly affecting the integrity of the
10 self refresh function.

[31] FIG. 7 illustrates an example of a HBM 700 according to the first embodiment. The explanations above may be applicable and/or identical at least in part to the first embodiment, and thus for simplicity, some common explanations are omitted. For example, the configurations shown above may be referred here
15 according to the first embodiment.

[32] As shown in FIG. 7, the HBM 700 may include an interface die 701, and a stack of core dice 702 (includes at least two dice such as a core die 702A and a core die 702B), which are connected to each other by TSVs 703.

[33] In some embodiments, the interface die 701 may include bumps 704
20 (such as a bump_A and a bump_B), and internal circuits 708. The internal circuits 708 of the interface die 701 may include a self refresh oscillator 717, receivers 710, transmitters 711, transceivers 712, logic 713, and buffers 714.

[34] Here, in some embodiments, the self refresh oscillator 717 may be located in the interface die 701, and may work in common with both the core die
25 702A and the core die 702B. In contrast, a self refresh oscillator 427 is not located in the interface die 401 and is located in each of dice 401A and 402B in FIG. 4. Thus, in the second embodiment, refresh operation may work independently of each other. According to the first embodiment, the self refresh oscillator 717 is configured common to stack of die including dice 702A and 702B.

[35] In some embodiments, the self-refresh oscillator 717 may be activated according to a reset signal when the HBM 700 is not in a reset state for example.

[36] In some embodiments, the core die 702A may include memory cells
5 located in a DRAM memory array 715, a command decoder 716, a data controller 718, and a delay adjust circuit 719A. Similarly, the core die 702B may include memory cells located in a DRAM memory array 715, a command decoder 716, a data controller 718, and a delay adjust circuit 719B. The core die 702A and the core die 702B may operate on commands respectively, and thus may work independently
10 of each other.

[37] Here, according to the first embodiment, the delay adjust circuit 719A of the core die 702A and the delay adjust circuit 719B of the core die 702B are coupled in series to each other. In such an arrangement, a delay amount of the delay adjust circuit 719A may be configured to be the same as a delay amount of the
15 delay adjust circuit 719B, and the delay adjust circuits 719A and 719B may be configured to be identical to each other.

[38] According to the first embodiment, the refresh timing of the channels may be different due to the delay adjust circuits 719 (such as the delay adjust circuit 719A and the delay adjust circuit 719B), and thus a peak current consumption of the
20 associated semiconductor device may be reduced.

[39] FIG. 8 illustrates a third example of a HBM 800 according to a third embodiment. As shown in FIG. 8, the HBM 800 may include an interface die 801, and a stack of core dice 802 (includes at least two dice such as a core die 802A and a core die 802B), which are connected to each other by TSVs 803. The
25 explanations above may be applicable and/or identical at least in part to the third embodiment, and thus for simplicity, some common explanations are omitted. For example, the configurations shown above may be referred here according to the third embodiment.

[40] In some embodiments, the interface die 801 may include bumps
30 (such as a bump_A and a bump_B), and internal circuits 808. The internal circuits

of the interface die 801 may include a self refresh oscillator 817, receivers 810, transmitters 811, transceivers 812, logic 813, and buffers 814.

[41] In some embodiments, the core die 802A may include memory cells located in a DRAM memory array 815, a command decoder 816, a data controller 818, and a delay adjust circuit 819A. Similarly, the core die 802B may include memory cells located in a DRAM memory array 815, a command decoder 816, and a data controller 818, and a delay adjust circuit 819B. The core die 802A and the core die 802B may operate on commands respectively, and thus may work independently of each other.

[42] According to the second embodiment, the delay adjust circuit 819A of the core die 802A and the delay adjust circuit 819B of the core die 802B are coupled in parallel to each other. In such an arrangement, a delay amount of the delay adjust circuit 819A may be different from a delay amount of the delay adjust circuit 819B, and the delay adjust circuits 819A and 819B may be configured to be different from each other.

[43] According to the second embodiment, the refresh timing of the channels may be different due to the delay adjust circuits 819 (such as the delay adjust circuit 819A and the delay adjust circuit 819B), and thus a peak current consumption of the associated semiconductor device may be reduced.

[44] FIG. 9 illustrates an example of a self refresh timing according to the first embodiment. The timing in FIG. 9 may be also referred according to other embodiments.

[45] As shown in FIG. 9, two self refresh operations to the core die 102A and the core die 102B can be performed at different timing values due to the delay adjust circuits 119A and 119B for example.

[46] According to the embodiments, two self oscillator signals SELF_OSC_A and SELF_OSC_B are commonly generated from one self oscillator signal SELF_OSC_IF and those two self oscillator signals SELF_OSC_A and SELF_OSC_B are triggered and activated to be high in different timing. Thus, simultaneous self-refresh operations of dice in stack can be prevented, and peak

current in a self-refresh operation of HMB can be mitigated and become lower than the second embodiment.

[47] FIG. 10 illustrates an example of a core die 102 according to the first embodiment. The configuration shown in FIG. 10 may be also referred according to other embodiments.

[48] As shown in FIG. 10, the core die 102 (e.g., the core die 102A as shown in FIG. 8) may include a command decoder 116, and a delay adjust circuit 119. When any channel is in a self-refresh mode, a self oscillator signal may be driven to the core die 102. The delay adjust circuit 119 in the core die 102 may change a self refresh timing in each channel of the core die 102.

[49] FIG. 11 illustrates an example of refresh waveforms in a core die 102 according to the first embodiment. The waveform in FIG. 11 may be also referred according to other embodiments.

[50] In FIG. 11, “self_en” represents a Self Refresh Entry signal, which may be provided by a GPU. “self_exit” represents a Self Refresh Exit signal, which may be provided by a GPU. “self_st” represents a Self Refresh State signal, which may go up from the “self_en” and go down from the “self_en”. “self_osc” represents a Self Refresh Oscillator signal. “ref_go” represents a Refresh Start signal. “soak” represents a signal that is generated from a rising edge of the “ref_go”. The “soak” signal may come from a memory array region, and may indicate that it is ok to finish the refresh operation. “ref_state” represents a Refresh Command (State) signal, which may go to a memory array region. The refresh operation may be started from a rising edge of the “ref_state”, and may be finished at a falling edge of the “ref_state”.

[51] FIG. 12 illustrates an example of a HBM 1200 according to a fourth embodiment. The explanations above may be applicable and/or identical at least in part to the fourth embodiment, and thus for simplicity, some common explanations are omitted. For example, the configurations shown above may be referred here according to the fourth embodiment.

[52] As shown in FIG. 12, the HBM 1200 may include an interface die 1201, and a stack of core dice 1202 (such as a core die 1202A and a core die 1202B), which are connected to each other by TSVs 1203.

[53] In some embodiments, the interface die 1201 may include bumps
5 (such as a bump_A and a bump_B), and internal circuits 1208. The internal circuits 1208 of the interface die 1201 may include a self refresh oscillator 1217, a delay adjust circuit 1219A, a delay adjust circuit 1219B, receivers 1210, transmitters 1211, transceivers 1212, logic 1213, and buffers 1214. The delay adjust circuit 1219A may receive a “self_osc” signal from the self-refresh oscillator 1217 for
10 example.

[54] Here, according to the fourth embodiment, a delay adjust circuit 1219A and a delay adjust circuit 1219B are located in the interface die 1201. In contrast, a delay adjust circuit 1219A and a delay adjust circuit 1219B are not located in the interface die 1201, and are located in core dice, respectively.

15 [55] According to the fourth embodiment, the delay adjust circuit 1219A may be coupled to the core die 1202A. The delay adjust circuit 1219B may be coupled between the delay adjust circuit 1219A and the core die 1202B, and thus the delay adjust circuit 1219B may be coupled in series with the delay adjust circuit 1219A. In such an arrangement, the circuit layout area in each core die (such as the
20 core die 1202A and the core die 1202B) may be reduced.

[56] In some embodiments, the core die 1202A may include memory cells located in a DRAM memory array 1215, a command decoder 1216, and a data controller 1218. Similarly, the core die 1202B may include memory cells located in a DRAM memory array 1215, a command decoder 1216, and a data controller 1218.
25 The core die 1202A and the core die 1202B may operate on command respectively, and thus may work independently of each other.

[57] FIG. 13 illustrates a fifth example of a HBM 1300 according to a fifth embodiment. The explanations above may be applicable and/or identical at least in part to the fifth embodiment, and thus for simplicity, some common

explanations are omitted. For example, the configurations shown above may be referred here according to the fifth embodiment.

[58] As shown in FIG. 13, the HBM 1300 may include an interface die 1301, and a stack of core dice 1302 (such as a core die 1302A and a core die 1302B), which are connected to each other by TSVs 1303.

[59] In some embodiments, the interface die 1301 may include bumps (such as a bump_A and a bump_B), and internal circuits 1308. The internal circuits 1308 of the interface die 1301 may include a self refresh oscillator 1317, a delay adjust circuit 1319A, a delay adjust circuit 1319B, receivers 1310, transmitters 1311, transceivers 1312, logic 1313, and buffers 1314.

[60] Here, according to the fourth embodiment, a delay adjust circuit 1319A and a delay adjust circuit 1319B are located in the interface die 1301. In contrast, a delay adjust circuit 1319A and a delay adjust circuit 1319B are not located in the interface die 1301, and are located in core dice, respectively.

[61] According to the fourth embodiment, the delay adjust circuit 1319A and the delay adjust circuit 1319B are coupled in parallel to each other, and may receive a "self_osc" signal from the self-refresh oscillator 1317 for example. The delay adjust circuit 1319A is coupled between the self refresh oscillator 1317 and the core die 1302A. The delay adjust circuit 1319B is coupled between the self-refresh oscillator 1317 and the core die 1302B.

[62] In some embodiments, the core die 1302A may include memory cells located in a DRAM memory array 1315, a command decoder 1316, and a data controller 1318. Similarly, the core die 1302B may include memory cells located in a DRAM memory array 1315, a command decoder 1316, and a data controller 1318. The core dice 1302A and 1302B may operate on command respectively, and thus may work independently of each other.

[63] In some embodiments, the delay adjust circuit 1319A of the interface die 1301 may be coupled to the DRAM memory array 1315 of the core die 1302A via elements (such as a transmitter 111 of the interface die 1301, a TSV 1303, a receiver 1310 of the core die 1302A, and logic 1313 of the core die 1302A in

series). Similarly, the delay adjust circuit 1319B of the interface die 1301 may be coupled to the DRAM memory array 1315 of the core die 1302B via elements (such as a transmitter 1311 of the interface die 1301, a TSV 1303, a receiver 1310 of the core die 1302A, and logic 1313 of the core die 1302A in series).

5 [64] In such an arrangement, an apparatus may only have one or more self refresh oscillators in an interface die, and the power consumption of the apparatus can be reduced.

[65] The Abstract of the Disclosure is provided to comply with 37 C.F.R.
10 §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure.
15 Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. An apparatus comprising:
an interface chip comprising an oscillator to produce an original clock signal;
5 a first memory chip comprising a first terminal to receive a first clock signal in response to the original clock signal, a second terminal to be supplied with a first control signal, and first memory cells subject to a first data refresh operation in response to the first clock signal when the first control single is active; and
a second memory chip comprising a third terminal to receive a second clock
10 signal in response to the original clock signal, a fourth terminal to be supplied with a second control signal, and second memory cells subject to a second data refresh operation in response to the second clock signal when the second control signal is active.
- 15 2. The apparatus of claim 1, wherein the second and fourth terminals are to independently receive the first and second control signals from the interface chip.
3. The apparatus of claim 1, wherein the first and second terminals are electrically coupled in series to the oscillator of the interface chip.
20
4. The apparatus of claim 1, wherein the first and second terminals are electrically coupled in parallel to the oscillator of the interface chip.
5. An apparatus comprising:
25 a chip stack structure comprising a first memory chip and a second memory chip stacked over one another; and
an interface chip coupled to the chip stack structure,
wherein the first memory chip comprises a first command decoder circuit, a first terminal to receive a first clock signal, a second terminal coupled to the first

command decoder circuit, and a plurality of first memory cells,

wherein the second memory chip comprises a second command decoder circuit, a third terminal to receive a second clock signal, a fourth terminal coupled to the second command decoder circuit, a fifth terminal, and a plurality of second
5 memory cells,

wherein the second terminal of the first memory chip is electrically coupled to the fifth terminal of the second memory chip, and

wherein the interface chip comprises sixth, seventh, and eighth terminals respectively electrically coupled to the third, fourth and fifth terminals of the second
10 memory chips.

6. The apparatus of claim 5, wherein the interface chip comprises an oscillator to produce an oscillation signal at the sixth terminal, and wherein the first terminal of the first chip is electrically coupled to the third terminal of the second chip.
15

7. The apparatus of claim 5, wherein the interface chip comprises a ninth terminal and an oscillator to respectively produce a first oscillation signal at the sixth terminal and a second oscillation signal at the ninth terminal, and wherein the second chip comprises a tenth terminal electrically coupled to the ninth terminal of
20 the interface chip and the first terminal of the first chip.

8. The apparatus of claim 6, wherein the first memory cells are refreshed in response to the first clock signal at the first terminal when the first command decoder circuit receives a first refresh command, and wherein the second memory
25 cells are refreshed in response to the second clock signal at the third terminal when the second command decoder circuit receives a second refresh command.

9. An apparatus comprising:
an interface chip comprising an oscillator to provide an oscillator signal;
30 a first memory chip on which a first refresh operation is performed in

response to a first refresh enable signal to be supplied at a first node and a first oscillator enable signal to be supplied at a second node; and

a second memory chip on which a second refresh operation is performed in response to a second refresh enable signal to be supplied at a third node and a
5 second oscillator enable signal to be supplied at a fourth node,

wherein the first and third nodes are to receive, from the interface chip, the first and second refresh enable signals independently of each other, and wherein the second and fourth nodes are to receive, based on the oscillator signal, the first and second oscillator enable signals in different timing values from each other.

10

10. The apparatus of claim 9,

wherein the first memory chip comprises a first delay circuit to delay the second oscillator enable signal to supply the first oscillator enable signal to the second node, and

15

wherein the second memory chip comprises a second delay circuit delay the oscillator signal to supply the second oscillator enable signal to the fourth node and the first delay circuit.

11. The apparatus of claim 10, wherein the first delay circuit and the second
20 delay circuit have a same delay amount.

12. The apparatus of claim 9,

wherein the first memory chip comprises a first delay circuit to delay the oscillator signal to supply the first oscillator enable signal to the second node,

25

and wherein the second memory chip comprises a second delay circuit to delay the oscillator signal to supply the second oscillator enable signal to the fourth node.

13. The apparatus of claim 12, wherein the first delay circuit and the second
30 delay circuit have different delay amounts from each other.

14. The apparatus of claim 9, wherein the interface chip comprises:
a first delay circuit to delay the second oscillator enable signal to supply the first oscillator enable signal to the second node, and
5 a second delay circuit to delay the oscillator signal to supply the second oscillator enable signal to the fourth node and the first delay circuit.
15. The apparatus of claim 14, wherein the first delay circuit and the second delay circuit have a same delay amount.
- 10 16. The apparatus of claim 9, wherein the interface chip comprises:
a first delay circuit to delay the oscillator signal to supply the first oscillator enable signal to the second node, and
a second delay circuit to delay the oscillator signal to supply the second
15 oscillator enable signal to the fourth node.
17. The apparatus of claim 16, wherein the first delay circuit and the second delay circuit have different delay amounts from each other.
- 20 18. The apparatus of claim 9, wherein the oscillator is activated in response to a reset signal supplied thereto.
19. The apparatus of claim 9, wherein the first and second memory chips are stacked over each other.

25

20. The apparatus of claim 9, wherein the first and second refresh operations are performed with different timing values from each other, when the first and third nodes receive the first and second refresh enable signals substantially simultaneously.

5

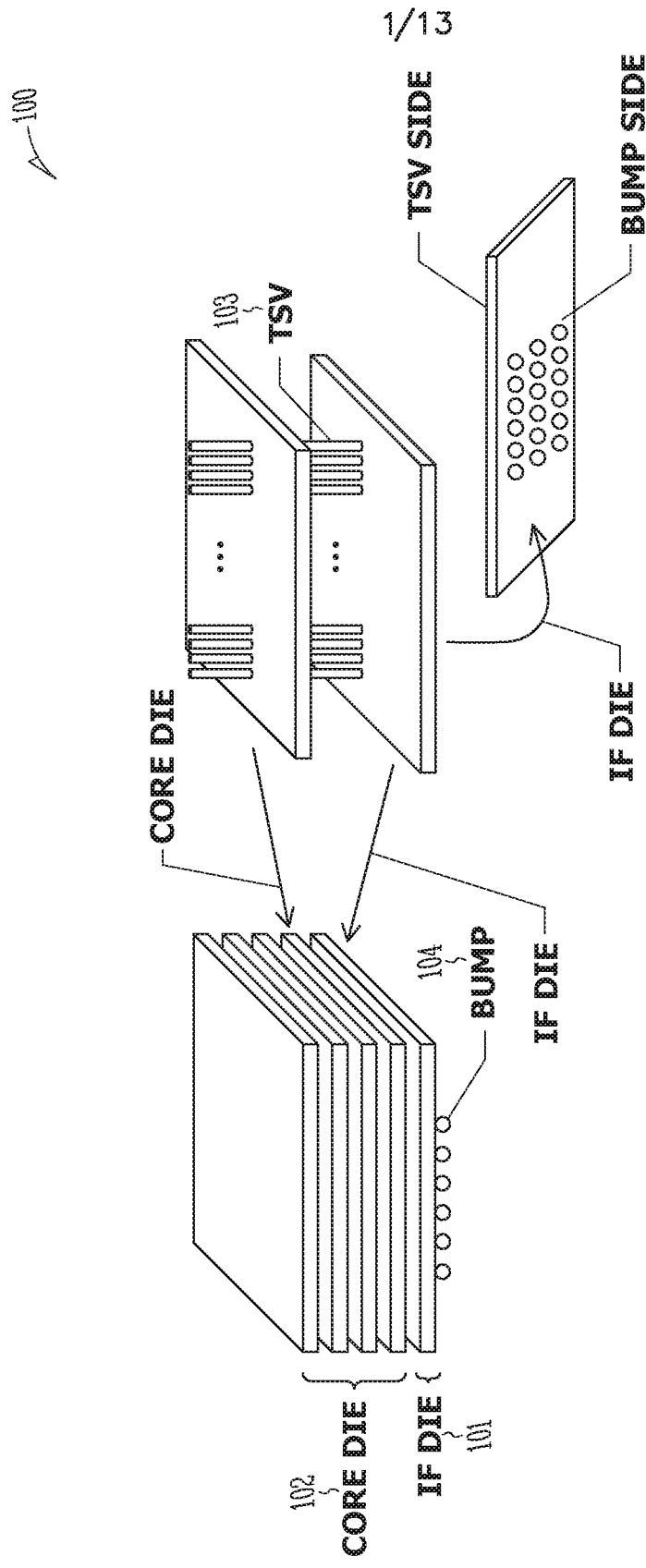


Fig. 1

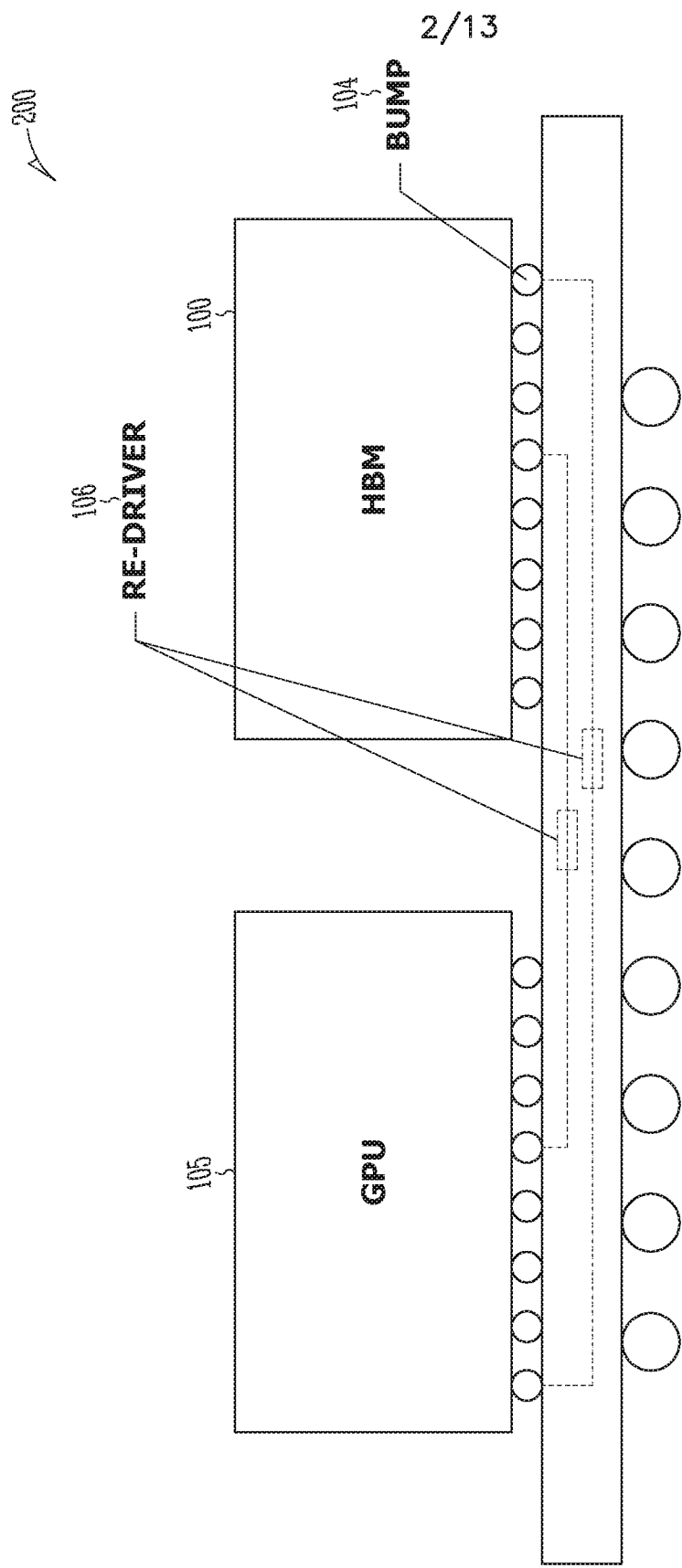
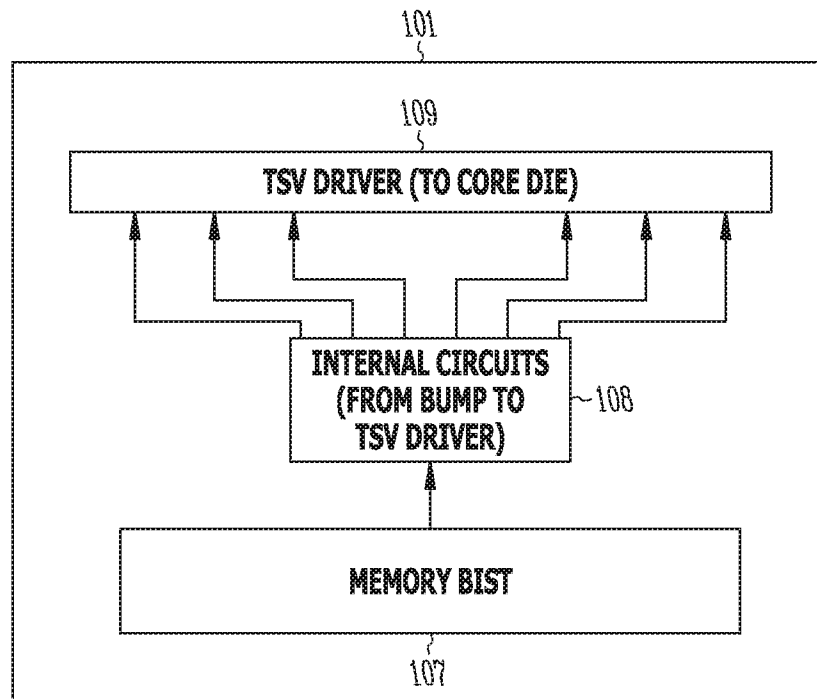


Fig. 2

3/13

*Fig. 3*

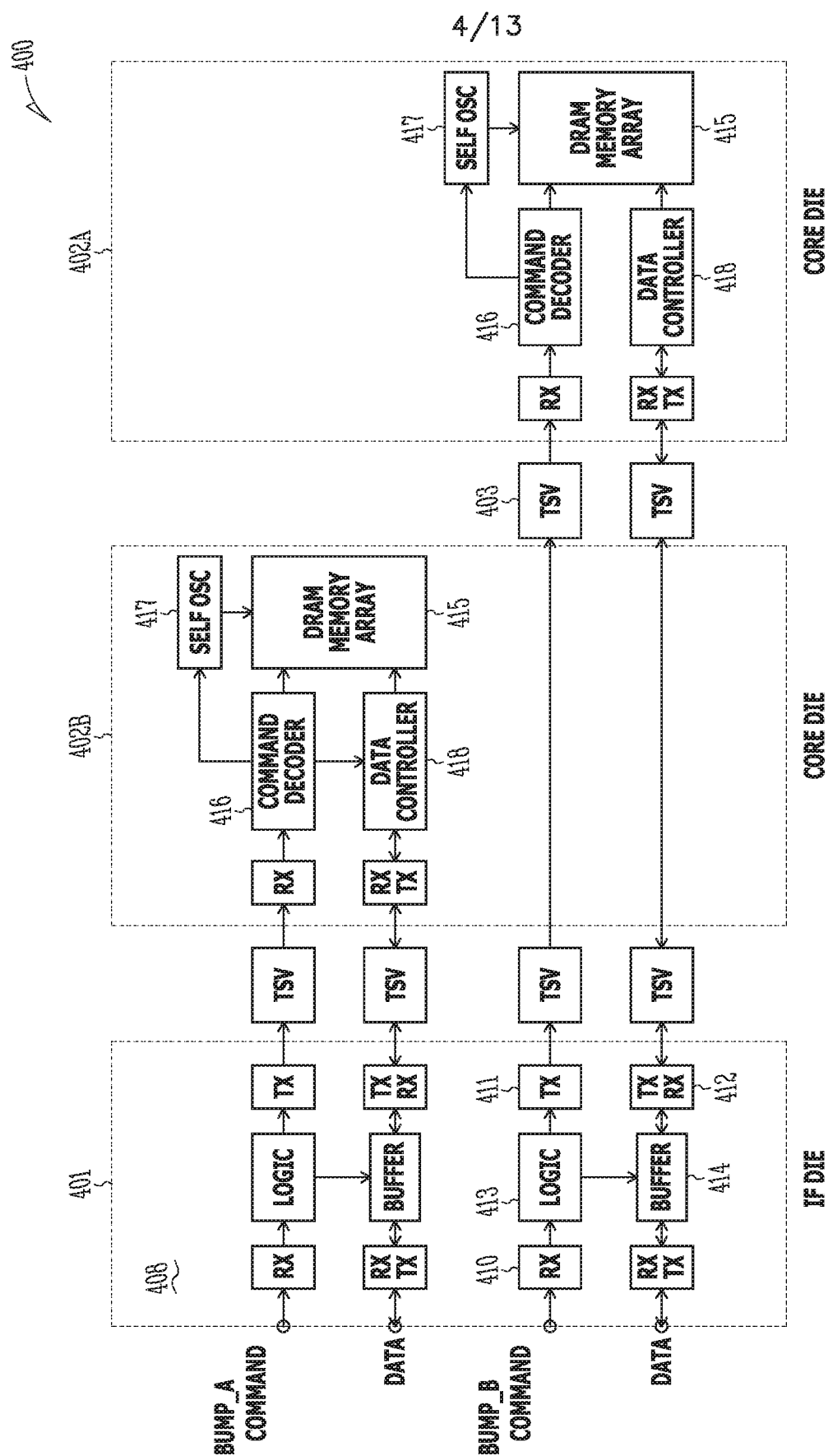


Fig. 4

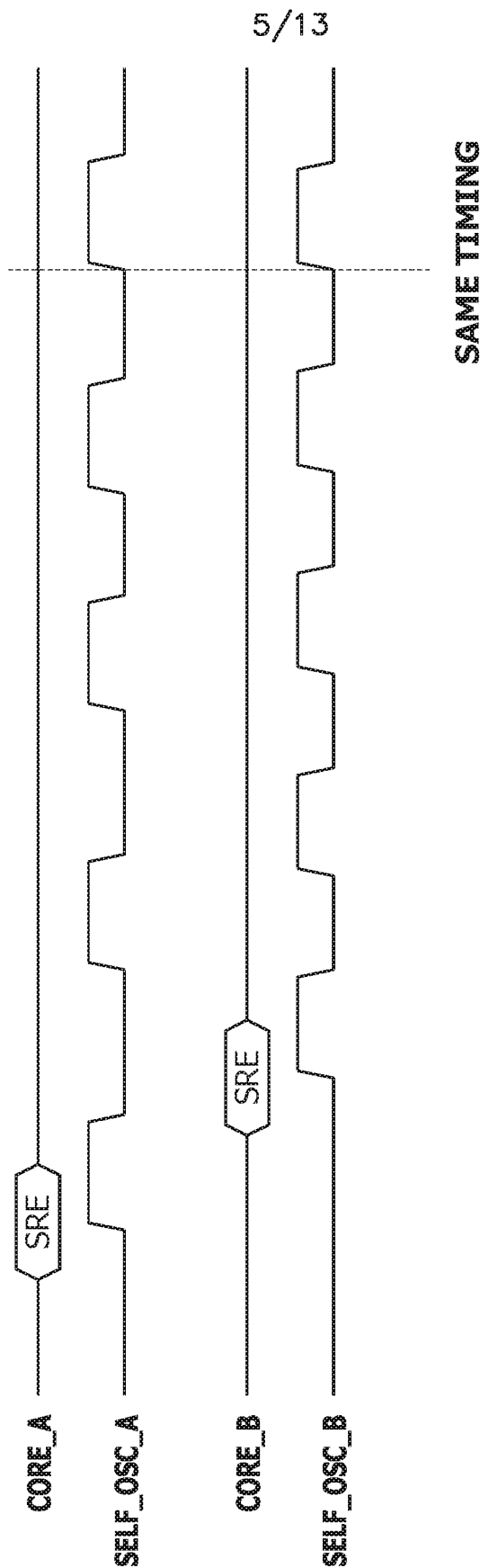


Fig. 5

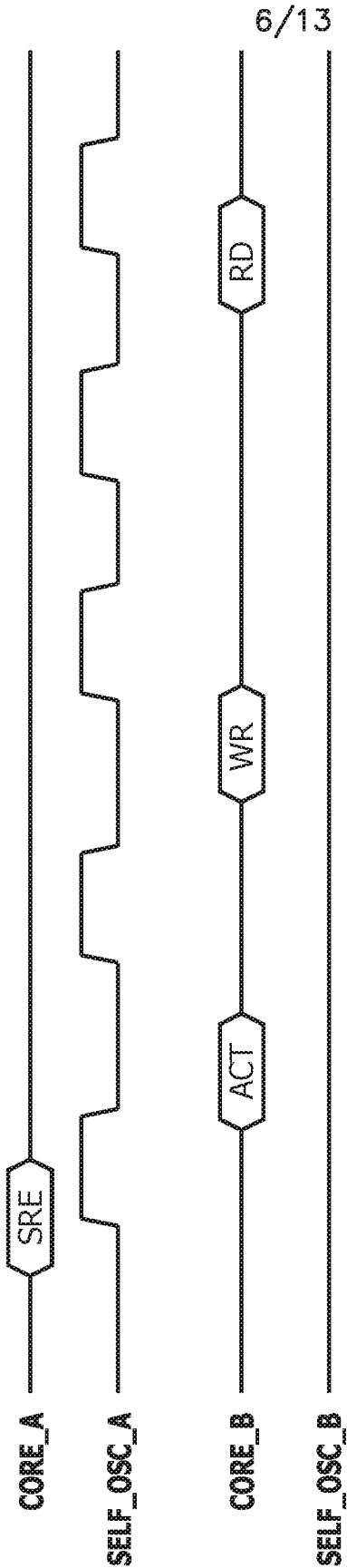


Fig. 6

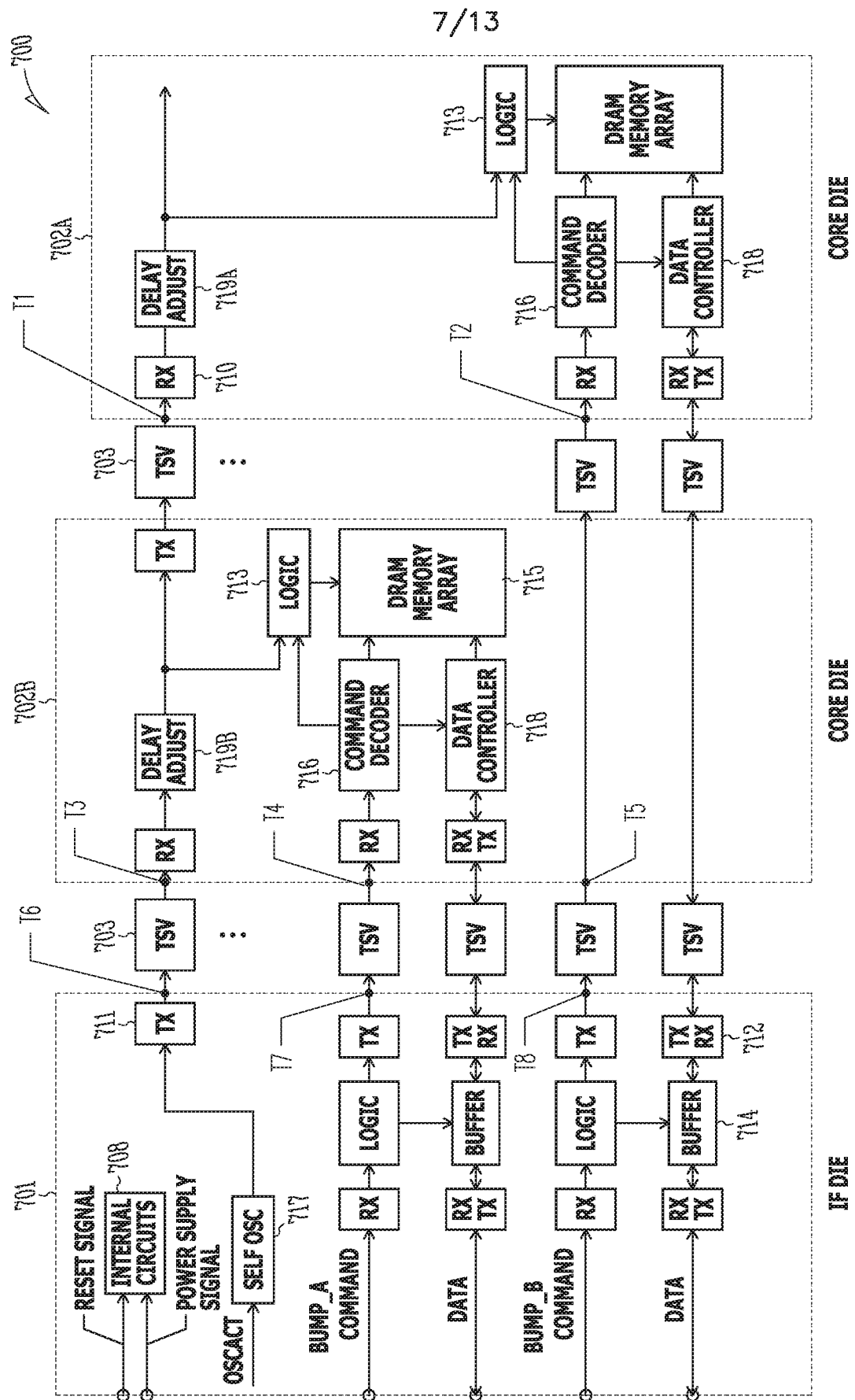


Fig. 7

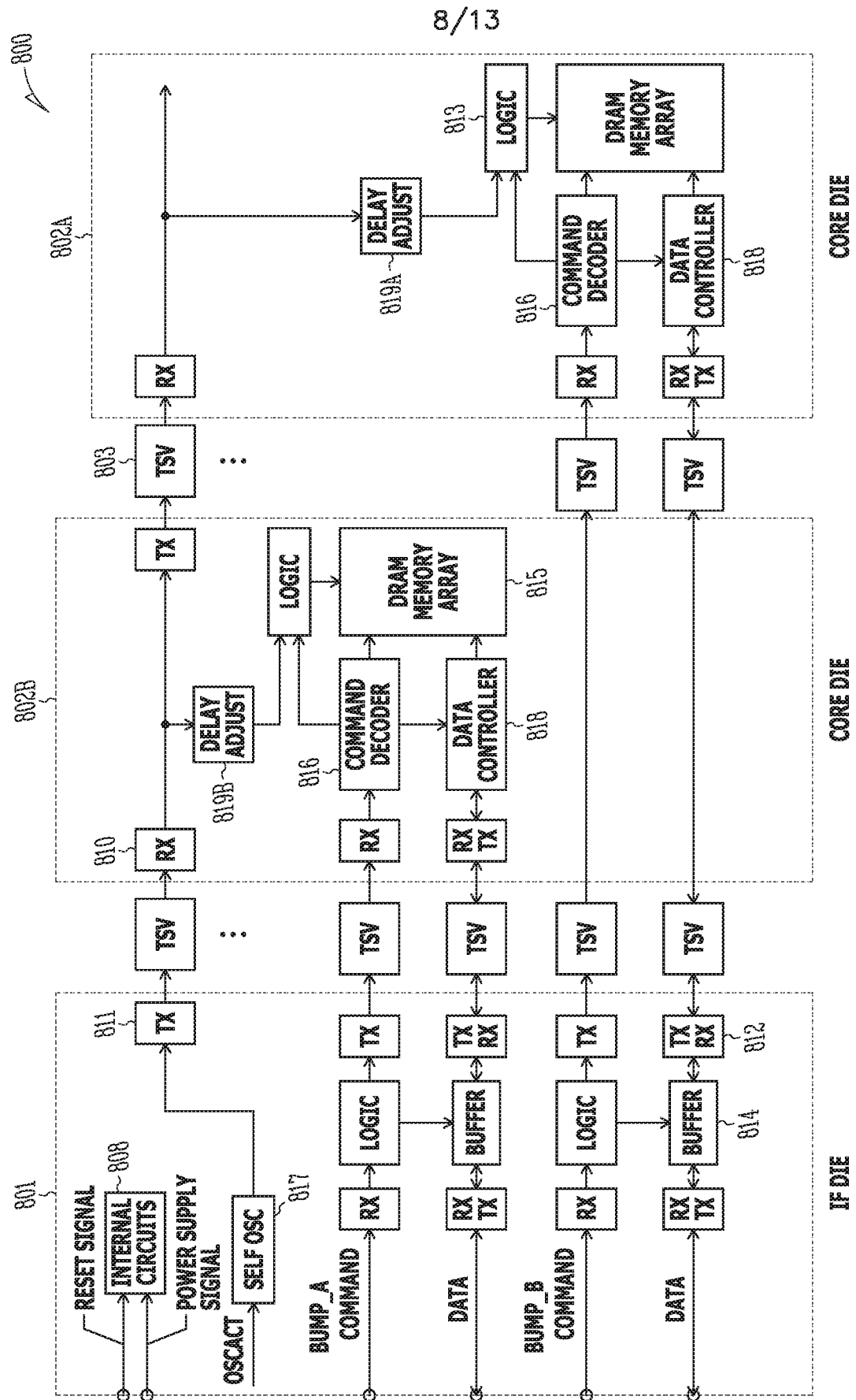


Fig. 8

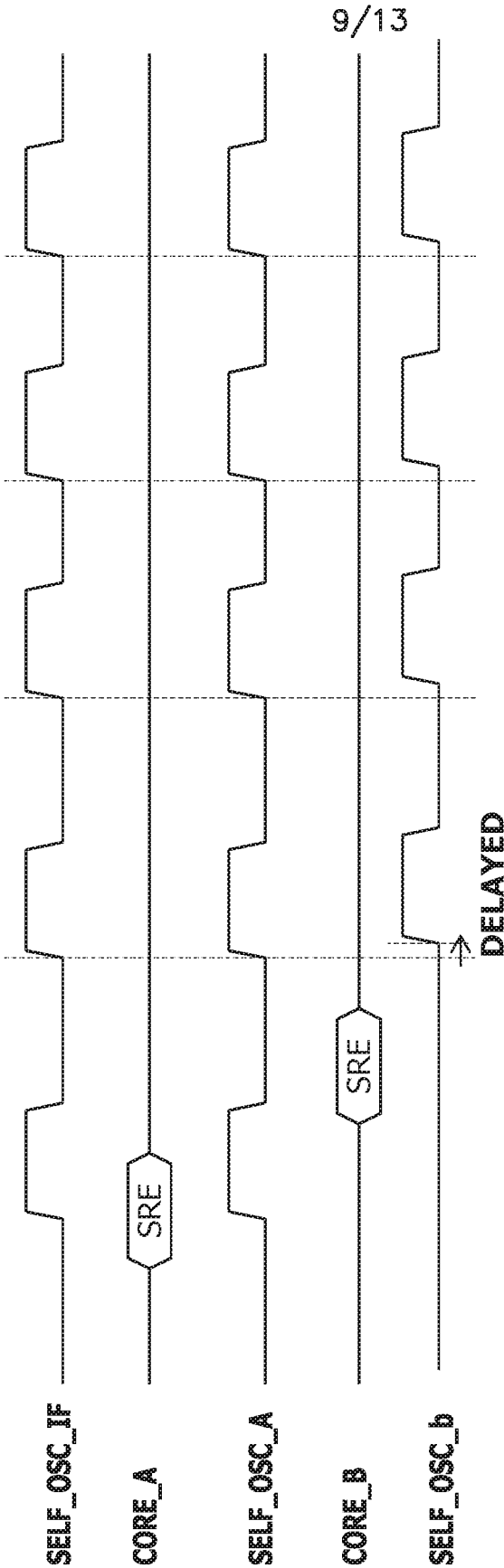


Fig. 9

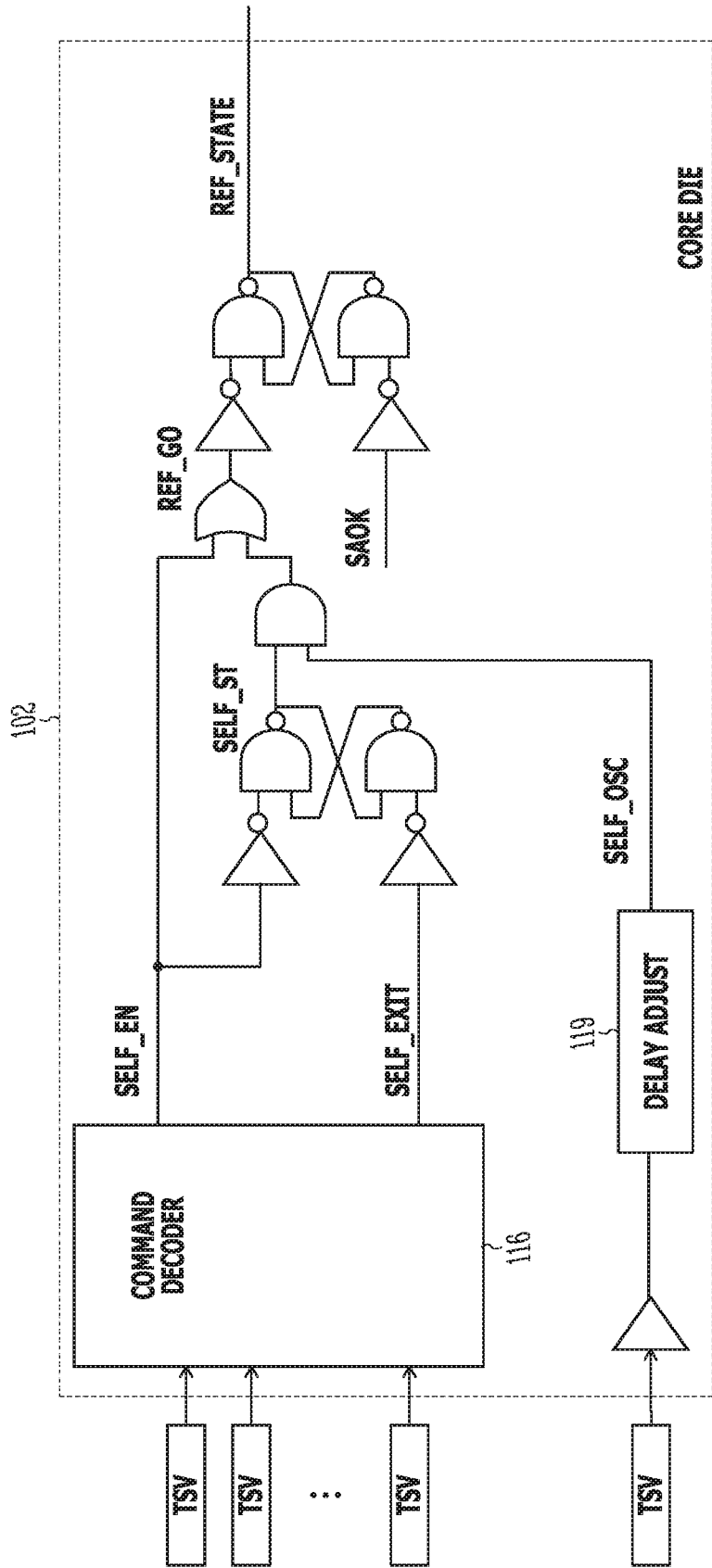


Fig. 10

11/13

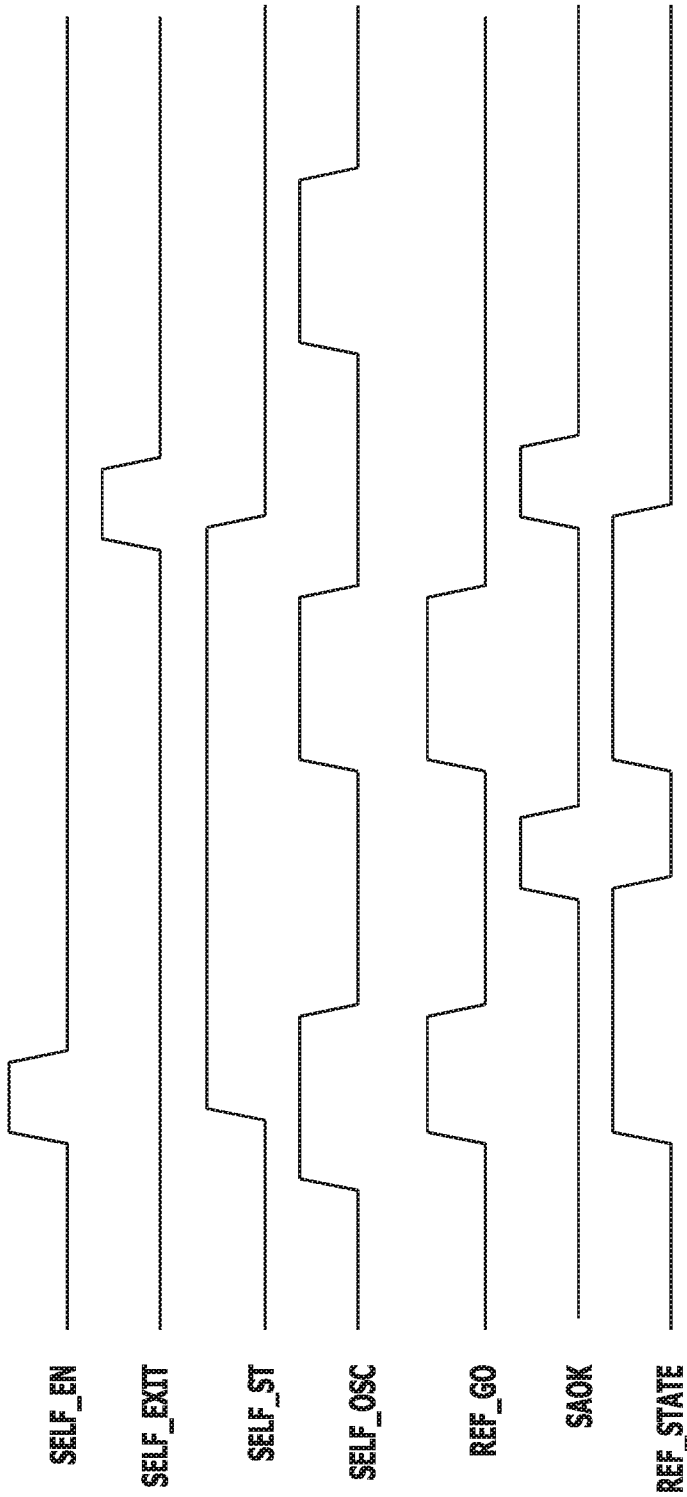


Fig. 11

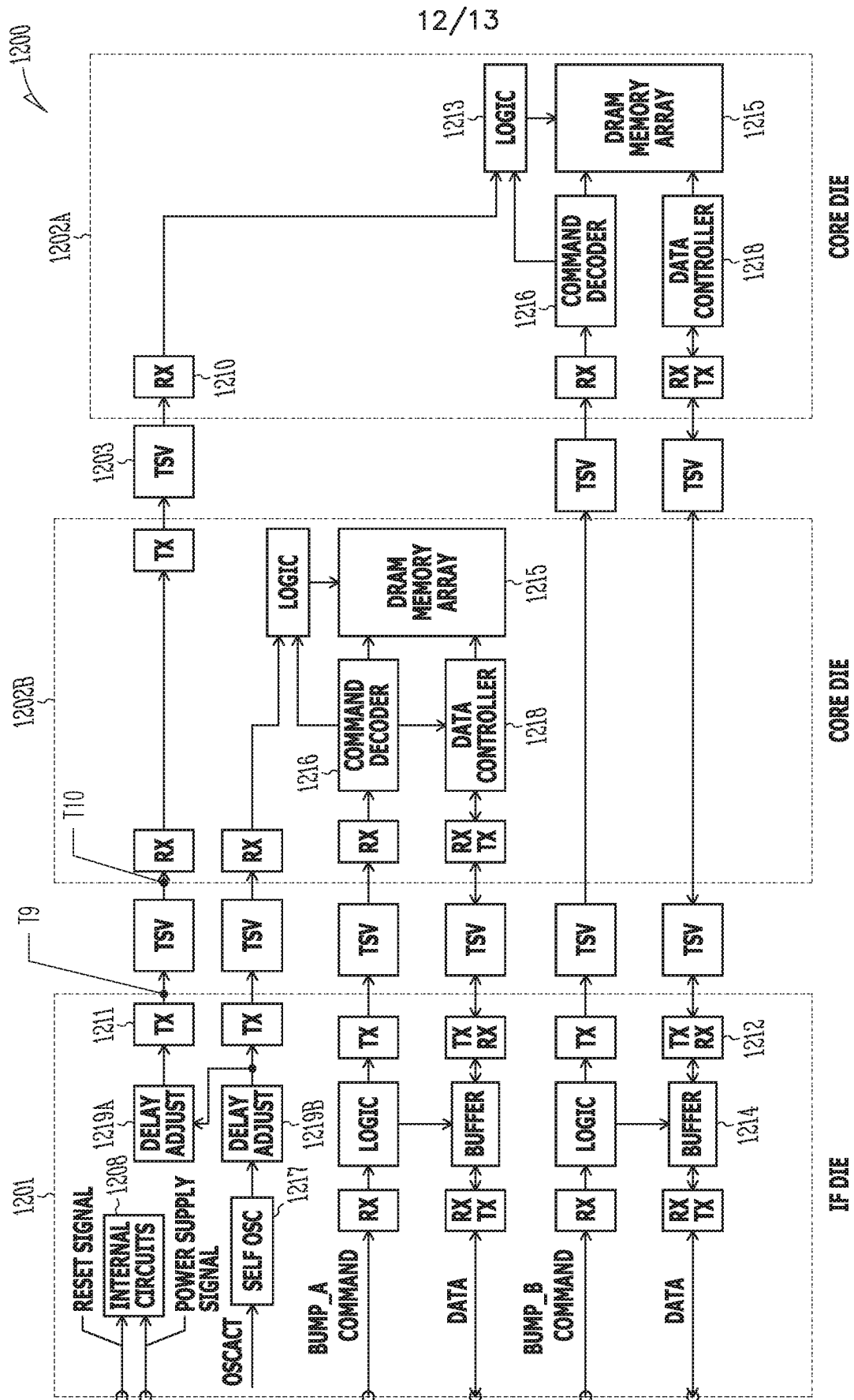


Fig. 12

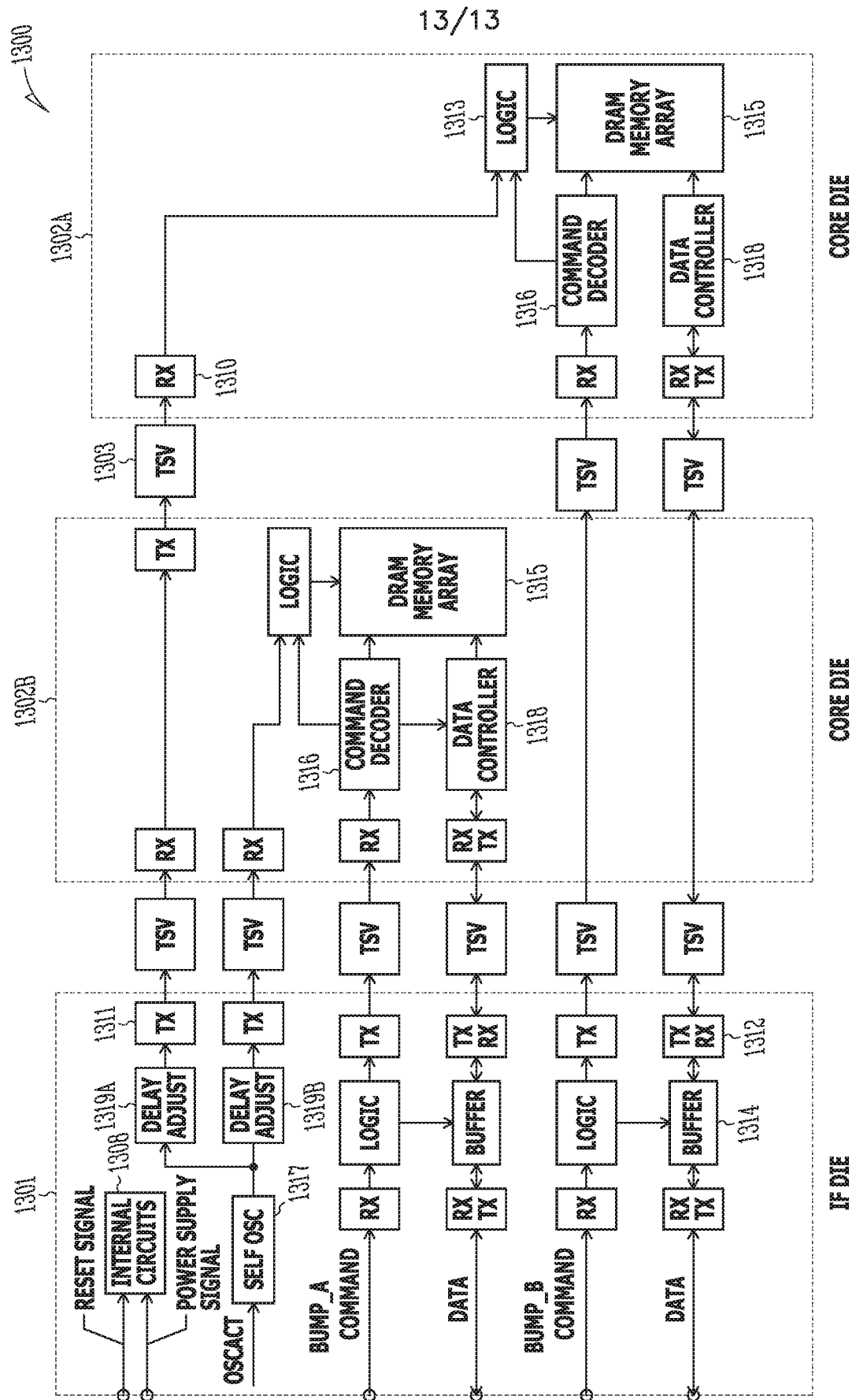


Fig. 13

A. CLASSIFICATION OF SUBJECT MATTER**G11C 11/406(2006.01)I, G11C 11/4076(2006.01)I, G11C 7/22(2006.01)I, G11C 5/06(2006.01)I**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/406; H01L 23/31; H01L 23/48; G06F 12/00; G06F 11/22; G11C 5/02; G11C 29/04; H01L 23/485; G11C 11/4076; G11C 7/22; G11C 5/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: interface, chip, oscillator, original, clock, signal, memory, chip, cell, data, refresh, operation, active, terminal, control

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0006699 A1 (KULJIT S. BAINS et al.) 02 January 2014 See paragraphs [0043]-[0045]; and figure 7.	5
A		1-4, 6-20
A	US 2011-0271158 A1 (JOSEPH M. JEDDELOH) 03 November 2011 See paragraphs [0011]-[0012]; and figure 1.	1-20
A	US 2014-0328104 A1 (SK HYNIX INC.) 06 November 2014 See paragraphs [0048]-[0055]; and figure 4.	1-20
A	US 2015-0001717 A1 (OMKAR G. KARHADE et al.) 01 January 2015 See paragraphs [0051]-[0052]; and figure 14.	1-20
A	US 2014-0327150 A1 (DEOK-YOUNG JUNG et al.) 06 November 2014 See paragraph [0191]; and figure 38.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

08 August 2016 (08.08.2016)

Date of mailing of the international search report

08 August 2016 (08.08.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, EUN KYU

Telephone No. +82-42-481-3580



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/032912

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0006699 A1	02/01/2014	DE 112013003219 T5 TW 201418981 A TW I493338 B US 9202551 B2 WO 2014-004010 A1	30/04/2015 16/05/2014 21/07/2015 01/12/2015 03/01/2014
US 2011-0271158 A1	03/11/2011	US 2009-300444 A1 US 7979757 B2 US 8799726 B2	03/12/2009 12/07/2011 05/08/2014
US 2014-0328104 A1	06/11/2014	KR 10-2014-0131623 A US 8953394 B2	14/11/2014 10/02/2015
US 2015-0001717 A1	01/01/2015	CN 104253115 A DE 102014108992 A1 KR 10-2015-0002518 A	31/12/2014 31/12/2014 07/01/2015
US 2014-0327150 A1	06/11/2014	KR 10-2014-0018745 A KR 10-2016-0011154 A US 2014-0038353 A1 US 2015-0132950 A1 US 8802495 B2 US 8963336 B2 US 9064941 B2	13/02/2014 29/01/2016 06/02/2014 14/05/2015 12/08/2014 24/02/2015 23/06/2015