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*[Continued on next page]*

(54) **Title**: ON-CHIP DUAL-SUPPLY MULTI-MODE CMOS REGULATORS

(57) **Abstract**: A method, an apparatus, and a computer program product are provided. The apparatus may be a regulator circuit. The regulator circuit includes a first voltage regulator to regulate a first input voltage to the first voltage regulator, the first voltage regulator including a P-type metal-oxide-semiconductor (PMOS), and a second voltage regulator to regulate a second input voltage to the second voltage regulator, the second voltage regulator including an N-type metal-oxide-semiconductor (NMOS). In an aspect, the first voltage regulator is coupled to the second voltage regulator.

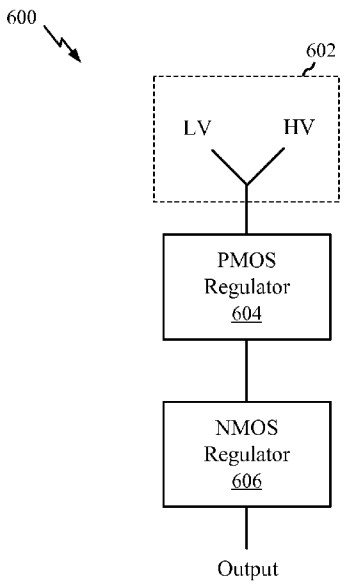


FIG. 6A

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# ON-CHIP DUAL-SUPPLY MULTI-MODE CMOS REGULATORS

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Serial No. 62/005,765, entitled "ON-CHIP DUAL-SUPPLY MULTI-MODE CMOS REGULATORS" and filed on May 30, 2014, and U.S. Patent Application No. 14/630,506, entitled "ON-CHIP DUAL-SUPPLY MULTI-MODE CMOS REGULATORS" and filed on February 24, 2015, which are expressly incorporated by reference herein in their entirety.

## BACKGROUND

### Field

[0002] The present disclosure relates generally to communication systems, and more particularly, to a voltage regulator for a voltage controlled oscillator (VCO).

### Background

[0003] A wireless device (e.g., a cellular phone or a smart phone) may transmit and receive data for two-way communication with a wireless communication system. The wireless device may include a transmitter for data transmission and a receiver for data reception. For data transmission, the transmitter may modulate a transmit local oscillator (LO) signal with data to obtain a modulated radio frequency (RF) signal, amplify the modulated RF signal to obtain an output RF signal having the desired output power level, and transmit the output RF signal via an antenna to a base station. For data reception, the receiver may obtain a received RF signal via the antenna, amplify and downconvert the received RF signal with a receive LO signal, and process the downconverted signal to recover data sent by the base station.

[0004] The wireless device may include one or more oscillators to generate one or more oscillator signals at one or more desired frequencies. The oscillator signal(s) may be used to generate the transmit LO signal for the transmitter and the receive LO signal for the receiver. The oscillator(s) may be required to generate the oscillator signal(s) to meet the requirements of the wireless communication system with which the wireless device communicates.

[0005] A VCO is used to generate the transmit LO signal and the receive LO signal. A VCO is generally connected to a regulator that provides an input voltage to the

VCO. The performance of the VCO may depend on the regulator. Therefore, an effective regulator for the VCO is desired for optimal performance and low noise.

## SUMMARY

[0006] In an aspect of the disclosure, a method and an apparatus are provided. The apparatus may be a regulator circuit. The regulator circuit includes a first voltage regulator to regulate a first input voltage to the first voltage regulator, the first voltage regulator including a P-type metal-oxide-semiconductor (PMOS), and a second voltage regulator to regulate a second input voltage to the second voltage regulator, the second voltage regulator including an N-type metal-oxide-semiconductor (NMOS). In an aspect, the first voltage regulator is coupled to the second voltage regulator. In an aspect, the regulator circuit may further include a switch circuit to selectively activate at least one of the first voltage regulator or the second voltage regulator. In an aspect, the first voltage regulator and the second voltage regulator are connected in series. In an aspect, the first voltage regulator and the second voltage regulator are connected in parallel. In an aspect, the first voltage regulator includes a two-stage amplifier circuit to amplify the first input voltage in two stages. In an aspect, the second voltage regulator circuit includes a-two-stage amplifier circuit to amplify the second input voltage in two stages. In an aspect, the second voltage regulator includes a pole-cancelation circuit. In an aspect, the second voltage regulator includes a capacitor and a resistor, and wherein one end of the resistor is connected to the capacitor and another end of the resistor is connected to a source of the NMOS. In an aspect, the first voltage regulator and the second voltage regulator are tunable to change a degree of input voltage regulation.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 illustrates a wireless device communicating with different wireless communication systems.

[0008] FIG. 2 is a block diagram of a wireless device.

[0009] FIG. 3 is an example circuit diagram of an NMOS regulator according to the disclosure.

[0010] FIG. 4A is an example PSSR plot of PSSR values in various cases at a regulator.

[0011] FIG. 4B is an example noise plot of noise values in various cases.

[0012] FIG. 5 is an example implementation circuit of an NMOS regulator according to the disclosure.

[0013] FIGs. 6A-6B are example structures of a CMOS regulator.

[0014] FIG. 7 is an example circuit diagram including a cascode CMOS regulator.

[0015] FIG. 8 is an example circuit diagram including a buffer circuit.

[0016] FIG. 9 is an example circuit structure at a system level according to the disclosure.

[0017] FIG. 10A is an example PSSR plot of PSSR values in various cases at a VCO.

[0018] FIG. 10B is an example noise plot of noise values in various cases at a VCO.

[0019] FIG. 11 is a flow chart of a method by a regulator circuit.

[0020] FIG. 12 is a conceptual data flow diagram illustrating the data flow between different modules/means/components in an exemplary apparatus.

[0021] FIG. 13 is a diagram illustrating an example of a hardware implementation for an apparatus employing a processing system.

## DETAILED DESCRIPTION

[0022] The detailed description set forth below in connection with the appended drawings is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well known structures and components are shown in block diagram form in order to avoid obscuring such concepts. The term "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other designs.

[0023] Several aspects of telecommunication systems will now be presented with reference to various apparatus and methods. These apparatus and methods will be described in the following detailed description and illustrated in the accompanying drawings by various blocks, modules, components, circuits, steps, processes, algorithms, etc. (collectively referred to as "elements"). These elements may be implemented using electronic hardware, computer software, or any combination thereof. Whether such elements are implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0024] By way of example, an element, or any portion of an element, or any combination of elements may be implemented with a "processing system" that includes one or more processors. Examples of processors include microprocessors, microcontrollers, digital signal processors (DSPs), field programmable gate arrays (FPGAs), programmable logic devices (PLDs), state machines, gated logic, discrete hardware circuits, and other suitable hardware configured to perform the various functionality described throughout this disclosure. One or more processors in the processing system may execute software. Software shall be construed broadly to mean instructions, instruction sets, code, code segments, program code, programs, subprograms, software modules, applications, software applications, software packages, routines, subroutines, objects, executables, threads of execution, procedures, functions, etc., whether referred to as software, firmware, middleware, microcode, hardware description language, or otherwise.

[0025] Accordingly, in one or more exemplary embodiments, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or encoded as one or more instructions or code on a computer-readable medium. Computer-readable media includes computer storage media. Storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise random-access memory (RAM), read-only memory (ROM), electronically erasable programmable ROM (EEPROM), compact disk (CD) ROM (CD-ROM), or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc, as used herein, includes CD, laser disc, optical disc, digital versatile disc (DVD), and floppy disk where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0026] FIG. 1 is a diagram 100 illustrating a wireless device 110 communicating with different wireless communication systems 120, 122. The wireless communication systems 120, 122 may each be a Code Division Multiple Access (CDMA) system, a Global System for Mobile Communications (GSM) system, a Long Term Evolution (LTE) system, a wireless local area network (WLAN) system, or some other

wireless system. A CDMA system may implement Wideband CDMA (WCDMA), CDMA 1X or cdma2000, Time Division Synchronous Code Division Multiple Access (TD-SCDMA), or some other version of CDMA. TD-SCDMA is also referred to as Universal Terrestrial Radio Access (UTRA) Time Division Duplex (TDD) 1.28 Mcps Option or Low Chip Rate (LCR). LTE supports both frequency division duplexing (FDD) and time division duplexing (TDD). For example, the wireless communication system 120 may be a GSM system, and the wireless communication system 122 may be a WCDMA system. As another example, the wireless communication system 120 may be an LTE system, and the wireless communication system 122 may be a CDMA system.

**[0027]** For simplicity, the diagram 100 shows the wireless communication system 120 including one base station 130 and one system controller 140, and the wireless communication system 122 including one base station 132 and one system controller 142. In general, each wireless system may include any number of base stations and any set of network entities. Each base station may support communication for wireless devices within the coverage of the base station. The base stations may also be referred to as a Node B, an evolved Node B (eNB), an access point, a base transceiver station, a radio base station, a radio transceiver, a transceiver function, a basic service set (BSS), an extended service set (ESS), or some other suitable terminology. The wireless device 110 may also be referred to as a user equipment (UE), a mobile device, a remote device, a wireless device, a wireless communications device, a station, a mobile station, a subscriber station, a mobile subscriber station, a terminal, a mobile terminal, a remote terminal, a wireless terminal, an access terminal, a client, a mobile client, a mobile unit, a subscriber unit, a wireless unit, a remote unit, a handset, a user agent, or some other suitable terminology. The wireless device 110 may be a cellular phone, a smartphone, a tablet, a wireless modem, a personal digital assistant (PDA), a handheld device, a laptop computer, a smartbook, a netbook, a cordless phone, a wireless local loop (WLL) station, or some other similar functioning device.

**[0028]** The wireless device 110 may be capable of communicating with the wireless communication system 120 and/or 122. The wireless device 110 may also be capable of receiving signals from broadcast stations, such as the broadcast station 134. The wireless device 110 may also be capable of receiving signals from satellites, such as the satellite 150, in one or more global navigation satellite systems

(GNSS). The wireless device 110 may support one or more radio technologies for wireless communication such as GSM, WCDMA, cdma2000, LTE, 802.11, etc. The terms "radio technology," "radio access technology," "air interface," and "standard" may be used interchangeably.

**[0029]** The wireless device 110 may communicate with a base station in a wireless system via the downlink and the uplink. The downlink (or forward link) refers to the communication link from the base station to the wireless device, and the uplink (or reverse link) refers to the communication link from the wireless device to the base station. A wireless system may utilize TDD and/or FDD. For TDD, the downlink and the uplink share the same frequency, and downlink transmissions and uplink transmissions may be sent on the same frequency in different time periods. For FDD, the downlink and the uplink are allocated separate frequencies. Downlink transmissions may be sent on one frequency, and uplink transmissions may be sent on another frequency. Some exemplary radio technologies supporting TDD include GSM, LTE, and TD-SCDMA. Some exemplary radio technologies supporting FDD include WCDMA, cdma2000, and LTE. The wireless device 110 and/or the base stations 130, 132 may include an exemplary VCO regulator 160. A VCO regulator 160 is provided *infra*.

**[0030]** FIG. 2 is a block diagram 200 of an exemplary wireless device, such as the wireless device 110. The wireless device includes a data processor / controller 210, a transceiver 218, and an antenna 290. The data processor / controller 210 may be referred to as a processing system. A processing system may include the data processor / controller 210 or both the data processor / controller 210 and the memory 216. The transceiver 218 includes a transmitter 220 and a receiver 250 that support bi-directional communication. The transmitter 220 and/or the receiver 250 may be implemented with a super-heterodyne architecture or a direct-conversion architecture. In the super-heterodyne architecture, a signal is frequency converted between RF and baseband in multiple stages, e.g., from RF to an intermediate frequency (IF) in one stage, and then from IF to baseband in another stage for a receiver. In the direct-conversion architecture, which is also referred to as a zero-IF architecture, a signal is frequency converted between RF and baseband in one stage. The super-heterodyne and direct-conversion architectures may use different circuit blocks and/or have different requirements. In the exemplary design shown in FIG.

2, the transmitter 220 and the receiver 250 are implemented with the direct-conversion architecture.

[0031] In the transmit path, the data processor / controller 210 may process (e.g., encode and modulate) data to be transmitted and provide the data to a digital-to-analog converter (DAC) 230. The DAC 230 converts a digital input signal to an analog output signal. The analog output signal is provided to a transmit (TX) baseband (lowpass) filter 232, which may filter the analog output signal to remove images caused by the prior digital-to-analog conversion by the DAC 230. An amplifier (amp) 234 may amplify the signal from the TX baseband filter 232 and provide an amplified baseband signal. An upconverter (mixer) 236 may receive the amplified baseband signal and a TX LO signal from a TX LO signal generator 276. The upconverter 236 may upconvert the amplified baseband signal with the TX LO signal and provide an upconverted signal. A filter 238 may filter the upconverted signal to remove images caused by the frequency upconversion. A power amplifier (PA) 240 may amplify the filtered RF signal from the filter 238 to obtain the desired output power level and provide an output RF signal. The output RF signal may be routed through a duplexer/switchplexer 264.

[0032] For FDD, the transmitter 220 and the receiver 250 may be coupled to the duplexer 264, which may include a TX filter for the transmitter 220 and a receive (RX) filter for the receiver 250. The TX filter may filter the output RF signal to pass signal components in a transmit band and attenuate signal components in a receive band. For TDD, the transmitter 220 and the receiver 250 may be coupled to switchplexer 264. The switchplexer 264 may pass the output RF signal from the transmitter 220 to the antenna 290 during uplink time intervals. For both FDD and TDD, the duplexer/switchplexer 264 may provide the output RF signal to the antenna 290 for transmission via a wireless channel.

[0033] In the receive path, the antenna 290 may receive signals transmitted by base stations and/or other transmitter stations and may provide a received RF signal. The received RF signal may be routed through duplexer/switchplexer 264. For FDD, the RX filter within the duplexer 264 may filter the received RF signal to pass signal components in a receive band and attenuate signal components in the transmit band. For TDD, the switchplexer 264 may pass the received RF signal from the antenna 290 to the receiver 250 during downlink time intervals. For both FDD and TDD,

the duplexer/switchplexer 264 may provide the received RF signal to the receiver 250.

[0034] Within the receiver 250, the received RF signal may be amplified by a low noise amplifier (LNA) 252 and filtered by a filter 254 to obtain an input RF signal. A downconverter (mixer) 256 may receive the input RF signal and an RX LO signal from an RX LO signal generator 286. The downconverter 256 may downconvert the input RF signal with the RX LO signal and provide a downconverted signal. The downconverted signal may be amplified by an amplifier 258 and further filtered by an RX baseband (lowpass) filter 260 to obtain an analog input signal. The analog input signal is provided to an analog-to-digital converter (ADC) 262. The ADC 262 converts an analog input signal to a digital output signal. The digital output signal is provided to the data processor / controller 210.

[0035] A TX frequency synthesizer 270 may include a TX phase locked loop (PLL) 272 and a VCO 274. The VCO 274 may generate a TX VCO signal at a desired frequency. The TX PLL 272 may receive timing information from the data processor / controller 210 and generate a control signal for the VCO 274. The control signal may adjust the frequency and/or the phase of the VCO 274 to obtain the desired frequency for the TX VCO signal. The TX frequency synthesizer 270 provides the TX VCO signal to the TX LO signal generator 276. The TX LO signal generator may generate a TX LO signal based on the TX VCO signal received from the TX frequency synthesizer 270.

[0036] A RX frequency synthesizer 280 may include an RX PLL 282 and a VCO 284. The VCO 284 may generate an RX VCO signal at a desired frequency. The RX PLL 282 may receive timing information from the data processor / controller 210 and generate a control signal for the VCO 284. The control signal may adjust the frequency and/or the phase of the VCO 284 to obtain the desired frequency for the RX VCO signal. The RX frequency synthesizer 280 provides the RX VCO signal to the RX LO signal generator 286. The RX LO signal generator may generate an RX LO signal based on the RX VCO signal received from the RX frequency synthesizer 280.

[0037] The LO signal generators 276, 286 may each include frequency dividers, buffers, etc. The LO signal generators 276, 286 may be referred to as frequency dividers if they divide a frequency provided by the TX frequency synthesizer 270 and the RX frequency synthesizer 280, respectively. The PLLs 272, 282 may each include a

phase/frequency detector, a loop filter, a charge pump, a frequency divider, etc. Each VCO signal and each LO signal may be a periodic signal with a particular fundamental frequency. The TX LO signal and the RX LO signal from the LO signal generators 276, 286 may have the same frequency for TDD or different frequencies for FDD. The TX VCO signal and the RX VCO signal from the VCOs 274, 284 may have the same frequency (e.g., for TDD) or different frequencies (e.g., for FDD or TDD).

**[0038]** The conditioning of the signals in the transmitter 220 and the receiver 250 may be performed by one or more stages of amplifier, filter, upconverter, downconverter, etc. These circuits may be arranged differently from the configuration shown in FIG. 2. Furthermore, other circuits not shown in FIG. 2 may also be used to condition the signals in the transmitter 220 and the receiver 250. For example, impedance matching circuits may be located at the output of the PA 240, at the input of the LNA 252, between the antenna 290 and the duplexer/switchplexer 264, etc. Some circuits in FIG. 2 may also be omitted. For example, the filter 238 and/or the filter 254 may be omitted. All or a portion of the transceiver 218 may be implemented on one or more analog integrated circuits (ICs), RF ICs (RFICs), mixed-signal ICs, etc. For example, the TX baseband filter 232 to the PA 240 in the transmitter 220, the LNA 252 to the RX baseband filter 260 in the receiver 250, the PLLs 272, 282, the VCOs 274, 284, and the LO signal generators 276, 286 may be implemented on an RFIC. The PA 240 and possibly other circuits may also be implemented on a separate IC or a circuit module.

**[0039]** The data processor / controller 210 may perform various functions for the wireless device. For example, the data processor / controller 210 may perform processing for data being transmitted via the transmitter 220 and received via the receiver 250. The data processor / controller 210 may control the operation of various circuits within the transmitter 220 and the receiver 250. The memory 212 and/or the memory 216 may store program codes and data for the data processor / controller 210. The memory may be internal to the data processor / controller 210 (e.g., the memory 212) or external to the data processor / controller 210 (e.g., the memory 216). The memory may be referred to as a computer-readable medium. An oscillator 214 may generate a VCO signal at a particular frequency. A clock generator 215 may receive the VCO signal from the oscillator 214 and may generate clock signals for various modules within the data processor / controller 210. The data processor / controller

210 may be implemented on one or more application specific integrated circuits (ASICs) and/or other ICs.

[0040] Frequency dividers, such as the frequency dividers in LO signal generators 276, 286, are used extensively for generating LO signals. There is a need for a programmable frequency divider for generating LO signals in multi-band cellular transceivers that meets stringent LO requirements such as small chip area, good phase noise requirement, and quadrature output.

[0041] A VCO (e.g., VCO 274 or VCO 284 of FIG. 2) is sensitive to noise spikes and spurs. Thus, a power management integrated circuit (PMIC) is generally used for the VCO to address such an issue. Based on a PMIC noise/spur profile, a power supply rejection ratio (PSRR) of at least 40dB at 1MHz is generally desired. For example, a spur (e.g., a spike) of noise is observed between 100kHz and 1MHz in the PMIC noise/spur profile. Thus, there is a demand for an effective VCO regulator that is capable of providing a good bandwidth (e.g., a wide bandwidth) and attenuating the spur (e.g., the large spike) for the VCO. It is noted that, although a wider PSRR bandwidth may provide improved performance of a VCO regulator, increasing the PSRR bandwidth may also cause the noise bandwidth to increase. Therefore, there is a trade-off between increasing the PSRR bandwidth and increasing noise bandwidth that is not desirable.

[0042] For a VCO to obtain desired power/phase noise conditions, the VCO may implement a VCO regulator with a dual supply configuration to supply voltage. The dual supply configuration may alleviate supply/electromagnetic pulling of the VCO. For example, the dual voltage supply configuration may supply high voltage (HV) for a GSM mode and may supply low voltage (LV) for a non-GSM mode (e.g., for CDMA, LTE, etc.). For an LV non-GSM mode, a specific LV PSRR for low voltage is a concern for satisfactory performance of a VCO regulator because the voltage supplied to the VCO regulator is low in the LV non-GSM mode. For example, in the LV non-GSM mode supplying low voltage, to mitigate PMIC pulse-frequency modulation (PFM) spurs, a VCO regulator should provide an LV PSRR of approximately 100dB in several hundreds KHz to MHz range with dropout voltage of less than 100mV. Example simulation results illustrate that for the LV non-GSM mode, a PSRR of approximately 100dB is desired at 100KHz to mitigate the PMIC PFM spurs. For an HV GSM mode, good noise performance is a concern for satisfactory performance of a VCO regulator because a high voltage supplied to

the VCO regulator may increase the noise bandwidth. For example, in the HV GSM mode supplying high voltage, the VCO regulator provides a certain PSRR at a frequency of several tens of MHz range, while maintaining low noise for the high voltage.

**[0043]** It is desired that a VCO regulator be programmable (e.g., tunable) to satisfy various PSRR/noise specifications and to adapt to the tradeoff between the PSRR and the noise. For example, the VCO regulator should be programmable to provide different PSRR and noise characteristics for different uses. Thus, for example, the VCO regulator should be programmable to provide different PSRR and noise characteristics depending on whether the mode is the LV mode or the HV mode.

**[0044]** It is noted that performance of the VCO regulator is related to a type of a pass element (e.g., DC bias, input/output impedance). In general, an N-type metal-oxide-semiconductor (NMOS) regulator is limited by a DC bias condition and a P-type metal-oxide-semiconductor (PMOS) regulator has a worse PSRR than the NMOS regulator. Table 1 illustrates comparison between an NMOS regulator and a PMOS regulator. In Table 1, a number of plus signs (+) represents a degree of desirable performance, and a number of minus signs (-) represents a degree of undesirable performance.

| Regulator type | **PSRR @low freq.** | **PSRR @high freq.** | **Rin @low freq** | **Rin @high freq** | Area | Noise |
|---|---|---|---|---|---|---|
| NMOS 1VDD | + + | + + | + + | + | - | + |
| NMOS 2VDD | + | + + | + + | + | - | + |
| PMOS 1VDD | + + | - - | + | - | + + | - |
| PMOS 2VDD | - | - - | + | - | + + | - |

Table 1: Comparison between an NMOS regulator and a PMOS regulator

**[0045]** The NMOS regulator according to the disclosure implements a two-stage operational transconductance amplifier (OTA) circuit to obtain a desirable PSRR (e.g., 100dB). The two-stage OTA circuit may limit the bandwidth to obtain 100dB at 100kHz via a compensation network. The compensation network in the two-stage OTA circuit also provides pole cancellation. FIG. 3 is an example circuit diagram 300 of an NMOS regulator according to the disclosure. The NMOS regulator 300 includes an NMOS 302. The NMOS 302 has a source (S), a drain (D), and a gate (G). The NMOS regulator 300 includes a first amplifier 304 and a second amplifier 306 to provide a two-stage OTA circuit. The second amplifier 306 may be a

common source amplifier. For example, a PSSR of 60-70 dB may be achieved in the first stage through the first amplifier 304, and a PSSR of 30-40dB may be achieved in the second stage through the second amplifier 306, thereby achieving a total PSSR of approximately 100dB for the two-stage OTA circuit. An output of the first amplifier 304 is connected to an input of the second amplifier 306, and the output of the second amplifier 306 is connected to the gate (G) of the NMOS 302. The output of the first amplifier 304 is also connected to a capacitor 308 with capacitance CM at a first end of the capacitor 308. A second end of the capacitor 308 is connected to a first end of a resistor 310 with resistance RM. A second end of the resistor 310 is connected to the source (S) of the NMOS 302 and a VCO 350. The VCO 350 may be equivalent to the VCO 274 or the VCO 284 of FIG. 2.

**[0046]** The capacitor 308 and the resistor 310 form a compensation network to compensate the regulator output 312 to the output of the first stage OTA circuit including the first amplifier 304. The capacitor 308 and the resistor 310 may be matched with transconductance (Gm) of the first stage OTA circuit. For example, the compensation network including the capacitor 308 and the resistor 310 may be tunable to match with the Gm of the first stage OTA circuit for stability and to minimize noise. It is noted that both the compensation network and the first stage OTA circuit are tunable to match with each other. Because at least one of the compensation network or the first stage OTA circuit is tunable, the regulator can maintain good stability, good regulator bandwidth, and lower noise. It is noted that, if the first stage OTA Gm is larger, the compensation network provides a stronger compensation, and thus provides better stability.

**[0047]** The following equations provide computation of the PSRR according to the example illustrated in FIG. 3. $A_{path}$ is a gain through $A_{path}$ shown in FIG. 3. $s$ is $j\omega$. $A$ is a DC gain from a supply to the regulator output 312. $A2$ is a DC gain at the second amplifier 306. $ro1$ is output resistance of the first amplifier 304. $\omega_{p1}$ is a pole at the output of the first amplifier 304, $\omega_{p2}$ is a pole at the output of the second amplifier 306, and $\omega_{p3}$ is a pole at the output 312 of the NMOS regulator. $\omega_z$ is a zero generated by the compensation network with the resistor 310 and the capacitor 308. $A_{LP}$ is an open loop DC gain from the input of first amplifier 304 to the regulator output 312.

$$A_{path} \approx \frac{A\left(1+\frac{s}{\omega_z}\right)}{1+\frac{s}{\omega_{p1}}}, \quad \omega_{p1} = \frac{1}{A2 \cdot CM \cdot ro1}, \omega_z = \frac{1}{CM \cdot ro1} \tag{1}$$

$$LoopGain \approx \frac{A_{LP}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \tag{2}$$

$$PSRR \approx \frac{A_{path}}{1+LoopGain} = \frac{\frac{A\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)}}{1+\frac{A_{LP}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)}}$$

$$= \frac{A\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{p2}}\right)}{A_{LP}+\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \tag{3}$$

**[0048]** FIG. 4A is an example PSSR plot 400 of PSSR values in various cases at a regulator. The PSSR plot 400 illustrates that the pole cancellation (PC) 2-stage OTA regulator circuit provides a PSSR plot that is closer to the desirable PSSR of -100 dB than the PSSR plots of a 1-stage OTA regulator and a conventional 2-stage OTA regulator. Thus, the pole cancellation provided by the 2-stage OTA regulator circuit of the disclosure (e.g., via the NMOS regulator of FIG. 3) helps extend the bandwidth of the PSSR. The more power the 2-stage OTA regular circuit provides, the wider the PSSR bandwidth is. FIG. 4B is an example noise plot 450 of noise values in various cases. According to the example noise plot 450, the noise plot of the PC 2-stage OTA regulator circuit is similar to the noise plots of a 1-stage OTA regulator and a conventional 2-stage OTA regulator, except for a portion 452. The portion 452 of the example noise plot 450 is zoomed to a zoomed portion 454. The zoomed portion 454 indicates that both the PC 2-stage OTA regulator circuit and the

conventional 2-stage OTA regular circuit experience slightly higher noise than the 1-stage OTA regular circuit.

[0049] FIG. 5 is an example implementation circuit 500 of the NMOS regulator according to the disclosure. The NMOS regulator 500 includes a two-stage OTA circuit 502 including two OTAs and a compensation network including a resistor and a capacitor. In an aspect, the two-stage OTA circuit 502 may be equivalent to the two-stage OTA circuit including the first amplifier 304 and the second amplifier 306 in FIG. 3. In an aspect, the compensation network 504 may be equivalent to the compensation network including the capacitor 308 and the resistor 310 in FIG. 3. The compensation network 504 may be tunable to match with a first stage OTA circuit of the two-stage OTA circuit 502.

[0050] According to the disclosure, a regulator circuit may be a complementary metal–oxide–semiconductor (CMOS) regulator circuit that includes a PMOS regulator and an NMOS regulator, where the NMOS regulator is coupled to the PMOS regulator. In one aspect, the PMOS regulator may be connected to the NMOS regulator in series (in cascode). In another aspect, the PMOS regulator may be connected to the NMOS regulator in parallel. The regulator circuit may be connected to a switch circuit to selectively choose an HV mode or an LV mode for the CMOS regulator circuit. In general, for the VCO, the HV mode may be used for better performance in terms of less pulling effect and better phase noise performance. However, the HV mode may cause higher power consumption. The LV mode generally causes lower power consumption than the HV mode. It is noted that the VCO is less sensitive to electromagnetic (EM) coupling in the HV mode. In one aspect, the switch circuit may select the HV mode for the PMOS regulator and bypass the NMOS regulator. In another aspect, for the LV mode, the switch circuit may select either the NMOS regulator and bypass the PMOS regulator, or may select both the PMOS regulator and the NMOS regulator. In addition, it is noted that the PMOS regulator and the NMOS regulator have different input impedance and output impedance. The PMOs regulator generally has lower input impedance and higher output impedance than the NMOS regulator. Thus, in one aspect, the switch circuit may be used to select either the PMOS regulator or the NMOS regulator, depending on whether the VCO is an aggressor or a victim to surrounding building blocks. For example, the switch circuit may select the PMOS regulator if the VCO is an aggressor that may affect the surrounding building blocks (e.g., by pulling the surrounding building blocks). For

example, the switch circuit may select the NMOS regulator if the VCO is a victim that may be affected by the surrounding building blocks (e.g., by being pulled by the surrounding building blocks). It is further noted that selecting both the PMOS regulator and the NMOS regulator that are connected in series would also provide isolation from affecting and/or being affected from the surrounding building blocks.

**[0051]** FIGs. 6A-6B are example structures of a CMOS regulator. FIG. 6A is an example structure 600 of a CMOS regulator where a PMOS regulator 604 and an NMOS regulator 606 are connected in series. In particular, a switch circuit 602 is connected to the PMOS regulator 604 that is connected to the NMOS regulator 606 in series. The switch circuit 602 is configured to select one of an LV mode and an HV mode. As discussed *supra*, for example, the LV mode is used to supply low voltage for a non-GSM mode, and the HV mode is used to supply high voltage for a GSM mode. Although not shown, in another example, the order of the PMOS regulator 604 and the NMOS regulator 606 may be different from the example structure 600 of FIG. 6A. The CMOS regulator includes a PMOS regulator and an NMOS regulator. FIG. 6B is an example structure 650 of a CMOS regulator where a PMOS regulator 654 and an NMOS regulator 658 are connected in parallel. In particular, a first switch circuit 652 is connected to the PMOS regulator 654 and a second switch circuit 656 is connected to the NMOS regulator 658, where the PMOS regulator 654 and the NMOS regulator 658 are connected in parallel. As discussed *supra*, for example, the LV mode is used to supply low voltage for a non-GSM mode, and the HV mode is used to supply high voltage for a GSM mode. Thus, if the LV mode is used, both the first switch circuit 652 and the second switch circuit 656 are configured to provide low voltage. If the HV mode is used, both the first switch circuit 652 and the second switch circuit 656 are configured to provide high voltage.

**[0052]** FIG. 7 is an example circuit diagram 700 including a cascode CMOS regulator. In particular, a switch circuit 710 is connected to a CMOS regulator that includes a PMOS regulator 730 and an NMOS regulator 750, where the PMOS regulator 730 and the NMOS regulator 750 are connected in series (cascode). The CMOS regulator is connected to a VCO circuit 770 via the NMOS regulator 750. The VCO circuit 770 may be equivalent to the VCO 274 or the VCO 284 of FIG. 2. The VCO circuit 770 may have a low frequency (LF) VCO output at 772 and a high frequency (HF) VCO output at 774. In an aspect, the switch circuit 710 may selectively supply either a voltage of an HV mode or a voltage of an LV mode for

the CMOS regulator. In the example of FIG. 7, the switch circuit 710 may supply the HV mode voltage of 1.6V or the LV mode voltage of 0.95V to the CMOS regulator. The switch circuit 710 may selectively supply either a voltage of the HV mode or a voltage of the LV mode depending on various factors such as following. The HV mode may provide better VCO phase noise and swing as well as better VCO buffer phase noise and swing than the LV mode. The LV mode may cause lower power consumption than the HV mode. The supply voltage domain of the voltage supplied to the CMOS regulator may be configured to experience less supply coupling. It is also noted that the VCO is less sensitive to EM coupling in the HV mode than in the LV mode.

**[0053]** In an aspect, the NMOS regulator 750 has a better PSRR at 100MHz than the PMOS regulator 730. In an aspect, the PMOS regulator 730 may have better noise performance (e.g., lower noise) at 100MHz (e.g., in GSM, HV and low PMOS regulator BW) than the NMOS regulator 750. In the example of FIG. 7, the PMOS regulator 730 can output Vdd=-50mV. In the example of FIG. 7, the NMOS regulator 750 can achieve a PSRR of 100dB at 1MHz with 100mV drop-out. For example, the NMOS regulator 750 has a two-stage OTA and pole cancellation features to achieve a PSRR of 100dB at 1MHz for PFM spurs.

**[0054]** FIG. 8 is an example circuit diagram 800 including a buffer circuit. In the example circuit diagram 800, a switch circuit 810 is connected to a buffer circuit 830. In an aspect, the switch circuit 810 may selectively provide either an HV mode or an LV mode. The buffer circuit 830 receives outputs from the VCO, such as the VCO circuit 770 of FIG. 7, and buffers the outputs. Thus, the buffer circuit 830 may be connected to the VCO circuit 770 of FIG. 7. For example, the LF VCO input 832 into the buffer circuit 830 may be from the LF VCO output 772 of FIG. 7, and the HF VCO input 834 into the buffer circuit 830 may be from the HF VCO output 774 of FIG. 7.

**[0055]** FIG. 9 is an example circuit structure 900 at a system level according to the disclosure. The example circuit structure 900 includes a transmission (TX) VCO regulator 902, a first reception (RX) carrier aggregation (CA) regulator 904, and a second RX CA regulator 906. The first RX CA regulator 904 is for receiving carrier aggregation at a first frequency, and the second RX CA regulator 906 is for receiving carrier aggregation at a second frequency. Each one of the TX VCO regulator 902, the first RX CA regulator 904, and the second RX CA regulator 906

includes a CMOS regulator structure having a PMOS regulator coupled to an NMOS regulator.

**[0056]** FIG. 10A is an example PSSR plot 1000 of PSSR values in various cases at a VCO. The PSSR plot 1000 illustrates that a 2-stage OTA regulator circuit provides a PSSR plot for the VCO that is closer to the desirable PSSR of -100 dB than the PSSR plots of a 1-stage OTA regulator. Thus, the PSRR of 100 dB at 100kHZ is achieved by the 2-stage OTA regulator. Further, according to FIG. 10A, the VCO may also experience 50 dB improvement when the 2-stage OTA regulator is used. FIG. 10B is an example noise plot 1050 of noise values in various cases at a VCO. According to the example noise plot 1050, the noise plot of the 1-stage OTA regulator has spurs 1052 and 1054, whereas the noise plot of a 2-stage OTA regulator does not have spurs. Thus, the VCO experiences spur reduction when the 2-stage OTA regulator is used. In addition, if the VCO VDD switches to a high-supply domain, 4-5 dB reference side band (RSB) improvement may be provided.

**[0057]** FIG. 11 is a flow chart 1100 of a method by a regulator circuit. The method may be performed by a regulator circuit (e.g., the regulator circuit 600, 650, the apparatus 1202/1202'). At 1102, the regulator circuit regulates, via a first voltage regulator, a first input voltage to the first voltage regulator, the first voltage regulator including a PMOS. At 1104, the regulator circuit regulates, via a second voltage regulator, a second input voltage to the second voltage regulator, the second voltage regulator including an NMOS, where the first voltage regulator is connected to the second voltage regulator. At 1106, the regulator circuit selectively activates, via a switch circuit, at least one of the first voltage regulator or the second voltage regulator. In an aspect, the at least one of the first voltage regulator or the second voltage regulator is selectively activated based on noise.

**[0058]** FIG. 12 is a conceptual data flow diagram 1200 illustrating the data flow between different modules/means/components in an exemplary apparatus 1202. The apparatus may be a regulator circuit. The apparatus includes a first voltage regulator module 1204, a second voltage regulator module 1206, and a switching module 1208.

**[0059]** The first voltage regulator module 1204 regulates a first input voltage to the first voltage regulator module 1204. In an aspect, the first voltage regulator module 1204 includes a PMOS. The second voltage regulator module 1206 regulates a second input voltage to the second voltage regulator module 1206. In an aspect, the second

voltage regulator module 1206 includes an NMOS. In an aspect, the first voltage regulator is connected to the second voltage regulator. The switching module 1208 selectively activates at least one of the first voltage regulator module 1204 or the second voltage regulator module 1206. In an aspect, the at least one of the first voltage regulator module 1204 or the second voltage regulator 1206 is selectively activated based on noise.

**[0060]** The apparatus may include additional modules that perform each of the blocks of the algorithm in the aforementioned flow charts of FIG. 11. As such, each block in the aforementioned flow charts of FIG. 11 may be performed by a module and the apparatus may include one or more of those modules. The modules may be one or more hardware components specifically configured to carry out the stated processes/algorithm, implemented by a processor configured to perform the stated processes/algorithm, stored within a computer-readable medium for implementation by a processor, or some combination thereof.

**[0061]** FIG. 13 is a diagram 1300 illustrating an example of a hardware implementation for an apparatus 1202' employing a processing system 1314. The processing system 1314 may be implemented with a bus architecture, represented generally by the bus 1324. The bus 1324 may include any number of interconnecting buses and bridges depending on the specific application of the processing system 1314 and the overall design constraints. The bus 1324 links together various circuits including one or more processors and/or hardware modules, represented by the processor 1304, the modules 1204, 1206, 1208, and the computer-readable medium / memory 1306. The bus 1324 may also link various other circuits such as timing sources, peripherals, voltage regulators, and power management circuits, which are well known in the art, and therefore, will not be described any further.

**[0062]** The processing system 1314 may be coupled to a transceiver 1310. The transceiver 1310 is coupled to one or more antennas 1320. The transceiver 1310 provides a means for communicating with various other apparatus over a transmission medium. The transceiver 1310 receives a signal from the one or more antennas 1320, extracts information from the received signal, and provides the extracted information to the processing system 1314. In addition, the transceiver 1310 receives information from the processing system 1314, and based on the received information, generates a signal to be applied to the one or more antennas 1320. The processing system 1314 includes a processor 1304 coupled to a computer-readable medium / memory

1306. The processor 1304 is responsible for general processing, including the execution of software stored on the computer-readable medium / memory 1306. The software, when executed by the processor 1304, causes the processing system 1314 to perform the various functions described *supra* for any particular apparatus. The computer-readable medium / memory 1306 may also be used for storing data that is manipulated by the processor 1304 when executing software. The processing system further includes at least one of the modules 1204, 1206, and 1208. The modules may be software modules running in the processor 1304, resident/stored in the computer readable medium / memory 1306, one or more hardware modules coupled to the processor 1304, or some combination thereof.

**[0063]** In one configuration, the apparatus 1202/1202' includes means for regulating a first input voltage to the means for regulating the first input voltage, the means for regulating the first input voltage including a PMOS, means for regulating a second input voltage to the means for regulating the second voltage, the means for regulating the second voltage including an NMOS, where the means for regulating the first input voltage is connected to the means for regulating the second voltage, and means for selectively activating at least one of the means for regulating the first input voltage or the means for regulating the second voltage. In an aspect, the means for selectively activating is configured to selectively activate at least one of the means for regulating the first input voltage or the means for regulating the second voltage based on noise. The aforementioned means may be one or more of the aforementioned modules of the apparatus 1202 and/or the processing system 1314 of the apparatus 1202' configured to perform the functions recited by the aforementioned means.

**[0064]** It is understood that the specific order or hierarchy of steps in the processes disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged. Further, some steps may be combined or omitted. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

**[0065]** The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be

limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more." Unless specifically stated otherwise, the term "some" refers to one or more. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase "means for."

## CLAIMS

**WHAT IS CLAIMED IS:**

1. A regulator circuit, comprising:

a first voltage regulator to regulate a first input voltage to the first voltage regulator, the first voltage regulator including a P-type metal-oxide-semiconductor (PMOS);

a second voltage regulator to regulate a second input voltage to the second voltage regulator, the second voltage regulator including an N-type metal-oxide-semiconductor (NMOS), wherein the first voltage regulator is connected to the second voltage regulator; and

a switch circuit to selectively activate at least one of the first voltage regulator or the second voltage regulator.

2. The regulator circuit of claim 1, wherein the switch circuit selectively activates at least one of the first voltage regulator or the second voltage regulator based on noise.

3. The regulator circuit of claim 1, wherein the first voltage regulator and the second voltage regulator are connected in series.

4. The regulator circuit of claim 1, wherein the first voltage regulator and the second voltage regulator are connected in parallel.

5. The regulator circuit of claim 1, wherein the first voltage regulator includes a two-stage amplifier circuit to amplify the first input voltage in two stages.

6. The regulator circuit of claim 1, wherein the second voltage regulator includes a-two-stage amplifier circuit to amplify the second input voltage in two stages.

7. The regulator circuit of claim 1, wherein the second voltage regulator includes a pole-cancelation circuit.

8. The regulator circuit of claim 1, wherein the second voltage regulator includes a capacitor and a resistor, and wherein one end of the resistor is connected to the capacitor and another end of the resistor is connected to a source of the NMOS.

9. The regulator circuit of claim 1, wherein the first voltage regulator and the second voltage regulator are tunable to change a degree of input voltage regulation.

10. The regulator circuit of claim 1, wherein the first voltage regulator and the second voltage regulator have different input impedance and output impedance.

11. A method by a regulator circuit, comprising:

regulating, via a first voltage regulator, a first input voltage to the first voltage regulator, the first voltage regulator including a P-type metal-oxide-semiconductor (PMOS);

regulating, via a second voltage regulator, a second input voltage to the second voltage regulator, the second voltage regulator including an N-type metal-oxide-semiconductor (NMOS), wherein the first voltage regulator is connected to the second voltage regulator; and

selectively activating, via a switch circuit, at least one of the first voltage regulator or the second voltage regulator.

12. The method of claim 11, wherein the at least one of the first voltage regulator or the second voltage regulator is selectively activated based on noise.

13. A regulator circuit, comprising:

means for regulating a first input voltage to the means for regulating the first input voltage, the means for regulating the first input voltage including a P-type metal-oxide-semiconductor (PMOS);

means for regulating a second input voltage to the means for regulating the second voltage, the means for regulating the second voltage including an N-type metal-oxide-semiconductor (NMOS), wherein the means for regulating the first input voltage is connected to the means for regulating the second voltage; and

means for selectively activating at least one of the means for regulating the first input voltage or the means for regulating the second voltage.

14. The regulator circuit of claim 13, wherein the means for selectively activating is configured to selectively activate at least one of the means for regulating the first input voltage or the means for regulating the second voltage based on noise.

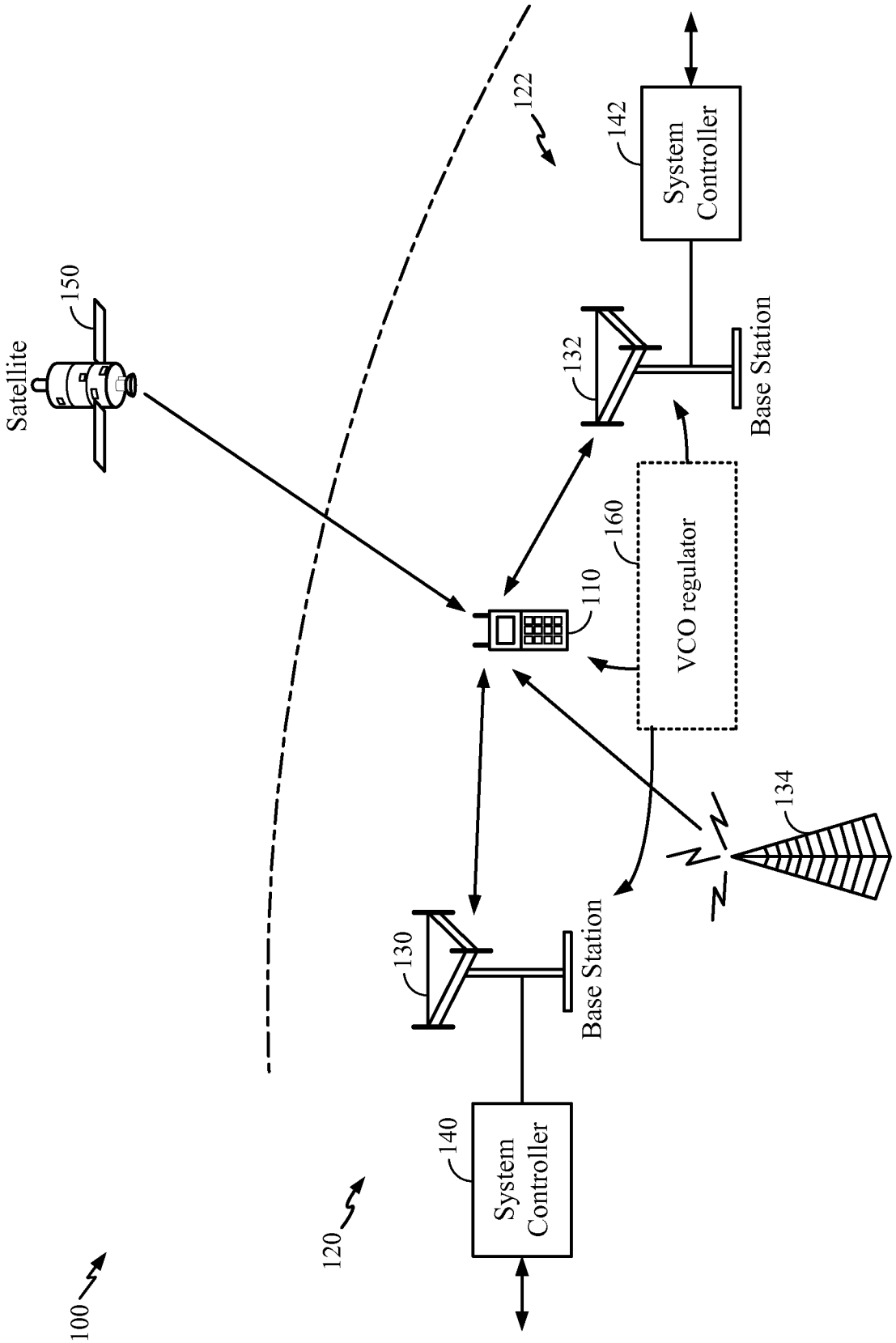
100
120
122
Satellite
150
System Controller
142
Base Station
132
VCO regulator
160
110
134
Base Station
130
System Controller
140

FIG. 1

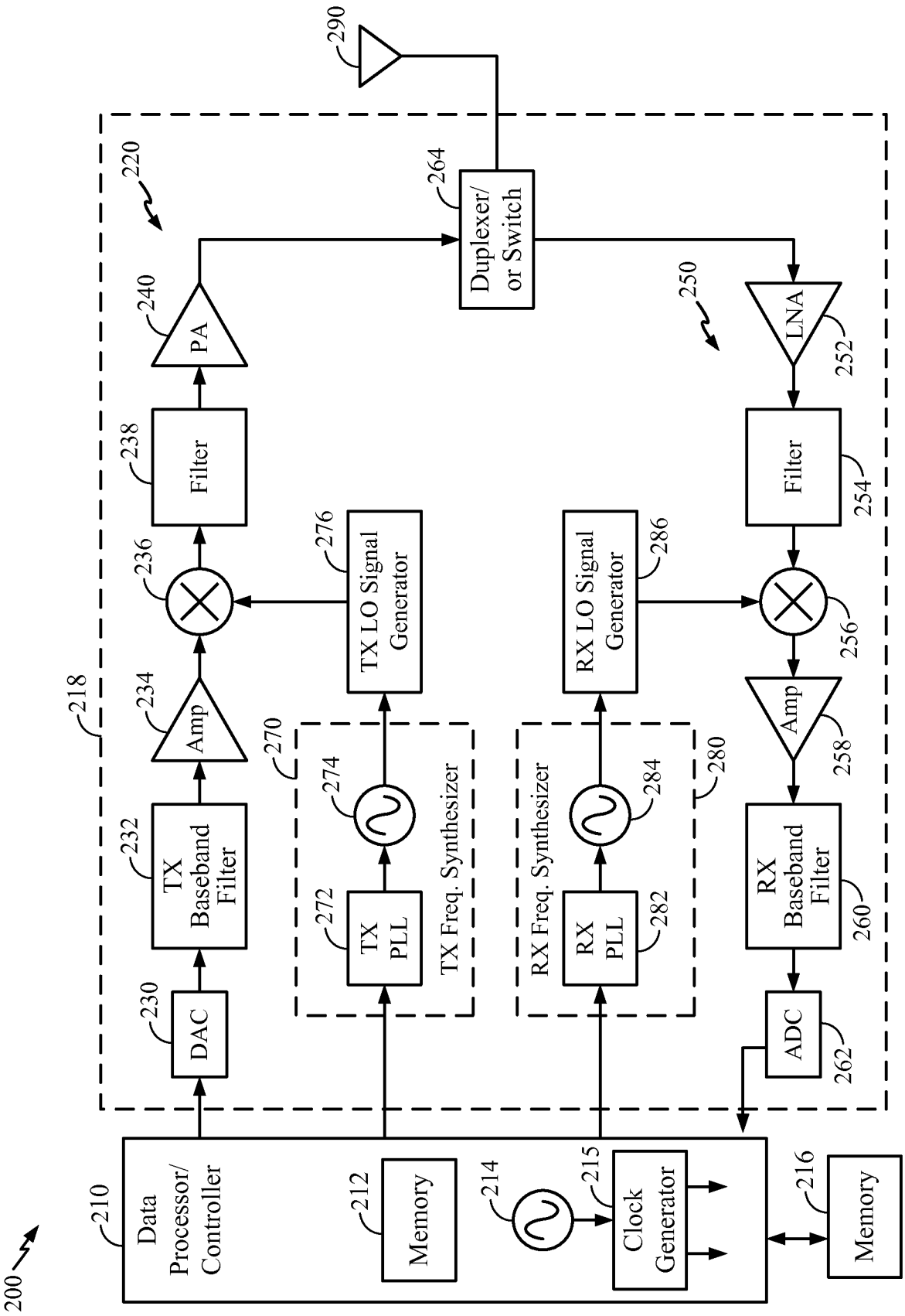
200
210
Data Processor/ Controller
212
Memory
214
215
Clock Generator
216
Memory
218
220
230
DAC
232
TX Baseband Filter
234
Amp
236
238
Filter
240
PA
264
Duplexer/ or Switch
290
270
TX Freq. Synthesizer
272
TX PLL
274
276
TX LO Signal Generator
280
RX Freq. Synthesizer
282
RX PLL
284
286
RX LO Signal Generator
250
252
LNA
254
Filter
256
258
Amp
260
RX Baseband Filter
262
ADC

FIG. 2

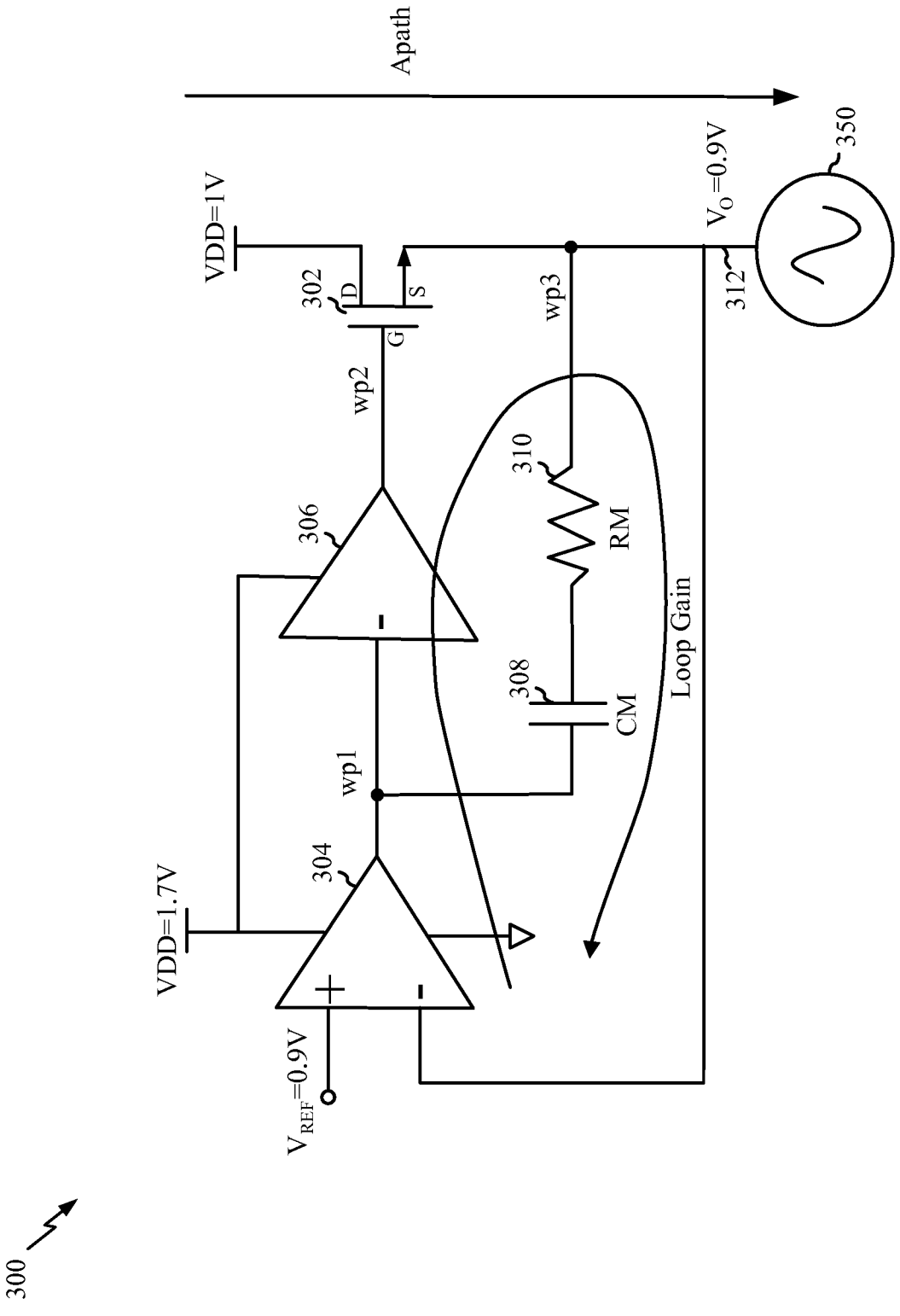
300
Apath
VDD=1V
302
D
S
G
wp2
wp3
312
$V_O$=0.9V
350
306
310
RM
308
CM
Loop Gain
wp1
304
VDD=1.7V
$V_{REF}$=0.9V

FIG. 3

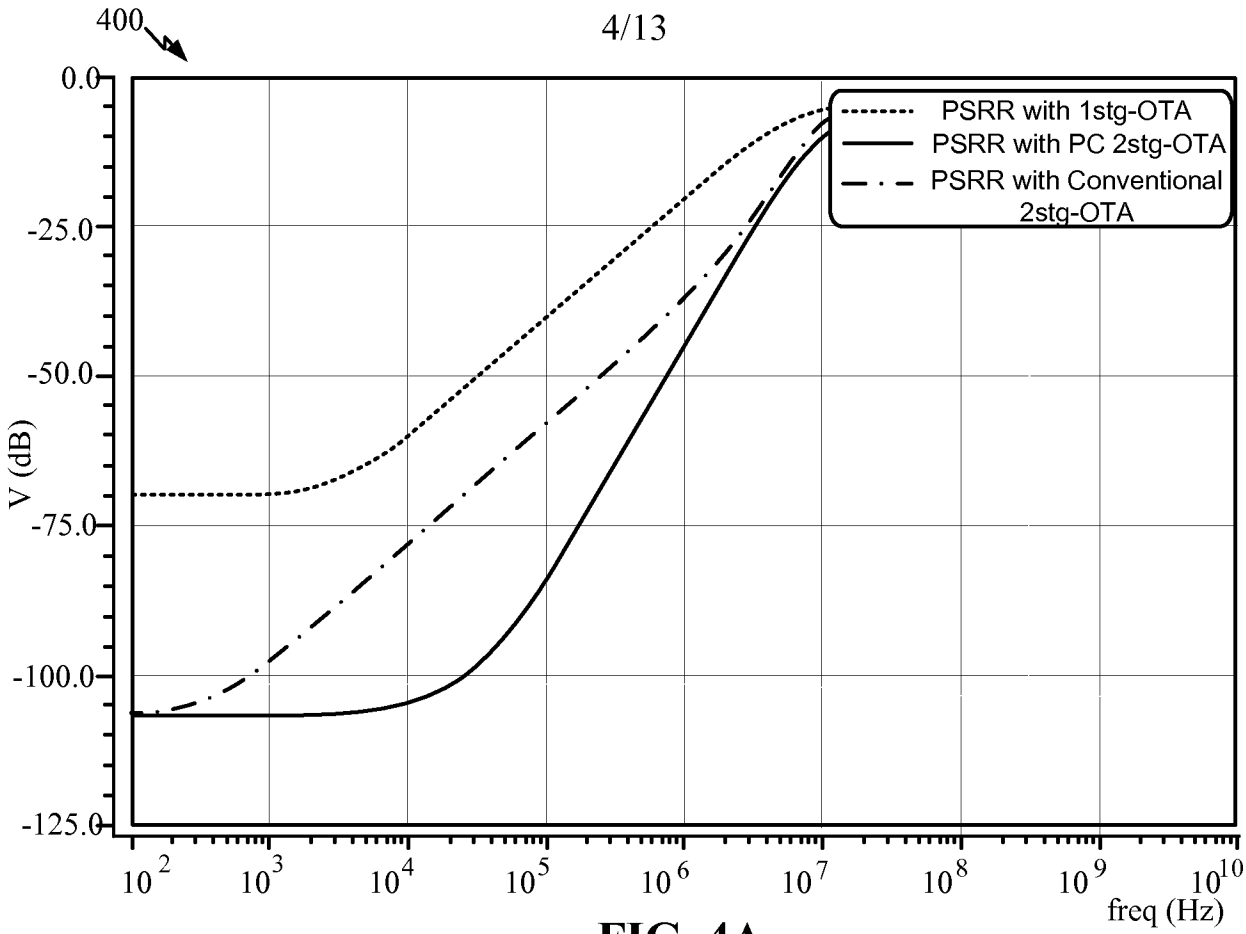
400
0.0
-25.0
-50.0
-75.0
-100.0
-125.0
V (dB)
PSRR with 1stg-OTA
PSRR with PC 2stg-OTA
PSRR with Conventional 2stg-OTA
10 2
10 3
10 4
10 5
10 6
10 7
10 8
10 9
10 10
freq (Hz)

FIG. 4A

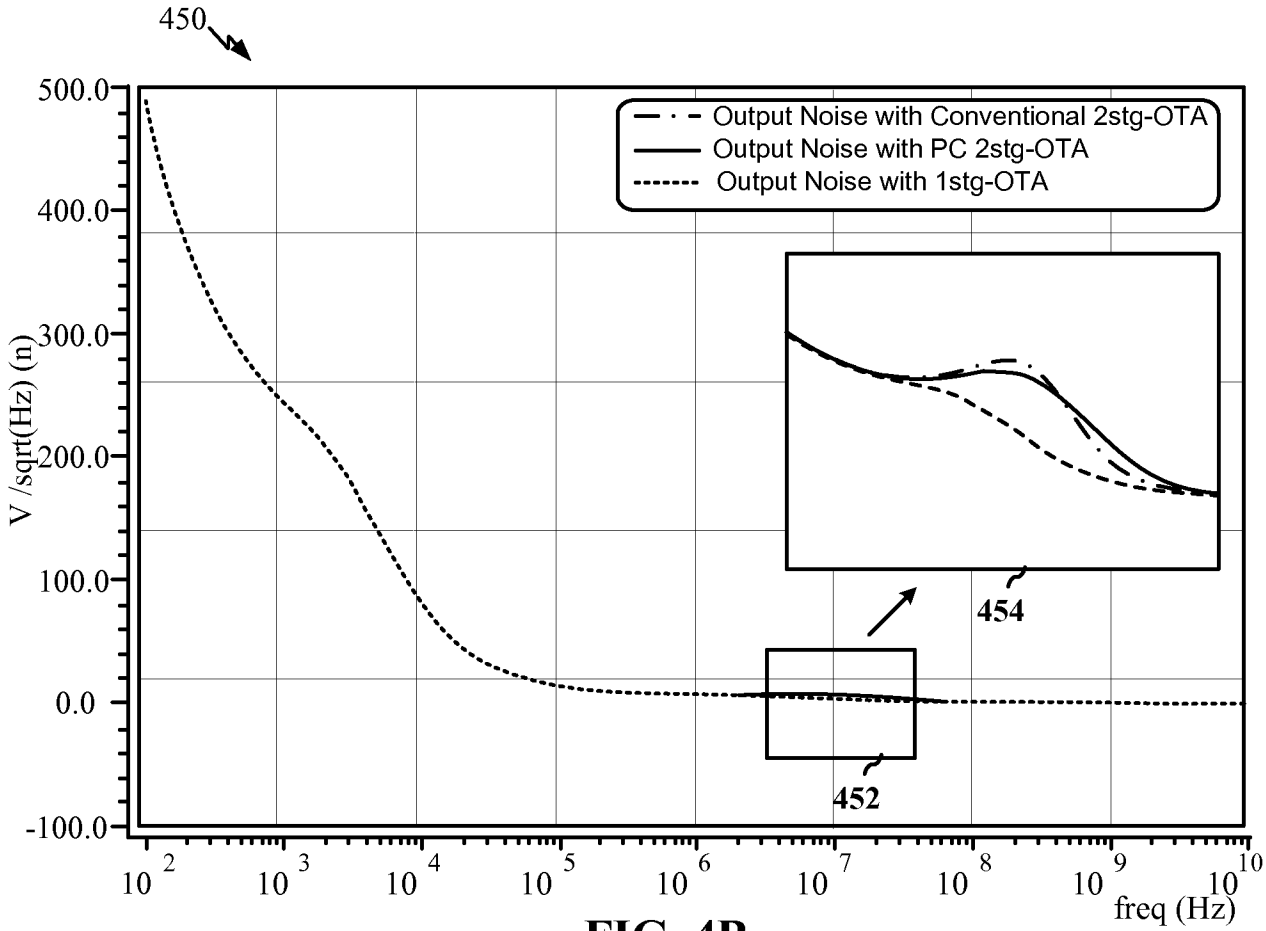
450
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
V /sqrt(Hz) (n)
Output Noise with Conventional 2stg-OTA
Output Noise with PC 2stg-OTA
Output Noise with 1stg-OTA
454
452
10 2
10 3
10 4
10 5
10 6
10 7
10 8
10 9
10 10
freq (Hz)

FIG. 4B

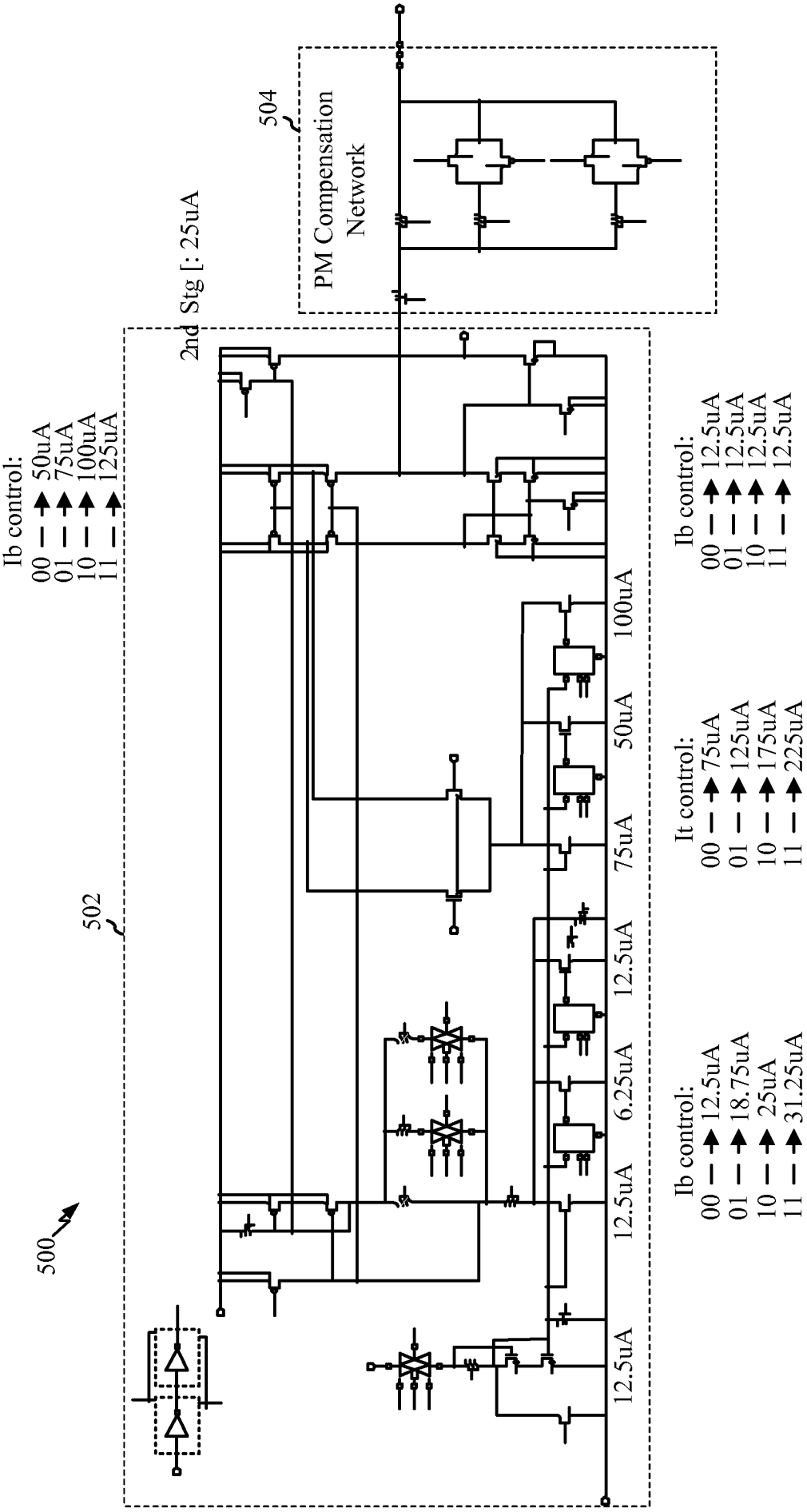
500
502
504
PM Compensation Network
2nd Stg [: 25uA
Ib control:
00 — 50uA
01 — 75uA
10 — 100uA
11 — 125uA
12.5uA
12.5uA
6.25uA
12.5uA
75uA
50uA
100uA
Ib control:
00 — 12.5uA
01 — 18.75uA
10 — 25uA
11 — 31.25uA
It control:
00 — 75uA
01 — 125uA
10 — 175uA
11 — 225uA
Ib control:
00 — 12.5uA
01 — 12.5uA
10 — 12.5uA
11 — 12.5uA

FIG. 5

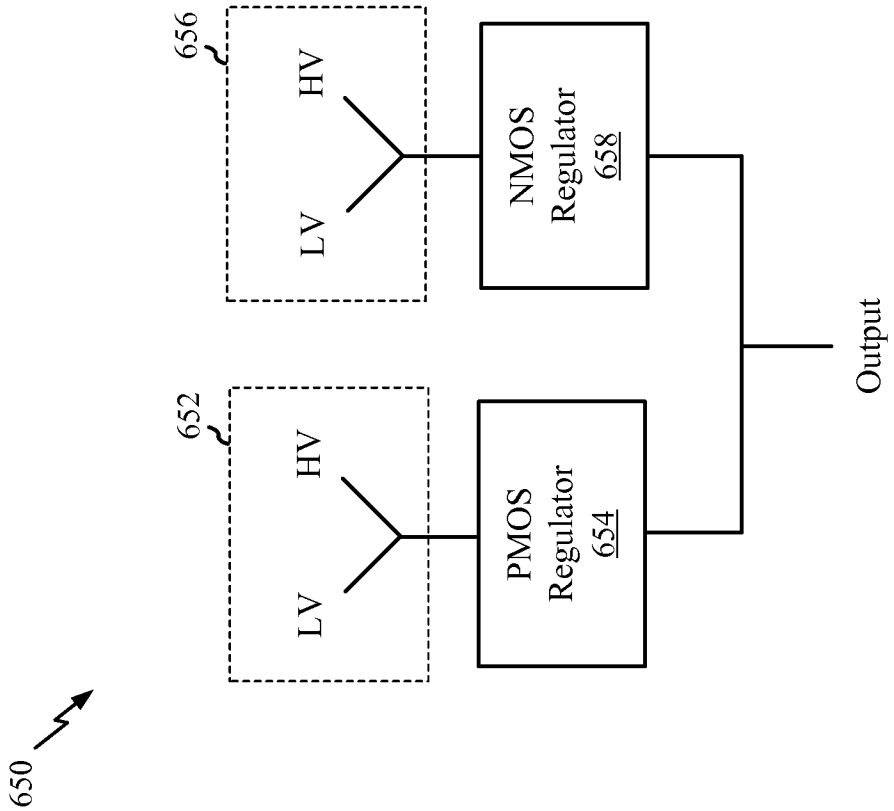
650
652
HV
LV
PMOS
Regulator
654
656
HV
LV
NMOS
Regulator
658
Output

FIG. 6B

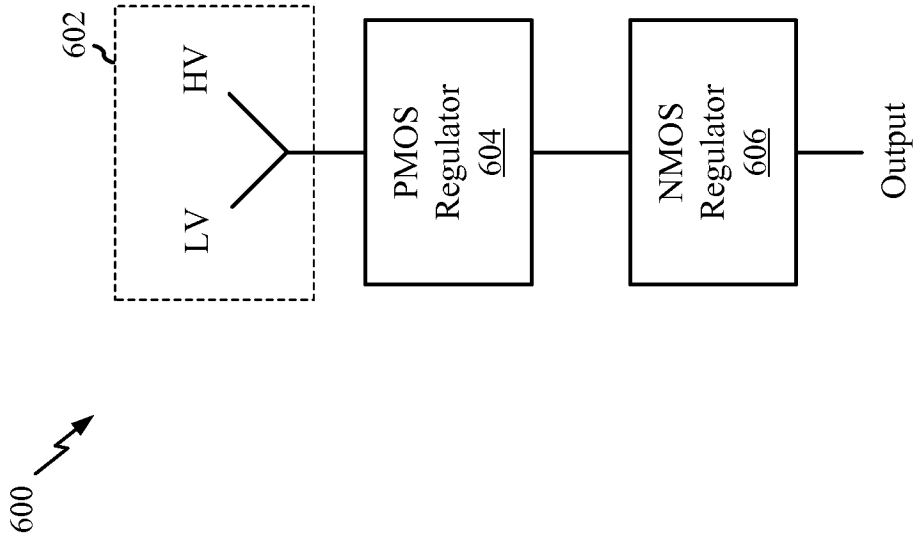
600
602
HV
LV
PMOS
Regulator
604
NMOS
Regulator
606
Output

FIG. 6A

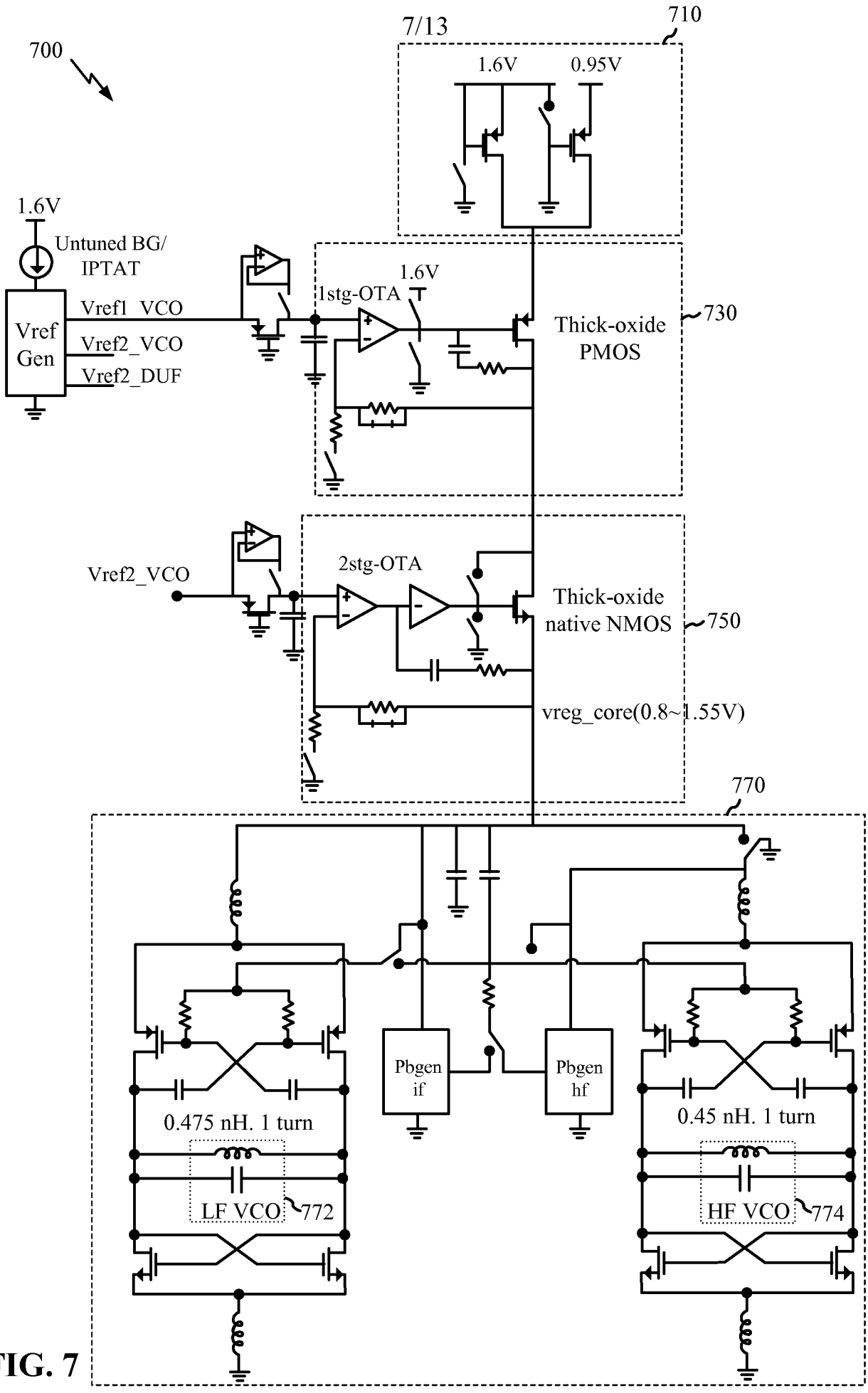
7/13
700
710
1.6V
0.95V
1.6V
Untuned BG/
IPTAT
Vref
Gen
Vref1_VCO
Vref2_VCO
Vref2_DUF
1.6V
1stg-OTA
Thick-oxide
PMOS
730
Vref2_VCO
2stg-OTA
Thick-oxide
native NMOS
750
vreg_core(0.8~1.55V)
770
Pbgen
if
Pbgen
hf
0.475 nH. 1 turn
LF VCO
772
0.45 nH. 1 turn
HF VCO
774

FIG. 7

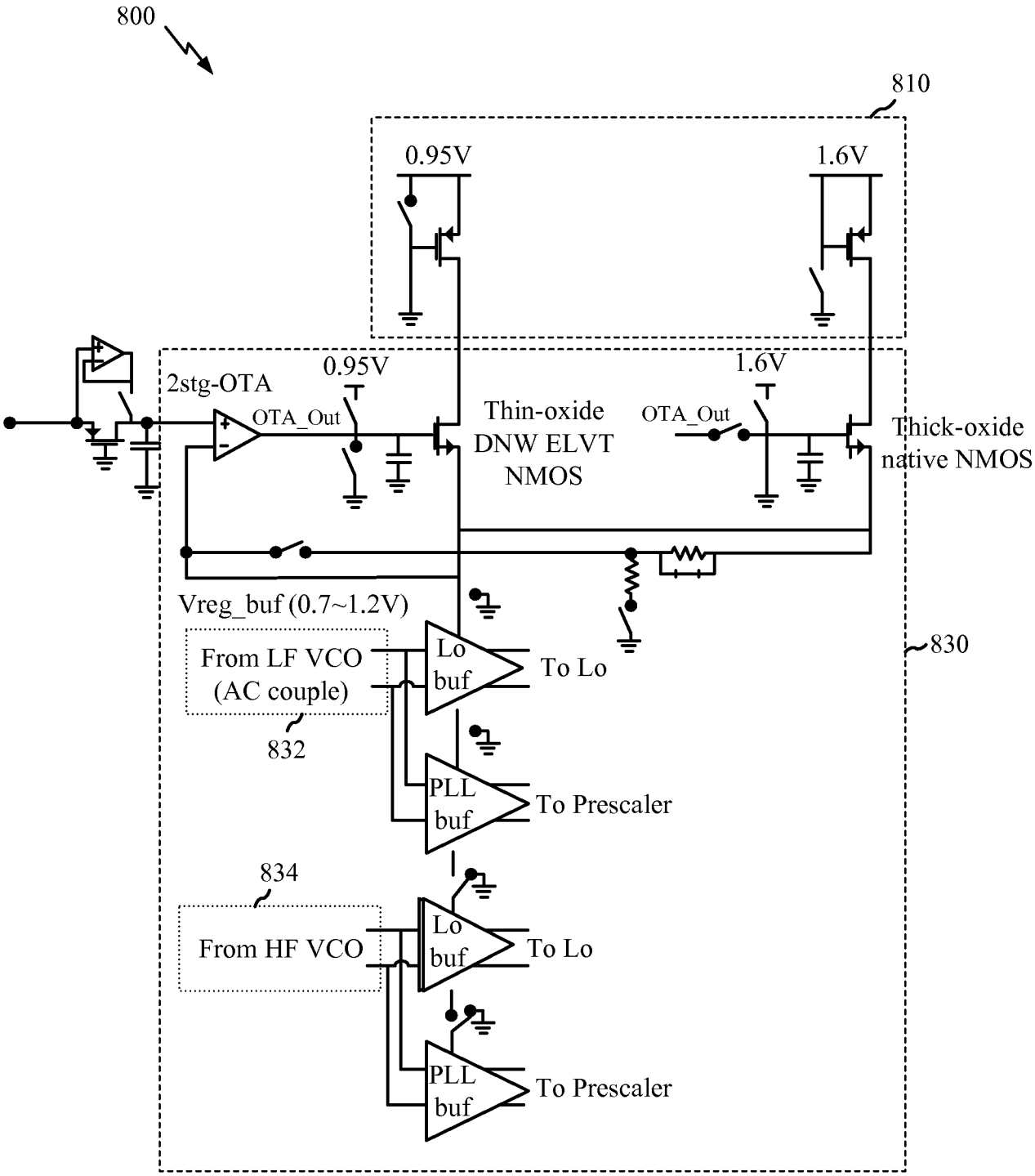
800
810
0.95V
1.6V
2stg-OTA
0.95V
1.6V
OTA_Out
OTA_Out
Thin-oxide
DNW ELVT
NMOS
Thick-oxide
native NMOS
Vreg_buf (0.7~1.2V)
830
From LF VCO
(AC couple)
832
Lo
buf
To Lo
PLL
buf
To Prescaler
834
From HF VCO
Lo
buf
To Lo
PLL
buf
To Prescaler

**FIG. 8**

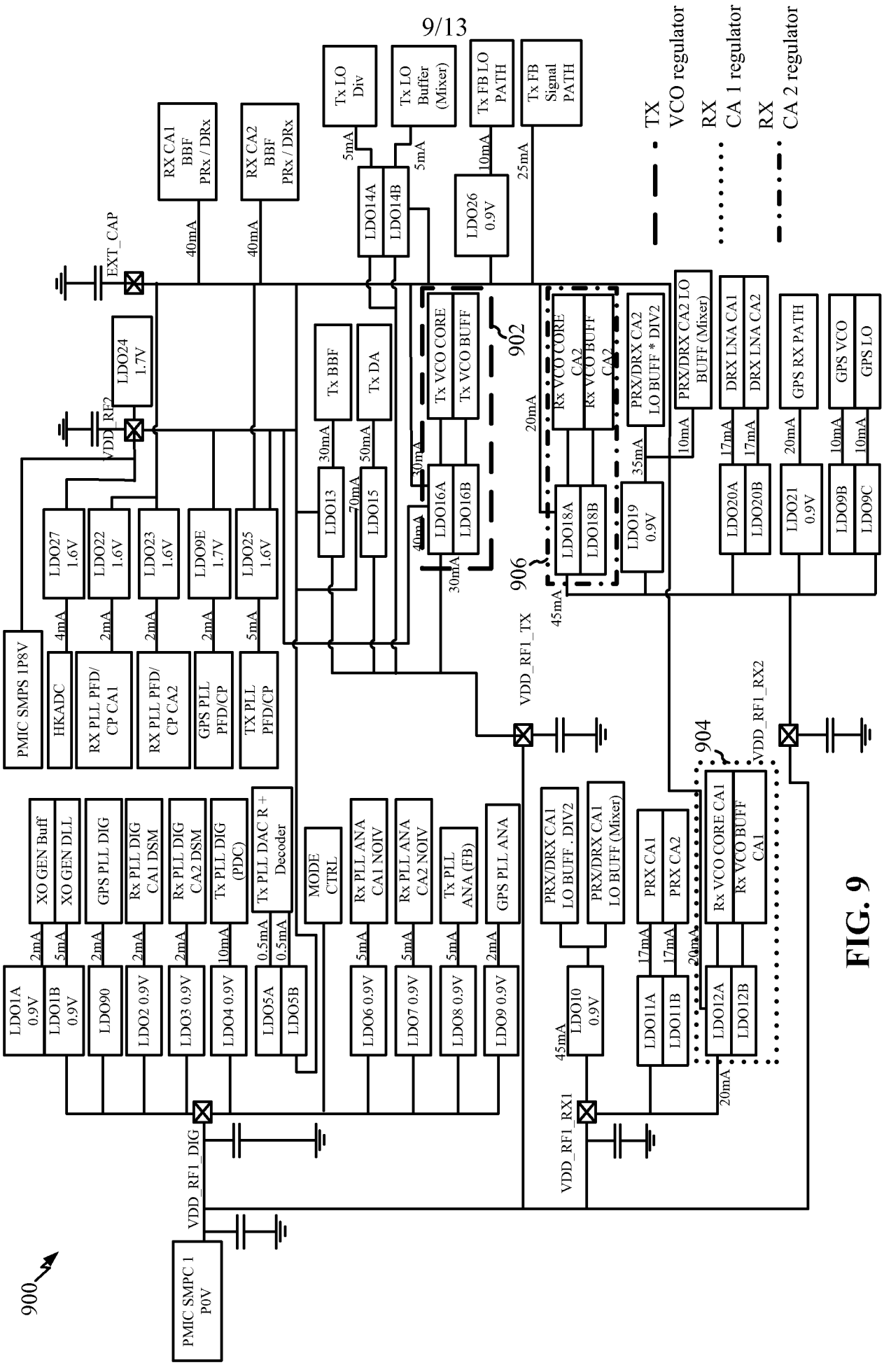
900
PMIC SMPC 1 P0V
VDD_RF1_DIG
VDD_RF1_RX1
VDD_RF1_TX
VDD_RF1_RX2
VDD_RF2
EXT_CAP
PMIC SMPS 1P8V
HKADC
RX PLL PFD/ CP CA1
RX PLL PFD/ CP CA2
GPS PLL PFD/CP
TX PLL PFD/CP
LDO1A 0.9V
LDO1B 0.9V
LDO90
LDO2 0.9V
LDO3 0.9V
LDO4 0.9V
LDO5A
LDO5B
LDO6 0.9V
LDO7 0.9V
LDO8 0.9V
LDO9 0.9V
LDO10 0.9V
LDO11A
LDO11B
LDO12A
LDO12B
LDO13
LDO15
LDO16A
LDO16B
LDO18A
LDO18B
LDO19 0.9V
LDO20A
LDO20B
LDO21 0.9V
LDO9B
LDO9C
LDO22 1.6V
LDO23 1.6V
LDO9E 1.7V
LDO25 1.6V
LDO27 1.6V
LDO24 1.7V
LDO014A
LDO014B
LDO26 0.9V
XO GEN Buff
XO GEN DLL
GPS PLL DIG
Rx PLL DIG CA1 DSM
Rx PLL DIG CA2 DSM
Tx PLL DIG (PDC)
Tx PLL DAC R + Decoder
MODE CTRL
Rx PLL ANA CA1 NOIV
Rx PLL ANA CA2 NOIV
Tx PLL ANA (FB)
GPS PLL ANA
PRX/DRX CA1 LO BUFF . DIV2
PRX/DRX CA1 LO BUFF (Mixer)
PRX CA1
PRX CA2
Rx VCO CORE CA1
Rx VCO BUFF CA1
Tx BBF
Tx DA
Tx VCO CORE
Tx VCO BUFF
Rx VCO CORE CA2
Rx VCO BUFF CA2
PRX/DRX CA2 LO BUFF * DIV2
PRX/DRX CA2 LO BUFF (Mixer)
DRX LNA CA1
DRX LNA CA2
GPS RX PATH
GPS VCO
GPS LO
RX CA1 BBF PRx / DRx
RX CA2 BBF PRx / DRx
Tx LO Div
Tx LO Buffer (Mixer)
Tx FB LO PATH
Tx FB Signal PATH
902
904
906
TX VCO regulator
RX CA 1 regulator
RX CA 2 regulator

FIG. 9

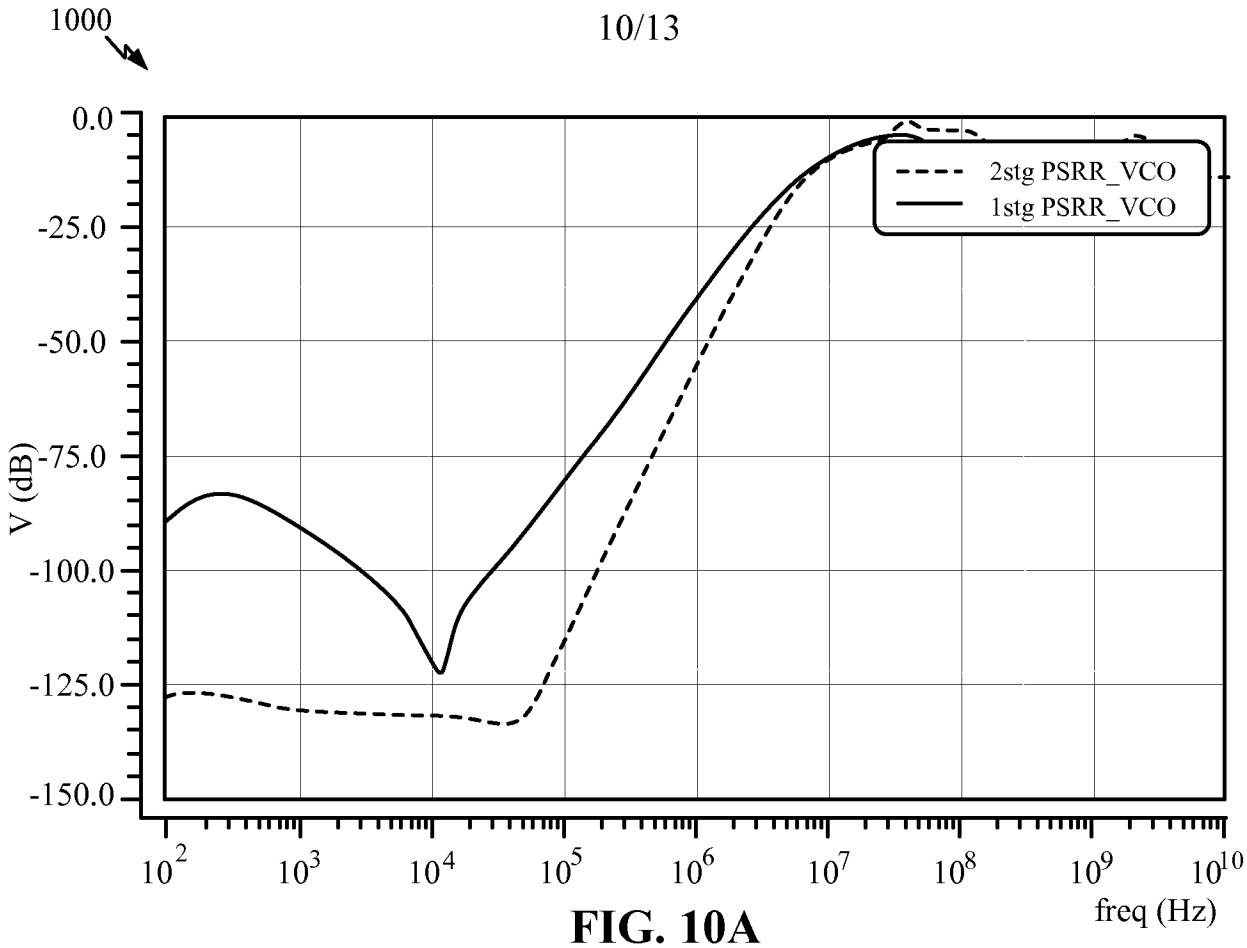


FIG. 10A

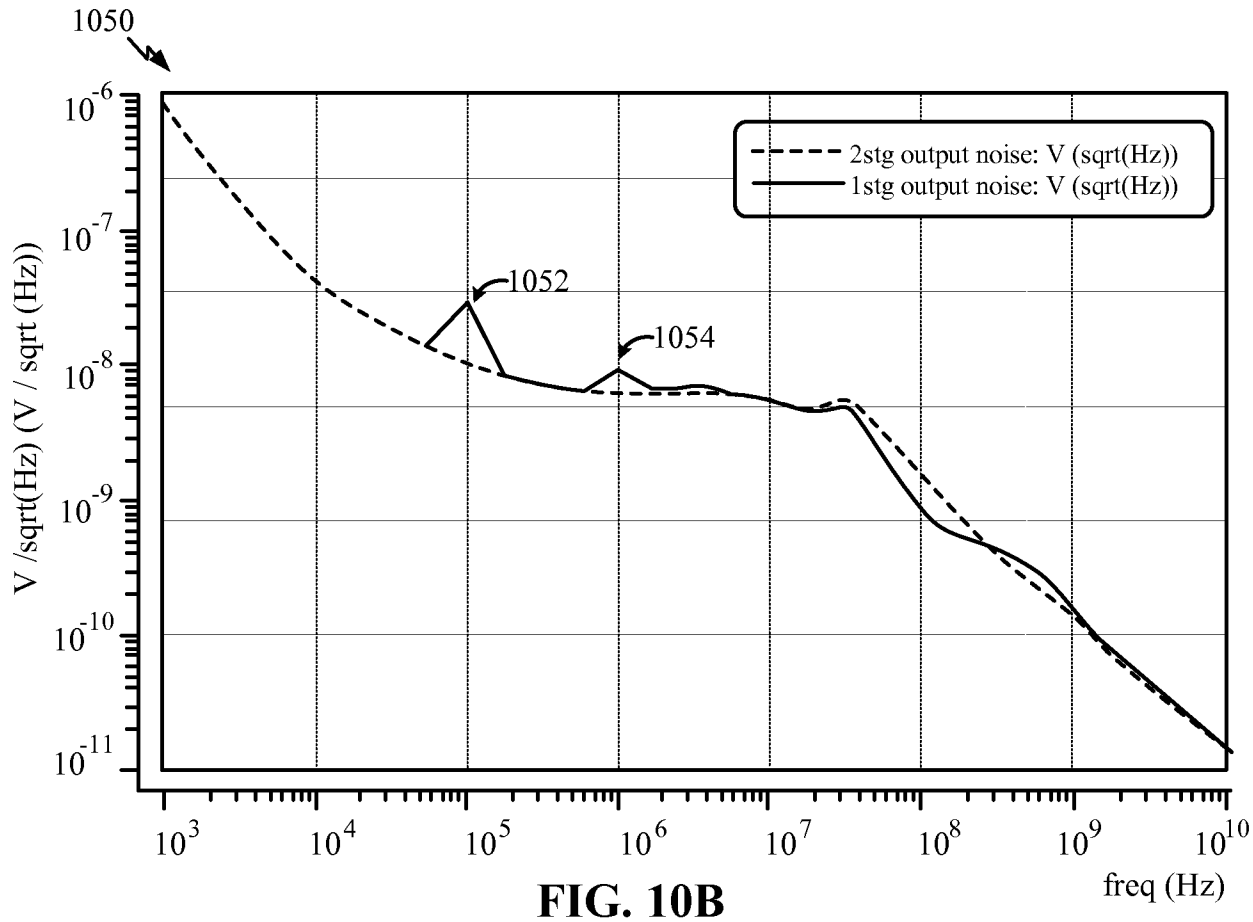


FIG. 10B

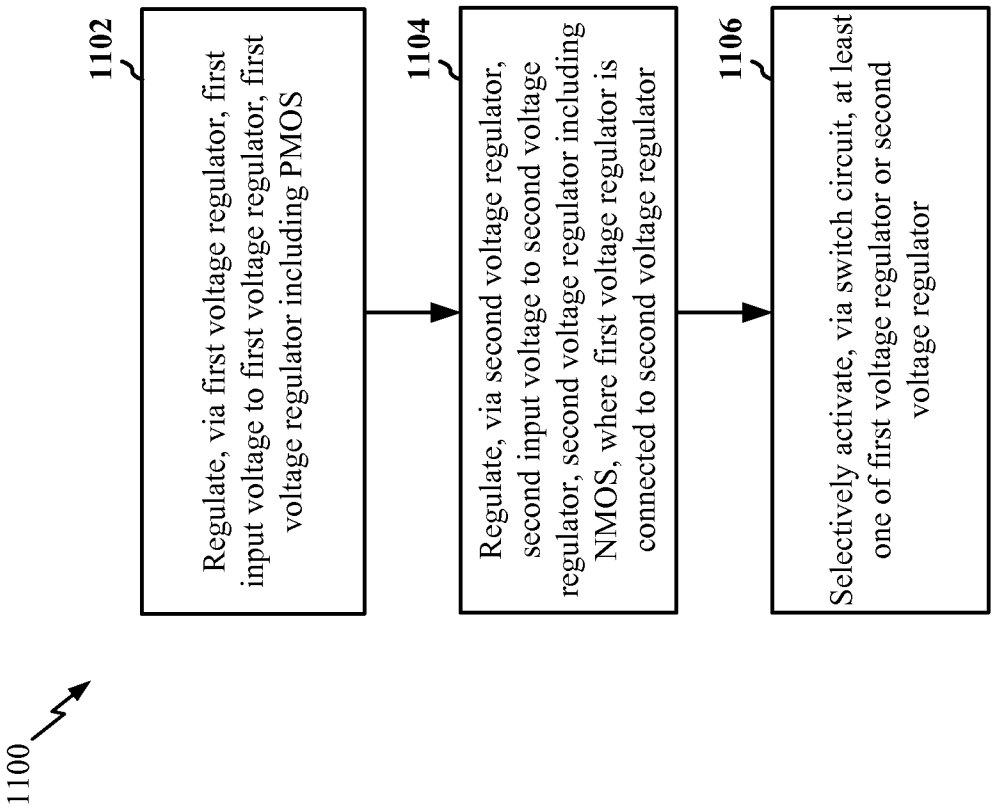
1100
1102
Regulate, via first voltage regulator, first input voltage to first voltage regulator, first voltage regulator including PMOS
1104
Regulate, via second voltage regulator, second input voltage to second voltage regulator, second voltage regulator including NMOS, where first voltage regulator is connected to second voltage regulator
1106
Selectively activate, via switch circuit, at least one of first voltage regulator or second voltage regulator

FIG. 11

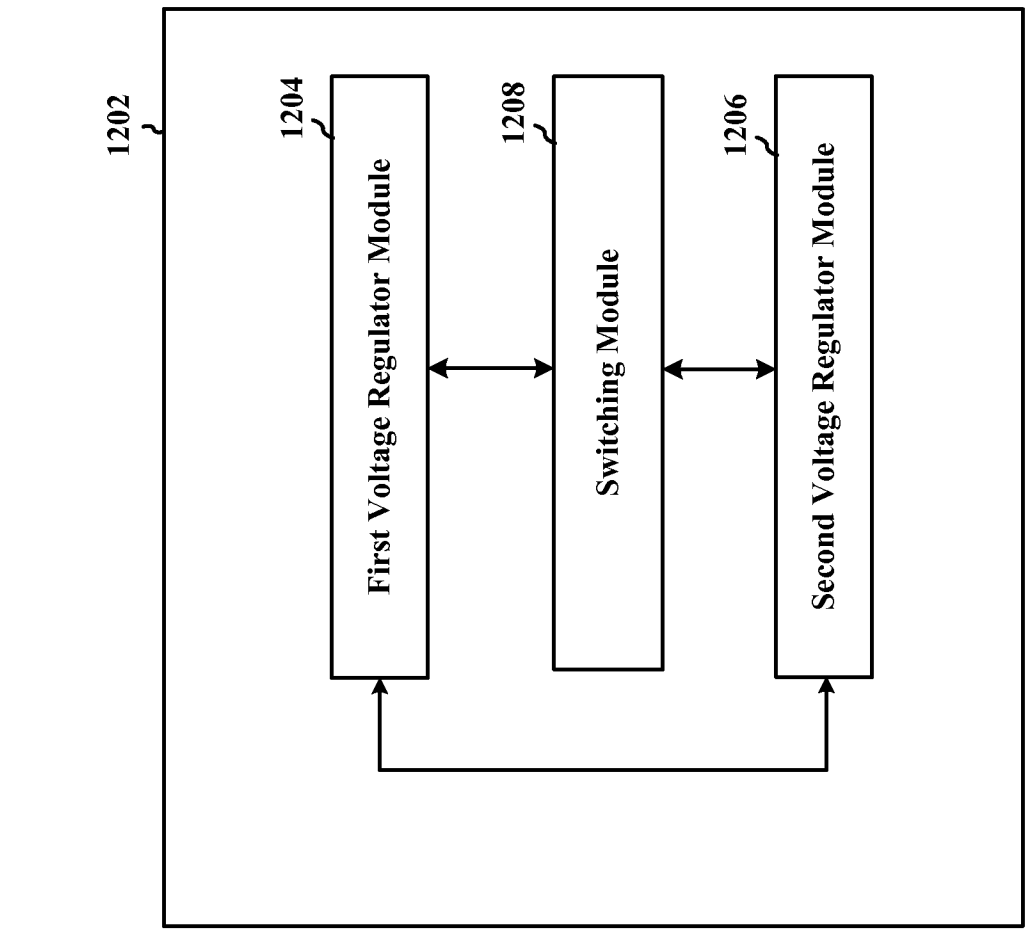
1202
1204
First Voltage Regulator Module
1208
Switching Module
1206
Second Voltage Regulator Module

FIG. 12

1200

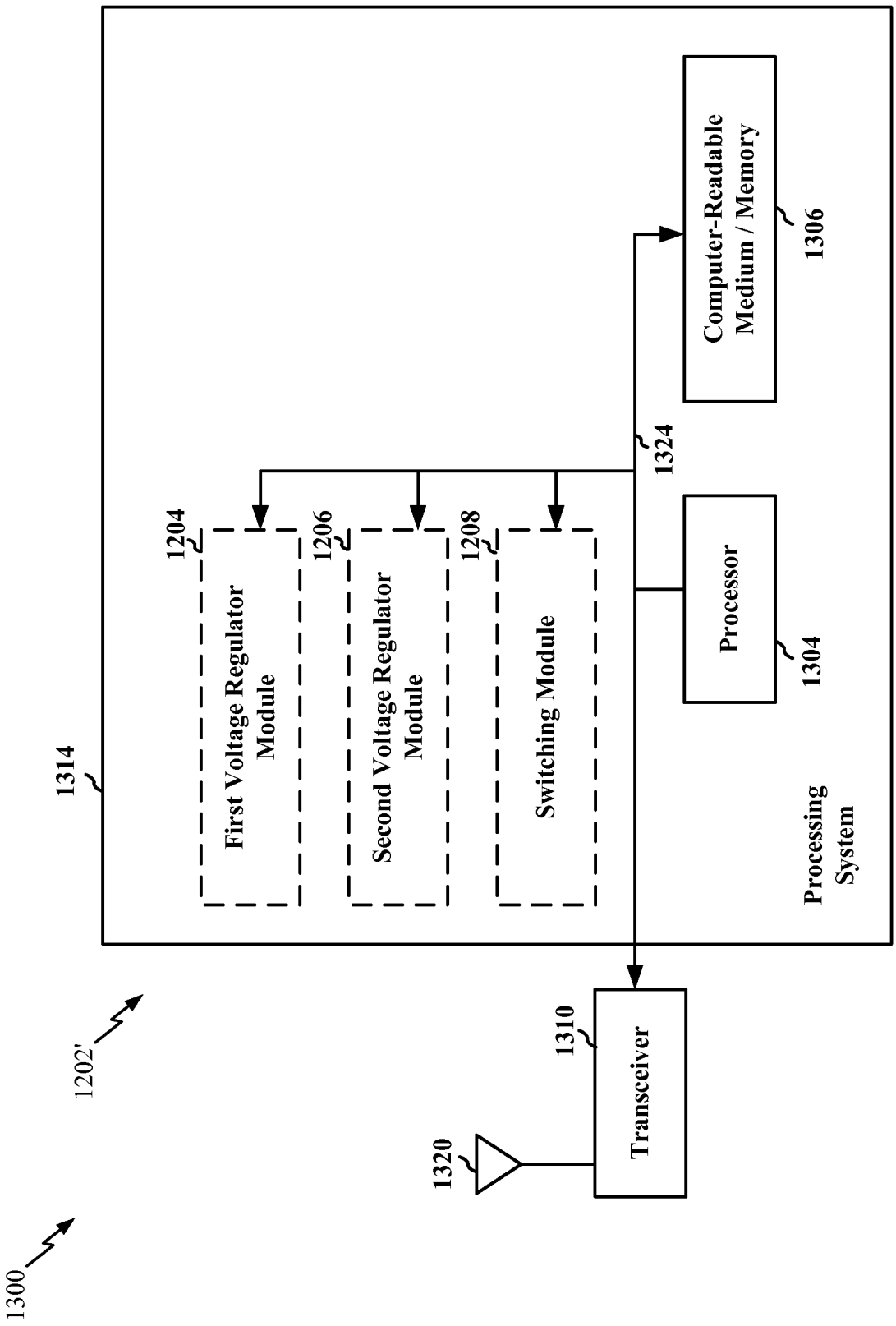
1300
1202'
1314
1204
First Voltage Regulator Module
1206
Second Voltage Regulator Module
1208
Switching Module
Processing System
1304
Processor
1306
Computer-Readable Medium / Memory
1324
1310
Transceiver
1320

FIG. 13

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/030948

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F1/575
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y<br>A | US 2005/110477 A1 (MAUTHE MANFRED [DE])<br>26 May 2005 (2005-05-26)<br>the whole document | 1-3,5-7,<br>11-14<br>4,8<br>9,10 |
| | ----- | |
| Y<br>A | US 2006/232255 A1 (HAIDER GUNTER [AT] ET AL) 19 October 2006 (2006-10-19)<br>column 1, paragraph 0005 - column 3, paragraph 0035; figure 1 | 4<br>1-3,5-14 |
| | ----- | |
| | -/-- | |

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 21 July 2015 | 28/07/2015 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Schobert, Daniel |

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# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/030948

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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International application No
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| | | WO 03085475 A2 | 16-10-2003 |
| US 2006232255 A1 | 19-10-2006 | DE 10334066 A1 | 24-02-2005 |
| | | EP 1649587 A1 | 26-04-2006 |
| | | US 2006232255 A1 | 19-10-2006 |
| | | WO 2005013466 A1 | 10-02-2005 |
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| | | US 2005264960 A1 | 01-12-2005 |
| | | WO 2004055613 A1 | 01-07-2004 |